EVM User's Guide: TCAN-SOIC8-EVM

Universal 8-pin CAN Evaluation Module

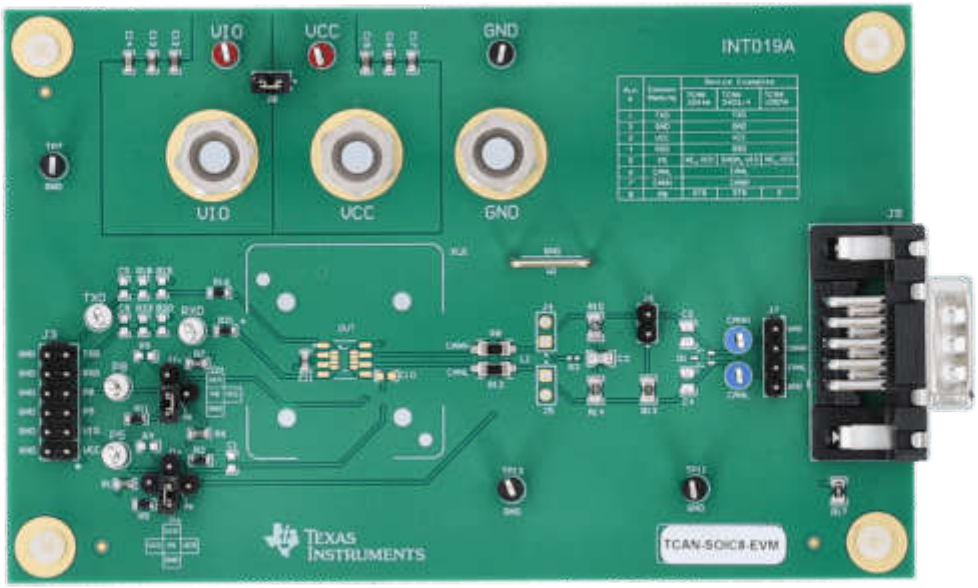
Description

The universal 8-pin CAN EVM provides users with the ability to evaluate all of TI's 8-pin CAN transceiver families. The universal 8-pin CAN EVM is configurable for use with all TI 8-pin CAN transceiver families by populating the transceiver and setting jumpers on the EVM.

This EVM also has the footprints for a SIC network, which can be connected to the CAN bus lines via user-installed J4 and J5. Connecting the SIC network to CANH and CANL simulates a noisy CAN bus by adding more reflections and ringing to the signals. This can be used to test the reliability of the transceiver in a very noisy environment.

Features

- Standard and split termination on the CAN bus
- Footprints for filter capacitors, common-mode choke, and TVS diode for CAN bus protection from RF noise and transient pulses
- Footprints for common 8-pin SOIC/SOT socket, and CAN FD SIC loading
- DSUB9 connector with the CAN bus signals and GND for typical automotive cable harness connections
- All digital signals for configuration and control brought out to a header for easy access
- Multifunctional jumpers for different functional use of generic pins
- EVM supports SOIC and SOT package options



TCAN-SOIC8-EVM

1 Evaluation Module Overview

1.1 Introduction

This user's guide details the universal 8-pin CAN (Controller Area Network) EVM operation. All of the options and the overall operation of the EVM are explained in this user's guide. This user's guide explains the EVM configurations for basic CAN evaluation, various load and termination settings.

1.2 Kit Contents

1. Universal 8-pin CAN EVM

1.3 Specification

TI offers a broad portfolio of high speed (HS) CAN, CAN FD, and CAN SIC transceivers. These include 5V V_{CC} only, 3.3V V_{CC} only, and 5V V_{CC} with I/O level shifting CAN transceivers. These CAN transceiver families include product mixes with varying features such as low-power standby modes with and without wake up, silent modes, loop back, and diagnostic modes.

TI's CAN EVM helps designers evaluate the operation and performance of various TI CAN transceivers in normal and SIC networks. CAN EVM also provides bus termination, bus filtering, and protection concepts. CAN EVM is easily configured by the user for the TI 8-pin CAN transceiver families as needed by jumper settings, simple soldering tasks, and replacement of standard components. A separate EVM is available for the galvanic-isolated CAN transceiver family.

1.4 Device Information

The CAN EVM has simple connections to all necessary pins of the CAN transceiver device, and jumpers where necessary to provide flexibility for device pin and CAN bus configuration. There are test points (loops) for all main points where probing is necessary for evaluation such as GND, V_{CC}, TXD, RXD, CANH, CANL, pin 8 (mode pin), or pin 5 (various functions). The EVM supports many options for CAN bus configuration. The CAN EVM allows for two termination schemes through a single jumper to select between just split termination configuration, or split with 120Ω resistor as well. If needed, there are footprints for a common-mode choke, TVS diode for ESD protection, and capacitors for further EMC protection, or signal conditioning. A DSUB9 connector is included to allow the evaluation and use of the CAN bus in larger systems.

2 Hardware

Jumper Information

Table 2-1 lists the jumper connections for the EVM.

Table 2-1. Jumper Connections

Connection	Type	Description
J1A, J1B, J1C	4-way jumper	Functional use of generic pin 5. Options for use are: • J1A1: V_{IO} for transceiver with digital I/O voltage input on pin 5. Populate C10 or C18 if pin 5 used as V_{IO}. Provides customer installable pulldown R4 to GND, and 0-Ohm pullup placeholder R2 • J1A3: 0Ω pulldown to GND for transceiver with digital input on pin 5 • J1B: Active split termination for CAN transceiver with V_{REF} or SPLIT on pin 5. Short J1A2 – J1B and populate R3 for split termination as required • J1C: 4.7kΩ pullup to V_{CC} for transceiver with digital input on pin 5, or external pullup for open drain output on pin 5
J2A, J2B	3-way jumper	Used for mode selection or polarity configuration. Options for use are: • J2A1: 4.7kΩ pullup to V_{IO} for transceivers with digital input on pin 5. Provides customer installable pulldown for devices with slew rate control R_S pin • J2A3: 0Ω pulldown to GND for transceiver with digital input on pin 5 • J2B: 4.7kΩ pullup to V_{CC} for transceivers with digital input on pin 5
J3	12-pin header	Connection for access to all critical digital I/O, supply, and GND for driving the CAN transceiver externally with test equipment or interfaced to a processor EVM
J4	2-pin jumper	Connect SIC network to CANH. Must be used in combination with J5
J5	2-pin header	Connect SIC network to CANL. Must be used in combination with J4
J6	2-pin jumper	Connect R13, a 120Ω CAN termination to the bus. Along with the already populated 120 ohms (R10 and R14 in series), this simulates the true CAN bus impedance of 60 ohms (two 120 ohm terminating resistors in parallel). Shunting J6 places R13 on the bus, not placing a shunt opens the bus and only leaves R10 and R14 for the termination.
J7	4-pin header	CAN bus connection (CANH, CANL) and GND
J8	2-pin jumper	V_{IO} and V_{CC} supply connection. Provides ability to short V_{CC} and V_{IO} together
J9	DSUB9 Connector	Provides an optional way to connect CANH, CANL, and GND all through a standard DB9 CAN pinout rather than through a regular header.
W1	Ground clip	Provides extra connection to GND
TP1	Test point	Device generic pin 5 test point
TP2		CANH (bus) test point
TP3		Device generic pin 8 test point
TP4		CANL (bus) test point
TP5		TXD, Device pin 1 test point
TP6		RXD, Device pin 4 test point
TP7, TP8, TP11, TP12		GND test points
TP9		V_{IO} test point
TP10		V_{CC} test point

2.1 EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation.

2.1.1 Overview and Basic Operation Settings

2.1.1.1 V_{CC} Power Supply (J3, P2, TP10)

The basic setup of the CAN EVM uses a single power supply required to evaluate standard 5V or 3.3V single-supply transceiver device performance. For single-supply transceivers, connect the 5V or 3.3V V_{CC} supply to the P2 banana jack, or the V_{CC} and GND test-point loops. The power supplied must meet the required specification of V_{CC} for the transceiver being tested.

2.1.1.2 I/O Power Supply V_{IO} or V_{RXD} (J3, J8, P1,or TP9)

For devices with I/O level shifting, a second supply pin for the I/O or RXD pin is on pin 5 of the transceiver device. A second power supply is needed to test one of these devices. Power can be supplied to this pin by either shunting V_{CC} and V_{IO} together via J8, or connecting a separate power supply via J3, P1 banana jack, or TP8. Install a local buffering and decoupling capacitor at C10 if the EVM is used for one of these devices.

2.1.1.3 Main Supply and I/O Header (J3)

All key I/O and supply GND functions are brought to this header. This header can be used on either interface to test equipment or a short cable can be made to connect to an existing customer-application board with a CAN controller.

Table 2-2. J3 Pin Definitions

Pin	Connection	Description
1	V_{CC}	Pin 3 of transceiver, V_{CC}
3	V_{IO}	Supports level-shifting functions of devices with V_{IO} or V_{RXD} pin
5	P5	Generic pin 5 of transceiver, various functions depending on transceiver, examples: V_{REF}, SPLIT, V_{RXD}, V_{IO}, LBK, EN, AB, SHDN, FAULT and No Connect (NC)
7	P8	Generic pin 8 of transceiver, normally used for mode control, examples: R_S, SW, S, STB and No Connect (NC)
9	RXD	Pin 4 of transceiver, RXD (receive data)
11	TXD	Pin 1 of transceiver, TXD (transmit data)
2	GND	Pin 2 of transceiver, GND
4		
6		
8		
10		
12		

This header is arranged to provide a separate ground for each signal pair (TXD/GND and RXD/GND). If the EVM is being used with lab equipment, connect separate cables to these main points via simple 2-pin header connectors. If connecting the board to a processor-based system, connect a single cable with all power and signals via a 12-pin header cable to this port.

2.1.1.4 TXD Input (J3 or TP5)

The TXD (pin 1) of the transceiver, transmit data, is routed to J3 and TP5. The signal path to the J3 header is pre-installed with a 0Ω series resistor, R16. An optional pullup resistor to VIO can be installed on R15, an optional pulldown resistor to GND can be installed on R18, and an optional filtering capacitor can be installed on C5.

2.1.1.5 RXD Output (J3 or TP6)

The RXD (pin 4) of the transceiver, receive data, is routed to J3 and TP6. The signal path to the J3 header is pre-installed with a 0Ω series resistor, R21. An optional pullup resistor to VIO can be installed on R20, an optional pulldown resistor to GND can be installed on R22, and an optional filtering capacitor can be installed on C9.

2.1.1.6 Generic Pin 8 (J2, J3, or TP3)

Pin 8 of the transceiver is normally a mode control or polarity switch pin of the device. Pin 8 of the device is routed to J2, J3, and TP3.

2.1.1.7 Pin 8 - J2 Configurations (3-Way Jumper)

If using separate I/O inputs, then J2 is used to configure pin 8 to: pullup to V_{IO}, pullup to V_{CC} or pulldown to GND. This pin can be pulled up to V_{IO} by connecting a shunt to the J2A1 and J2A2 pins on J2, pulled up to V_{CC} by connecting a shunt to the J2A2 and J2B pins, or pulled down to GND by connecting a shunt to the J2A2 and J2A3 pins on J1.

- **Mode Control input (S , STB, R_S)**: if the device and application use pin 8 as mode control, set J2 to pulldown to GND for a normal or high-speed mode, (R11 is pre-installed with 0Ω resistor to GND for this purpose) or pullup to V_{CC}/V_{IO} for a silent or low-power standby mode.
- **Slope Control (R_S)**: if the device and application use pin 8 as slope control, use the resistance to ground value to determine the slope of the driver output. R9 is left open for customers who want to install a resistance to ground and use slope mode.
- **Polarity Configuration (SW)**: if the device and application use pin 8 as polarity configuration, set J2 to pulldown to GND for normal polarity, or pullup to V_{IO} for reverse polarity.
- **No Connection (NC)**: If the device and application require no use of pin 5, then leave open or pulled to GND.

2.1.1.8 TP3 Configuration

This connects directly to device pin 8. Make sure J2 configuration is not conflicting if TP3 is used as the input connection.

2.1.1.9 Generic Pin 5 (J1, J3 or TP1)

Pin 5 of the transceiver has various uses depending on the transceiver. Pin 5 of the device is routed to J1, J3 and TP1.

2.1.1.10 Pin 5 – J1 Configurations (4-Way Jumper)

If using separate I/O inputs, J2 is used to configure pin 8 to: pullup to V_{IO} supply input, pullup to V_{CC}, pulldown to GND, or V_{REF} or SPLIT termination output. This pin can be pulled up to V_{IO} by connecting a shunt to the J1A2 and J1A1 pins on J2, pulled up to V_{CC} by connecting a shunt to the J1A2 and J1C pins, pulled down to GND by connecting a shunt to the J1A2 and J1A3 pins on J1, or SPLIT termination output by connecting a shunt to the J1A2 and J1B pins.

- **V_{REF} or SPLIT termination (V_{CM}):** If the device and application support split termination, set J1 to V_{CM} (V common mode) to drive the V_{REF} or SPLIT pin common mode stabilizing voltage output to the center tap of the split termination capacitor.
- **No Connection (NC):** If the device and application require no use of pin 5, leave open. If the device has the V_{REF} or SPLIT pin, but the application is not using the pin for split termination, then add a capacitor on C1 to improve EMC performance.
- **2nd Mode or Control Input (LBK, EN, AB, SHDN):** If the device and application use pin 5 as a second mode or control pin, then set J1 as either a pullup to V_{CC} or pulldown to GND, as necessary. R4 is left open for customers who want to install a resistance to ground.
- **I/O and RXD level-shifting supply:** If the device and application used with V_{IO} or V_{RXD} to level shift I/O pins on the transceiver, then set J1 to V_{IO} connecting pin 5 of the device to the V_{IO} supply input. Install local buffering and bypass capacitor C10 (no socket) or C18 (has socket).
- **Open Drain Output (FAULT):** If the device and application use pin 5 as an open drain output, then external pullup is required. Set J1 as either a pullup to V_{CC} or V_{IO}.

2.1.1.11 TP1 Configuration

This connects directly to device pin 5. Make sure J1 configuration is not conflicting if P5 is used as an input connection.

2.1.1.12 J8 Configuration

If using a device that supports I/O level shifting with a V_{IO} pin on pin 5, this jumper can be used to provide power to pin 5. A shunt can be placed between pins 1 and 2 of J8 to short V_{CC} and V_{IO} together and allow V_{CC} to power V_{IO}.

2.1.1.13 SIC Network Configuration (J4 & J5)

The SIC network can be enabled connecting shunts to J4 and J5. This connects the network of inductors, capacitors, and resistors to the CANH and CANL lines and create a much noisier CAN bus. Note that both J4 and J5 need to be shunted for this to work. All SIC network components are left open and need user installation.

2.1.2 Using CAN Bus Load, Termination, and Protection Configurations

The generic 8-pin CAN EVM is populated with one 120Ω resistor selectable via jumper, between CANH and CANL, and the 120Ω split termination (two 60Ω resistors in series) including the split capacitor. When using only split termination, the EVM is used as a terminated end of a bus. For electrical measurements to represent the total loading of the bus, use both the split termination and the 120Ω resistor in parallel to give the standard 60Ω load for parametric measurement. Table 2-3 summarizes how to use these termination options.

Table 2-3. Bus Termination Configuration

Termination Configuration	120Ω Resistor	Split Termination Resistors		Split Termination Capacitor
	J6	R10	R14	C3
60Ω load - electrical parameterics	shorted	60Ω	60Ω	populated
Split termination (common mode stabilization)	open			

The EVM also has footprints for various protection schemes to enhance robustness for extreme system-level EMC requirements. Table 2-4 summarizes these options.

Table 2-4. Protection and Filtering Configuration

Configuration	Footprint Reference	Use Case	Population and Description
Series resistors or common mode choke	R8/R12 or L1 (common footprint)	Direct CAN transceiver to bus connection	R8 and R12 populated with 0Ω (default population)
		Series resistance protection, CAN transceiver to bus connection	R8 and R12 populated with MELF resistor as necessary for harsh EMC environment
		CM choke (bus filter)	L1 populated with CM choke to filter noise as necessary for harsh EMC environment
Bus filtering caps transient protection	C2/C4	Bus filter	Filter noise as necessary for harsh EMC environment. Use filter caps in combination with L1 CM choke
	D1	Transient and ESD protection	To add extra protection for system level transients and ESD protection, D1 populated with ESD2CAN24-Q1

2.1.3 Using Customer Installable I/O Options for Current Limiting, Pullup and Pulldown, Noise Filtering

The generic 8-pin CAN EVM has footprints on the PCB for the installation of various filtering and protection options to adapt the EVM to match CAN network topology requirements if the EVM is being used as a CAN node.

Each digital input or output pin has footprints allowing for series current-limiting resistors (default populated with 0Ω), pullup or down resistors (depending on pin use), and a capacitor to GND which allows for RC filters when configured with a series resistor. Table 2-5 lists these features for each of the digital input and output pins of the EVM. Replace or populate the RC components as necessary for the application.

Table 2-5. RC Filter and Protection Lists

Device Pin			Jumper		Series R	Pullup and Pulldown	C to GND	Description
No.	Description	Type	Pullup	Pulldown				
1	TXD	Input	N/A	N/A	R16	R15 PU/ R18 PD	C5	
4	RXD	Output	N/A	N/A	R21	R20 PU/ R22 PD	C9	
5	NC	No Connect	N/A	N/A	N/A	N/A	N/A	
	SHDN, AB, EN, and LBK	Input	R1/R2 (J1)	R4/R5 (J1)	N/A	N/A	C1	
	FAULT	Output	R1/R2(J1)	R4/R5 (J1)	N/A	N/A	C1	
	V_{REF} and SPLIT	Output	N/A	N/A	N/A	N/A	C1/C3	Split termination: J1 to route output to split termination center point capacitor C3. EMC for systems not using split termination: C1 to GND.
	V_{IO} and V_{RXD}	Supply Input	N/A	N/A	N/A	R2 PU/ R4 PD	C1/C10/C18	Use J3, J8, P1 and TP9 as necessary to provide supply input.
8	SW, R_S, S, STB	Input	R6/R7 (J2)	R9/R11 (J2)	N/A	N/A	N/A	R9 pulldown to GND (J2) user-installable for use with slope mode on devices with R_S pin.
	NC	No Connect	N/A	N/A	N/A	N/A	N/A	

3 Hardware Design Files

3.1 Schematics

Figure 3-1 shows the EVM schematic.

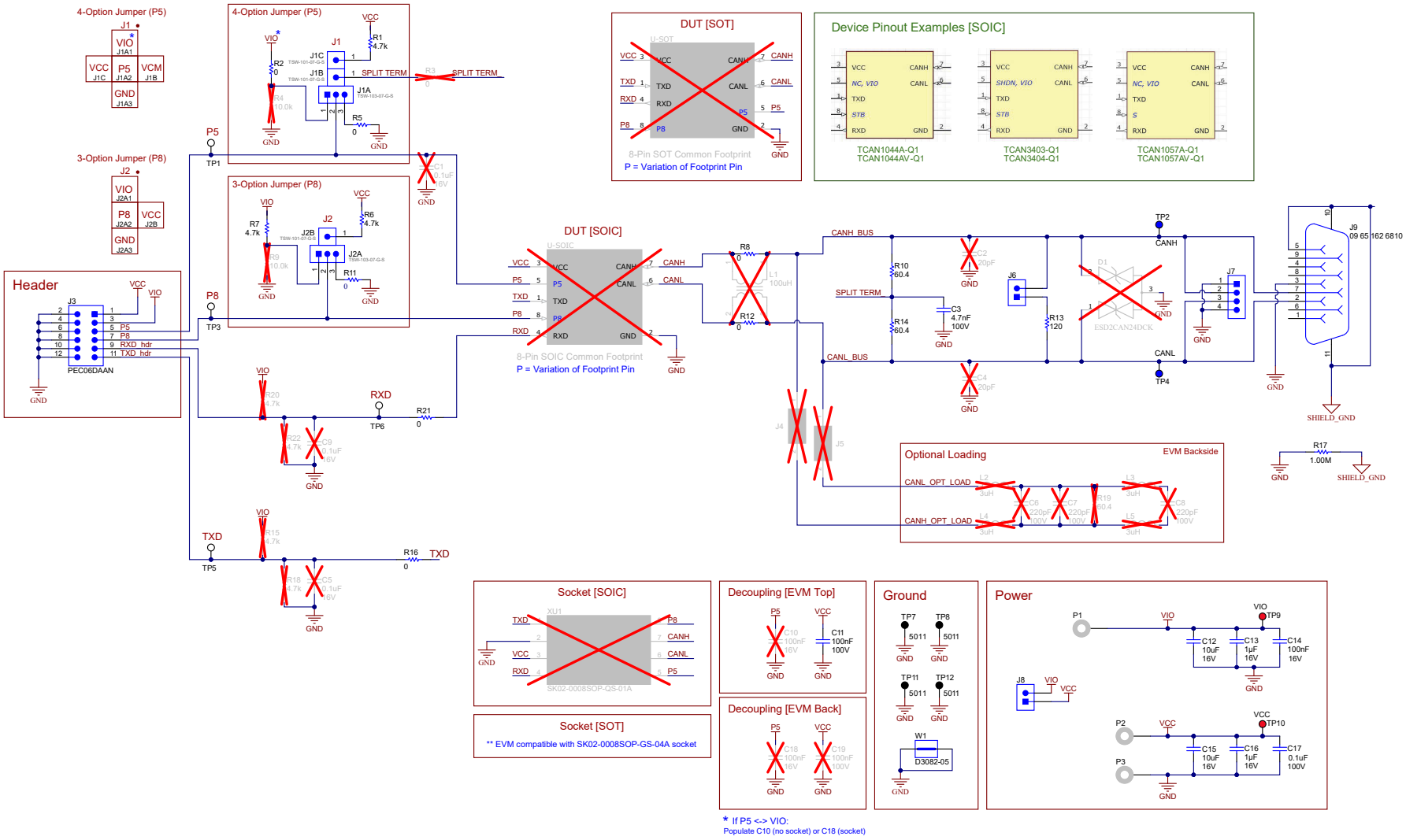


Figure 3-1. EVM Schematic

3.2 PCB Layouts

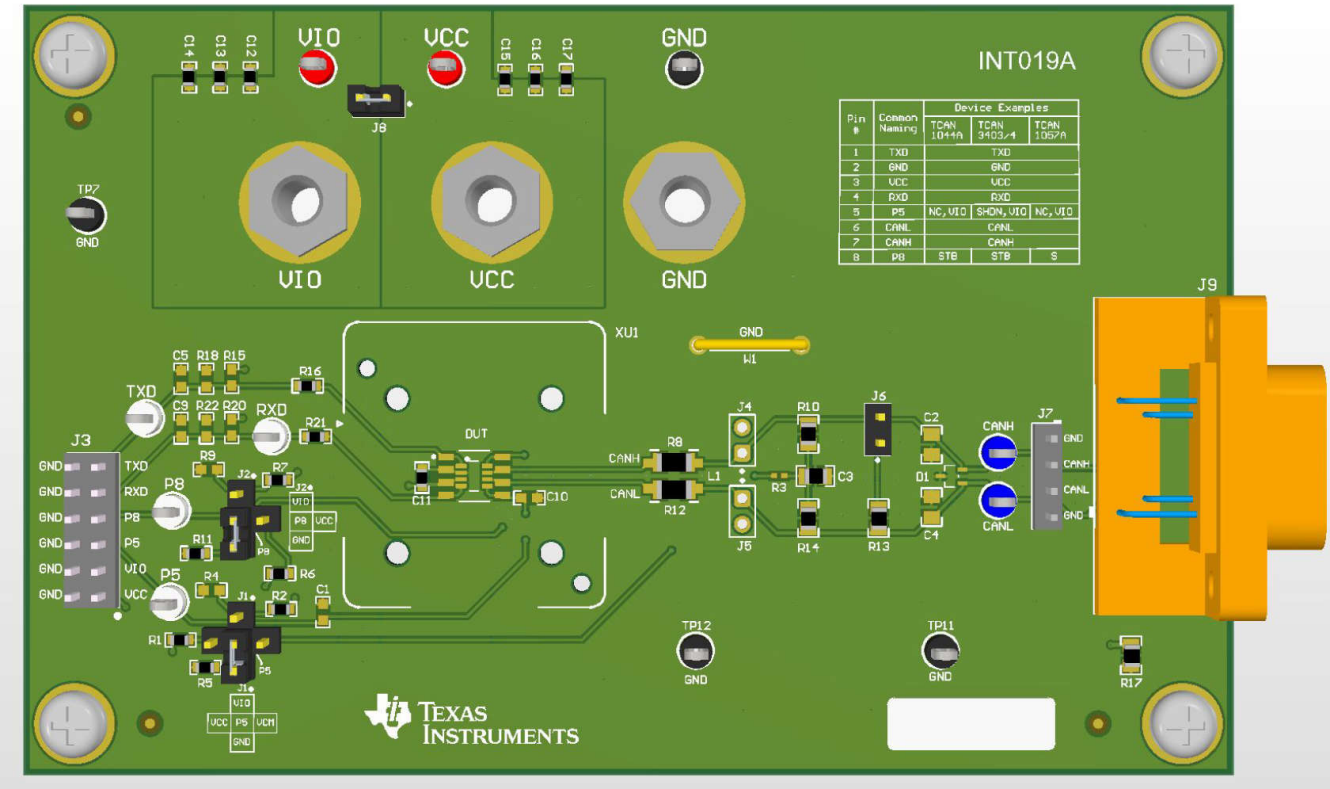


Figure 3-2. EVM Layout (Top View)

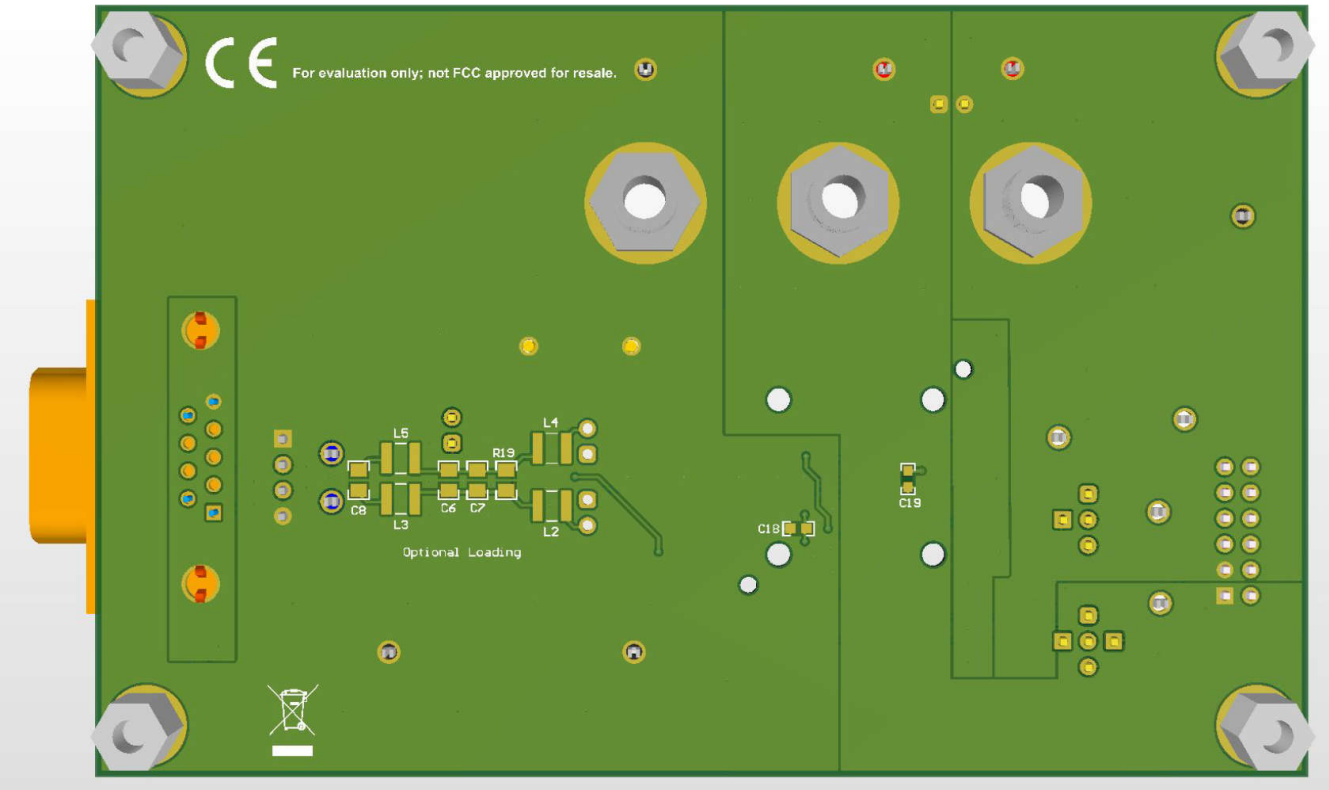


Figure 3-3. EVM Layout (Bottom View)

3.3 Bill of Materials (BOM)

Table 3-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C3	1	4700pF	CAP, CERM, 4700pF, 100V, +/- 10%, X7R, 0805	805	08051C472KAT2A	AVX
C11	1	0.1uF	CAP, CERM, 0.1uF, 100V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	GCJ188R72A104KA01D	MuRata
C12, C15	2	10uF	CAP, CERM, 10uF, 16V, +/- 20%, X5R, 0603	603	GRM188R61C106MAALD	MuRata
C13, C16	2	1uF	CAP, CERM, 1uF, 16V, +/- 10%, X7R, 0603	603	C1608X7R1C105K080AC	TDK
C14	1	0.1uF	CAP, CERM, 0.1µF, 16V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	0603YC104K4T4A	AVX
C17	1	0.1uF	CAP, CERM, 0.1uF, 100V, +/- 10%, X7S, AEC-Q200 Grade 1, 0603	603	CGA3E3X7S2A104K080AB	TDK
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1A, J2A	2		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J1B, J1C, J2B	3		Header, 100mil, 1pos, Gold, TH	Test point	TSW-101-07-G-S	Samtec
J3	1		Header, 100mil, 6x2, Tin, TH	Header, 6x2, 100mil, Tin	PEC06DAAN	Sullins Connector Solutions
J6, J8	2		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J7	1		Header, 100mil, 4x1, Tin, TH	Header, 4x1, 100mil, TH	PEC04SAAN	Sullins Connector Solutions
J9	1		D-Sub-9, 11Pos, Male, TH	D-Sub-9, 2rows, Male, TH	09 65 162 6810	Harting
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
P1, P2, P3	3		Standard Banana Jack, Uninsulated, 15A	Banana Jack	108-0740-001	Cinch Connectivity
R1, R6, R7	3	4.7k	RES, 4.7 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06034K70JNEA	Vishay-Dale
R2, R5, R11, R16, R21	5	0	RES, 0, 0%, 0.25 W, AEC-Q200 Grade 0, 0603	603	PMR03EZPJ000	Rohm

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R8, R12	2	0	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	CRCW12060000Z0EA	Vishay-Dale
R10, R14	2	60.4	RES, 60.4, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	CRCW080560R4FKEA	Vishay-Dale
R13	1	120	RES, 120, 5%, 0.5 W, 0805	805	ERJ-P06J121V	Panasonic
R17	1	1.00Meg	RES, 1.00M, 1%, 0.125W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1004V	Panasonic
SH-J1, SH-J2, SH-J8	3		Shunt, 2.54mm, Gold, Black	Shunt, 2.54mm, Black	60900213421	Wurth Elektronik
TP1, TP3, TP5, TP6	4		Test Point, Multipurpose, White, TH	White Multipurpose Test point	5012	Keystone Electronics
TP2, TP4	2		Test Point, Multipurpose, Blue, TH	Blue Multipurpose Test point	5127	Keystone Electronics
TP7, TP8, TP11, TP12	4		Test Point, Multipurpose, Black, TH	Black Multipurpose Test point	5011	Keystone Electronics
TP9, TP10	2		Test Point, Multipurpose, Red, TH	Red Multipurpose Test point	5010	Keystone Electronics
W1	1		1mm Uninsulated Shorting Plug, 10.16mm spacing, TH	Shorting Plug, 10.16mm spacing, TH	D3082-05	Harwin
C1, C5, C9, C10, C18	0	0.1uF	CAP, CERM, 0.1uF, 16V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	CGJ3E2X7R1C104K080AA	TDK
C2, C4	0	20pF	CAP, CERM, 20pF, 100V, +/- 5%, C0G/NP0, 0805	805	08051A200JAT2A	AVX
C6, C7, C8	0	220pF	CAP, CERM, 220pF, 100V, +/- 5%, C0G/NP0, 0805	805	C0805C221J1GACTU	Kemet
C19	0	0.1uF	CAP, CERM, 0.1µF, 100V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	HMK107B7104KAHT	Taiyo Yuden
D1	0		24V, 2-Channel ESD Protection Diode for In-Vehicle Networks, SC70-3	SC70-3	ESD2CAN24DCK	Texas Instruments
J4, J5	0		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
L1	0	100uH	Inductor, Ferrite, 100uH, 0.15A, 2 ohm, SMD	SMD, 4-Leads, Body 4.7 x 3.7mm	ACT45B-101-2P-TL003	TDK

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
L2, L3, L4, L5	0	3uH	Ind Chip Wirewound 3uH 5% 7.9MHz 20Q-Factor Ceramic 300mA 1210 T/R	1210	AISC-1210-3R0J-T	Abracon
R3	0	0	RES, 0, 5%, 0.063 W, 0402	402	RC0402JR-070RL	Yageo America
R4, R9	0	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	RMCF0603FT10K0	Stackpole Electronics Inc
R15, R18, R20, R22	0	4.7k	RES, 4.7 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06034K70JNEA	Vishay-Dale
R19	0	60.4	RES, 60.4, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	CRCW080560R4FKEA	Vishay-Dale
SH-J3, SH-J4, SH-J5, SH-J6, SH-J7	0		Shunt, 2.54mm, Gold, Black	Shunt, 2.54mm, Black	60900213421	Wurth Elektronik
U-SOIC	0		Fault-Protected CAN FD Transceiver with Signal Improvement Capability (SIC) and Standby Mode	SOIC8		Texas Instruments
U-SOT	0		Automotive High Speed CAN Transceiver	SOT23-8		Texas Instruments
XU1	0		Socket, SOIC-8, 1.27mm Pitch	Socket, SOIC-8, 1.27mm Pitch	SK02-0008SOP-QS-01A	RS Tech Incorporated

4 Additional Information

All TI's 8-pin CAN transceivers supported by this EVM are listed on ti.com: CAN transceivers.

4.1 Trademarks

All trademarks are the property of their respective owners.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2024) to Revision A (September 2024)	Page
• Added *Feature* for SOIC and SOT packages	1
• Updated the *Bill of Materials* line item for U-SOT	10

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265