Practical Guidelines to Designing an EMI Compliant PoE Powered Device with Isolated Flyback

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1.1 Introduction

Power over Ethernet (PoE), as defined in the IEEE 802.3-2005 (clause 33) standard, provides both data and power over unshielded twisted-pair copper wiring, such as Category 5 (CAT-5) cable. Power is supplied to the cable by Power Sourcing Equipment (PSE) that may be located at the Ethernet router/hub or between the router/hub and the Powered Device (PD). The PSE applies a nominal 48 VDC to the CAT-5 cable after a process that confirms a PD is connected. The PD typically includes a DC/DC converter that converts the 48 VDC to voltages required by the PD circuitry.

The PD needs to comply with EMC standards, such as that defined by EN 55022 / CISPR 22, in order to be sold in many markets. The EN 55022 / CISPR 22 standard establishes limits for both conducted emissions and radiated emissions. The limits are defined for Class A (commercial) and Class B (residential) equipment, with Class B being the more stringent. The conducted emissions generated by a PD, which is considered to be a telecommunication port, are measured as common-mode disturbances on the CAT-5 cable. The radiated emissions associated with a PD can be in the form of emissions radiating from the CAT-5 cable as a result of the PD's conducted common-mode noise (i.e. antenna mode disturbances), or emissions that radiate directly from the PD itself.

DC/DC converters used in PD applications can be sources of conducted and radiated emissions. The PD should employ design techniques to mitigate or eliminate potential emissions associated with its DC/DC converter. This application report presents some practical guidelines that can be followed to obtain an EMI compliant PD. These guidelines are illustrated by working through an actual design example of an isolated flyback converter employing the Texas Instruments TPS23750. The TPS23750 includes an IEEE 802.3-2005 compliant PD front-end and a DC/DC controller. Refer to datasheet SLVS590 and user's guide SLVU137 for more information on using the TPS23750.

1.2 PD Design Example Schematic

Figure 1-1 shows a schematic of the circuit used to demonstrate the EMI guidelines presented in this application report. The circuit uses the TPS23750 in an isolated flyback converter topology to produce a 3.3V at 3A output. The IEEE 802.3-2005 standard requires that circuits connected to the 10/100Base-T Ethernet port be isolated from all external electrical connections that can be touched by users or connected to other equipment. PDs without these connections may use non-isolated converters for their simplicity, while isolated converter topologies are used to otherwise meet the standard or for their added layer of safety to users. Refer to application report SLUA454 for more information on EMI guidelines for non-isolated converters.

The schematic is shown to be divided into three separate sections (input, intermediate, and power) to facilitate discussion of the EMI guidelines. The input section on the left side of the schematic is considered to be the "quiet side" of the circuit, while the power section on the right side of the schematic is considered to be the "noisy side" of the circuit. It's desirable to maintain both physical and electrical (filtering) separation between these two sides of the circuit in order to keep conducted and radiated noise from entering the input-related circuitry (which connects to the CAT-5 cable).

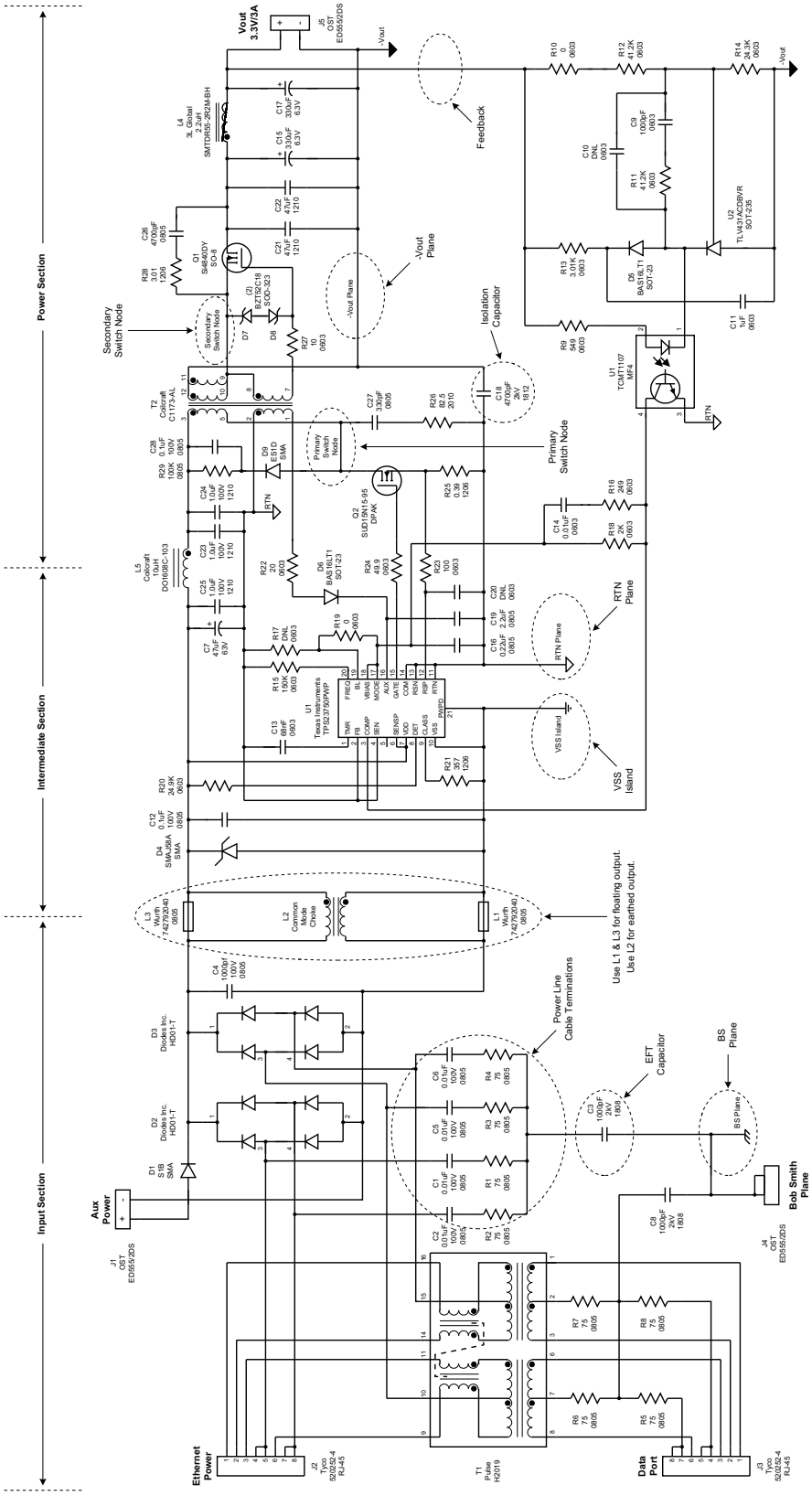

Figure 1-1. TPS23750 Isolated Flyback Converter Schematic

1.3 PD Design Example Circuit Board Layout

The board layout used for the circuit of Figure 1-1 is shown in Figure 1-2 through Figure 1-4. The board is 2” x 4” in size and consists of two layers of 2 oz. copper on a FR-406 substrate with an overall thickness of 0.062”. A photo of the actual circuit board assembly is shown in Appendix A.

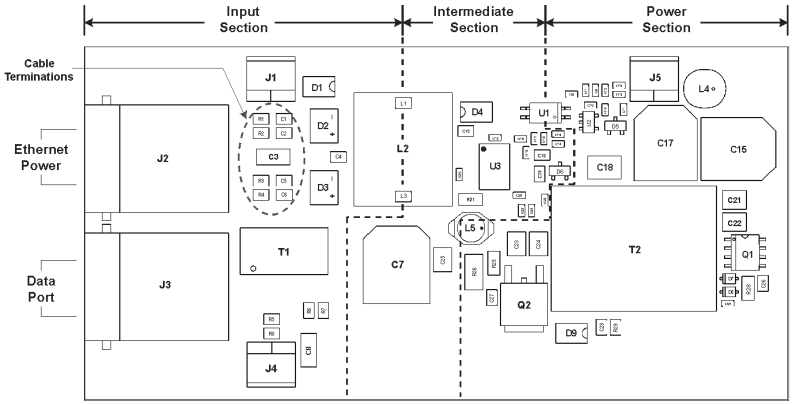

Figure 1-2. Component Layout

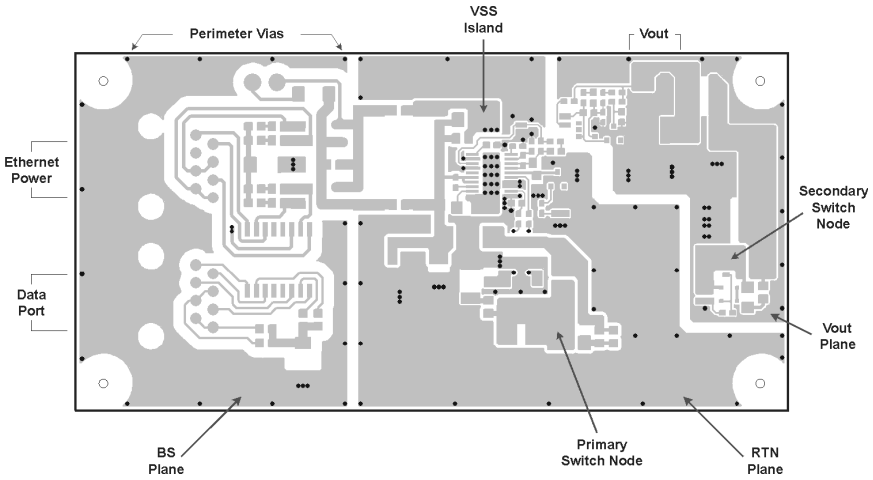

Figure 1-3. Top-Side Copper

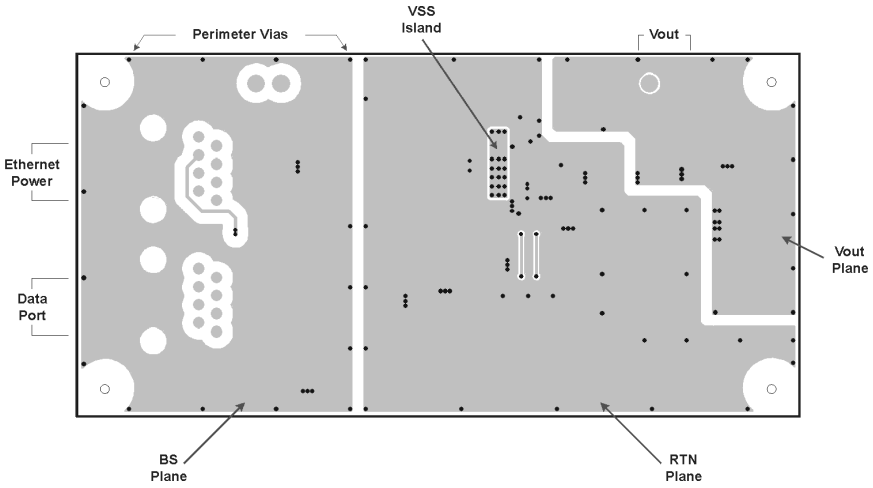

Figure 1-4. Bottom-Side Copper (Viewed Through Top)

1.4 Input Section

Referring to Figure 1-2 through Figure 1-4, the input section is shown to comprise components that are typically used for the front-end of PD applications. For EMI considerations, the guidelines below were followed for this section of the circuit:

- Congregate the input-related components toward the RJ-45 input connectors.
- Include the 75 Ω / 0.01 μF Bob Smith cable terminations on the input power lines as shown.
- Include the 1000 pF 2kV bypass capacitor (C3) to tie the Bob Smith cable terminations to a copper plane (shield) which is commonly referred to as the Bob Smith plane (BS plane). Connect C3 to the BS plane using dedicated vias located directly at the capacitor termination.
- Treat the BS plane as a phantom or literal earth connection and use it to create a top and bottom layer ground plane that surrounds the input-related circuitry. Maintain a 0.060” high voltage spacing between the BS plane and all other circuitry.
- Use a number of perimeter vias to stitch the top and bottom layers of the BS plane together.
- Include the PoE transformer (T1) with internal common-mode chokes (most common topology available from magnetics suppliers).
- To minimize the possibility of radiated and magnetic coupling into the input section (from the power section), do not oversize the copper traces interconnecting the input-related components. Size the traces so that they meet current handling and thermal requirements without being excessive.
- Include provisions for inserting ferrite beads (L1/L3) to separate the input and intermediate sections of the circuit. Along with acting as high frequency filters, the beads also serve to isolate the lower input impedance of the PD from the Bob Smith termination impedance. If not needed, the beads could always be replaced by zero ohm resistors.
- For applications where the isolated output voltage is referenced to earth, include provisions for a common-mode choke (L2) that may need to be used in place of the above-mentioned ferrite beads. The affect of referencing the output to earth is further discussed in Section 1.9.
- Include provisions for a ceramic capacitor (C4) at the output of the diode bridges (D2/D3) to form a filter with the ferrite beads. C4 would typically be on the order of 1000 pF. The combined value of C4 and C12 (intermediate section) should not exceed 0.12 μF to be IEEE 802.3-2005 compliant.

The 75 Ω impedance matching resistors used for the cable terminations are routinely employed in Ethernet applications to minimize EMI and reduce susceptibility (see Section 1.13, Reference 5). The 0.01 μF capacitors used for the cable terminations are required for PoE applications in order to AC couple the 75 Ω resistors (since DC is present in a PoE system). Although the 1000 pF 2 kV bypass capacitor has historically been used to reduce susceptibility in PD applications, it seems reasonable that it would also have the reciprocal affect of suppressing EMI. A closer look at the schematic reveals that the combination of this bypass capacitor and the cable terminations appears to resemble a “Y-capacitor” type of circuit which is commonly used to suppress common-mode noise in mains port applications. The return end of a Y-capacitor circuit is typically connected to earth or chassis ground. The above-mentioned BS plane was introduced in the design example to emulate such a connection. For some earthed applications, the BS plane might actually be physically connected to earth. For unearthed applications, the BS plane is intended to present itself as a phantom earth connection. For either instance, the BS plane might also be connected to a shielded enclosure (chassis ground).

1.5 Intermediate Section

Referring to Figure 1-2 through Figure 1-4, the intermediate section of the circuit is shown to comprise the PoE interface and DC/DC controller circuitry. For EMI considerations, the guidelines below were followed for this section of the circuit:

- Include the 0.1 μF filter capacitor (C12) which is also required to be IEEE 802.3-2005 compliant.
- Include the LC filter (L5/C7/C25) to separate the intermediate and power sections of the circuit. The filter attenuates the input ripple generated by the DC/DC converter located in the power section. The “winding start” of L5 should be connected to the input side of the DC/DC converter in order to keep the relatively noisy end of the winding embedded within the innermost section of L5. The inductor manufacturer’s data sheet should be consulted to determine the location of the winding start and its relationship to any markings on the inductor. The proper orientation of the inductor should be specified in production to ensure consistent EMI performance.

- Orient the TPS23750 IC (U1) so that pins 1-10 (input-related) are toward the input side of the board and pins 11-20 (output-related) are toward the output side of the board.
- Locate the peripheral components associated with U1 in close proximity to the IC, making short and direct connections to the IC's pins to eliminate any possibility of erratic or unstable operation.
- Locate the AUX bypass capacitor (C19) so as to create a short compact path between the AUX pin of U1 and the return side of the current sense resistor (R25). The AUX pin of U1 is the supply for the internal gate driver and C19 provides the high frequency energy for the gate drive pulses to the MOSFET (Q2). Gate drive paths are often overlooked sources of EMI.
- Include provisions for a gate resistor (R24) to connect the gate output of U1 to the gate of Q2. The resistor provides a level of control over EMI by adjusting the slew rate of Q2. It can play a role in controlling both conducted and radiated emissions. The resistor value, which is typically 10 to 75 ohms, can be optimized to balance efficiency and EMI margins.
- Create a top-side and bottom-side ground island (VSS island) for the VSS connections associated with pin 10 of U1. Size the VSS island to make direct connections to the VSS-related components and to provide heat-sinking for the power pad of U1 without being excessive.
- Create a top-side and bottom-side ground plane (RTN plane) for the RTN connections associated with pin 11 of the U1. Use the RTN plane as the main ground plane associated with the intermediate and primary-side power sections of the board. Ideally, the bottom side of the RTN plane should be as uninterrupted as possible. Allow the top-side of the RTN plane to flood into unused areas and surround the intermediate and primary-side power circuitry, creating a return shield for any stray radiated noise.
- Use multiple perimeter vias to stitch the top and bottom layers of the RTN plane together. To eliminate any possibility of erratic or unstable operation, locate the output feedback circuitry away from the power section components.
- Use dedicated vias to connect the return end of each bypass/decoupling capacitor to its respective ground plane. Locate the vias directly at the capacitor termination to create a low impedance return path. Use multiple vias for gate drive and power related capacitors such as C19 and C25.

1.6 Power Section

Referring to Figure 1-2 through Figure 1-4, the power section of the circuit is shown to comprise the DC/DC converter which can be a main source of EMI due to its inherently high dv/dt and di/dt operation. For EMI considerations, the guidelines below were followed for this section of the circuit:

- Include the high frequency ceramic capacitors (C23/C24) on the right side of L5. These capacitors provide the high frequency pulsating current for the DC/DC converter. The magnitude of the peak-to-peak AC ripple voltage developed across these capacitors, which can contribute to EMI, is inversely proportional to the capacitance and proportional to the ESR of the capacitors. The capacitors should be physically located to create a compact, low-inductive path between the RTN side of R25 (i.e. Q2 return path) and the flyback transformer primary winding (T2 pin 3). This minimizes any EMI-generating voltage spikes that can be caused by the relatively high di/dt operation associated with this circuit path.
- Use multiple vias to connect the RTN side of C23/C24 to the RTN plane in order to create a low impedance return path for any stray radiated noise picked up by the above-mentioned RTN plane.
- While maintaining the proper isolation requirement between primary and secondary, allow the RTN plane copper to flow under the T2 flyback transformer to provide an added level of shielding. This would preferably be accomplished using both top-side and bottom-side copper. top-side copper associated with the RTN plane was allowed to flood under T2 of the design example after confirming that the outer winding of the transformer was primary referenced (primary-side bias winding) and that high voltage tape was also used to wrap the transformer.
- Use compact, low-inductive paths for all connections to the power-related components to minimize any EMI-generating voltage spikes and any possible higher frequency ringing that can be related to circuit board and component parasitics. The main power paths to consider are the primary-side Q2 path and the secondary-side Q1 path. The component flows associated with the two paths are summarized as follows:
  - Q2 path: C23/C24 → T2 primary → Q2 → R25 → C23/C24
  - Q1 path: T2 secondary → Q1 → C21/C22/C15 → T2 secondary.

- The connection between Q2 and T2 is commonly referred to as the “primary switch node” of an isolated converter. The voltage on this node switches from 0V to approximately 2 x Vin in typically 50 ns. Due to this high dv/dt operation, the primary switch node can potentially be the largest contributor to EMI. The circuit board copper connected to the primary switch node presents itself as a radiating surface capable of radiating significant EMI. This problem is usually complicated by the fact that this copper is also used to provide heat-sinking for the primary switch node components. The amount of copper used for the primary switch node should be optimized to minimize the size of the EMI radiating surface, while still providing adequate heat-sinking. An effective technique for reducing the radiating surface area is to hide a portion of the switch node copper under shielded magnetics, such as the flyback transformer (T2).
- Include provisions for an RC snubber (R26/C27) across Q2. The snubber might be used to dampen any higher frequency ringing that may be present on the primary switch node due to circuit board and component parasitics. It can play a role in controlling both conducted and radiated emissions. This RC snubber was used in conjunction with the D9/R29/C28 clamp snubber in the design example. The clamp snubber acts to limit the peak voltage of the primary switch node, while the RC snubber controls the rate of rise and dampens any ringing.
- The connection between Q1 and T2 is commonly referred to as the “secondary switch node” of an isolated converter. The dv/dt operation of this node can also be a contributor to EMI. The above-mentioned guidelines discussed for the primary switch node should also be applied for the secondary switch node.
- Include provisions for an RC snubber across Q1. Like the primary-side RC snubber across Q2, this snubber might be used to dampen any higher frequency ringing that may be present on the secondary switch node due to circuit board and component parasitics.
- Include provisions for a gate resistor (R27) to connect the secondary bias winding of T2 to the gate of Q1. The resistor might be used to dampen any ringing associated with this transformer-driven gate drive signal. The value of R27 would typically be on the order of 10 Ω.
- Create a top-side and bottom-side ground plane ($-V_{OUT}$ plane) for the $-V_{OUT}$ connections associated with the secondary-side circuitry. Ideally, the bottom side of the $-V_{OUT}$ plane should be as uninterrupted as possible. Allow the top-side of the $-V_{OUT}$ plane to flood into unused areas and surround the secondary-side circuitry, creating a return shield for any stray radiated noise. Like the primary-side RTN plane, use multiple perimeter vias to stitch the top and bottom layers of the $-V_{OUT}$ plane together.
- Connect the “winding start” of L4 to Q1 in order to keep the noisier end of the winding embedded within the innermost section of L4. The outermost section of the winding would then be connected to the DC output, providing some level of shielding. The inductor manufacturer’s data sheet should be consulted to determine the location of the winding start and its relationship to any markings on the inductor. The proper orientation of the inductor should be specified in production to ensure consistent EMI performance.
- Provide heat-sinking for the “quiet end” of power components where possible. This is related to the primary and secondary switch node discussions above. In an effort to minimize the EMI radiating surface presented by the copper area of each switch node, additional heat-sinking of the power components can be provided by placing copper at the relatively quiet end of the component.
- Include the high voltage isolation capacitor (C18) that connects between the $-V_{OUT}$ plane (secondary) and the RTN plane (primary). This capacitor suppresses EMI by providing a return path for noise that is coupled across the flyback transformer. Provide low impedance connections from each plane to the capacitor by using multiple vias located directly at the capacitor terminations. The value of C18 is typically on the order of 1000 pF to 0.01 μF.

1.7 Conducted Emissions Pre-Compliance Test Setup

Figure 1-5 shows a block diagram and Figure 1-6 shows a photo of the pre-compliance test setup that was used to measure the conducted emissions of the design example. The test setup was constructed per EN 55022:1998 - Figure 4. An Impedance Stabilization Network (ISN) specifically designed to perform conducted emissions tests on balanced pair telecommunication lines was used. The EMC Analyzer was programmed with the proper correction factors to account for the attenuation characteristics of the ISN, the coax cable, and the Transient Limiter.

The conducted emissions test was performed under full power conditions by connecting a 10-W resistive load to the output of the isolated flyback converter. In order to simulate a worst case scenario, the test was performed with no reliance on a shielded enclosure as shown in the photo. The emissions were measured against the more stringent Class B requirement of the EN 55022 / CISPR 22 standard.

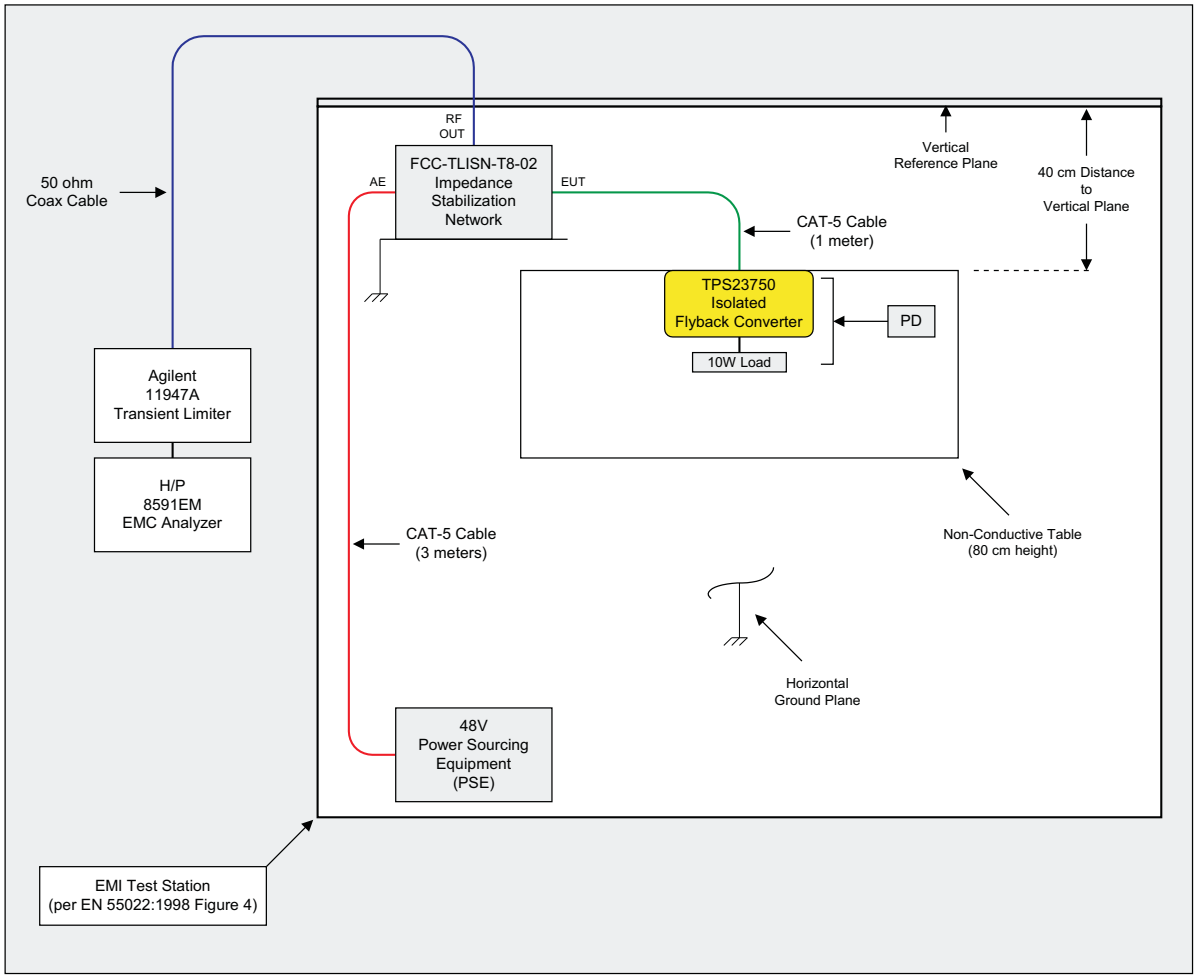

Figure 1-5. Conducted Emissions Pre-Compliance Test Setup Block Diagram

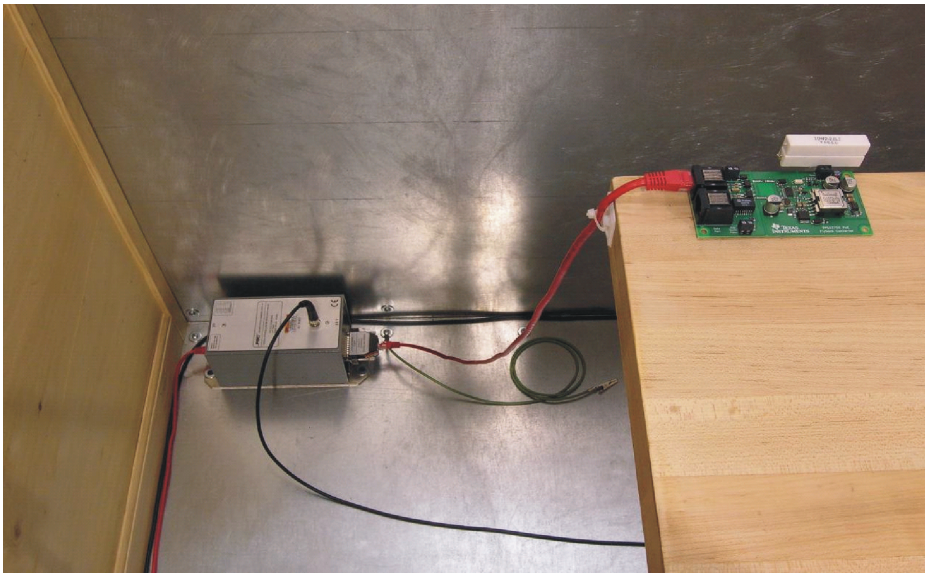

Figure 1-6. Conducted Emissions Pre-Compliance Test Setup Photo

1.8 Conducted Emissions Results

The results of the pre-compliance conducted emissions test for the design example are shown in Figure 1-7. The peak detector mode of the H/P 8591EM EMC analyzer was used to be conservative. The peak measurements are seen to be approximately 25dB below the Class B quasi-peak limit and approximately 15dB below the Class B average limit. These margins comfortably meet the 6dB to 10dB minimums that are typically used by the industry. The added margin at 30 MHz is a reasonable indicator that radiated emissions will also be low.

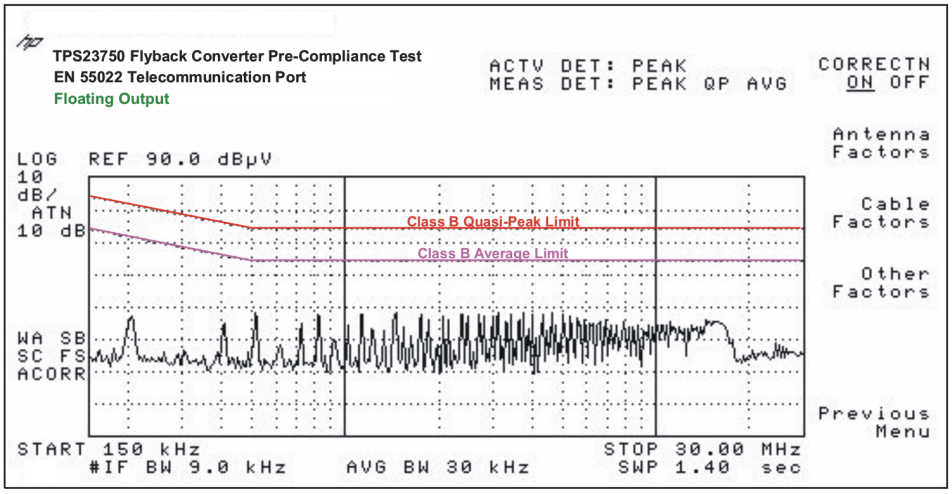

Figure 1-7. TPS23750 Flyback Converter Conducted Emissions Results

The above results were obtained with the output of the flyback converter floating, which is considered to be a typical configuration for most PoE PD applications. Referring to the schematic of Figure 1-1, ferrite beads L1 and L3 were loaded and common-mode choke L2 was not loaded for this floating output condition.

1.9 Referencing Converter Output to Earth

In some PD applications, the output of its isolated DC/DC converter might be referenced to earth ground using an earthing wire. Conducted EMI generally worsens under these conditions due to creating a second path for the flow of common-mode noise current as indicated by i_2 in Figure 1-8.

The i_2 current is shown to flow from the converter to earth ground through the application's earthing wire, from earth ground to the CAT-5 cable through the RF measurement resistors associated with the ISN and spectrum analyzer, and from the CAT-5 cable through the PD input back to the converter. This second noise current path is shown to run in parallel with noise current i_1 which is normally present to some extent due to the converter's capacitive coupling to earth, C_{PD-E}. The i_1 noise current is also present for floating output configurations.

As a result of earthing the output, the added noise current due to i_2 causes an increased voltage to be developed across the RF measurement resistors. This voltage increase would typically be more apparent within the low to mid range of the measured frequency span due to the inductance associated with the earthing wire. At low to mid frequencies, the earthing wire would appear as a low impedance and allow more i_2 noise current to flow. At higher frequencies, the impedance of the earthing wire would increase to a point where most of the total noise current would revert back to i_1 (i.e. current through C_{PD-E}), which would then be similar to a floating output configuration.

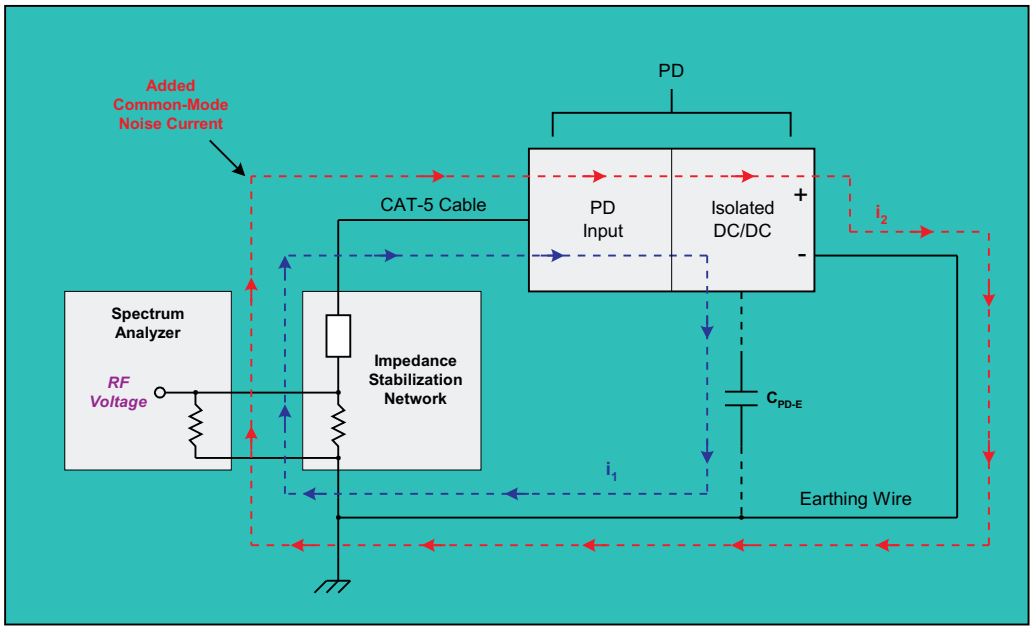

Figure 1-8. Earthed Output Common-Mode Noise Current Path

The above discussion of Figure 1-8 was confirmed by connecting $-V_{OUT}$ (and the BS plane) of the design example to earth ground using a 1-meter earthing wire. As in the case of Figure 1-7, ferrite beads L1 and L3 were loaded and common-mode choke L2 was not loaded. The results of this earthed output condition are shown in Figure 1-9.

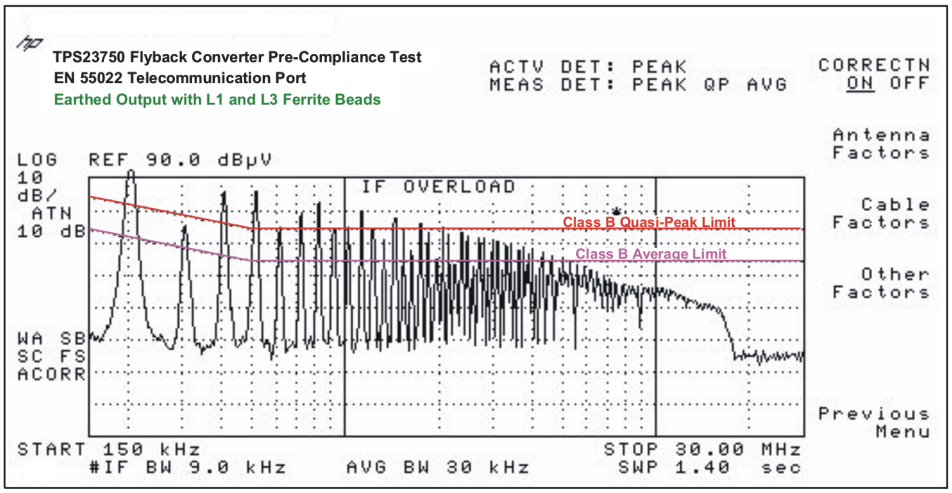

Figure 1-9. Conducted Emissions with Ferrite Beads and Earthed Output

In order to suppress the increased conducted emissions caused by the earthed output condition, it seems reasonable that an appropriate impedance could be placed in series with the added current path shown in Figure 1-8 in order to make the path less inviting for the common-mode noise currents. This is normally accomplished by placing a common-mode choke at the front-end of the DC/DC converter. In some situations, this might also be accomplished by inserting a ground inductor in series with the earthing wire, although this method would usually require a larger value of inductance. A common-mode choke would provide the added benefit of being in series with both the i_1 and i_2 currents, while the ground inductor would only be in series with i_2. These insertion impedance options are illustrated in Figure 1-10.

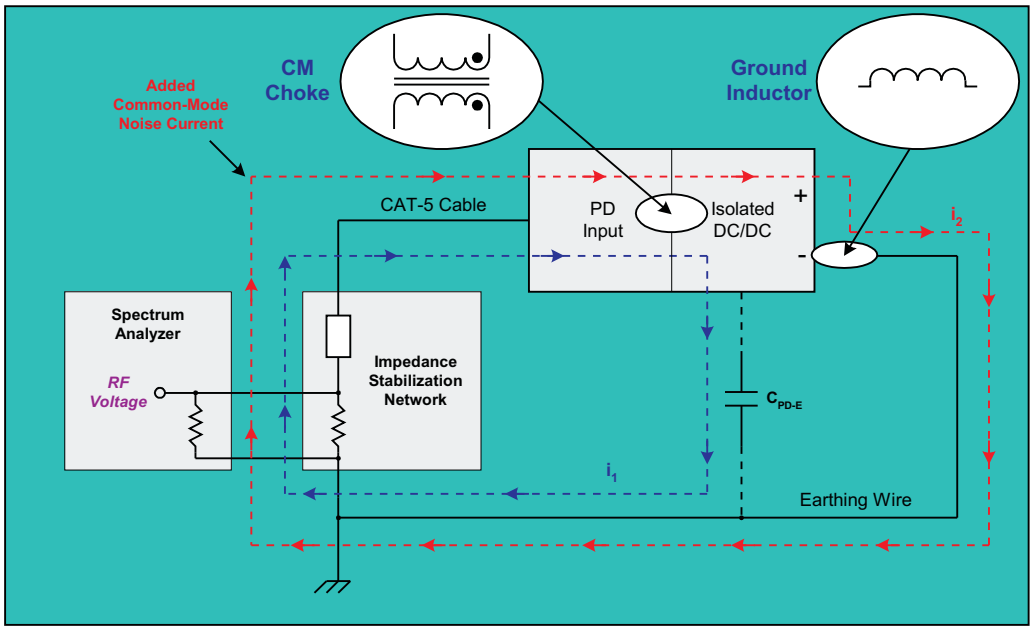

Figure 1-10. Earthed Output Insertion Impedance Options

The effect of using a common-mode choke for the earthed output condition was tested by removing the L1 and L3 ferrite beads and loading a Pulse PE-53913NL common-mode choke for L2 in the design example. The pre-compliance test results are shown Figure 1-11. The highest peak measurement is seen to be approximately 15dB below the Class B average limit.

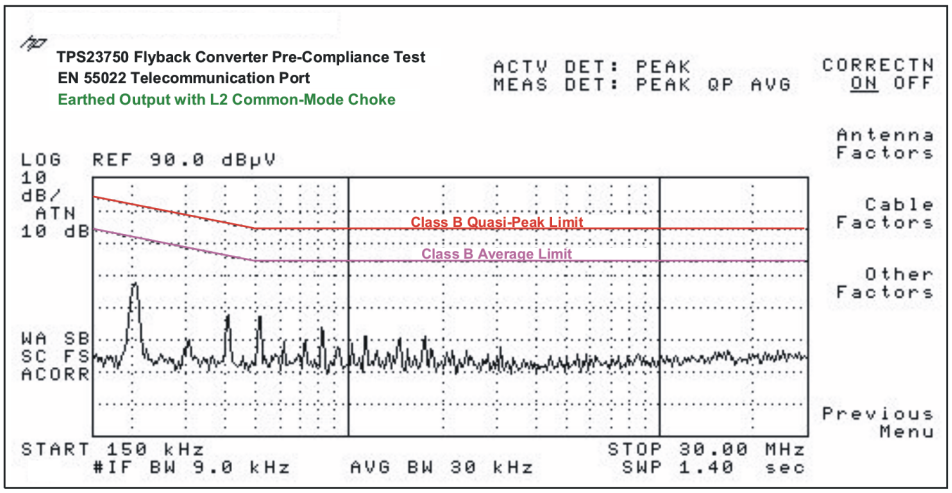

Figure 1-11. Conducted Emissions with Common-Mode Choke and Earthed Output

The impedance curve of the common-mode choke needs to be considered when selecting it for the application. The above common-mode choke used for the design example had an impedance curve that peaked at approximately 6 kΩ at 200 kHz, which was coincident with the frequency of the highest offending peak for the earthed output condition. Other chokes might be considered depending on the amount of margin desired. In some instances, the value of the C18 isolation capacitor discussed in Section 1.6 can be adjusted to accommodate chokes with different impedance curves. For example, 10dB of margin was obtained for the design example when using a smaller Wurth 744272392 common-mode choke in combination with increasing C18 from 4700 pF to 0.01 µF.

1.10 Radiated Emissions

Radiated emissions associated with a PD can be in the form of antenna mode disturbances from the CAT-5 cable or emissions that radiate directly from the PD itself. The antenna mode disturbances should be addressed by meeting the common-mode conducted emissions requirements of the EN 55022/ CISPR 22 standard. As mentioned in Section 1.8, having a significant amount of margin at the 30 MHz upper end of the conducted emissions span is a reasonable indicator that emissions radiated directly from the PD will also be low. The following guidelines can be considered if further adjustments to radiated emissions are required:

- Use an oscilloscope to see if any higher frequency ringing is present on any of the switching waveforms. This ringing could be related to circuit board and component parasitics. If any ringing is present, determine if it can be reduced or eliminated by an improvement in board layout, by the slowing of slew rates (increasing R24 in the design example), or by optimizing RC snubber circuits (R26/C27 and R28/C26 in the design example).
- The slew rate of a DC/DC converter's switch node can also present an inherent EMI signature within the radiated range. The magnitude of this signature can be lowered by slowing the slew rate of the switch node (increasing R24 or optimizing R26/C27 in the design example), at some cost in efficiency.
- Further improvements in EMI performance may be realized in PD applications that make use of a shielded enclosure, especially in the case of radiated emissions. For these applications, the shield of the enclosure would most likely be connected to an internal circuit board plane, such as the BS plane introduced in Section 1.4.

1.11 Considerations

Another objective of the design example was to obtain the desired EMI performance while using components that are commonly used for PoE and DC/DC circuits. Other PD applications might consider the use of components such as shielded RJ-45 jacks that integrate the PoE transformer and cable termination components discussed in Section 1.4. Depending on power levels and grounding configurations, some PD applications might benefit from the use of possible Y-capacitors.

1.12 Summary

Practical guidelines to designing an EMI compliant PoE PD have been presented in this application report. The guidelines were implemented into an actual design example of an isolated flyback converter using the TPS23750 which includes an IEEE 802.3-2005 compliant PD front-end and a DC/DC controller. The design example was subjected to pre-compliance conducted emissions testing per the telecommunication ports requirement of the EN 55022 / CISPR 22 standard. The peak emissions of the design example were found to be approximately 25 dB below the Class B quasi-peak limit and approximately 15 dB below the Class B average limit defined by the standard. The EMI results were shown to be obtainable for both floating output and earth-referenced output configurations.

1.13 References

1. EN 55022:1998 CISPR 22:1997
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1.14 Acknowledgements

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1. Martin Patoka – overall guidance
2. Vince Paku – circuit board layout
3. Illya Kovarik – photography
4. Tony Merfeldas – EMI test setup construction

Appendix A

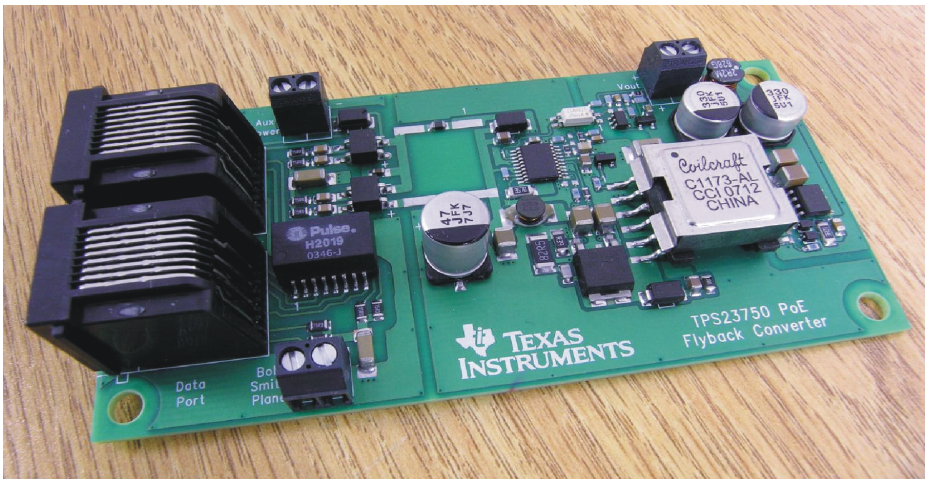

Figure A-1. TPS23750 Isolated Flyback Converter Design Example

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