Power over Ethernet Consortium
Clause 33 PSE Conformance Test Suite v 2.10 Report

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Enclosed are the results from the Clause # 33 PSE Conformance testing performed on:

Device Under Test (DUT):	Texas Instruments, Inc. TPS2388
UNH-IOL Device Identification Number:	18954
Port Tested:	5

The test suite referenced in this report is available at the UNH-IOL website:

https://www.iol.unh.edu/sites/default/files/testsuites/ethernet/CL33_PSE/PSE_test_suite_V2.10.pdf

The tables below contain summarized test results. For more details please see the detailed test results:

The Following Tests Exhibited Non-Conformant Behavior
No conformance issues were discovered during the testing process.

The Following Tests Were Either Not Performed Or Have Additional Comments	
33.1.6 – Detector Circuit Output Voltage **33.1.9 Part F – Physical Layer Classification** **33.2.2 Part A – Load Regulation** **33.3.4 Part A – Output Current in Startup Mode** **33.4.2 – Midspan PSE Insertion Loss** **33.4.3 – Midspan PSE NEXT Loss** **33.4.4 – PSE Impedance Balance**	These tests are currently under development.
33.1.13 – Alternative B Backoff Cycle	This test only applies to devices which source power on Alternative B.
33.2.6 Part A – PSE Current Unbalance	This test only applies to Type 1 PSEs.
33.3.6 Part B – Range of T_{MPDO} Timer **33.3.9 – AC MPS Signal Parameters** **33.3.10 – AC MPS Signature**	These tests only apply to devices which support AC MPS.
33.4.1 – Midspan PSE Return Loss	This test only applies to Midspan devices.
33.4.5 – PSE Common Mode Output Voltage	This test only applies to devices with a PHY.

Testing Completed 11/25/2014

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Result Key

The following table contains possible results and their meanings:

Result	Meaning	Interpretation
PASS	Pass	The Device Under Test (DUT) was observed to exhibit conformant behavior.
PWC	Pass With Comments	The Device Under Test (DUT) was observed to exhibit conformant behavior, however changes were made to the normal test procedure or the behavior observed requires additional comments.
FAIL	Fail	The Device Under Test (DUT) was observed to exhibit non-conformant behavior.
RTC	Refer to Comments	From the observations, a valid pass or fail was not determined. An additional explanation of the situation is included.
Info	Informative	Test is designed for informational purposes only. The results may help ensure the interoperability of the DUT, but are not standards requirements.
Warn	Warning	The DUT was observed to exhibit behavior that is not recommended.
N/A	Not Applicable	This test does not apply to the device type or is not applicable to the testing program selected.
N/S	Not Supported	The Device Under Test (DUT) was not observed to support the necessary functionality required to perform these tests or the requirement is optional and not supported by this device.
N/T	Not Tested	This test was not performed and therefore this is not a complete test report. Please see the comments for additional reasons.
UA	Unavailable	The test was not performed due to limitation of the test tool(s) or interoperable systems, or the test methodology is still under development.

Initialization Information

The following table contains the steps taken to initialize the DUT prior to testing:

Component	Description
Initialization	Initialization was performed by an onsite representative from Texas Instruments during testing.

Revision History

The following table contains a revision history for this report:

Revision	Explanation
1.0	Initial Version

Test Setup

Testing Equipment	
Real-time DSO	TEKTRONIX, TDS 3014
Current Probe and Amplifier	TEKTRONIX, TCP305 and TCPA300
Digital Multimeter	HEWLETT-PACKARD, 34401A
Digital Power Supply	AGILENT TECHNOLOGIES, E3641A
Chroma DC Electronic Load	Chroma,6312A,0,01.40,0
Vector Network Analyzer	HEWLETT-PACKARD,8712B,US34400165,B.03.02
UNH-IOL Developed Test Board	PoE Shark Board Rev4.0

Basic Testing Configuration

The basic testing configuration is defined in the UNH Interoperability Laboratory PSE Parametric Test Suite v2.10

GROUP 1: DETECTION CHARACTERISTICS

Test # and Label	Part(s)	Result(s)
33.1.1 – Valid PSE Pinout	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE has a compliant pinout and that it is in a valid location with respect to the link segment.

a. A PSE may operate on either Alternative A or Alternative B. An Alternative A device may have either polarization. An Alternative B device must supply positive Vport on pins 4 and 5, and negative Vport on pins 7 and 8.

Comments on Test Results

a. The PSE is in a valid location and its power supply has a valid pinout: ALT A MDI

Test # and Label	Part(s)	Result(s)
33.1.2 - Open Circuit Voltage	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the open circuit voltage at the PI of the PSE during detection mode is below the conformance limits.

a. The open circuit voltage (V_{oc}) should not exceed 30 Volts.

Comments on Test Results

a. V_{oc} = 25.23 V

Test # and Label	Part(s)	Result(s)
33.1.3 - Detection Circuit	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify the Thevenin equivalent detection circuit of the PSE detection source.

a. The DUT loaded circuit voltage should be less than half the open circuit PI voltage to confirm that the Thevenin equivalent of the DUT greater than 45kΩ.

Comments on Test Results

a. Loaded open circuit voltage = Not Applicable

The DUT was observed to reject current into the Vdetect+ port. This is compliant with the Alternative PSE detection source shown in IEEE Std 802.3-2012 Figure 33-12. Output impedance was not calculated (not applicable due to diode configuration).

Test # and Label	Part(s)	Result(s)
33.1.4 - Backdriven Current	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the detection circuit of the PSE can withstand maximum backdriven current over the range of V_{Port}.

a. A backdriven current of 5mA should not affect the DUT.

Comments on Test Results

a. The DUT was observed to properly ignore the backdriven current.

Test # and Label	Part(s)	Result(s)
33.1.5 – Detector Circuit Output Current	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the short circuit output current of the PSE during PD detection is within the conformance limits.

a. The output short circuit current should not exceed 5 mA.

Comments on Test Results

a. I_{SC} = 0.27 mA.

Test # and Label	Part(s)	Result(s)
33.1.6 – Detector Circuit Output Voltage	**a**	**PASS**
	b	**PASS**
	c	**UA**

Expected Results and Procedural Comments

Purpose: To verify the voltage output of the PSE's detection circuit conforms to the specified limits.

a. The loaded circuit voltage should be between 2.8 and 10V.
b. The voltage difference between detection probe voltages should be at least 1V.
c. The slew rate of the probe voltages should be no greater than 0.1V/µs.

Comments on Test Results

a. Probe Voltage 1 = 4.94 V
   Probe Voltage 2 = 7.71 V
   Probe Voltage 3 = 4.96 V
   Probe Voltage 4 = 7.72 V
b. Detection probe voltage difference = 2.77 V, 2.76 V
c. This test is currently under development.

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.7 – PD Detection Timing	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE probes its PI with valid detection pulses and completes an entire detection sequence within the proper time period.

a. The total pulse width of the detection pulse should not be greater than 500ms.
b. The detection probe voltages should have a duration of at least 2 ms.

Comments on Test Results

a. T_{DET} = 306.76 ms
b. Probe Voltage 1 pulse width = 69.28 ms
Probe Voltage 2 pulse width = 67.80 ms
Probe Voltage 3 pulse width = 68.28 ms
Probe Voltage 4 pulse width = 75.80 ms
T_{BP} > 2 ms

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.8 – PD Signature Detection Limits	**a**	**PASS**
	b	**PASS**
	c	**PASS**
	d	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT will properly detect a PD's Signature impedance.

a. The minimum accepted input resistance should be between 15 kΩ and 19 kΩ.
b. The maximum accepted input resistance should be between 26.5kΩ and 33 kΩ.
c. The DUT should detect a proper signature if the input capacitance is less than 150nF.
d. The DUT should accept capacitances below 10µF and reject capacitances above 10µF.

Comments on Test Results

a. 16.60 kΩ ≤ $R_{accept(min)}$ ≤ 16.70 kΩ
b. 29.70 k Ω ≤ $R_{accept(max)}$ ≤ 29.80 kΩ
c. The DUT was observed to accept capacitances less than 150nF.
d. The DUT was observed to reject improper capacitances above 10µF.

Test # and Label	Part(s)	Result(s)
33.1.9 – Physical Layer Classification	**a**	**PASS**
	b	**PASS**
	c	**PASS**
	d	**PASS**
	e	**PASS**
	f	**UA**

Expected Results and Procedural Comments

Purpose: To verify that a DUT supporting Classification properly performs PD class detection.

a. For 1-Event classification the DUT should produce a single classification pulse at V_{CLASS} (15.5-20.5V).
b. For 2-event classification the DUT should produce the following sequence V_{CLASS}, V_{Mark}, V_{CLASS}, V_{Mark} where V_{CLASS} is 15.5-20.5 volts, and V_{Mark} is 7-10V.
c. The DUT should accurately classify the PD.
d. If the current drawn is equal to or greater than 51mA, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0: a Type 2 PSE shall return to the IDLE state.
e. I_{CLASS_LIM} should be less than 100 mA.
f. For 2-Event classification I_{MARK_LIM} should be between 5 and 100mA for all mark events.

Comments on Test Results

The DUT implements 2-event Classification.

a. V_{CLASS}= 18.69 V
b. V_{CLASS1}= 18.60 V
   V_{Mark1}= 9.02 V
   V_{CLASS2}= 18.61V
   V_{Mark2} = 9.05 V
c. The DUT was observed to accurately classify the PD.
d. The DUT was observed to return to the IDLE state.
e. I_{CLASS_LIM} = 65.82 mA.
f. This test is currently under development.

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.10 – Classification Timing	**a**	**PASS**
	b	**PASS**
	c	**PASS**
	d	**PASS**
	e	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that a PSE capable of classifying a PD completes classification within the proper time period after successfully completing the detection of a PD.

a. For the 1-Event class pulse, T_{PDC} must be between 6ms and 75ms (inclusive).
b. T_{CLE1} must be between 6ms and 30ms
c. T_{ME1} must be between 6ms and 12ms
d. T_{CLE2} must be between 6ms and 30ms
e. T_{ME2} must be greater than 6ms

Comments on Test Results

a. 1-Event: T_{PDC} = 9.65 ms
b. T_{CLE1}= 9.44 ms
c. T_{ME1}= 6.17 ms
d. T_{CLE2}= 9.10 ms
e. T_{ME2}= 7.24 ms

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.11 – Allowed Classification Permutations	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify whether the DUT fits a valid classification permutation.

a. The DUT should function as a Type 1 or Type 2 PSE as defined in Table 33-8

Comments on Test Results

a. The DUT was observed to function as a Type 2 PSE with 2 event physical layer classification and without data link layer classification. Its functionality matches the behavior described by IEEE Std 802.3-2012 Table 33-8.

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.12 – New Detection Cycle	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that if the PSE is unable to supply power within T_{pon} then, it initiates and successfully completes a new detection cycle before powering on.

a. The DUT should complete a full detection cycle before applying power onto the link segment.

Comments on Test Results

a. The DUT was observed to successfully complete a new detection cycle before applying power onto the link segment.

Test # and Label	Part(s)	Result(s)
33.1.13 – Alternative B Backoff Cycle	**a**	**N/S**
	b	**N/S**

Expected Results and Procedural Comments

Purpose: To verify that if a PSE implementing Alternative B fails to detect a valid detection signature at its PI, it will wait for the appropriate period of time before beginning a new detection cycle and applies a voltage on to the PI that falls within the defined limits.

a. The DUT should not apply a voltage greater than 2.8 V_{dc} to the PI.
b. The value for T_{dbo} should be at least 2 sec.

Comments on Test Results

These tests only apply to devices which power on Alternative B.

GROUP 2: POWER FEED CHARACTERISTICS

Test # and Label	Part(s)	Result(s)
33.2.1 – Power Feed Ripple and Noise	**a**	**PASS**
	b	**PASS**
	c	**PASS**
	d	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the power feeding ripple and noise are within the conformance limits.

The peak-to-peak values of ripple and noise transmitted on the line by the DUT, in both the common mode and pair-to-pair, should not exceed:

a. 500 mV_{pp} between 0-500 Hz
b. 200 mV_{pp} between 500 Hz -150 kHz
c. 150 mV_{pp} between 150-500 kHz
d. 100 mV_{pp} between 500 kHz-1 MHz

Comments on Test Results

a. 57.4 mV_{pp} between 0-500Hz
b. 71.1 mV_{pp} between 500Hz-150kHz
c. 40.0 mV_{pp} between 150-500kHz
d. 45.3 mV_{pp} between 500kHz-1MHz

Test # and Label	Part(s)	Result(s)
33.2.2 – Load Regulation	**a**	**UA**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE performs load regulation while supplying power to the PI.

a. Voltage transients should not exceed 3.5 V/µs.
b. For Type-1 PSEs, the DUT output voltage should be between 44 and 57 V for all values of I_{Port}.
   For Type-2 PSEs, the DUT output voltage should be between 50 and 57 V for all values of I_{Port}.

Comments on Test Results

a. This test is currently under development.
b. V_{Port} (max)= 53.10 V
   V_{Port} (min)= 52.06 V

Test # and Label	Part(s)	Result(s)
33.2.3 – Voltage Transients	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that a Type-2 PSE maintains proper output voltages for transient conditions.

a. Vport should not go below 46.2 Volts for any transient between 30µs and 250µs, and Vport should not go below 50V for any transient lasting more than 250µs.

Comments on Test Results

a. Transients between 30µs and 250µs were observed to produce a minimum Vport of 52.08 Volts. Transients above 250µs were observed to produce a minimum Vport of 52.08 Volts.

Test # and Label	Part(s)	Result(s)
33.2.4 – Power Turn On Timing	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT supplies power onto the link segment within the acceptable turn on time after it has successfully detected a PD.

a. The DUT should start supplying power within T_{pon} (400ms) after detection.

Comments on Test Results

a. T_{pon} = 32.8 ms

Test # and Label	Part(s)	Result(s)
33.2.5 – Apply Power	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE applies power on the same pairs as those used for detection after completing a valid detection.

a. The PSE should perform a valid detection sequence before powering the PD.
b. The PSE should supply power on the same pairs as that it performed detection for the PD.

Comments on Test Results

a. The DUT performed a valid detection sequence before supplying power onto the link segment.
b. The DUT applied power on the same pairs as those it detected on.

Test # and Label	Part(s)	Result(s)
33.2.6 – PSE Current Unbalance	**a**	**N/A**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the current unbalance between the two conductors of the power pairs of the PSE over the current load range is within the permissible range.

a. For a Type 1 PSE, current unbalance between the two conductors per power pair should not exceed 3% of I_{CABLE}.
b. For a Type 2 PSE, current unbalance between the two conductors per power pair should not exceed 3% of I_{PEAK}.

Comments on Test Results

a. This test is not applicable to Type 2 PSEs.
b. The DUT was observed to have a current unbalance less than 1.449% of I_{PEAK}.

GROUP 3: ERROR DETECTION AND POWER REMOVAL

Test # and Label	Part(s)	Result(s)
33.3.1 – Overload Current Detection Range	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that I_{CUT} is within the specified limits. a. I_{CUT} should be between P_{CLASS}/V_{PORT} and I_{LIM}.		
Comments on Test Results		
a. I_{CUT} = 637.0 mA		

Test # and Label	Part(s)	Result(s)
33.3.2 – Overload Time Limits	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that T_{CUT} is within the specified limits. a. The overload time limit (T_{CUT}) should be between 50ms and 75ms (inclusive).		
Comments on Test Results		
a. T_{CUT} = 60.25 ms		

Test # and Label	Part(s)	Result(s)
33.3.3 – Output Current at Short Circuit Condition	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE will start removing power from the PI within T_{LIM} when it detects a short circuit condition.

a. The DUT should limit I_{PORT} when current draw exceeds the PSE upperbound template
b. The DUT should not remove power when below the PSE lowerbound template

Comments on Test Results

a. The DUT was observed to limit I_{PORT} when the current draw exceeded the upperbound template.

Listed below are a number of inflection points used to determine how the PSE's current draw profile fits into the PSE upperbound template.

Attempted Current Draw	Idraw =40 A	Idraw =1.75 A	Idraw =750 mA
Maximum Current	I1 = 1.29 A	I2 = 1.29 A	I3 = 655 mA
Cut Time	T1 = 59.2 ms	T2 = 59.0 ms	T3 = 59.0 ms

b. The DUT was observed to continue powering the PI while current draw was below the PSE lowerbound template.

Listed below are a number of inflection points used to determine how the PSE's current draw profile fits into the PSE lowerbound template.

Attempted Current Draw	Idraw = 650 mA	Idraw = 600 mA	Idraw = 560 mA
Maximum Current	I4 = 650 mA	I5 = 600 mA	I6 = 560 mA
Cut Time	T4 = 61.2 ms	Not observed to remove power *1	Not observed to remove power *1

Please see the appended figure.
*1 Monitored for at least 60 seconds.

Test # and Label	Part(s)	Result(s)
33.3.4 – Output Current in Startup Mode	**a**	**UA**
	b	**PASS**
	c	**PASS**
	d	**PASS**

Expected Results and Procedural Comments

Purpose To verify that when the PSE detects a short circuit condition it starts removing power from the PI within T_{LIM} and must be done removing power within the conformant time limit.

a. For voltages from 0V to 10V, I_{INRUSH} must be between 5mA and 450mA.
b. For voltages from 10V to 30V, I_{INRUSH} must be between 60mA and 450mA.
c. For voltages above 30V, I_{INRUSH} must be between 400mA and 450mA.
d. The short circuit time limit (T_{INRUSH}) should be between 50ms and 75ms.

All ranges are inclusive.

Comments on Test Results

a. This test is currently under development
b. I_{INRUSH} (10V to 30V) = 361.00 mA
c. I_{INRUSH} (30V and above) = 418.56 mA
d. T_{INRUSH} = 59.84 ms

Test # and Label	Part(s)	Result(s)
33.3.5 – Error Delay Timing	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE waits for at least the minimum conformant time before attempting subsequent detection after it removes power due to detection of error condition.

a. The DUT should wait for at least 750ms after detecting a short circuit condition and removing power before resuming detection
b. The DUT should wait for at least 750ms after detecting an overload condition and removing power before resuming detection

Comments on Test Results

a. The DUT was observed to wait 1.10 s after a short circuit event before resuming signature detection.
b. The DUT was observed to wait 1.03 s after an overload event before resuming signature detection.

Test # and Label	Part(s)	Result(s)
33.3.6 – Range of T_{MPDO} Timer	**a**	**PASS**
	b	**N/S**

Expected Results and Procedural Comments

Purpose: To verify that PSE correctly monitors the PD Maintain Power Signature

a. *DC disconnect:* 300ms $\leq T_{MPDO} \leq$ 400ms
b. *AC disconnect:* 300ms $\leq T_{MPDO} \leq$ 400ms

Comments on Test Results

a. *DC disconnect:* 360.00 ms $\leq T_{MPDO} \leq$ 362.00 ms
b. This test only applies to devices that support AC MPS.

Test # and Label	Part(s)	Result(s)
33.3.7 - PD MPS Dropout Current Limits (I_{MIN} measurement)	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that PSE correctly monitors the PD Maintain Power Signature for DC disconnect.

a. The DUT may remove power if the current drawn is between 5 mA and 10 mA ($I_{MIN2\ (max)}$) for 400 ms.
b. The DUT must remove power if the current drawn is less than 5 mA ($I_{MIN1\ (max)}$) for 400 ms.

Comments on Test Results

a. 7.40 mA $\leq I_{MIN2\ (max)} \leq$ 7.50 mA
b. The DUT removes power when current draw is less than 5mA.

Test # and Label	Part(s)	Result(s)
33.3.8 – PD MPS Time for Validity	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE waits for at least the minimum MPS validity time when it monitors the DC MPS component.

a. The DUT should not remove power from a PD that provides a valid DC MPS signature for at least T_{MPS} every T_{MPS}+T_{MPDO}.

Comments on Test Results

a. The DUT was observed to remain powering when a valid DC MPS signature was presented for at least T_{MPS} every T_{MPS}+T_{MPDO}.

Test # and Label	Part(s)	Result(s)
33.3.9 – AC MPS Signal Parameters	**a**	**N/S**
	b	**N/S**
	c	**N/S**
	d	**N/S**

Expected Results and Procedural Comments

Purpose: To verify that the PI probing AC signals fall within the conformance limits.

a. The PI probing AC voltage (V_open) should be between 1.9V to 10% of Vport (V_{pp}).
b. The AC probing signal frequency, Fp, should not be greater than 500 Hz.
c. The AC probing signal slew rate should not be greater than 0.1V/µs.
d. The measured V_{Port} (Vp) should not exceed 60V.

Comments on Test Results

These tests only apply to devices that support AC MPS.

Test # and Label	Part(s)	Result(s)
33.3.10 – AC MPS Signature	**a**	**N/S**
	b	**N/S**

Expected Results and Procedural Comments

Purpose: To verify that the PSE that implements AC MPS component correctly monitors the PD Maintain Power Signature.

a. The DUT should supply power to the PD for signature impedance less than 27KΩ.
b. The measured impedance should be between 27KΩ and 1980KΩ (inclusive).

Comments on Test Results

These tests only apply to devices that support AC MPS.

Test # and Label	Part(s)	Result(s)
33.3.11 – Turn Off Time Limits	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE disconnects power within T_{Off} through a test resistor.

a. The DUT should remove power in times less than 500ms through a test resistor of 320kΩ.

Comments on Test Results

a. The DUT was observed to remove power within 28.86 ms.

GROUP 4: PSE TRANSMITTER AND RECEIVER CHARACTERISTICS

Test # and Label	Part(s)	Result(s)
33.4.1 – Midspan PSE Return Loss	**a**	**N/A**
Expected Results and Procedural Comments		
Purpose: To verify that the return loss of a Midspan PSE is greater than the minimum conformant value. a. The DUT's return loss should be greater than 23dB from 1 to 20MHz and greater than 14dB from 20MHz to 100MHz.		
Comments on Test Results		
This test only applies to Midspan devices.		

Test # and Label	Part(s)	Result(s)
33.4.2 – Midspan PSE Insertion Loss	**a**	**UA**
Expected Results and Procedural Comments		
Purpose: To verify that the insertion loss of a Midspan PSE is no greater than the maximum conformant value. a. The DUT's insertion loss should be no greater than the limit described by equation 33-6 and the maximum conformant value of 0.1dB.		
Comments on Test Results		
This test only applies to Midspan devices. In addition, it is currently under development.		

Test # and Label	Part(s)	Result(s)
33.4.3 – Midspan PSE NEXT Loss	**a**	**UA**
Expected Results and Procedural Comments		

Purpose: To verify that the NEXT between the transmit and receive pairs of the DUT is within conformance limits.

a. The DUT's NEXT loss should be no greater than the limit described by equation 33-5 and the minimum conformant value of 65 dB.

Comments on Test Results

This test only applies to Midspan devices. In addition, it is currently not implemented.

Test # and Label	Part(s)	Result(s)
33.4.4 – PSE Impedance Balance	**a**	**UA**
Expected Results and Procedural Comments		

Purpose: To verify that the common-mode to differential-mode impedance balance of the transmit and receive pairs of the PI is greater than the specified limits.

a. The common-mode to differential-mode impedance balance for a 100Mb/s transmitter and receiver should exceed $34-19.2\log_{10}(f/50)$ dB (where f is the frequency in MHz) over the frequency range of 1.0 MHz to 100 MHz

Comments on Test Results

This test only applies to devices with a PHY. In addition, it is currently not implemented.

Test # and Label	Part(s)	Result(s)
33.4.5 – PSE Common Mode Output Voltage	**a**	**N/A**
Expected Results and Procedural Comments		

Purpose: To verify that the common mode AC output voltage at the PI is below the conformant limits.

a. The magnitude of the common-mode AC output voltage, *E*cm_out, should not exceed 50 mV peak when operating at 10 Mb/s, and 50 mV peak-to-peak when operating at 100 Mb/s or greater.

Comments on Test Results

This test only applies to devices with a PHY.

Annex A: Figures

Attached are the figures illustrating the measurements made during testing. These were captured either with the real time DSO or the Vector Network Analyzer and post-processed using custom MATLAB scripts.

Figure 1: Open Circuit Voltage (V_{OC})

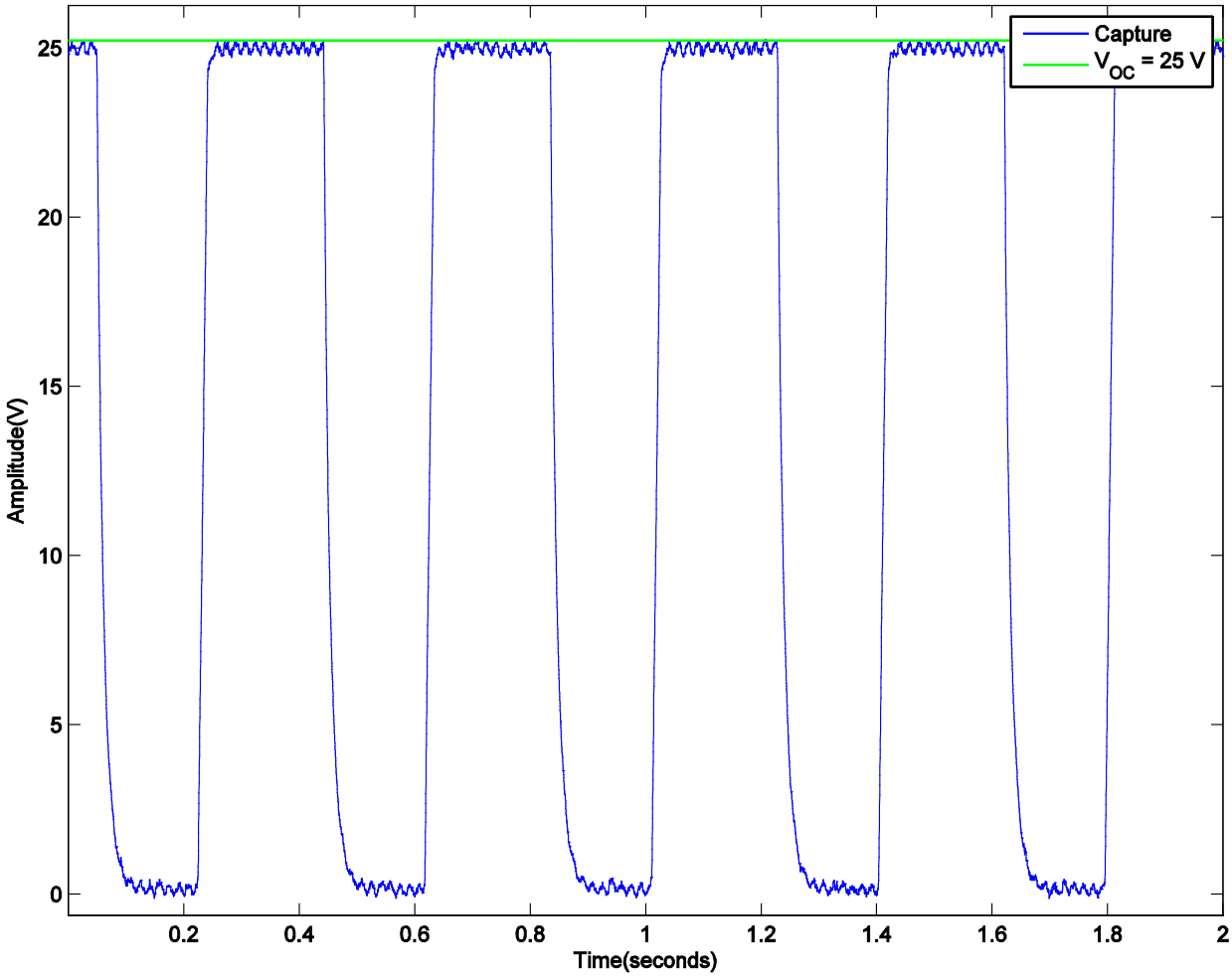


Figure 2: Detection Pulse Identification

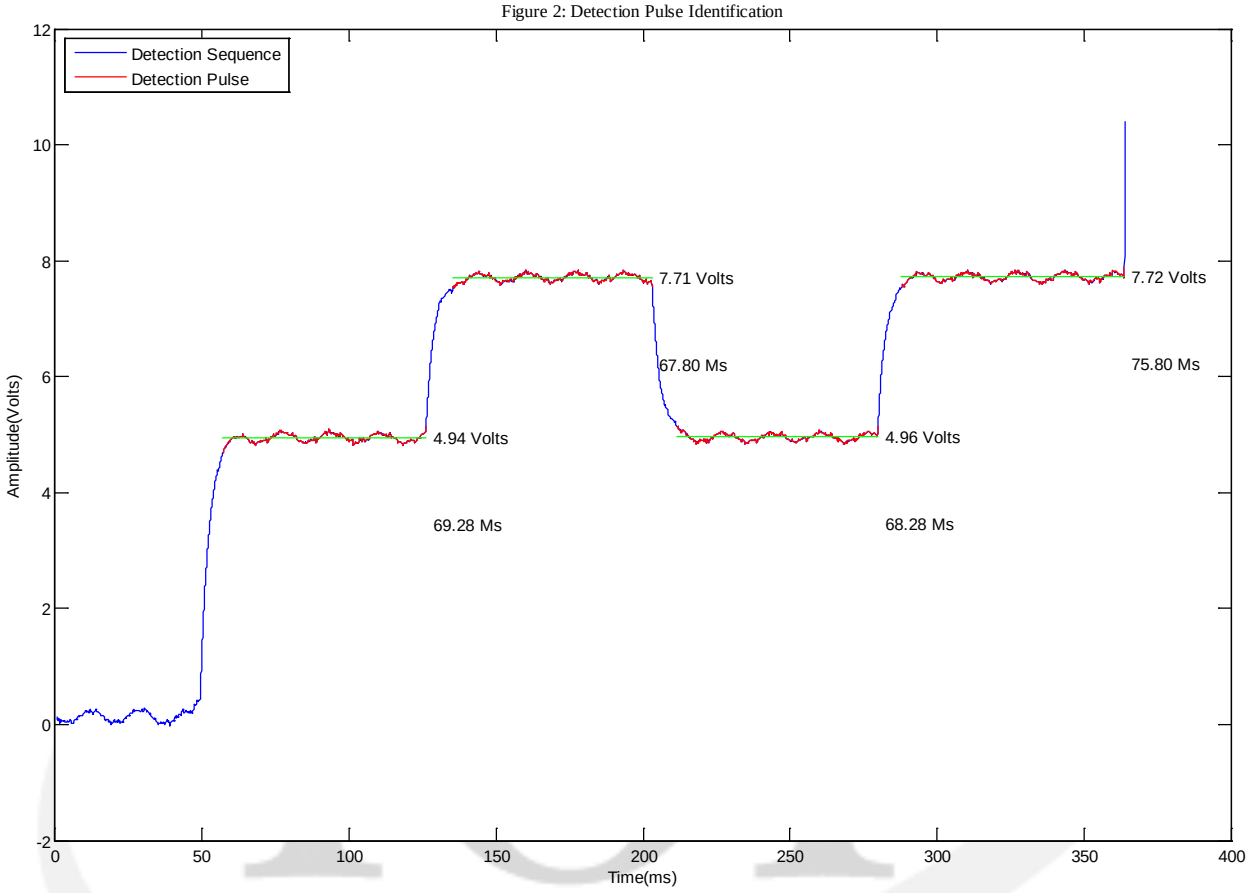


Figure 3: Short Circuit Output Current (I_{SC})

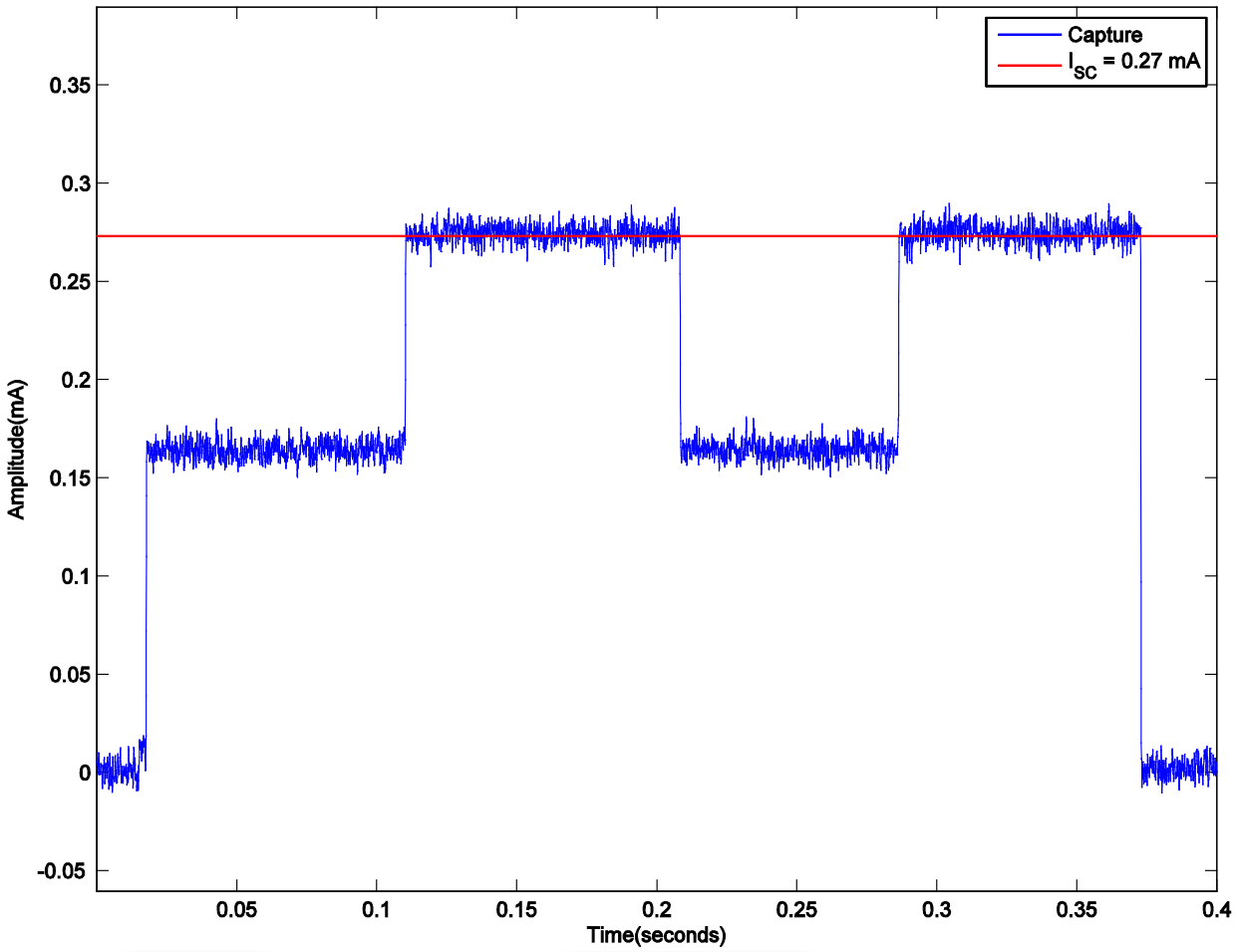


Figure 4: 1-Event Classification Pulse

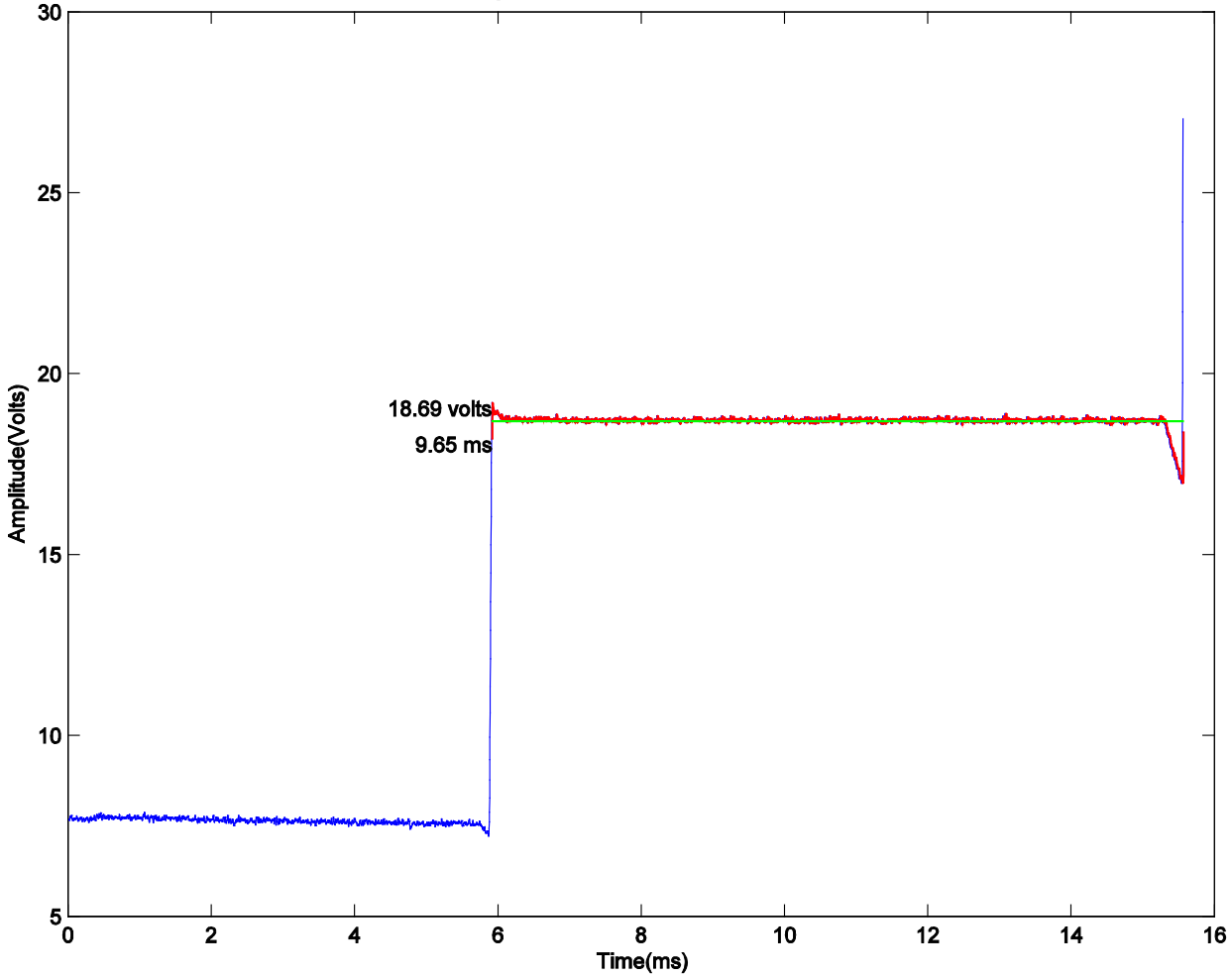


Figure 5: 2-Event Classification

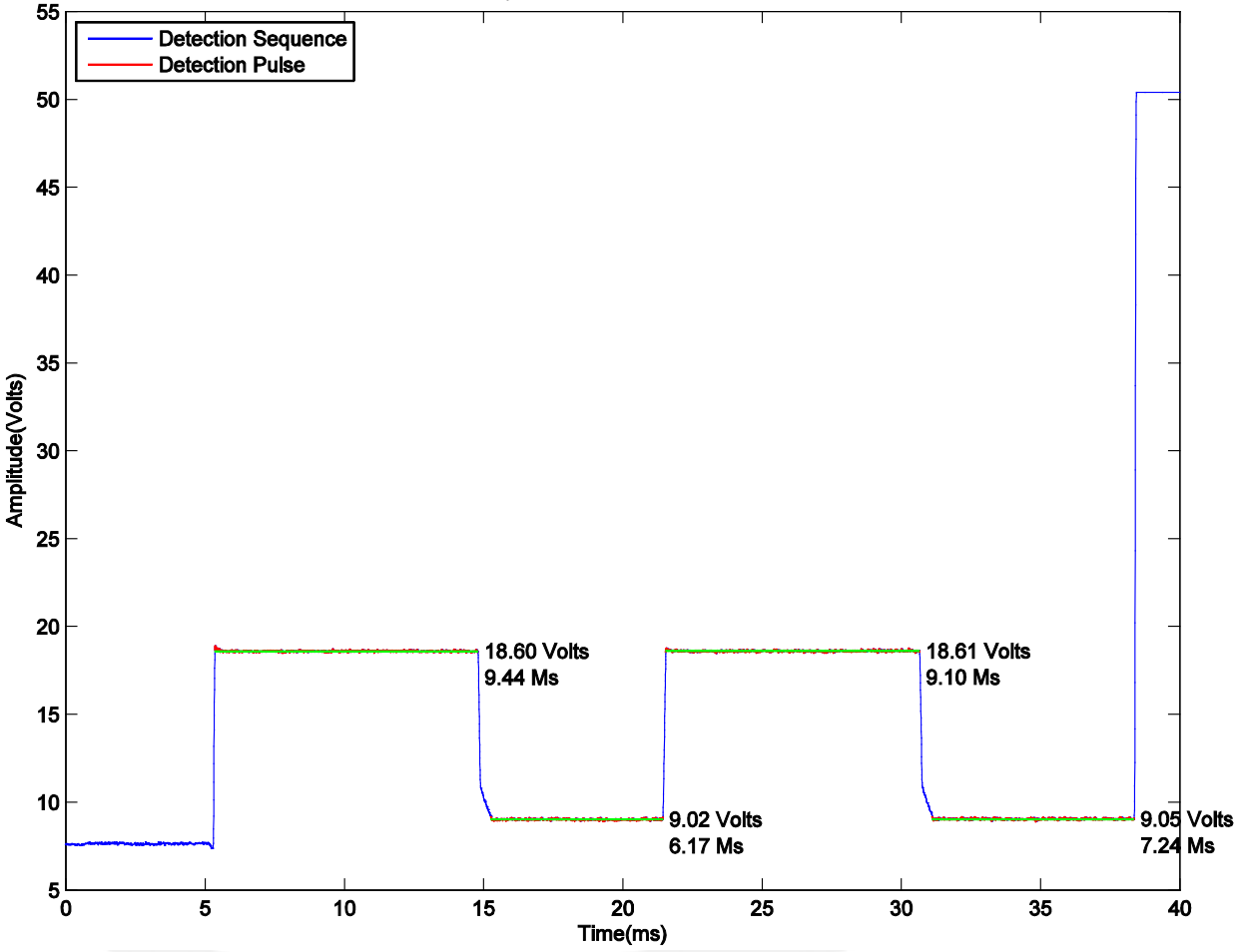
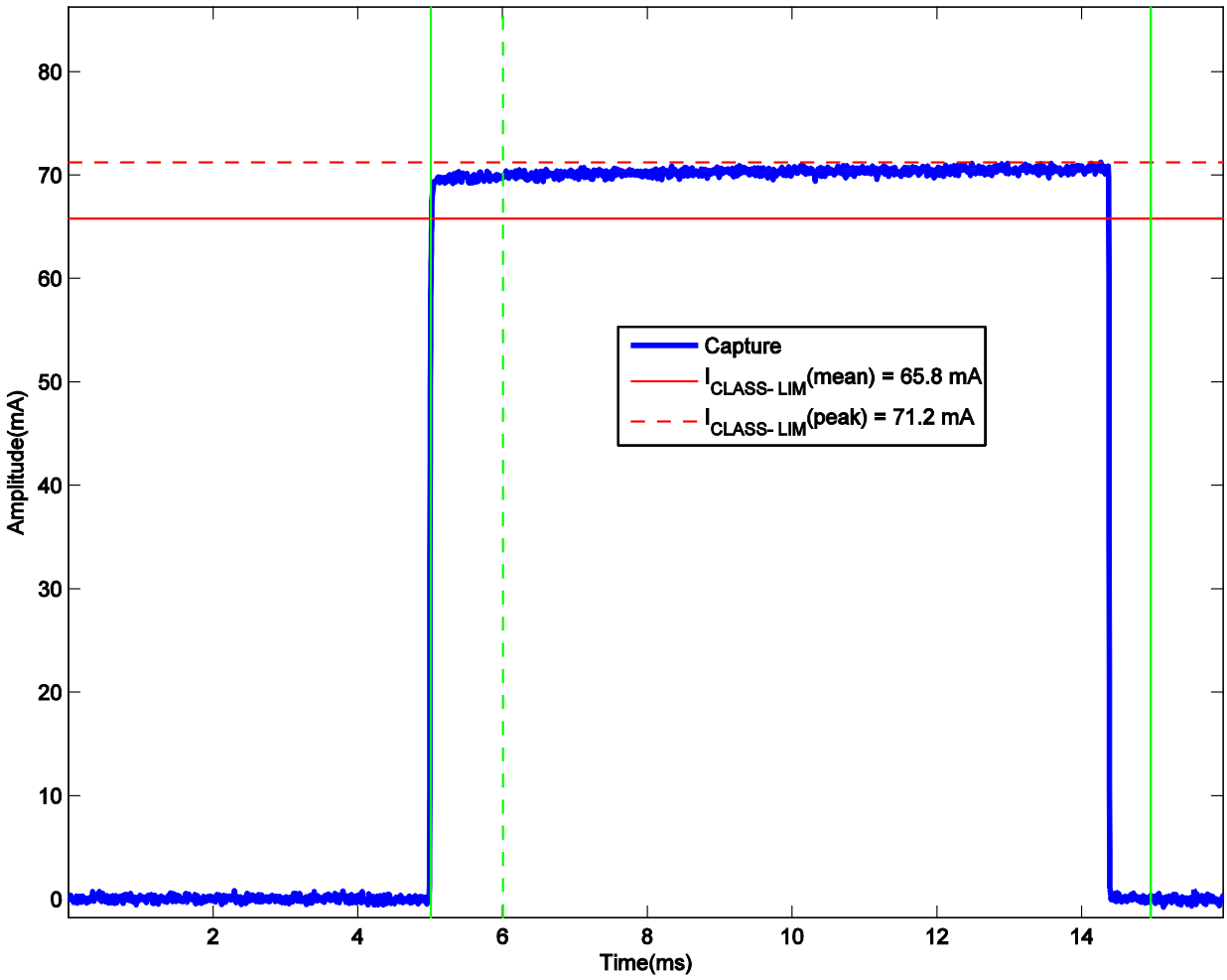


Figure 6: Class Event Current Limit ($I_{CLASS-LIM}$)



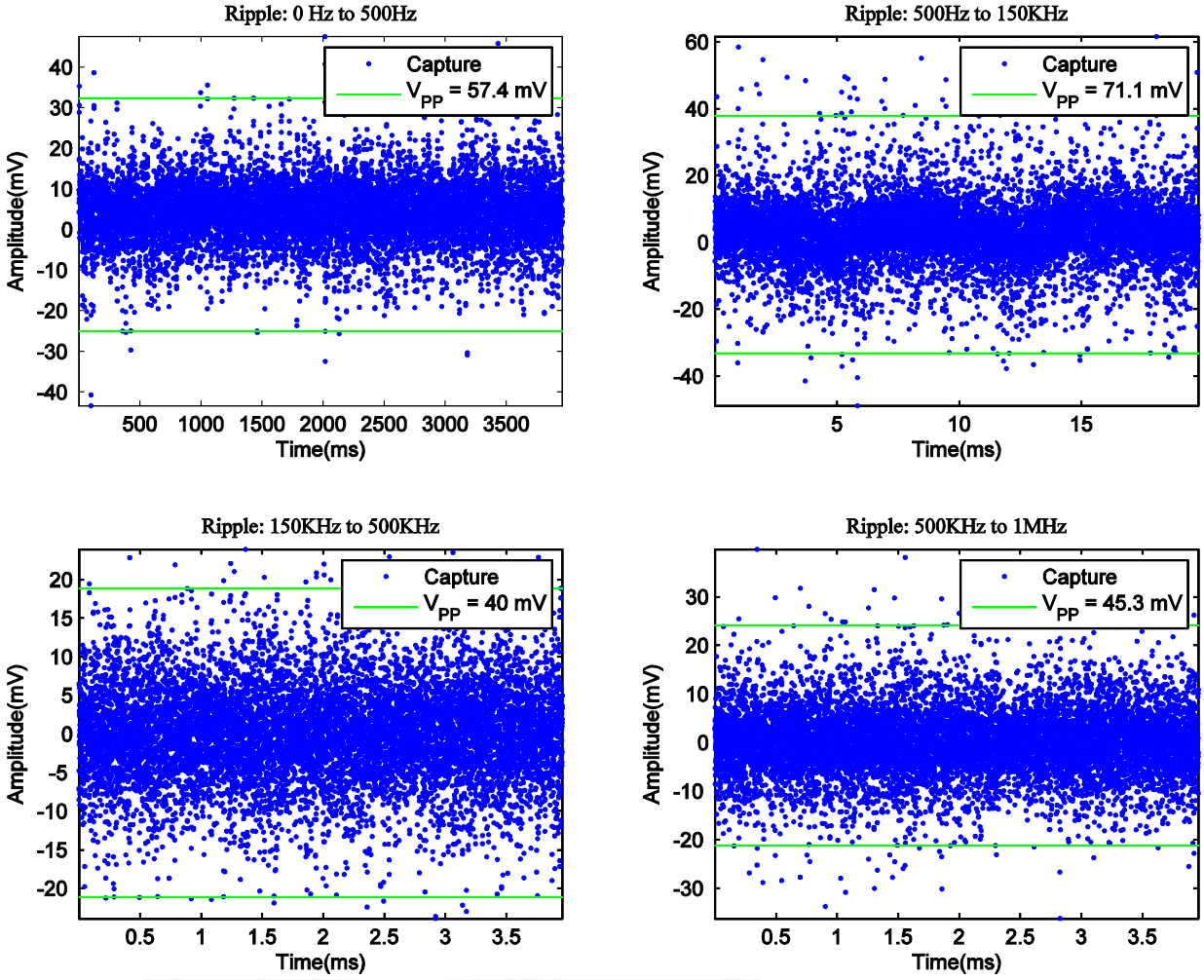

Ripple: 0 Hz to 500Hz
Capture
V_{PP} = 57.4 mV
Amplitude(mV)
Time(ms)
Ripple: 500Hz to 150KHz
Capture
V_{PP} = 71.1 mV
Amplitude(mV)
Time(ms)
Ripple: 150KHz to 500KHz
Capture
V_{PP} = 40 mV
Amplitude(mV)
Time(ms)
Ripple: 500KHz to 1MHz
Capture
V_{PP} = 45.3 mV
Amplitude(mV)
Time(ms)

Figure 8: T_{PON}

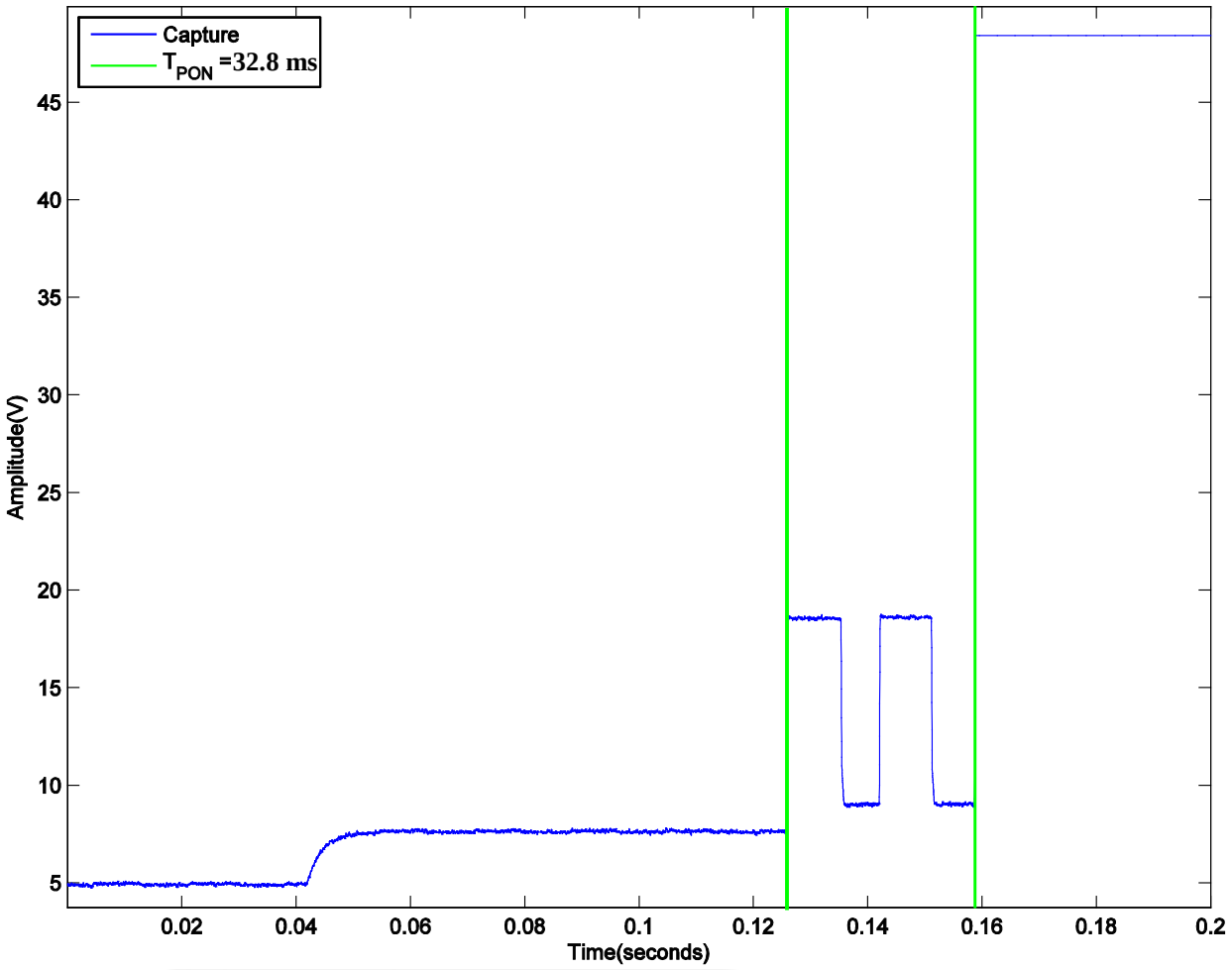


Figure 9:Overload Error Delay Timing (T_{ED}(overload))

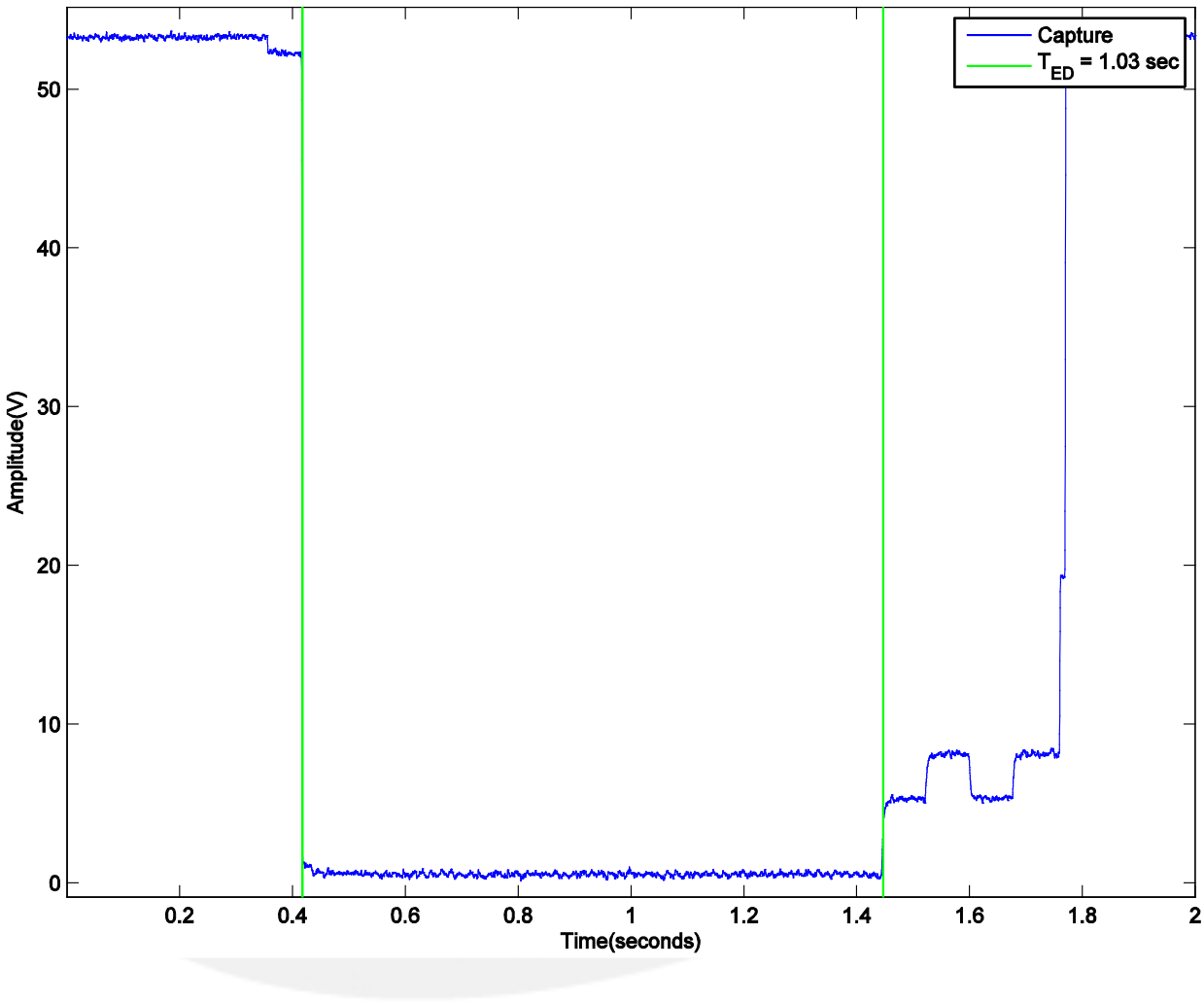


Figure 10: Short Circuit Error Delay Timing (T_{ED}(short))

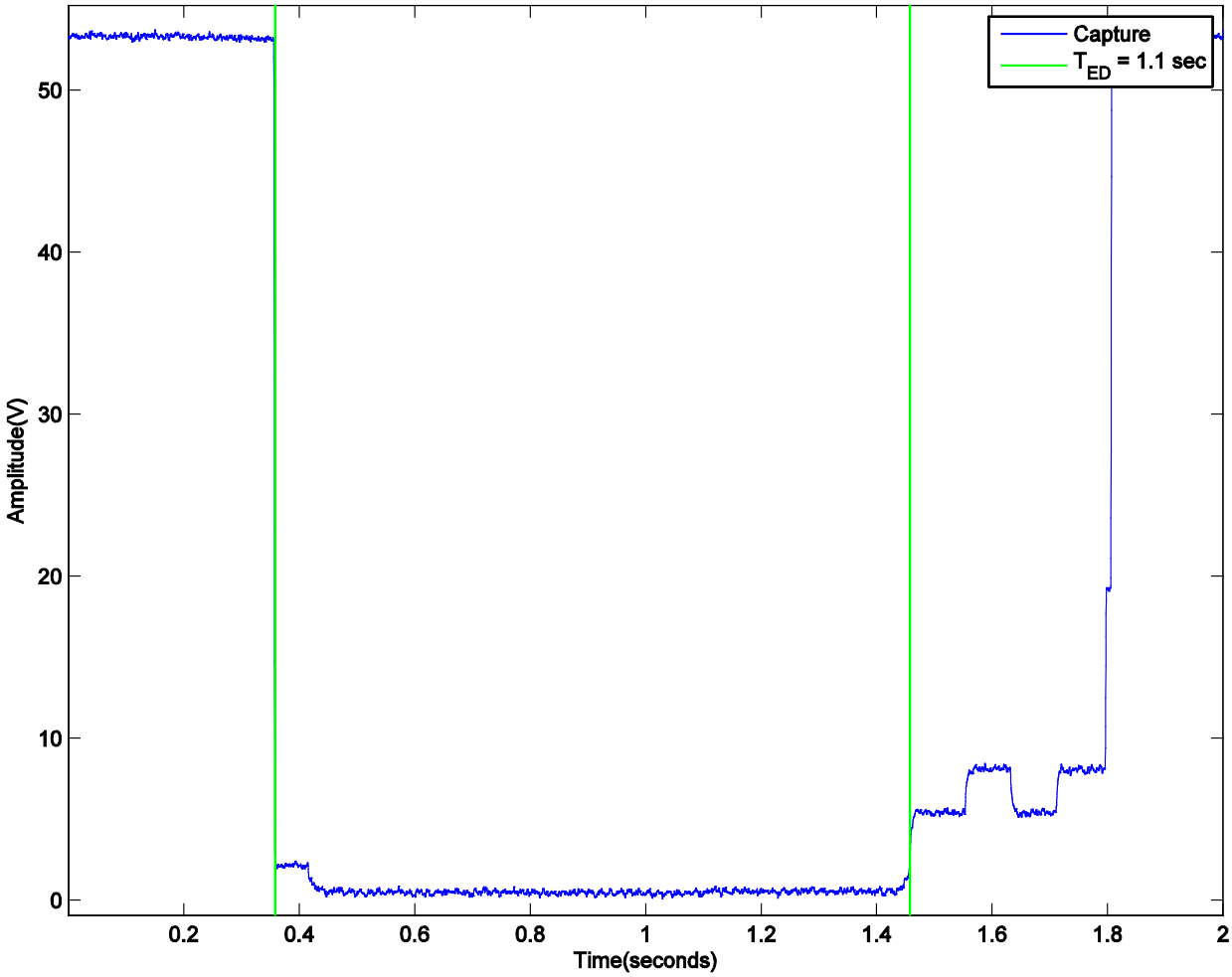


Figure 11: Overload Current (I_{CUT})

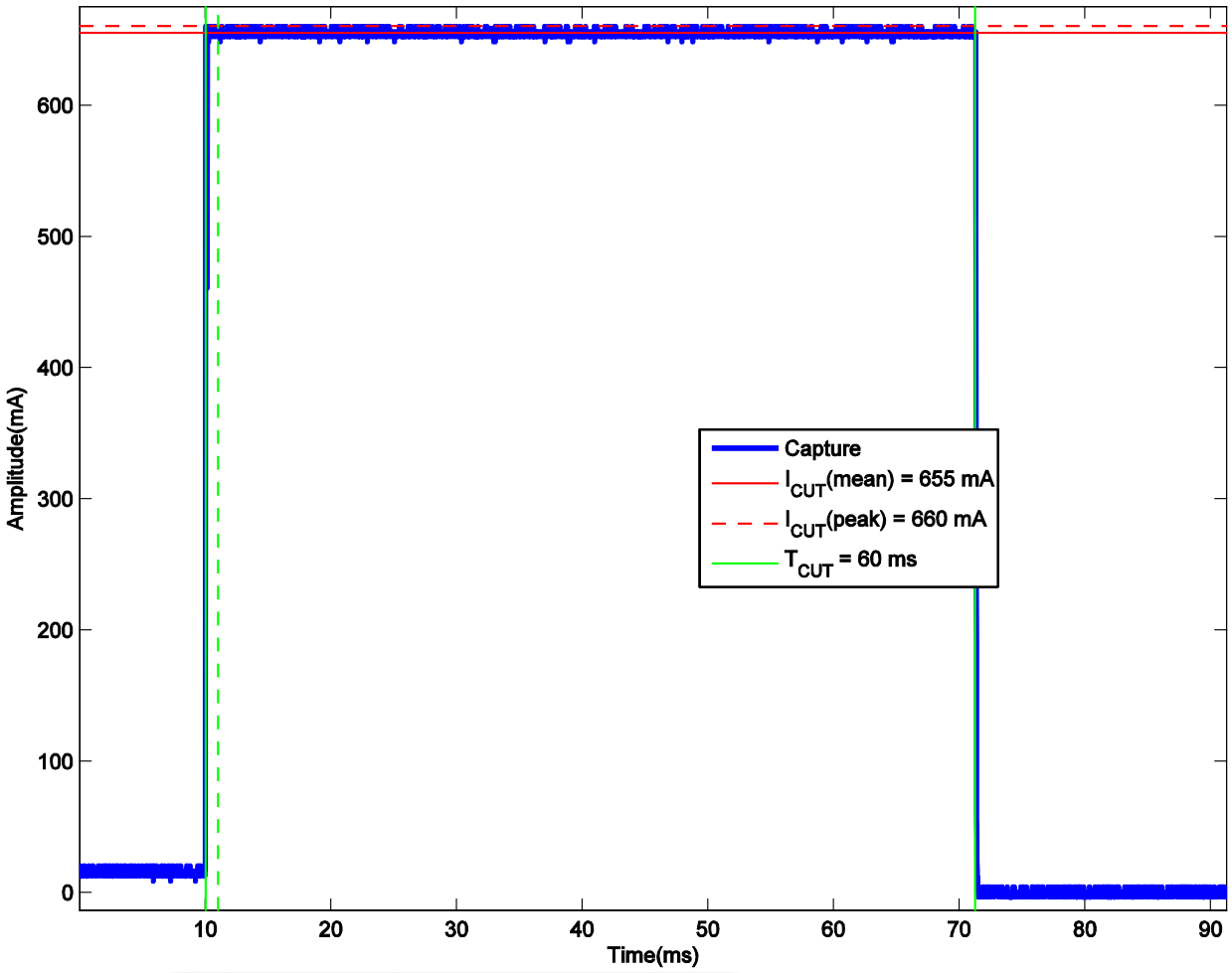


Figure 12:Output Current in Startup Mode - I_{INRUSH}(10V-30V)

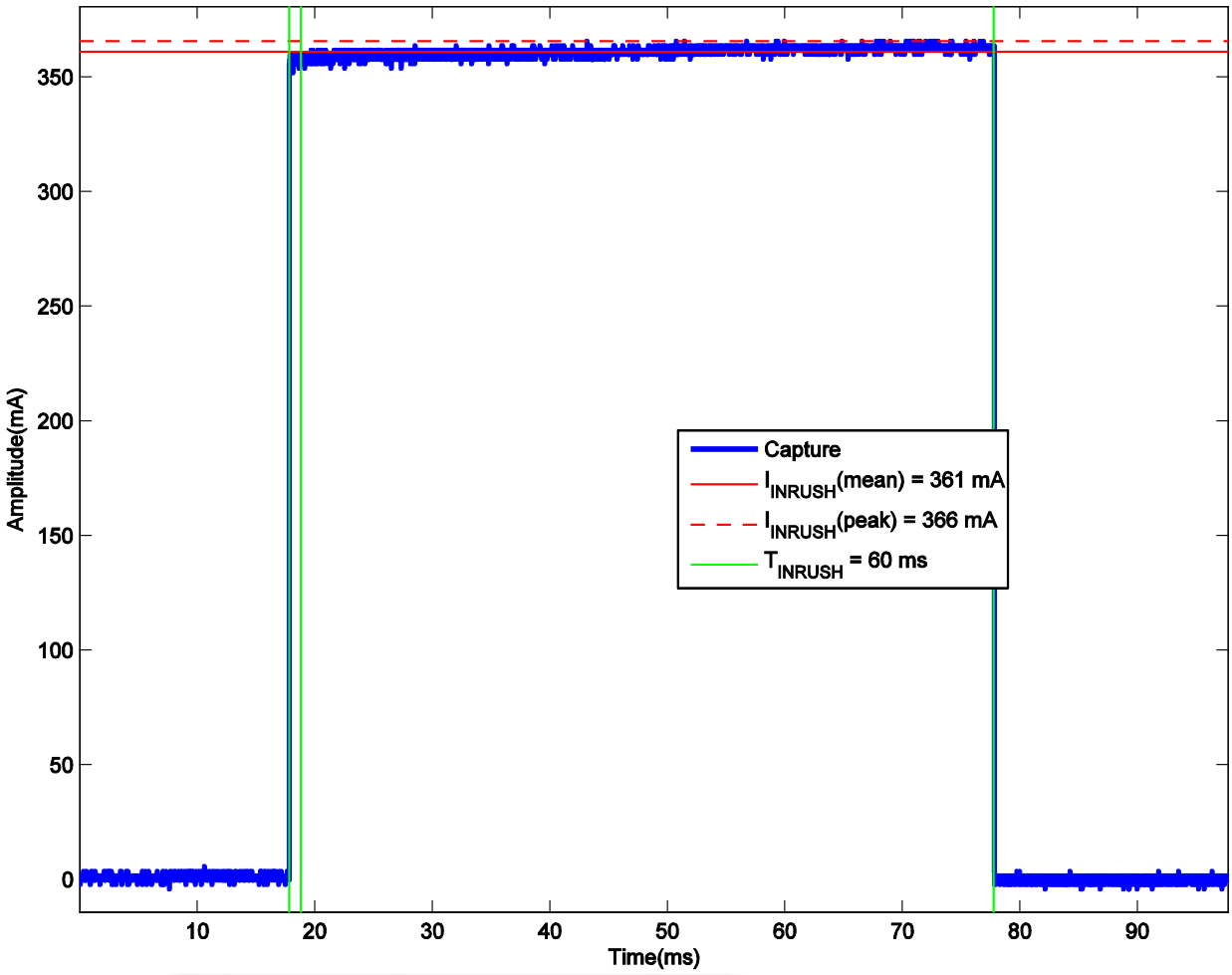
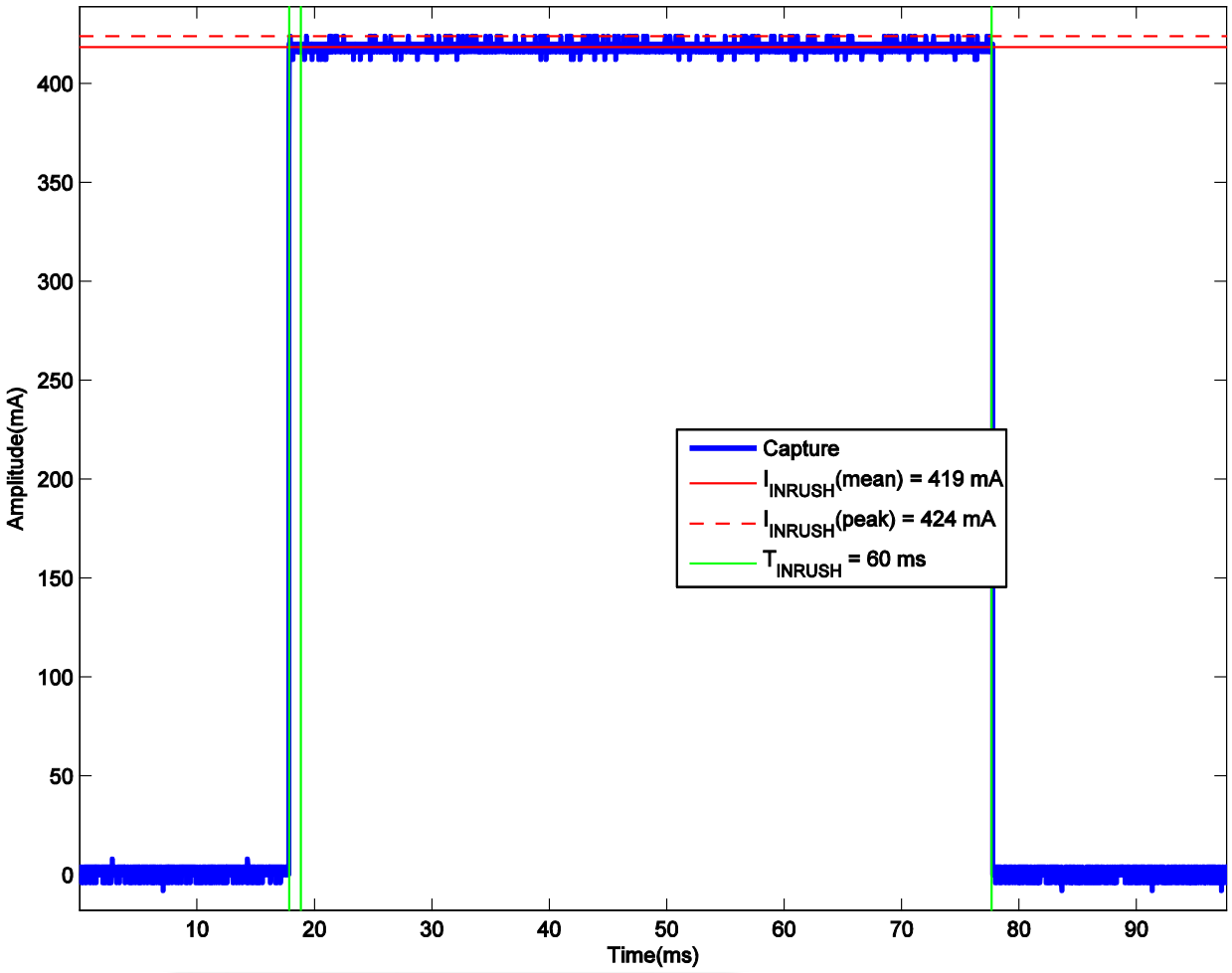


Figure 13:Output Current in Startup Mode - I_{INRUSH}(30V and above)



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