Pairing the PFC controller with Gate Drivers in On-Board Chargers for Electric Vehicles

Introduction

An on-board charger (OBC) takes as input AC voltage from the grid and converts to DC voltage in order to charge the electric vehicle battery. This AC-DC system is located within the hybrid electric and electric vehicle (HEV/EV). An example AC/DC block diagram solution for the on-board charger is shown in Figure 1. [1] The boost converter can be designed using the Two-Phase Interleaved PFC controller UCC28070-Q1 and the Phase-Shifted Full-Bridge (PSFB) is designed using the UCC28951-Q1 which are both automotive grade controllers. The same AC-DC system may be found in electric vehicle charging stations, also known as electric vehicle service equipment, where non-automotive grade components can be utilized. [2]

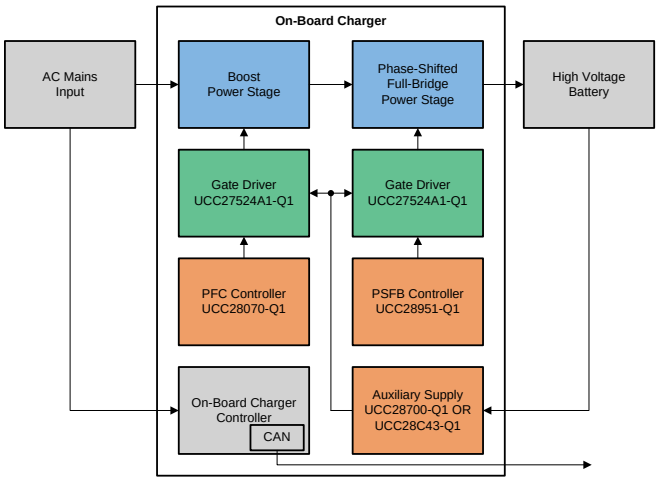

Figure 1. On-Board Charger Block Diagram Example

Notice the green boxes highlighting gate drivers upstream from the PFC and PWM controller boxes. The gate driver is used to switch on/off the MOSFETs or other semiconductor devices like silicon carbide (SiC), gallium nitride (GaN) or insulated gate bipolar transistors (IGBT). A common question is how to select the gate driver for these controllers.

There are many criteria on selecting the gate driver but in this report the topic will examine the output sink and source current requirement to achieve a desired MOSFET turn-on/turn-off switching speed to minimize the MOSFET switching losses due to the linear operation of the MOSFET and the Miller plateau region. Designing a gate drive circuit one must consider in addition to switching speed other factors for example; isolation using the gate driver or a magnetic transformer, dv/dt immunity, bypassing rules, input logic levels, negative voltage tolerance on pins, start-up and transient conditions, power dissipation/thermal/reliability, protection features, package, layout guidelines, and cost to name but a few considerations. Ultimately, ringing and performance checks are required for verification on the final printed circuit design. [3]

1 MOSFET Turn-on

The turn-on of a MOSFET is classified in four intervals as shown in Figure 2. The physical explanation for each interval is described in “Fundamentals of MOSFET and IGBT Gate Driver Circuits slua618.” [3] The focus of this report is to minimize MOSFET switching losses during intervals 2, linear operation, and 3, the Miller plateau region; the key is the source-sink current capability of the gate driver. The peak current capability of a gate drive is at full V_{DRV} across the driver’s output impedance but what is needed is the current capability of the driver during the MOSFETs V_{TH} and $V_{GS,Miller}$ interval. MOSFET turn-off is the reverse transition to turn-on.

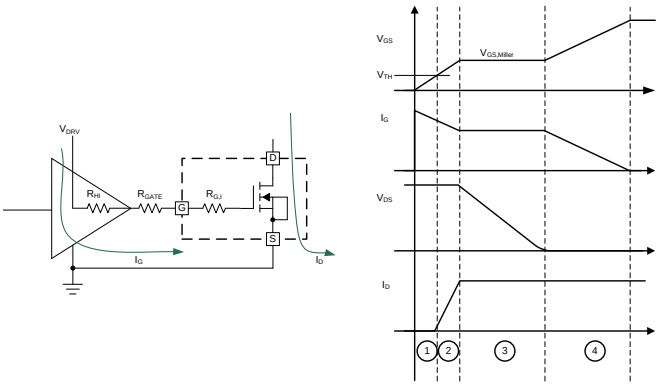

Figure 2. MOSFET Turn-On Time Intervals

An estimate of the gate driver output current during the 2nd and 3rd interval is approximated as:

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$$I_{G2} = \frac{V_{DRV} - 0.5 \times \left(V_{GS,Miller} + V_{TH}\right)}{R_{HI} + R_{GATE} + R_{G,1}}$$

$$I_{G3} = \frac{V_{DRV} - V_{GS,Miller}}{R_{HI} + R_{GATE} + R_{G,1}} \quad (1)$$

And from here the approximate switching times are:

$$t2 = C_{ISS} \times \frac{V_{GS,Miller} - V_{TH}}{I_{G2}}$$

$$t3 = C_{RSS} \times \frac{V_{DS,off}}{I_{G3}} \quad (2)$$

Trace resistance and inductance will slow down the rise and fall times of the gate driver outputs and further reduce the current capabilities of the gate drive and MOSFET manufacturers recommend an external resistor to control switching speed – use resistors rated for high peak currents, 1206 size is generally ok. The voltage-current characteristics showing turn-off second order effects are depicted in Figure 19 of the High-side/Low-side Driver UCC27201A-Q1 datasheet.

Sometimes the MOSFET datasheet will provide the total gate charge Q_g as a function of the gate-source voltage V_{GS} over the different intervals 2 and 3 therefore equations 2 can be simplified to

$$t2 + t3 = Q_g / I_{G2,3} \quad (3)$$

Usually the assumption is made that the gate driver current available during t2+t3 is half the peak rating provided in datasheets at V_{DRV}. In examining equations 1, with $V_{GS,Miller} \approx V_{TH}$ and the assumption this voltage is half the output driver voltage, R_{GATE} and $R_{G,I}$ not included

$$I_{G2,3} = 0.5 \times V_{DRV} / R_{HI} = I_{GATE_DRIVE_PEAK} / 2 \quad (4)$$

The R_{GATE} and $R_{G,I}$ resistors control EMI and the MOSFET switching speed so they should be part of your design.

2 Matching a Gate Driver with the PFC Controller

Equation 3 can be used to size the gate driver for the Two-Phase Interleaved PFC controller UCC28070-Q1. Starting with a transition time of t2+t3 = 40 ns and selecting the IPW65R045C7 MOSFET from Infineon which has a typical Q_g of 93 nC,

$$I_{G2,3} = 93\ nC / 40\ ns = 2.325\ A \quad (5)$$

And the estimate for the gate drive peak current rating is

$$I_{GATE_DRIVE_PEAK} = 4.65\ A \quad (6)$$

The gate driver UCC27524A1-Q1 which is rated for 5 A peak output is selected for the PFC circuit in this OBC design.

The PSFB design makes use of zero-voltage switching therefore the switching time of the MOSFET needs to be minimized to get the current flow from the MOSFET body diode into the MOSFET channel as quickly as possible. If the PSFB controller is located on the secondary side, an isolated gate driver like the UCC21520-Q1 should be selected to drive the primary side MOSFETs.

3 Summary

AN OBC example has been shown involving the Two-Phase Interleaved PFC controller UCC28070-Q1 and the PSFB controllerUCC28951-Q1. The description and approximate gate driver output current equations for MOSFET switching are of interest in this report to minimize turn-on and turn-off intervals 2 and 3. It was shown that the UCC27524A1-Q1 gate drive was selected in order to reduce PFC stage MOSFET losses. There are many other design considerations for the gate driver selection but the focus on this report is the MOSFET switching intervals.

4 Related Documentation

- Driving the future of HEV/EV with high-voltage solutions
- Which new semiconductor technologies will speed electric vehicle charging adoption
- Fundamentals of MOSFET and IGBT Gate Driver Circuits

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