Application Report
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Understanding Dead-time Based On TPS51225/275/285

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ABSTRACT

The TPS512X5 series is a dual synchronous buck regulator controller with two LDOs. It is optimized for 5-V / 3.3-V system controller, enabling designers to create cost-effective complete 2-cell to 4-cell notebook system power supplies. Dead-time is important parameter and its true value will be affected by using different MOSFETs. This application report introduces the concept of what is Dead-time and how Dead-time can be measured accurately.

NOTE: This application report is specifically used for synchronous buck controller IC. Generally, for buck converter, which is integrated power MOSFETs, Dead-time is specified by design.

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1 Introduction

The TPS512X5 series is a dual synchronous buck regulator controller with two LDOs. It is optimized for 5-V / 3.3-V system controller. Power FETs are needed for regulation, and using different FETs will generate different rising and falling time because of the different C_{iss} / Q_g (Refer to Mosfet Driver Circuit Design Guide for TPS512xx), and this results in different Dead-time. What Dead-time is and how Dead-time can be measured accurately is presented in this paper.

2 Dead-time

2.1 What is Dead-time

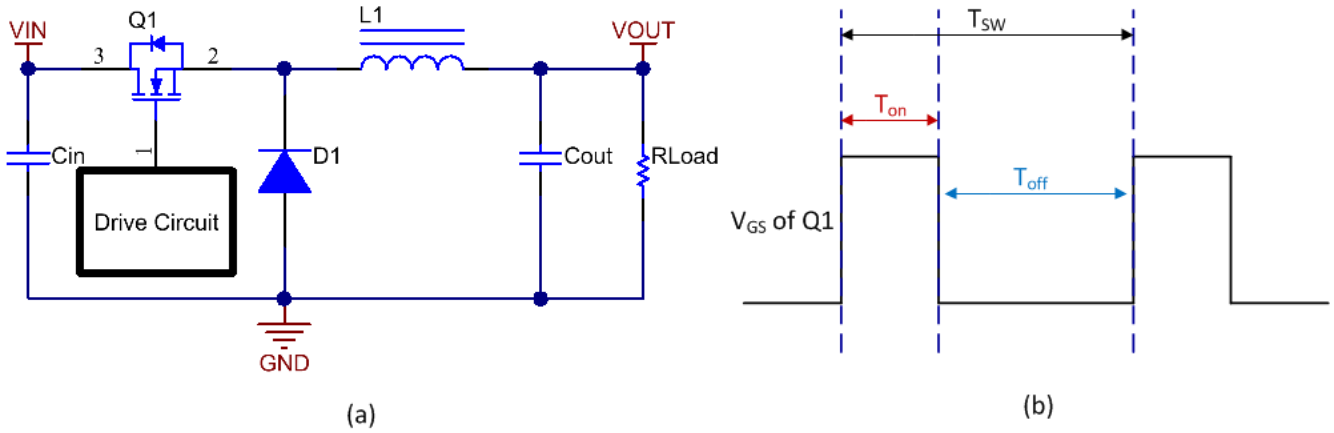


Figure 1. Non-Synchronous Buck Circuit and Drive Signal

Figure 1-(a) shows the non-synchronous Buck circuit that consists of the switching FET Q1, together with the flywheel circuit, includes diode D1, inductor L1 and output capacitor C_{out}. Figure 1-(b) shows Q1 drive signal.

When the Q1 is switched on, it supplies the load with current. Initially, current flow to the load is restricted as energy is also being stored in L1, therefore the current in the load and the charge on C_{out} builds up gradually during the 'on' period. Notice that throughout the on period, there will be a large positive voltage on D1 cathode. The diode will be reverse biased and therefore play no part in the action.

When the Q1 is switched off, the energy stored in the magnetic field around L1 is released back into the circuit. The voltage across the inductor is now in reverse polarity to the voltage across L1 during the 'on' period, and sufficient stored energy is available in the collapsing magnetic field to keep current flowing, D1 will play a part to keep current provided for load.

Above all, no delay time is inserted for current flow switching between Q1 and D1, and Dead-time is not defined for this architecture.

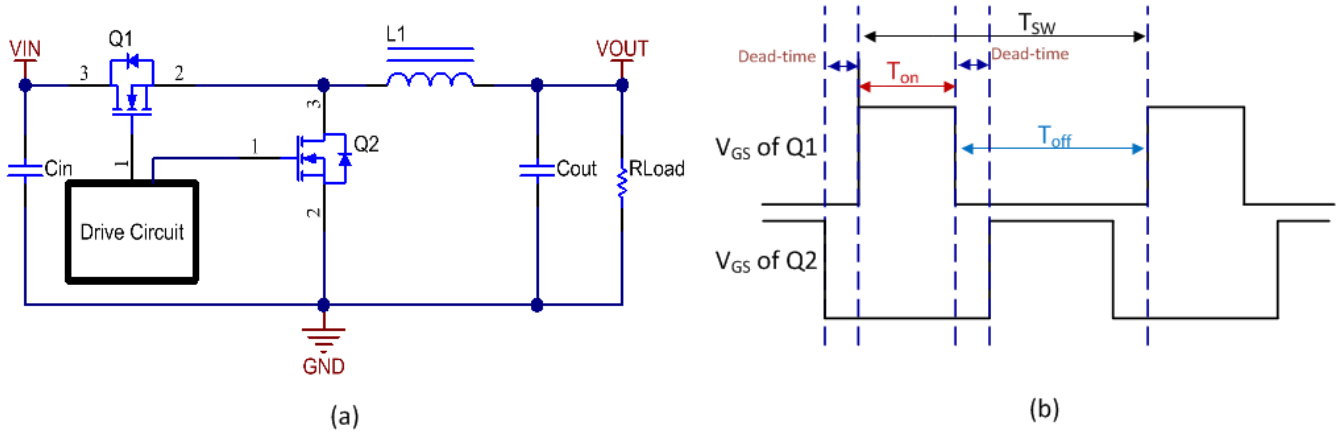


Figure 2. Synchronous Buck Circuit, Drive Signal with Dead-time

As shown in Figure 2-(a), the Synchronous Buck circuit consists of the switching FET Q1 (High side MOSFET), together with the flywheel circuit, include sync FET Q2 (Low side MOSFET), inductor L1 and output capacitor C_{out}.

When the Q1 is switched on, it supplies the load with current. Initially, current flow to the load is restricted as energy is also being stored in L1, therefore the current in the load and the charge on C_{out} builds up gradually and the sync FET Q2 is off during the 'on' period.

When the Q1 is switched off, the energy stored in the magnetic field around L1 is released back into the circuit. The voltage across the inductor is now in reverse polarity to the voltage across L1 during the 'on' period, and current flow will be restricted to go through body diode of Q2 for a short time. Then Q2 will be switched on to keep current provided for the load.

Figure 2-(b) shows Q1 and Q2 drive signal, a short delay time is inserted between Q1 and Q2 switch over, which is defined as Dead-time.

2.2 Why the Dead-time is Needed

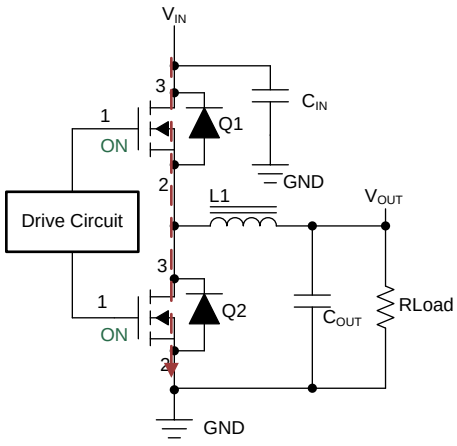


Figure 3. Shoot Through

The purpose for setting Dead-time is to avoid shoot through.

As shown in Figure 3, shoot though means V_{in} power rail will be shorted to ground when both high side MOSFET (HS FET Q1) and low side MOSFET (LS FET Q2) turn on simultaneously without Dead-time. When shoot through happens, power FETs may burnt out, and even controller could be damaged either. To prevent this, after one FET turns off, the controller will generate a short Dead-time before another FET switching on. Both FETs are off during the Dead-time, inductor current will be conducted by body diode of LS FET to keep the current continuously.

2.3 Dead-time in TPS512X5

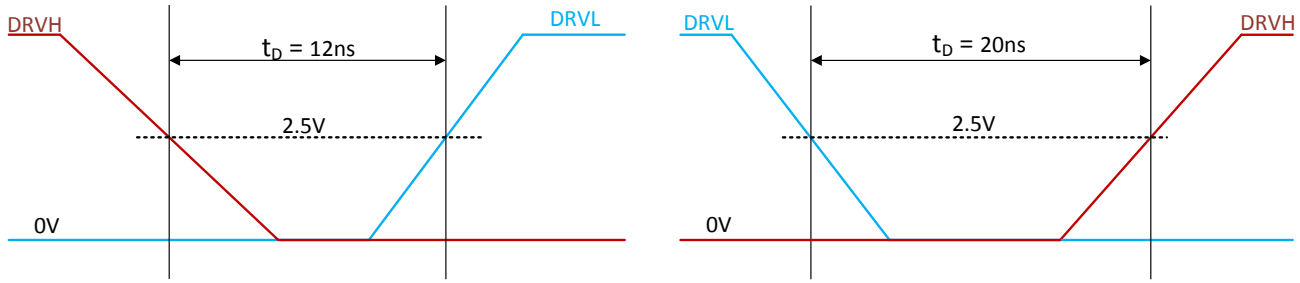
2.3.1 Dead-time in EC Table

Table 1. Dead-time in TPS512X5 EC Table

Parameter		Test Condition(1)(2)	MIN	TYP	MAX	Unit
t_D	Dead-time	DRVH-off to DRVL-on		12		ns
		DRVL-off to DRVH-on		20		ns

(1) DRVH is the high side FET drive signal
(2) DRVL is the low side FET drive signal

Table 1 is Dead-time spec of TPS512X5 shown in the Datasheet. This data is generated by ATE test, which is tested under open loop and makes IC work by adding proper power source at VIN/VFB/EN/VBST/VSW pins, trigger points of Dead-time are set at 2.5 V level for both DRVL off/on and DRVH off/on, the typical Dead-times measured are 12 ns from DRVH-off to DRVL-on and 20 ns from DRVL-off to DRVH-on. Figure 4 shows the detailed measurement.



(a) Dead-time from HS FET-off to LS FET-on

(b) Dead-time from LS FET-off to HS FET-on

Figure 4. Dead-time at ATE Test

2.3.2 Dead-time in Design

Figure 5 shows Dead-time control logic design in TPS512X5. Before LS FET turns on, LSD (low side driver) will detect DRVH signal. When DRVH is detected lower than 1 V, DRVL will get high and LSD goes to turn on LS FET, the typical delay time from DRVL-off to DRVH-on is 8.5 ns, likewise before HS FET turns on, HSD (high side driver) will detect DRVL signal, when DRVL is detected lower than 1 V, DRVH will get high and HSD goes to turn on HS FET, the typical delay time from DRVL-off to DRVH-on is 15 ns. The two types of delays described above are defined as Dead-time.

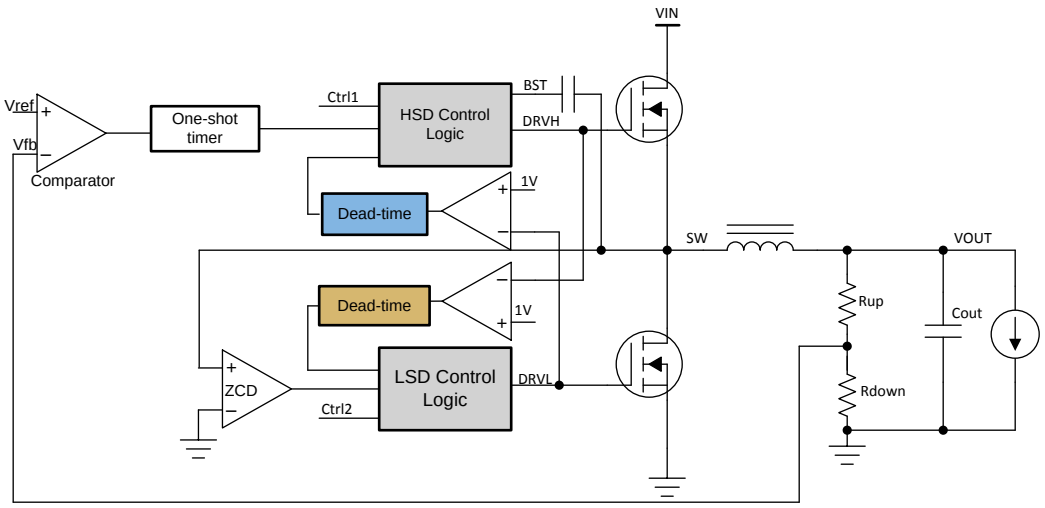
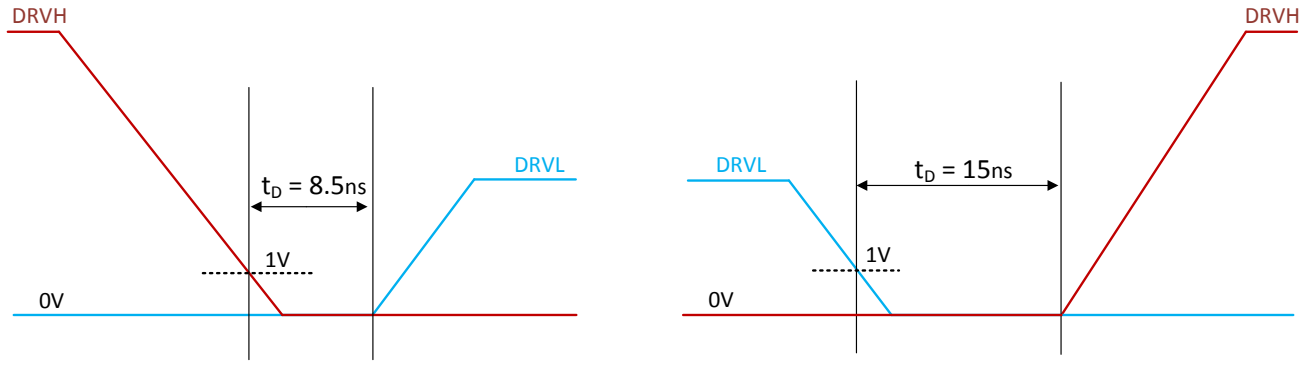


Figure 5. Block Diagram of the Dead-Time Control Circuit

Figure 6 shows Dead-time trigger points, from 1 V of DRVH falling edge to the beginning of DRVL rising edge is the Dead-time from DRVH-off to DRVL-on, from 1 V of DRVL falling edge to the beginning of DRVH rising edge is the Dead-time from DRVL-off to DRVH-on.



(a) Dead-time from HS FET-off to LS FET-on

(b) Dead-time from LS FET-off to HS FET-on

Figure 6. Dead-time at Design

3 How to Measure the Dead-time More Accurately in application

3.1 Probes and Test Points

Figure 7 shows test points at TPS51225EVM, MOSFET P/N is CSD87352Q5D.

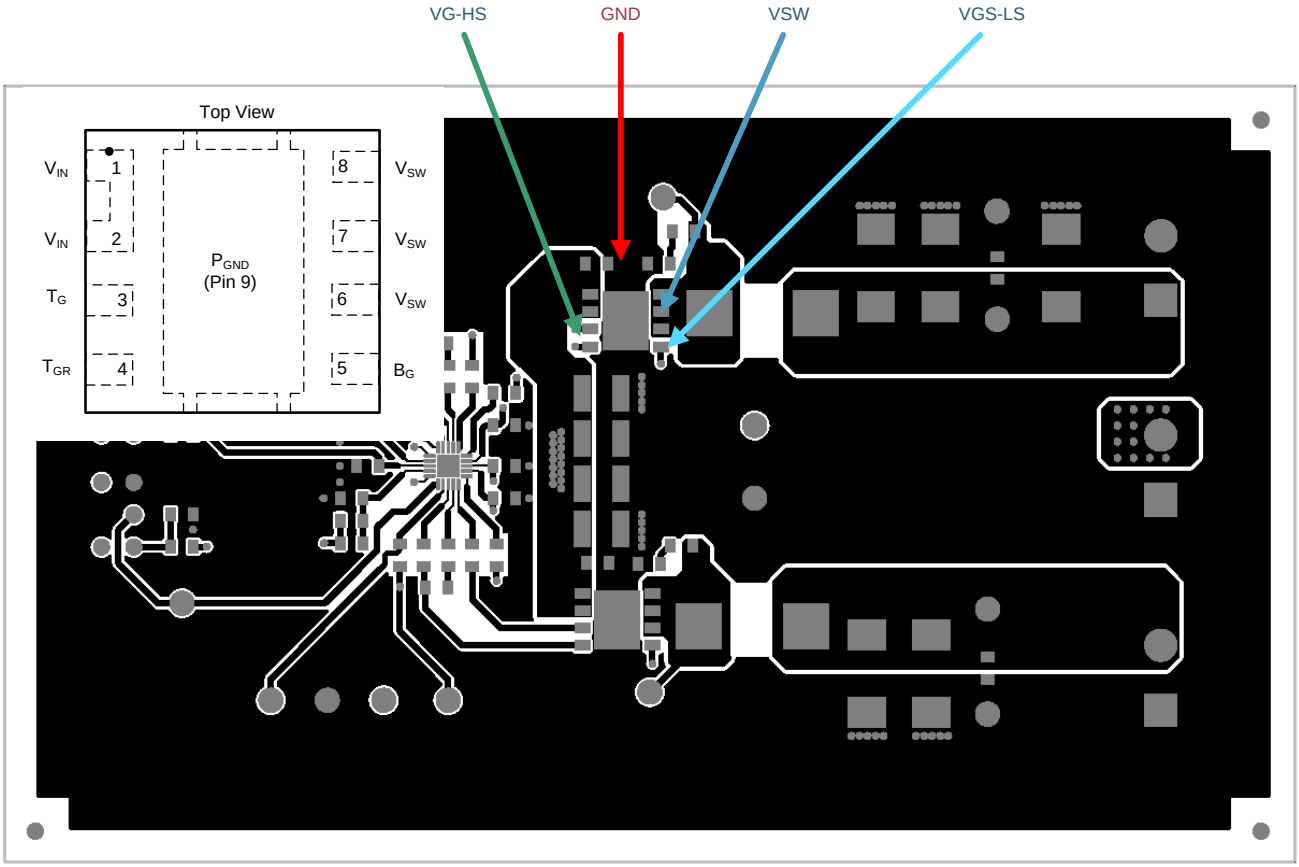


Figure 7. Probe Points

If using a passive probe (such as TEK P6139A), test with 3 probes, put each probe as close as possible to pin3, pin6~8 and pin5 to catch gate signal of HS FET, switching node and V_{GS} signal of LS FET, what need to be noticed is that all ground need to refer to pin9 (PGND). Do math by gate signal of HS FET minus switching node(VG_HS-Vsw) to get V_{GS} signal of HS FET.

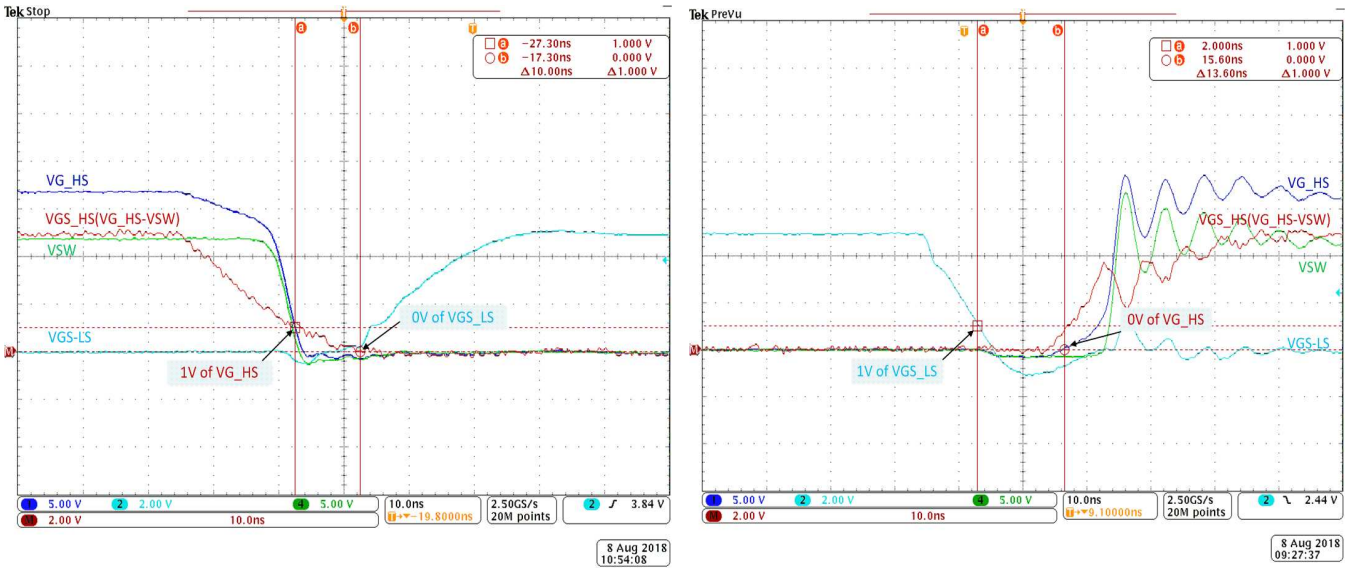
Differential probe (such as TEK TDP1000, P6251) also can be selected to catch V_{GS} signal of HS FET directly without math.

For oscilloscope selection, no smaller than 500 MHz bandwidth with 4 channels is needed.

3.2 Four Methods for Dead-time Measurement

As described above and shown in EC table as well, two Dead-times need to be tested, Dead-time from HS FET off to LS FET on and Dead-time from HS FET on to LS FET off. Based on TPS51225EVM, here are four methods for Dead-time measurement.

1. Cursors locate at detection threshold of HS FET and LS FET, Dead-time measurement follows design, from HS FET-off to LS FET-on is 10 ns and from LS FET-off to HS FET-on is 13.6 ns. (See Figure 8)

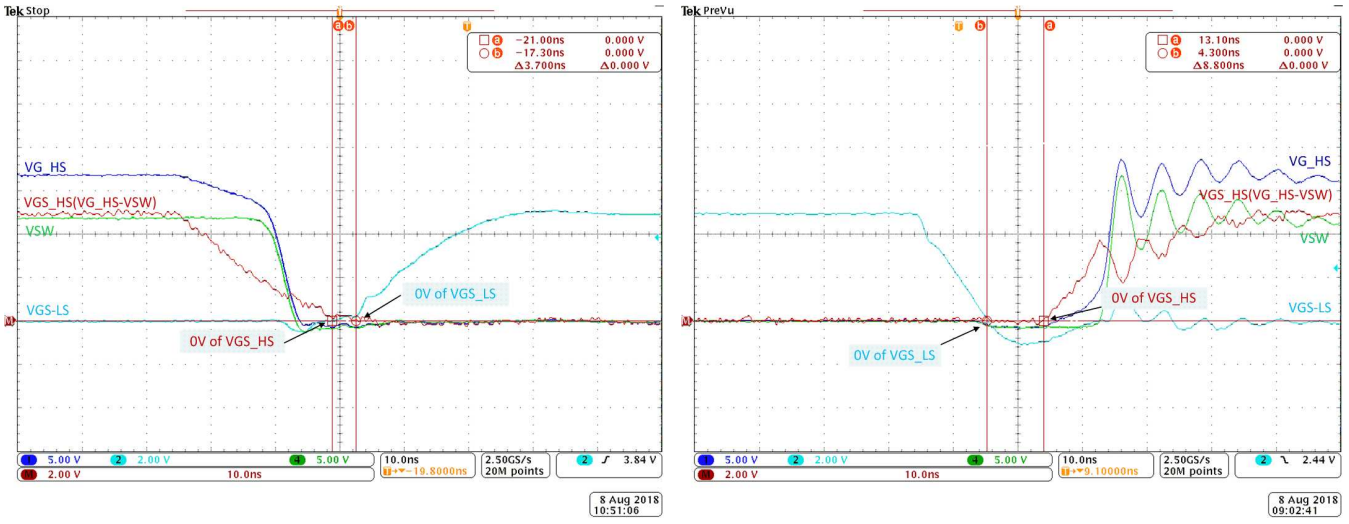


(a) Dead-time from HS FET-off to LS FET-on

(b) Dead-time from LS FET-off to HS FET-on

Figure 8. Dead-time Measurement Follows Design

2. Cursors locate at 0 V of V_{GS} of both HS FET and LS FET, Dead-time from HS FET-off to LS FET-on is 3.7 ns and from LS FET-off to HS FET-on is 8.8 ns. (See Figure 9)

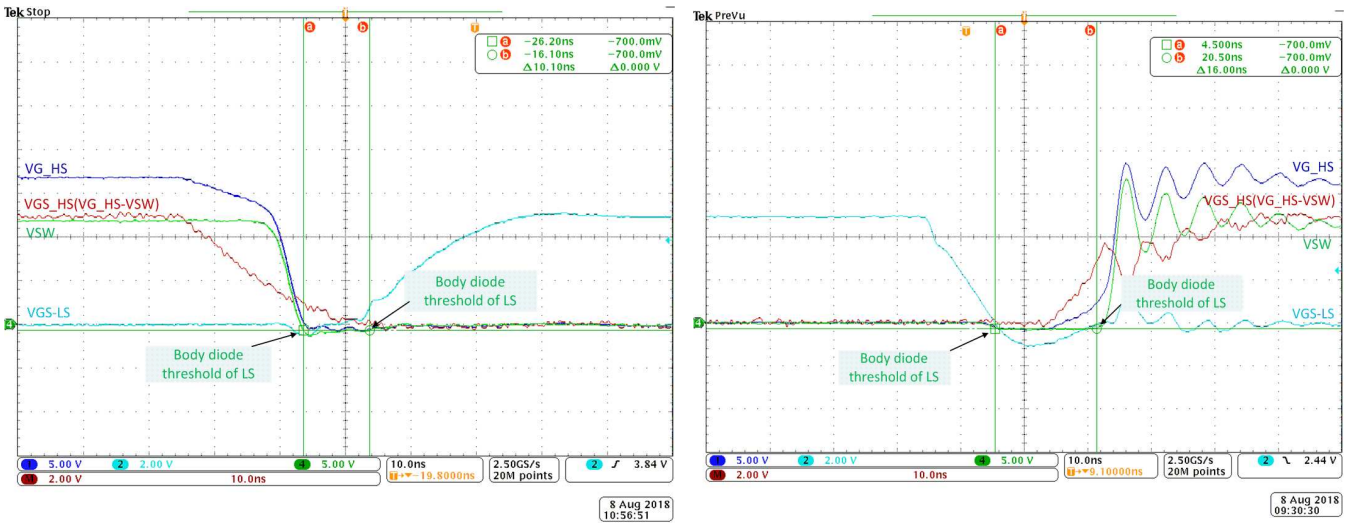


(a) Dead-time from HS FET-off to LS FET-on

(b) Dead-time from LS FET-off to HS FET-on

Figure 9. Dead-time Measurement for V_{GS} at 0 V

3. Cursors locate at conduction time of LS FET body diode, generally it is –700 mv, Dead-time from HS FET-off to LS FET-on is 10.1 ns and from LS FET-off to HS FET-on is 16 ns (See Figure 10)



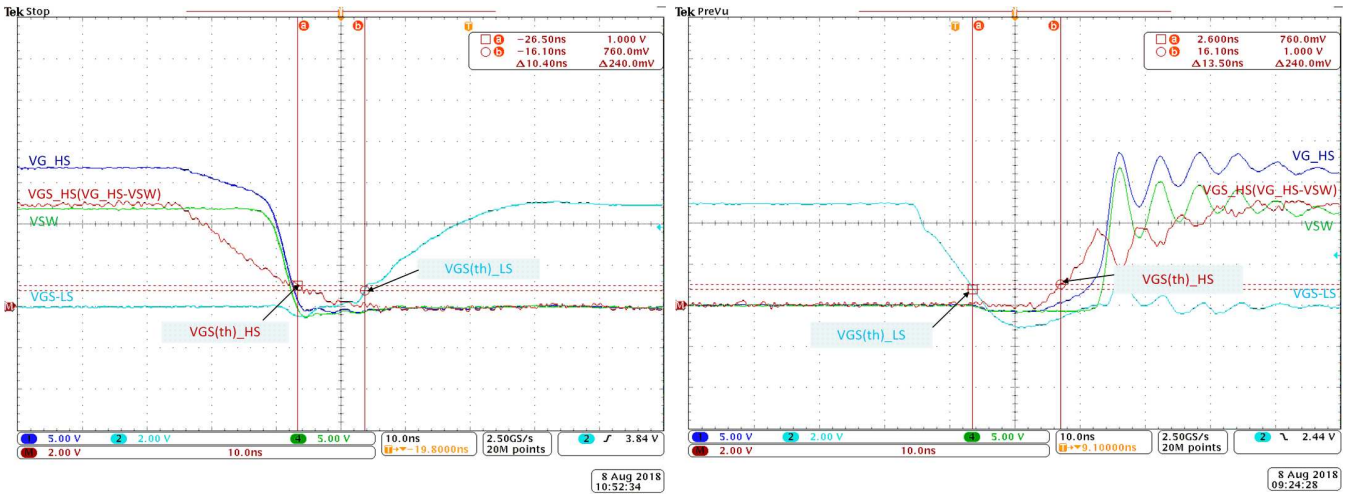
(a) Dead-time from HS FET-off to LS FET-on

(b) Dead-time from LS FET-off to HS FET-on

Figure 10. Dead-time Measurement for LS FET Body Diode Conduction

4. Cursors locate at $V_{GS(th)}$ of both HS FET and LS FET, Dead-time from HS FET-off to LS FET-on is 10.4 ns and from LS FET-off to HS FET-on is 13.5 ns (See Figure 11)

$V_{GS(th)}$ spec can be found from MOSFET datasheet. CSD87352Q5D is used on TPS51225EVM, minimum $V_{GS(th)}$ of HS FET is 1 V and minimum $V_{GS(th)}$ of LS FET is 0.75 V.



(a) Dead-time from HS FET-off to LS FET-on

(b) Dead-time from LS FET-off to HS FET-on

Figure 11. Dead-time Measurement for $V_{GS(th)}$

4 Conclusion

Dead-time is an important parameter for a synchronous buck circuit. The application note presents fundamental knowledge of Dead-time and shows some methods to check the Dead-time. The last method which uses $V_{GS(th)}$ of MOSFETs as check points is more accurately and recommended. Rightly measure the real Dead-time can be used to justify the risk of shoot though.

5 References

- TPS51225 Datasheet (Dual Synchronous, Step-Down Controller with 5-V and 3.3-V LDOs)
- TPS51225EVM User Guide (Dual Synchronous, Step-Down Controller with 5-V and 3.3-V LDOs)
- TPS51275 Datasheet (Dual Synchronous, Step-Down Controller with 5-V and 3.3-V LDOs)
- TPS51285 Datasheet (Ultra-Low Quiescent (ULQ ™) Dual Synchronous Step-Down Controller with 5V and 3.3V LDOs)
- MOSFET Drive Circuit Design Guide for TPS512XX (MOSFET Drive Circuit Design Guide for TPS512xx)
- CSD87352Q5D Datasheet (CSD87352Q5D Synchronous Buck NexFET ™ Power Block)

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