

Application Report

BQ24610

Functional Safety FIT Rate, and Pin FMA



Table of Contents

1 Overview.....	2
2 Functional Safety Failure In Time (FIT) Rates.....	4
3 Pin Failure Mode Analysis (Pin FMA).....	5

Trademarks

All other trademarks are the property of their respective owners.

1 Overview

This document contains information for BQ24610 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Pin failure mode analysis (Pin FMA)

[Figure 1-1](#) shows the device functional block diagram for reference.

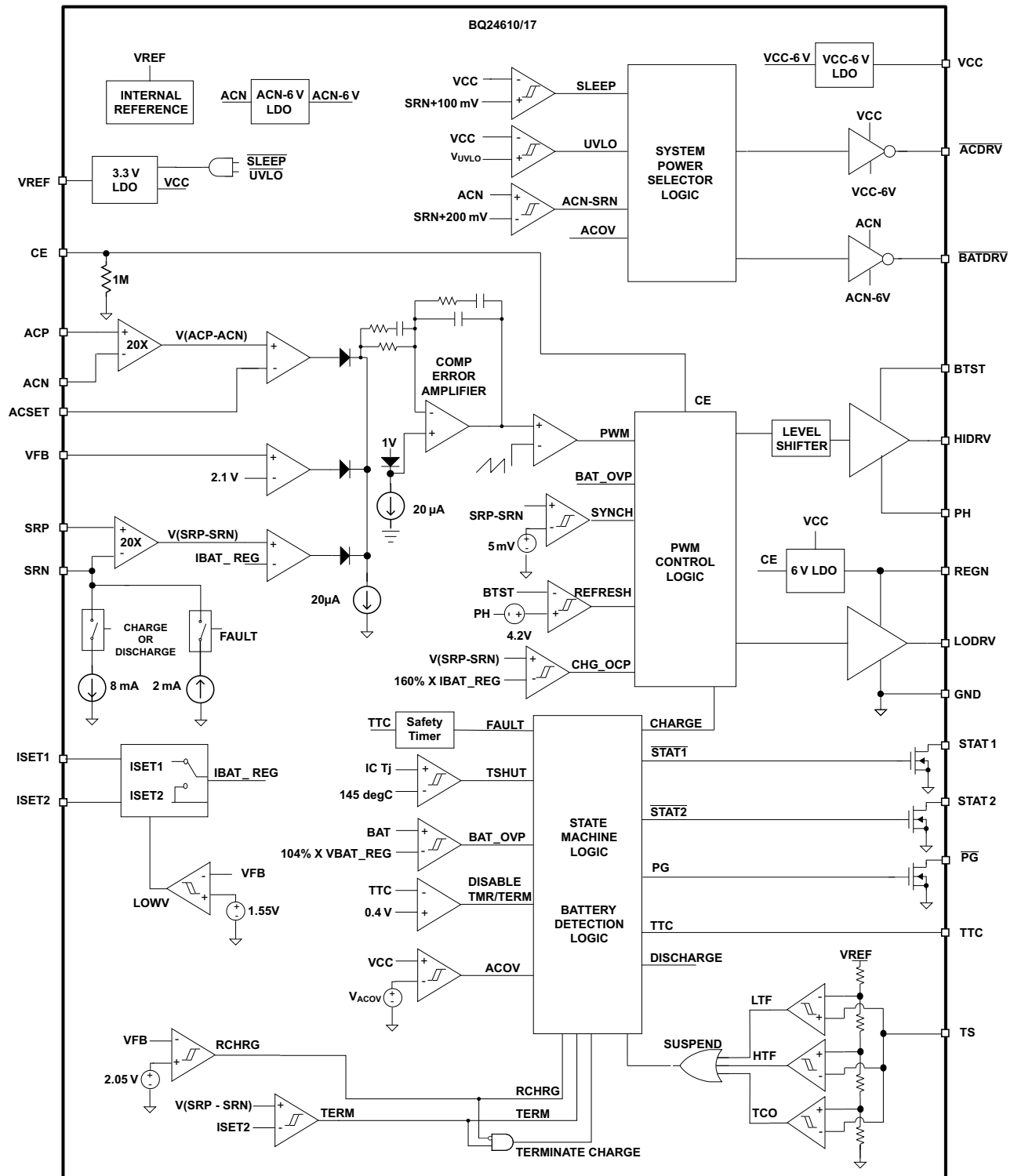


Figure 1-1. Functional Block Diagram

BQ24610 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for BQ24610 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total Component FIT Rate	14
Die FIT Rate	3
Package FIT Rate	11

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 250 mW
- Climate type: World-wide Table 8
- Package factor (λ_3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the BQ24610. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 3-2](#))
- Pin open-circuited (see [Table 3-3](#))
- Pin short-circuited to an adjacent pin (see [Table 3-4](#))
- Pin short-circuited to input supply (+15V) (see [Table 3-5](#))

[Table 3-2](#) through [Table 3-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 3-1](#).

Table 3-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 3-1](#) shows the BQ24610 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the BQ24610 data sheet.

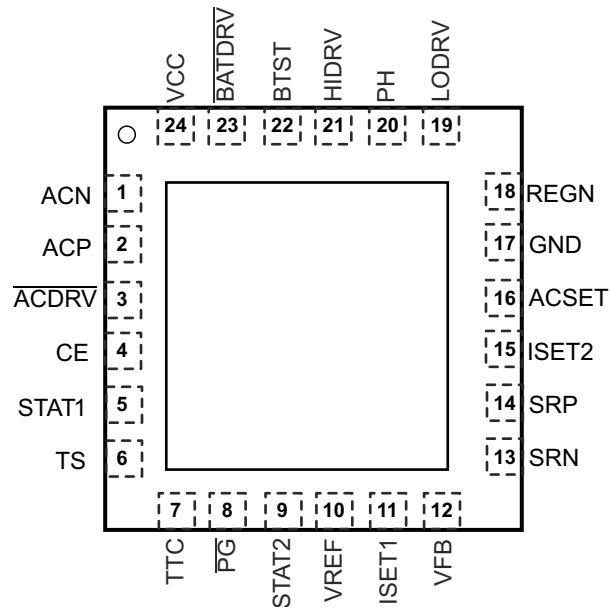


Figure 3-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Input supply = 15V
- Battery = 11.4V
- Default EVM setup otherwise

Table 3-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ACN	1	Unregulated current flow from adapter to GND which can potentially damage the input reverse blocking FET	A
ACP	2	Unregulated current flow from adapter to GND which can potentially damage the input reverse blocking FET	A
ACDRV	3	Normal charging operation but input reverse blocking FETs will remain permanently on. Possible damage of input reverse blocking FETs if VCC > max -VGS of PFET	C
CE	4	No charging because charge is disabled based on CE logic. Cannot control charge function	B
STAT1	5	Normal charging operation but incorrect charge status indication	D
TS	6	No charging because charge is disabled due to TS fault as VTS < VHTF	B
TTC	7	Normal charging operation but safety timer and termination will be disabled	C
PG	8	Normal charging operation but PG will always indicate adapter present	D
STAT2	9	Normal charging operation but incorrect charge status indication	D
VREF	10	Charge is disabled as VREF to GND causes REGN to collapse.	B
ISET1	11	Normal charging operation but as ISET1 is tied to GND, charge current will be clamped at 125mA	C
VFB	12	No charging because charger will always detect precharge mode, regardless of battery voltage and charge at precharge current. Charge will be disabled after 30 minutes due to precharge safety time.	B
SRN	13	No charging as there is a direct short from battery straight to GND which is a source of potential damage	A
SRP	14	No charging as there is a direct short from battery straight to GND which is a source of potential damage	A
ISET2	15	Normal charging operation but precharge/termination current clamped to 125mA	C
ACSET	16	No charging because input current limit set to 0A	B
GND	17	Normal charging operation	D
REGN	18	No charging as REGN is directly shorted to GND. Neither HSFET nor LSFET can turn on.	B
LODRV	19	Normal charging operation through body diode of LSFET, however LSFET will not turn on.	C
PH	20	No charging but shoot through current can damage switching FET. Shorting PH to GND is also equivalent to having battery short to GND through the inductor as well which is a cause for potential damage.	A
HIDRV	21	No charging as device cannot turn on HSFET.	B
BTST	22	No charging as device cannot turn on HSFET.	B
BATDRV	23	No charging because BATDRV pulled to GND will keep the PFET between BAT and SYS permanently on, and shorts the battery to the input permanently, potentially causing damage.	A
VCC	24	No charging because device cannot power up charger and charger is not functional.	B

Table 3-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ACN	1	No charging because input current limited to 0A	B
ACP	2	No charging because input current limited to 0A	B
ACDRV	3	No charging because device cannot control input reverse blocking FETs	B
CE	4	No charging because charge is disabled by internal 1M Ω pull down resistor according to CE logic. Charging function cannot be controlled	B
STAT1	5	Normal charging operation but STAT1 LED indicator will not show correct charging status	D
TS	6	No charging because charge is disabled due to VTS<VHTF fault	B
TTC	7	No charging as parasitic capacitance causes ~20s safety timer before charge is disabled	C
$\overline{\text{PG}}$	8	Normal charging operation but $\overline{\text{PG}}$ indicator will not show correct adapter status	D
STAT2	9	Normal charging operation but STAT2 indicator will not show correct charging status	D
VREF	10	Normal Charging Operation	D
ISET1	11	Normal charging operation but charge current will be reduced	C
VFB	12	No charging because VFB has internal pulldown and charger IC will detect 0V at VFB regardless of real battery voltage, and will charge at precharge current value. After 30 minutes precharge timer will expire and charge will be disabled.	B
SRN	13	No charging because charge current will be 0A	B
SRP	14	No charging because charge current will be 0A	B
ISET2	15	Normal charging operation but precharge/termination clamped to 125mA	C
ACSET	16	Normal charging operation but ACSET voltage floats causing charge current to rise to setpoint as ACSET voltage changes	C
GND	17	No charging as ground return path is disconnected	B
REGN	18	No charging. REGN charges bootstrap capacitor to provide positive VGS to turn on HSFET, and if REGN is floating, HSFET cannot turn on	B
LODRV	19	Normal charging however device cannot turn on LSFET. Body diode of LSFET will conduct current.	C
PH	20	No charging because device cannot turn on HSFET and converter cannot charge the battery	B
HIDRV	21	No charging because device cannot turn on HSFET and cannot charge the battery	B
BTST	22	No charging because device cannot turn on HSFET and cannot charge the battery	B
BATDRV	23	Normal charging operation when adapter present. BATFET cannot be turned on, so SYS load will flow through body diode of BATFET when adapter is removed.	C
VCC	24	No charging because device cannot power up and charger is not functional.	B

Table 3-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effect(s)	Failure Effect Class
ACN	1	ACP	Normal charging operation but input current limit will not function	C
ACP	2	ACDRV	No charging as input reverse blocking FETs will be permanently turned off	B
ACDRV	3	CE	Normal charging operation as CE is always enabled	D
CE	4	STAT1	Normal charging operation but CE pulls high on STAT1 and STAT1 LED indicator will report incorrect charging status	D
STAT1	5	TS	Battery charge current fluctuates periodically based on STAT, TS, and deglitch timers. Device enters in and out of TS faults.	C
TS	6	TS	Last pin of row	N/A
TTC	7	PG	Normal charging operation, but safety timer and termination disabled as PG pulls low on TTC	C
PG	8	STAT2	Normal charging operation but incorrect adapter and charge status indication.	D
STAT2	9	VREF	Normal charging operation but incorrect STAT2 termination indication as VREF pulls STAT2 high.	D
VREF	10	ISET1	Normal charging operation but charge current will be higher than expected as VREF pulls ISET1 to 3.3V causing ISET1 to be clamped at 2V.	C
ISET1	11	VFB	Normal charging operation but charge current will change depending on VFB voltage	C
VFB	12	VFB	Last pin of row	N/A
SRN	13	SRP	Normal charging operation but unregulated charge current due to lack of feedback to current loop. Input current will be regulated by ACSET setpoint.	C
SRP	14	ISET2	Potential pin damage if battery voltage exceeds abs max of ISET2.	A
ISET2	15	ACSET	Normal charging operation but ISET2 is pulled to ACSET voltage, resulting in precharge and termination settings being different than expected	C
ACSET	16	GND	No charging and input current limit set to 0A	B
GND	17	GND	Last pin of Row	N/A
REGN	18	LODRV	Potential damage as LSFET will always be on, and shoot through current can damage switching FETs	A
LODRV	19	PH	Device cannot turn off LSFET and cannot charge the battery. When HSFET turns on, shoot through current can damage switching FETs, and potential damage to LODRV if PH exceed abs max of LODRV	A
PH	20	HIDRV	No charging as device cannot turn on the HSFET	B
HIDRV	21	BTST	HSFET will only turn on when LSFET is on which can cause shoot through current that potentially damages switching FETs	A
BTST	22	BATDRV	Abnormal charging operation as BATFET can be turned ON every switching cycle, shorting the battery to the input supply while the low-side FET is on (BTST = REGN). Potential for damage when LSFET is on.	A
BATDRV	23	VCC	Normal charging operation when adapter is connected, but device cannot turn on BATFET. When adapter removed, system current will flow through body diode of BATFET	C
VCC	24	VCC	Last pin of row	N/A

Table 3-5. Pin FMA for Device Pins Short-Circuited to input supply (+15V)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ACN	1	Normal charging operation but input current limit will not function	C
ACP	2	Normal charging operation but input current limit will not function	C
ACDRV	3	No charging as input reverse blocking FETs will always be off	B
CE	4	Normal charging operation based on CE logic	C
STAT1	5	Normal charging operation but incorrect charging status indication	D
TS	6	No charging as TS fault will be detected. Potential damage if input supply voltage exceeds abs max of TS	A
TTC	7	Normal charging operation but safety timer will be disabled. Potential damage if input supply voltage exceeds abs max of TTC	A
/PG	8	Normal charging operation but PG indicator will not show correct adapter status	D
STAT2	9	Normal charging operation but STAT2 indicator will not show correct charging status	D
VREF	10	No charging and potential pin damage if input supply voltage exceeds abs. max of VREF.	A
ISET1	11	No charging and potential pin damage if input supply voltage exceeds abs max rating of ISET1	A
VFB	12	No charging as charger will detect battery overvoltage if VFB > 2.1V and potential pin damage if input supply voltage exceeds abs max rating of VFB.	A
SRN	13	No charging as there is a direct short from input supply to battery which is a source for potential damage, as well as potential damage if input supply voltage exceeds abs max of SRN	A
SRP	14	No charging as there is a direct short from input supply to battery which is a source for potential damage, as well as potential damage if input supply voltage exceeds abs max of SRN	A
ISET2	15	No charging and potential pin damage if input supply voltage exceeds abs max rating of ISET2	A
ACSET	16	No charging and potential pin damage if input supply voltage exceeds abs max rating of ACSET	A
GND	17	No charging but battery will supply SYS through BATFET.	B
REGN	18	No charging and potential damage if input supply exceeds abs max of REGN	A
LODRV	19	No charging as device cannot turn off LSFET which will result in shoot through current and potential damage the switching FETs. Potential pin damage if input supply voltage exceeds abs max of LODRV pin	A
PH	20	No charging and potential damage as uncontrolled current will flow from input supply to battery, and shoot through current can damage the switching FETs	A
HIDRV	21	No charging and potential damage as HSFET will turn on when LSFET runs on, shoot through current can damage the switching FETs	A
BTST	22	Cannot turn on the HSFET as it requires a positive VGS but BTST = VCC	B
BATDRV	23	Normal charging operation but BATFET cannot turn on when adapter is removed and when no adapter is present, SYS current will flow through body diode of BATFET	C
VCC	24	No issue as this is the supply	D

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated