Application Note

How to Compensate for Cable Losses With BQ25758

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ABSTRACT

Many dc/dc converters like BQ25758 provide a remote sense pin for regulating the converters output voltage. This remote sense pin can be unable to connect directly to the system load. A cable that connects this regulated output to the system load has a finite resistance. The voltage drop created by this resistance and load current varies with system load. This results in the load voltage being less than the programmed voltage as the system load increases. This application note provides an external analog circuit to compensate for the resistive voltage drop across a cable as a function of system load.

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Trademarks

1 Introduction

Figure 1-1 is a block diagram of the BQ25758 dc/dc regulator.

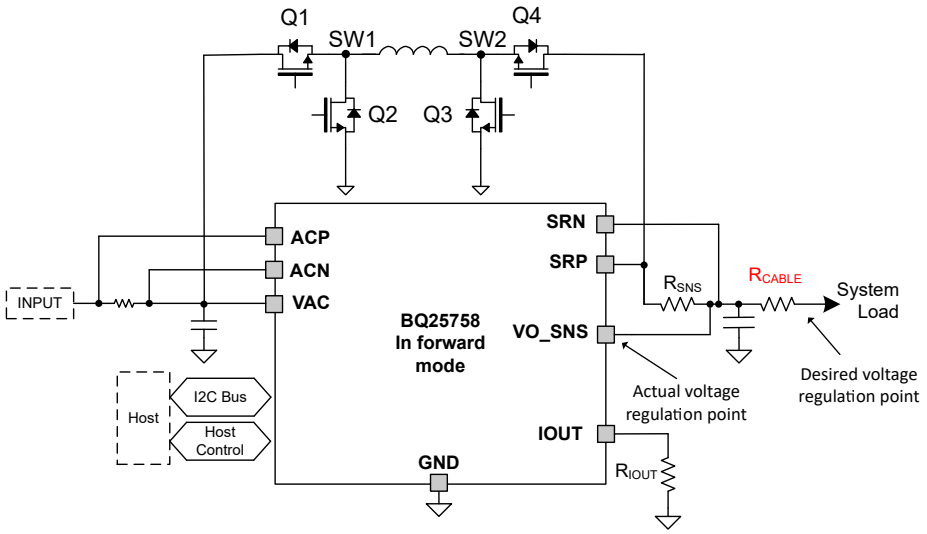

Figure 1-1. BQ25758 Typical Application Block Diagram

The BQ25758's regulation point is the VO_SNS pin. The converter's VO_SNS is connected as close as possible to the system load to account for resistance losses. However, if a cable is required to connect the output of the end equipment to the system load, the cable resistance causes a voltage drop from the VO_SNS regulation point to the system load. If the cable resistance and the system load current is always known, or an ADC is available to measure the system load, host software can increase the regulation point as a function of system load to account for the voltage drop. Typically, the system load varies too much or too quickly for the host software to respond. A different method to dynamically compensate for the voltage drop across a known cable resistance is presented in the following section.

2 Derivation

Composed of four additional components, an analog feedback circuit, as highlighted in blue in Figure 2-1, can account for the voltage drop across the cable as a function of system load.

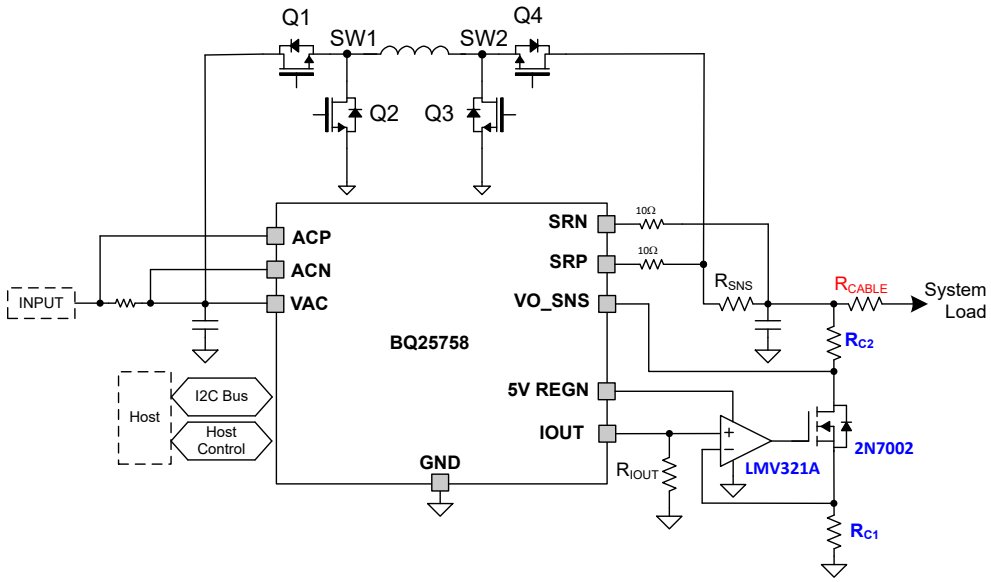

Figure 2-1. BQ25758 with Cable Compensation Circuit Block Diagram

The host software programs the BQ25758 VOUT_REG register to the desired regulation voltage. R_{IOUT} is sized to be least 10% higher than the maximum expected system load current. The converter then regulates the VO_SNS pin to VOUT_REG voltage, regardless of load current. But, we want the voltage at the other side of the cable, VSYS_LOAD to be VOUT_REG, which means:

$$V(SRN) = V_{OUT\_REG} + I_{SYS} \times R_{CABLE} = V_{SYS\_LOAD} + I_{SYS} \times R_{CABLE} \quad (1)$$

The IOUT pin voltage, V(IOUT), is proportional to the system load current as sensed across resistor R_{SNS} by SRN and SRP pins. Specifically,

$$V\left(IOUT\right) = \frac{I_{SYS} \times V_{REF\_IOUT} \times R_{IOUT}}{K_{IOUT(A \times k\Omega)}} \quad (2)$$

Where V_{REF_IOUT} is 2V ± 0.5% and K_{IOUT} is 50A x kΩ ± 4%. The LMV321A amplifier negative feedback loop regulates the voltage across compensation resistor RC1 to be V(IOUT) so

$$V_{OUT\_REG} + \frac{V(IOUT)}{R_{C1}} \times R_{C2} = V\left(SRN\right) \quad (3)$$

Combining these equations gives

$$V_{SYS\_LOAD} + I_{SYS} \times R_{CABLE} = V_{OUT\_REG} + \frac{I_{SYS} \times V_{REF\_IOUT} \times R_{IOUT}}{K_{IOUT(A \times k\Omega)}} \times \frac{R_{C2}}{R_{C1}} \quad (4)$$

Where as,

$$V_{SYS\_LOAD} + I_{SYS} \times R_{CABLE} = V_{OUT\_REG} + \frac{I_{SYS} \times V_{REF\_IOUT} \times R_{IOUT}}{K_{IOUT(A \times k\Omega)}} \times \frac{R_{C2}}{R_{C1}} \quad (5)$$

Which reduces to

$$\frac{R_{C2}}{R_{C1}} = R_{CABLE} \times \frac{K_{IOUT(A \times k\Omega)}}{V_{REF\_IOUT} \times R_{IOUT}} \quad (6)$$

With R_{SNS} << R_{CABLE} and knowing that K_{IOUT}/V_{REF_IOUT} is approximately 125Ω / R_{SNS}, the equation below can be used to find the value of one compensation resistors after selecting the other to be in the 10kΩ range.

$$\frac{R_{C2}}{R_{C1}} = \frac{125\Omega \times R_{CABLE}}{R_{SNS} \times R_{IOUT}} \quad (7)$$

3 Measured Results

With PFM disabled to lower the voltage regulation point at no load, the converter's voltage regulation accuracy over temperature at the VO_SNS pin is ±2%, regardless of system load current. If R_{CABLE} = 0.250Ω connects VO_SNS to the system load and no cable compensation is provided, the voltage at VSYS_LOAD can be VOUT_REG ±2% - 0.250mV/A of system load.

The cable compensation circuit intends to correct for this reduction in voltage at the system load. Measured results with the cable compensation circuit, R_{CABLE} = 0.250Ω, R_{IOUT} = 6.19kΩ, RC1 = 10kΩ and from Equation 7, RC2 =10.1kΩ are shown in Table 3-1.

Table 3-1. Measured Results for VAC = 20V and T_A = 25°C

VOUT_REG (V)	ISYS_LOAD (A)	VSYS_LOAD (V)
5	0	5.007
5	1	5.035
5	3	5.063
9	0	9.025
9	1	9.042
9	3	9.066
12	0	12.018
12	1	12.037
12	3	12.063
15	0	15.023
15	1	15.046
15	3	15.072
15	5	15.090
20	0	20.057
20	1	20.077
20	3	20.095
20	5	20.105

With V(IOUT) having K ±4% and VREF ± 0.5% variation in the computation and ignoring the effects of ±0.5% or better resistors, the worst case dc regulation accuracy over temperature is ± (4%+0.5%+2%) = 6.5% with an average +14mV/A rising slope, a 20X improvement over the -250mV/A for a 0.250Ω cable.

4 Summary

This application note provides an external analog circuit, consisting of an op amp, n-channel mosfet and two resistors, to compensate for the resistive losses that create a voltage drop from the BQ25758 VO_SNS pin to the system load connection point.

5 References

- Texas Instruments, *BQ25758: I2C Controlled, Bidirectional Buck-Boost Controller with Wide Voltage Range,* data sheet.
- Texas Instruments, *LMV3xxA Low-Voltage Rail-to-Rail Output Operational Amplifiers,* data sheet.
- Onsemi, *2N7002-N-Channel Enhancement Mode Field Effect Transistor,* data sheet.

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