User's Guide

TPSM5D1806 Power Module Evaluation Module User's Guide

ABSTRACT

The TPSM5D1806 evaluation module (EVM) is designed as an easy-to-use platform that facilitates an extensive evaluation of the features and performance of the TPSM5D1806 power module. The module (U1) located on the top-half of the board is configured as a dual output (VOUT1 and VOUT2) device. The module (U2) located on the bottom-half of the board is configured as an interleaved buck converter where the two outputs are paralleled to provide a higher output current (VOUT3). Each of the three output voltages can be set to one of five popular values by using a configuration jumper. Input and output capacitors are included on the board to accommodate the entire range of input voltage and the selectable output voltages on the EVM. Monitoring test points are provided to allow measurement of the following:

- Efficiency
- Power dissipation
- Input ripple
- Output ripple
- Line and load regulation
- Transient response

Control test points and component footprints are provided for use of the enable (EN), power-good (PGOOD), and SYNC features of the device. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

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Trademarks

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1 Getting Started

Figure 1-1 highlights the user interface items associated with the EVM. The *VIN* and *PGND* terminal blocks (J1 and J3) are used for connection to the host input supply and the *VOUT* and *PGND* terminal blocks (J4, J10, J13, J16) are used for connection to the load. These terminal blocks can accept up to 16-AWG wire.

Table 1-1. TPSM5D1806EVM Operating Range

Device	Output Voltage	Output Current Range	Input Voltage
U1 Dual Output	V_{OUT1} = 0.8 V, 1.0 V, 1.2 V, 1.8 V, or 3.3 V	0 to 6 A per output	V_{IN} = 4.5 V to 15 V
	V_{OUT2} = 0.9 V, 1.1 V, 1.2 V, 1.5 V, or 2.5 V		
U2 Parallel Output	V_{OUT3} = 0.9 V, 1.0 V, 1.1 V, 1.2 V, or 1.8 V	0 to 12 A	

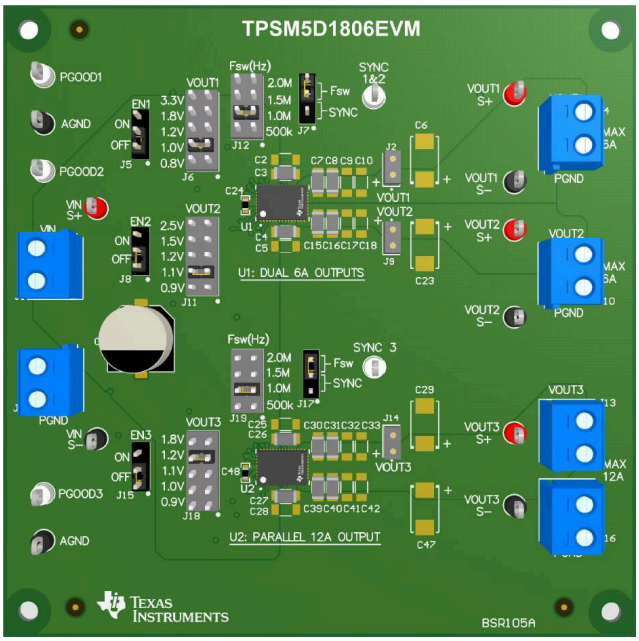

Figure 1-1. EVM User Interface

- The VIN S+ and VIN S- input voltage test points as well as the VOUT S+ and VOUT S- output voltage test points, located near the power terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure VIN and VOUT. **Do not use these S+ and S- monitoring test points as the input supply or output load connection points.** The PCB traces connecting to these test points are not designed to support high currents.
- The VOUT1 (J2), VOUT2 (J9) and VOUT3 (J14) scope sockets can be used to monitor VOUT waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1 inch centers. The scope probe tip should be inserted into the socket marked with a white dot printed on the board and the scope ground lead should be inserted into the other socket.
- The control test points located around the device are made available to test the features of the device. Refer to Test Point Descriptions for more information on the individual control test points.
- The VOUT jumpers (J6, J11, J18) and F_{SW} jumpers (J12, J19) are provided to select the desired output voltage and appropriate switching frequency. The Fsw/SYNC jumpers (J7, J17) are provided to select the desired switching frequency method, either to an external clock (SYNC) or the switching frequency (Fsw) selected by the F_{SW} jumpers. Before applying power to the EVM, make sure that the jumpers are present and properly positioned for the intended output voltage. Always remove input power before changing the jumper settings.

2 Test Point Descriptions

Wire-loop test points and scope probe sockets are included for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. A description of each test point follows:

Table 2-1. Test Point Descriptions

Name[1]	Description
VIN S+	Input voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency.
VIN S-	Input voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency.
VOUT1 S+	Output 1 voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation and load regulation.
VOUT1 S-	Output 1 voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation and load regulation.
VOUT2 S+	Output 2 voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation and load regulation.
VOUT2 S-	Output 2 voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation and load regulation.
VOUT3 S+	Output 3 voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation and load regulation.
VOUT3 S-	Output 3 voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation and load regulation.
AGND	Analog ground test point.
PGND	Power ground test point.
VOUT SCOPE (J2, J9, J14)	Output voltage scope monitor. Connect an oscilloscope probe to this set of points to measure output ripple voltage and transient response.
ENABLE (J5, J8, J15)	For ease of use, J13 can be set in the ON position to enable the device or in the OFF position to disable the device.
PGOOD1	Monitors the power good signal of Channel 1 output. This is an open drain signal.
PGOOD2	Monitors the power good signal of Channel 2 output. This is an open drain signal.
PGOOD3	Monitors the power good signal of Channel 3 output. This is an open drain signal.
SYNC1&2	Synchronization input test point of U1. When synchronizing to an external clock connect to this test point.
SYNC 3	Synchronization input test point of U2. When synchronizing to an external clock connect to this test point.

(1) Refer to the product data sheet for absolute maximum ratings associated with above features.

3 PCB Layout

Figure 3-1 through Figure 3-8 show the PCB layers of the TPSM5D1806EVM.

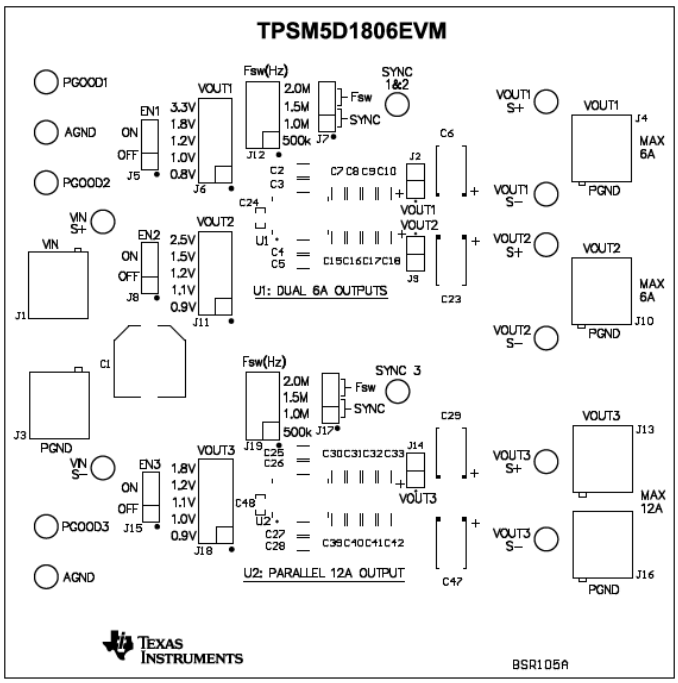

Figure 3-1. Topside Component View (Top View)

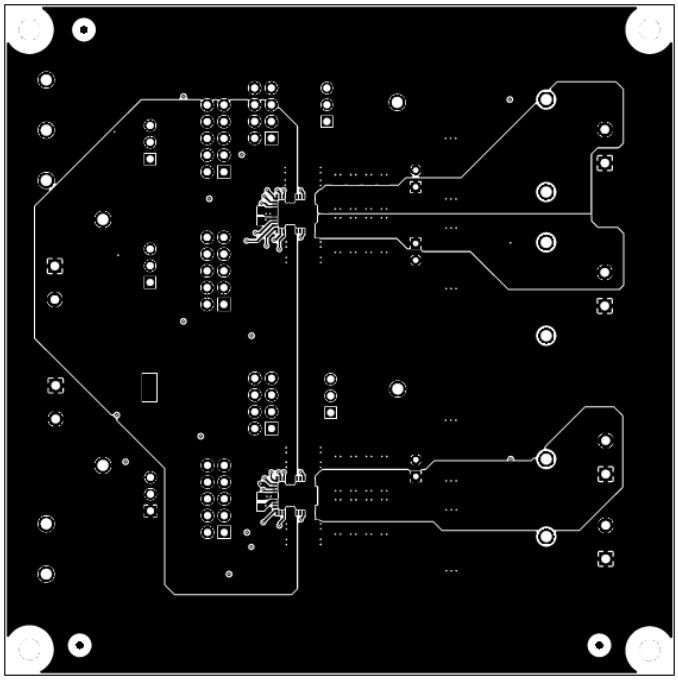

Figure 3-2. Layer 1 (Top View)

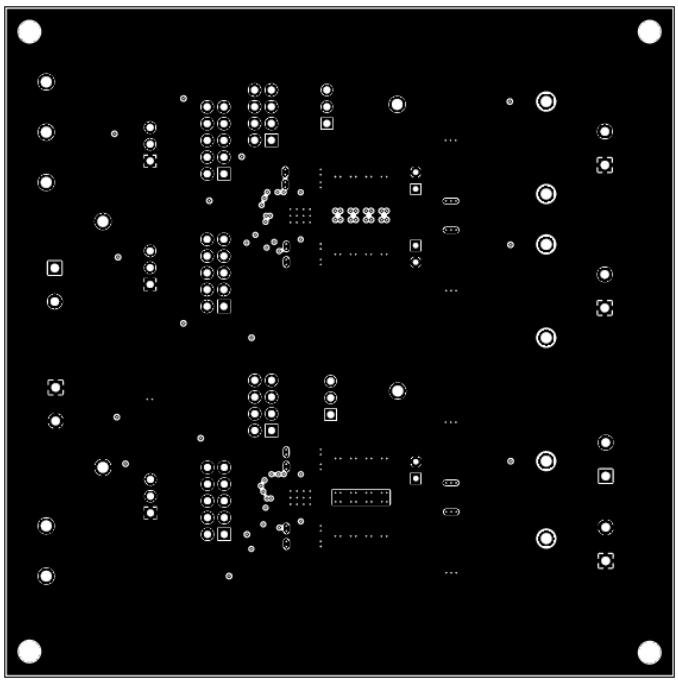

Figure 3-3. Layer 2 (Top View)

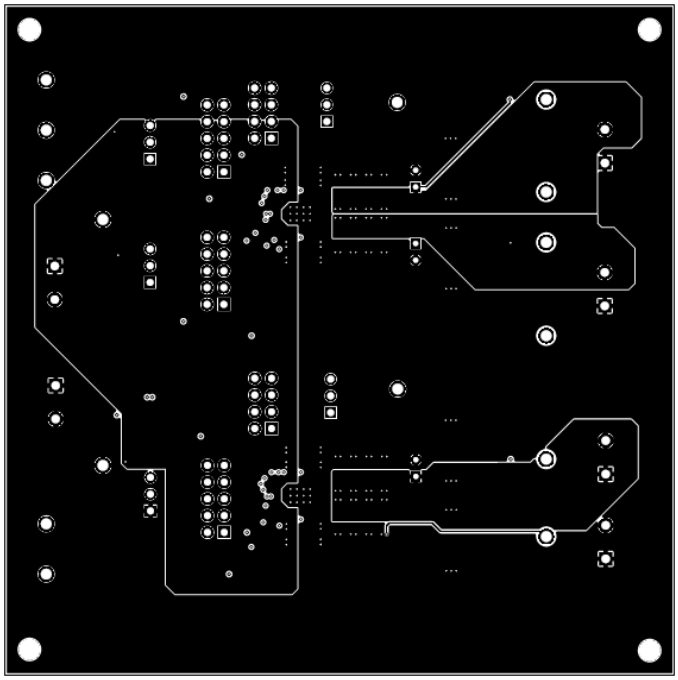

Figure 3-4. Layer 3 (Top View)

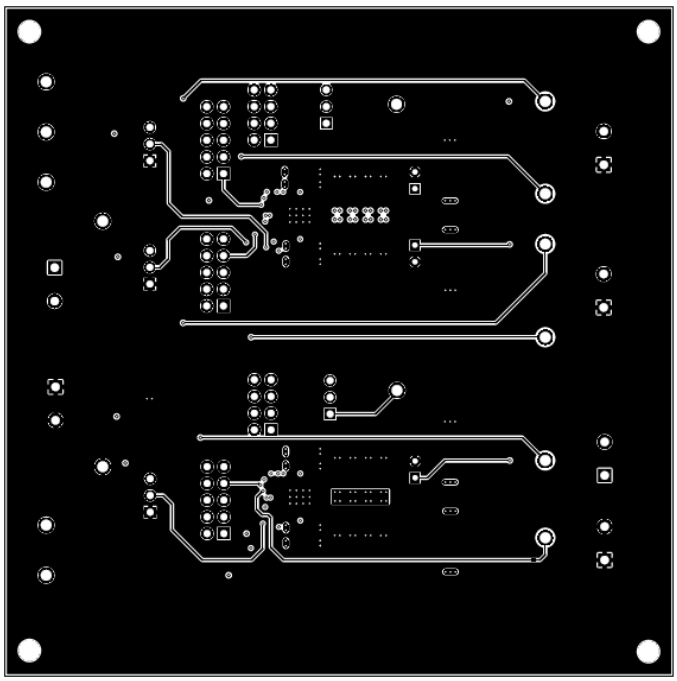

Figure 3-5. Layer 4 (Top View)

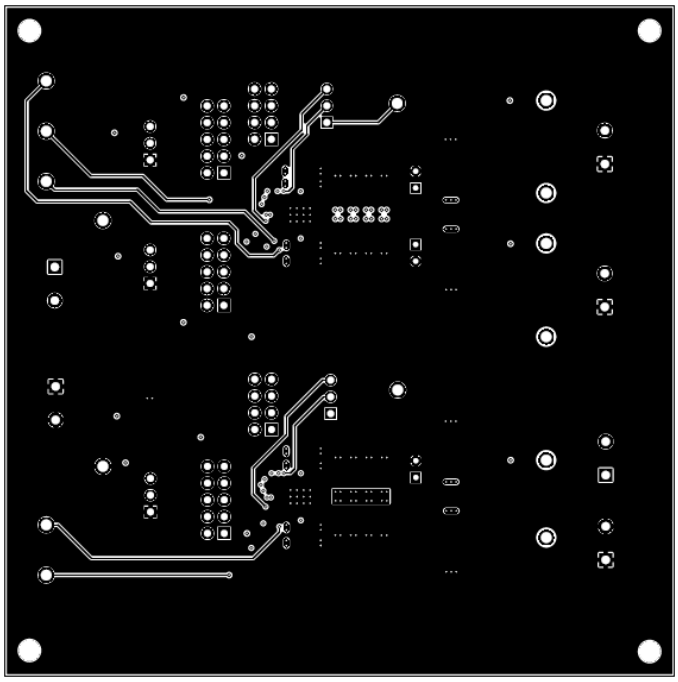

Figure 3-6. Layer 5 (Top View)

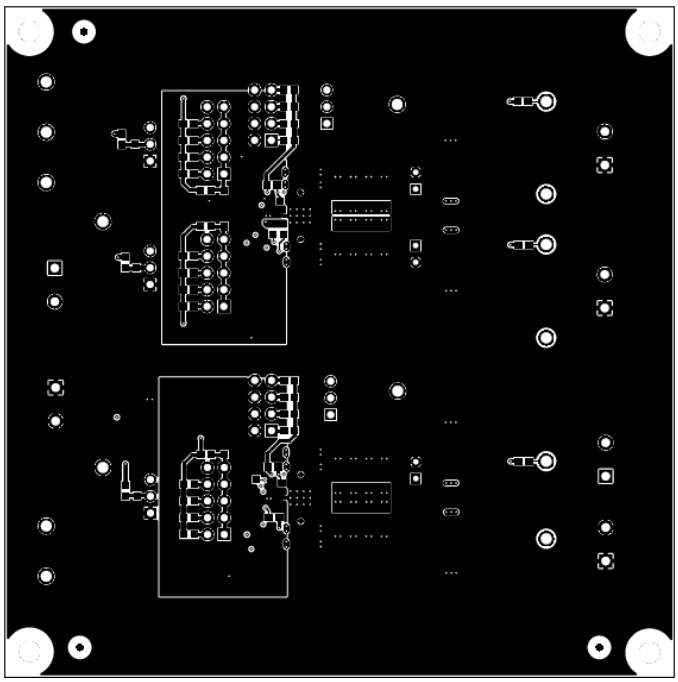

Figure 3-7. Layer 6 (Top View)

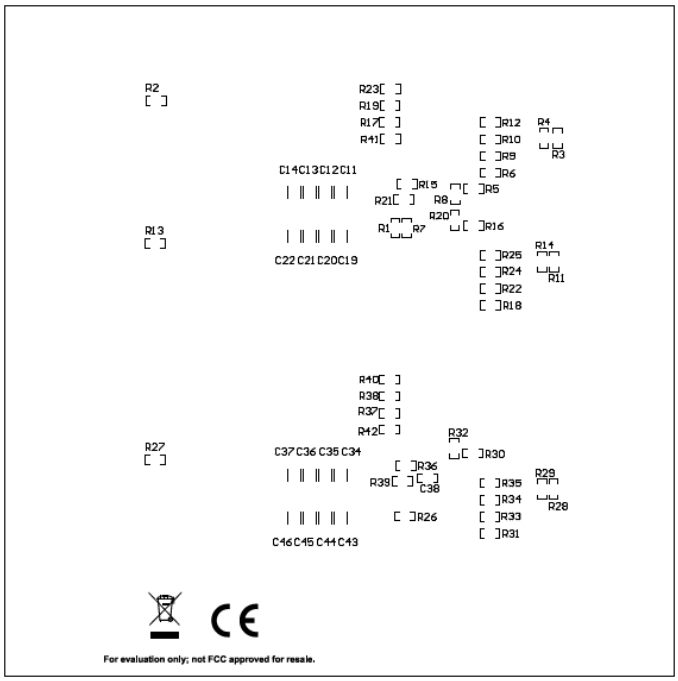

Figure 3-8. Bottom-Side Component Layout (Bottom View)

4 Schematic

Figure 4-1 is the schematic for the top-half of TPSM5D1806EVM.

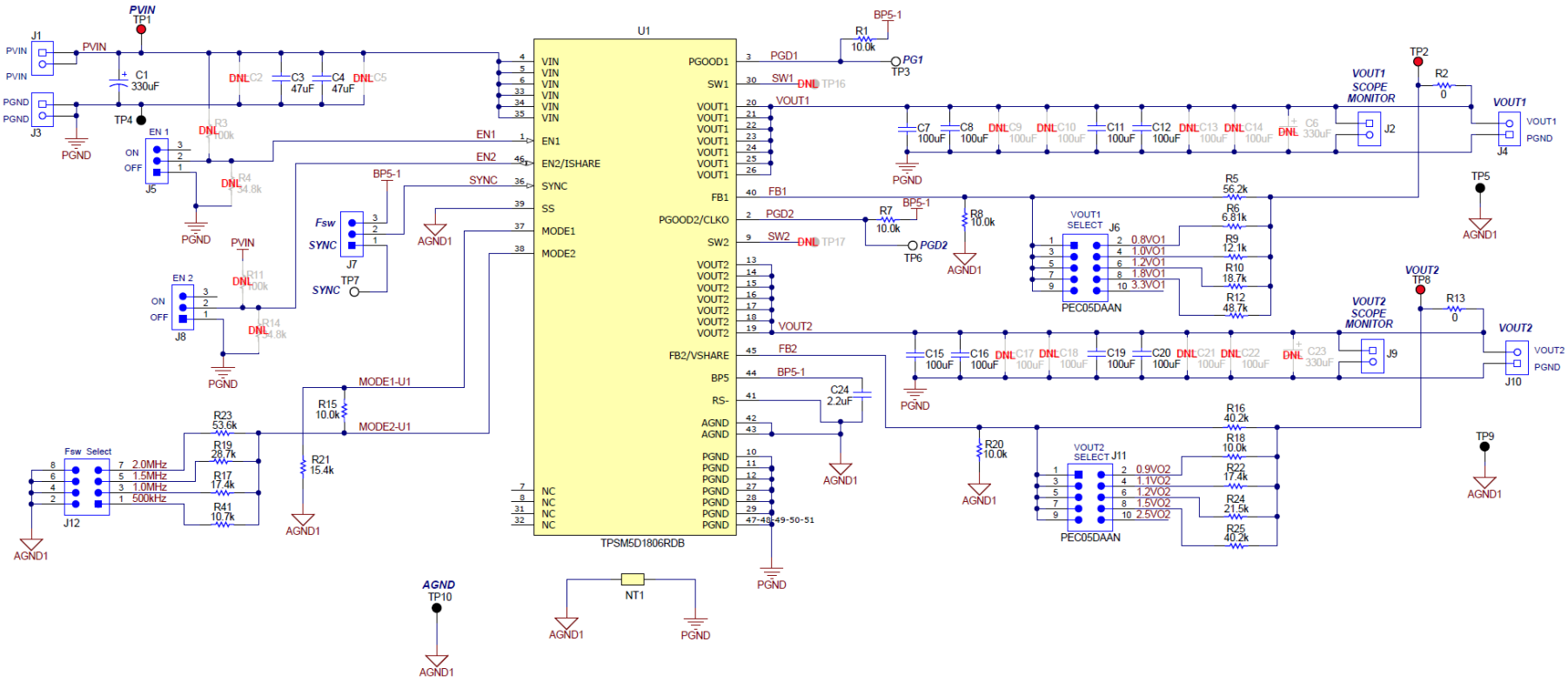

Figure 4-1. TPSM5D1806EVM Independent Dual Output Schematic

Figure 4-2 is the schematic for the bottom-half of TPSM5D1806EVM.

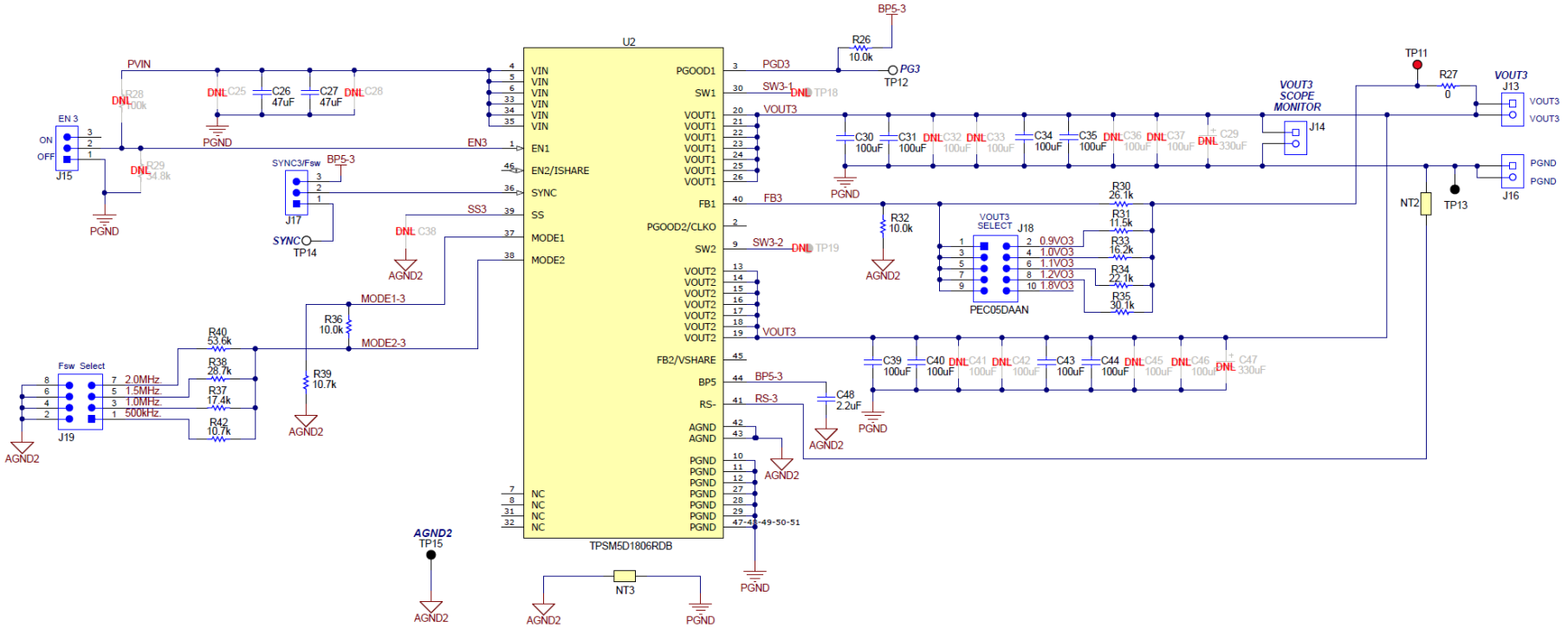

Figure 4-2. TPSM5D1806EVM Independent Parallel Output Schematic

5 Bill of Materials (BOM)

Table 5-1 lists the EVM BOM.

Table 5-1. TPSM5D1806EVM Bill of Materials

Designator	Qty	Value	Description	Size	Part Number
C1	1	330uF	CAP, AL, 330 uF, 25 V	SMT Radial G	EEE-FC1E331P
C3, C4, C26, C27	4	47uF	CAP, CERM, 47 uF, 25 V, X5R	1206	C3216X5R1E476M160AC
C7, C8, C11, C12, C15, C16, C19, C20, C30, C31, C34, C35, C39, C40, C43, C44	16	100uF	CAP, CERM, 100 uF, 25 V, X5R	1206	GRM31CR60J107ME39L
C24, C48	2	2.2uF	CAP, CERM, 2.2 uF, 16 V, X6S	0603	GRM188Z71C225KE43
J1, J3, J4, J10, J13, J16	6		Terminal Block, 5.08 mm, 2x1	2x1 5.08mm	ED120/2DS
J2, J9, J14	3		Socket Strip, 2x1, 100mil	2x1, 100mil	310-43-102-41-001000
J5, J7, J8, J15, J17	5		Header, 100mil, 3x1, Tin, TH	3x1, 100mil	PEC03SAAN
J6, J11, J18	3		Header, 100mil, 5x2, Tin, TH	5x2, 100mil	PEC05DAAN
J12	1		Header, 100mil, 4x2, Tin, TH	4x2, 100mil	PEC04DAAN
J19	1		Header, 100mil, 3x2, Tin, TH	3x2, 100mil	PEC03DAAN
R1, R7, R8, R15, R18, R20, R26, R32, R36	9	10.0k	RES, 10.0 k, 1%, 0.1 W	0603	CRCW060310K0FKEA
R2, R13, R27	3	0	RES, 0, 5%, 0.1 W	0603	CRCW06030000Z0EA
R5	1	56.2k	RES, 56.2 k, 1%, 0.1 W	0603	CRCW060356K2FKEA
R6	1	6.81k	RES, 6.81 k, 1%, 0.1 W	0603	CRCW06036K81FKEA
R9	1	12.1k	RES, 12.1 k, 1%, 0.1 W	0603	CRCW060312K1FKEA
R10	1	18.7k	RES, 18.7 k, 1%, 0.1 W	0603	CRCW060318K7FKEA
R12	1	48.7k	RES, 48.7 k, 1%, 0.1 W	0603	CRCW060348K7FKEA
R16, R25	2	40.2k	RES, 40.2 k, 1%, 0.1 W	0603	CRCW060340K2FKEA
R17, R22, R37	3	17.4k	RES, 17.4 k, 1%, 0.1 W	0603	CRCW060317K4FKEA
R19, R38	2	28.7k	RES, 28.7 k, 1%, 0.1 W	0603	CRCW060328K7FKEA
R21	1	15.4k	RES, 15.4 k, 1%, 0.1 W	0603	CRCW060315K4FKEA
R23, R40	2	53.6k	RES, 53.6 k, 1%, 0.1 W	0603	CRCW060353K6FKEA
R24	1	21.5k	RES, 21.5 k, 1%, 0.1 W	0603	CRCW060321K5FKEA
R30	1	26.1k	RES, 26.1 k, 1%, 0.1 W	0603	CRCW060326K1FKEA
R31	1	11.5k	RES, 11.5 k, 1%, 0.1 W	0603	CRCW060311K5FKEA
R33	1	16.2k	RES, 16.2 k, 1%, 0.1 W	0603	CRCW060316K2FKEA
R34	1	22.1k	RES, 22.1 k, 1%, 0.1 W	0603	CRCW060322K1FKEA
R35	1	30.1k	RES, 30.1 k, 1%, 0.1 W	0603	CRCW060330K1FKEA
R39, R41, R42	3	10.7k	RES, 10.7 k, 1%, 0.1 W	0603	CRCW060310K7FKEA
TP1, TP2, TP8, TP11	4		Test Point, Multipurpose, Red	Red TP	5010
TP3, TP6, TP7, TP12, TP14	5		Test Point, Multipurpose, White	Black TP	5012
TP4, TP5, TP9, TP10, TP13, TP15	6		Test Point, Multipurpose, Black	White TP	5011
U1, U2	2		18-V, 6A, Power Module	QFN-FCMOD51	TPSM5D1806RDB
Not Loaded					
C6, C23, C29, C47	0			7343-40	
C2, C5, C9, C10, C13, C14, C17, C18, C21, C22, C25, C28, C32, C33, C36, C37, C41, C42, C45, C46	0			1206	
C38	0			0603	
R3, R4, R11, R14, R28, R29	0			0603	

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2021) to Revision B (April 2021)	Page
• Updated user's guide title	2

Changes from Revision * (November 2020) to Revision A (February 2021)	Page
• Updated Input Voltage range in *Table 1-1*	2

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265