User's Guide

TPS543B22EVM SWIFT Step-Down Converter Evaluation Module

ABSTRACT

This user's guide contains information for the TPS543B22 evaluation module (BSR178) and the 20 A DC/DC converter. Also included are the performance characteristics, schematic, and bill of materials for the TPS543B22EVM.

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1 Introduction

1.1 Background

The TPS543B22 DC/DC converter is a synchronous buck converter designed to provide up to a 20-A output. The input (VIN) is rated for 4 V to 18 V. Table 1-1 provides the rated input voltage and output current range for the evaluation module.

The high-side and low-side MOSFETs are incorporated inside the TPS543B22 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS543B22 to achieve high efficiencies and helps keep the junction temperature low at the rated output current. Fixed frequency advanced current mode control allows you to synchronize the regulators to an external clock source. An external divider allows for an adjustable output voltage. The TPS543B22 FSEL and MODE pins provide selectable switching frequency, soft-start time, current limit, and internal compensation. Lastly, the TPS543B22 includes an enable pin and a power-good output, which can be used for sequencing multiple regulators.

This evaluation module includes two designs with the TPS543B22. The first design is designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the TPS543B22 regulator. The small area design fits within 275 mm^2. The second design is designed to demonstrate the high efficiency that can be achieved when designing with the TPS543B22 regulator. The second design also includes jumpers that can be used to easily evaluate the features of the TPS543B22.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS543B22EVM	V_{IN} = 4 V to 18 V	0 A to 20 A

1.2 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS543B22EVM. Observe all safety precautions.

CAUTION

The TPS543B22EVM can become hot during operation due to dissipation of power in some operating conditions. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

Caution: Hot surface.

Contact can cause burns.

Do not touch!

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This can result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, then check equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to equipment.

1.3 Performance Characteristics Summary

A summary of the TPS543B22EVM performance characteristics is provided in Table 1-2 and Table 1-3. The TPS543B22EVM is designed and tested for V_{IN} = 4 V to 18 V. Characteristics are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.2 V, unless otherwise specified. The ambient temperature is room temperature (25°C) for all measurements, unless otherwise noted.

Table 1-2. TPS543B22EVM Small Size (U1) Performance Characteristics Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} voltage range		11.7	12	12.3	V
Output voltage setpoint			1.2		V
Output current range	V_{IN} = 11.7 V to 12.3 V	0		20	A
Output rise time	Set by MODE pin resistor		2		ms
Current limit	Set by MODE pin resistor		High		
Switching frequency (f_{SW})	Set by FSEL pin resistor		2200		kHz

Table 1-3. TPS543B22EVM High Efficiency (U2) Performance Characteristics Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} voltage range		4	12	18	V
Output voltage setpoint	J3 short pins 1 and 2		1		V
Output current range	V_{IN} = 4 V to 18 V	0		20	A
Output rise time	Set by MODE pin resistor, All default J13 options		2		ms
Current limit	Set by MODE pin resistor, J9 short pins 1 and 2, 3 and 4, or 5 and 6		High		
Switching frequency (f_{SW})	Set by FSEL pin resistor, J7 short pins 3 and 4		1000		kHz

2 Configurations and Modifications

These evaluation modules are designed to provide access to the features of the TPS543B22. The U2 design provides jumpers for testing different configurations. Jumper selections must be made prior to enabling the TPS543B22.

If a desired configuration is not available, then some modifications can be made to this module. When modifications are made to the components on the EVM, the internal compensation option selected with the MODE pin resistor needs to be changed. Changes to the f_{SW}, output voltage, output inductor, and output capacitors require a change in the compensation. TPS543B22 data sheet equations or WEBENCH can be used to calculate the output capacitor value, compensation, f_{SW}, and inductance. Verify all components have sufficient voltage and current ratings.

2.1 Output Voltage

In the U1 design, the output voltage is set by the resistor divider network of R63 (R_{FBT}) and R60 (R_{FBB}). R60 is fixed at 10.0 kΩ to set the FB divider current at approximately 50 µA. To change the output voltage of the EVM, the value of resistor R63 must change. Changing the value of R63 can change the output voltage above the 0.5-V reference voltage (V_{REF}). The value of R63 for a specific output voltage can be calculated using Equation 1. After changing R63, the feedfoward capacitor (C45) can also need to be changed.

$$R_{FBT} = R_{FBB} \times \left[\frac{V_{OUT}}{V_{REF}} - 1\right] \quad (1)$$

In the U2 design, there are a few ways to set the output voltage. First, jumper J6 can be used to select between the options shown in Table 2-1. If the desired output voltage is not available, a resistor must be changed. For output voltages less than 1.0 V, TI recommends leaving J3 open and increasing R20. R20 becomes R_{FBB} and the required value for can be calculated with Equation 2, where R_{FBT} is R7 which is 10 kΩ. For output voltages greater than 1.0 V, the jumper output voltage options can be changed by changing one of the resistors R16-R19. The R_{FBJ} resistor value to get a desired equivalent R_{FBB} resistance can be calculated with Equation 3. To use J6 for output voltages 3.3 V or larger, R13 must be reduced from 825 Ω to 0 Ω.

$$R_{FBB} = R_{FBT} \times \left[\frac{V_{REF}}{V_{OUT} - V_{REF}}\right] \quad (2)$$

$$R_{FBJ} = \frac{R_{FBB} \times (R13 + R20) - R13 \times R20}{R20 - R_{FBB}} \quad (3)$$

Table 2-1. VOUT Selection

JUMPER SETTING	EQUIVALENT BOTTOM FB RESISTOR (R_{FBB})	NOMINAL OUTPUT VOLTAGE
Open	R20 = 10.0 kΩ	1.00 V
1 to 2 pin shorted(1)	(R16 + R13)||R20 = 7.15 kΩ	1.20 V
3 to 4 pin shorted	(R17 + R13)||R20 = 4.98 kΩ	1.50 V
5 to 6 pin shorted	(R18 + R13)||R20 = 3.87 kΩ	1.80 V
7 to 8 pin shorted	(R19 + R13)||R20 = 1.8 kΩ	3.3 V

(1) Default Setting

2.2 Switching Frequency (FSEL Pin)

In the U2 design, jumper J7 can be used to select between the switching frequency options shown in Table 2-2. If the desired option is not available, change one of the resistors to the value which sets the desired option.

In the U1 design, change the FSEL resistor to the value which sets the desired option.

Table 2-2. FSEL Selection

JUMPER SETTING	FSEL RESISTOR	SWITCHING FREQUENCY
1 to 2 pin shorted	17.4 kΩ	750 kHz
3 to 4 pin shorted(1)	11.8 kΩ	1000 kHz
5 to 6 pin shorted	8.06 kΩ	1500 kHz
7 to 8 pin shorted	4.99 kΩ	2200 kHz

(1) Default Setting

2.3 Current Limit, Soft-Start Time, and Internal Compensation (MODE Pin)

In the U2 design, jumper J9 can be used to select between the current limit, soft-start time, and internal compensation options shown in Table 2-3. If the desired option is not available, change one of the resistors to the value which sets the desired option.

In the U1 design, change the MODE resistor to the value which sets the desired option.

Table 2-3. MODE Selection

JUMPER SETTING	MODE RESISTOR	CURRENT LIMIT	SOFT-START TIME	RAMP
1 to 2 pin shorted	2.21 kΩ	High	2 ms	1 pF
3 to 4 pin shorted(1)	4.87 kΩ	High	2 ms	2 pF
5 to 6 pin shorted	11.3 kΩ	High	2 ms	4 pF
7 to 8 pin shorted	60.4 kΩ	Low	2 ms	2 pF

(1) Default Setting

2.4 Adjustable UVLO

The undervoltage lockout (UVLO) for U2 can be adjusted externally using R12 (R_{ENT}) and R15 (R_{ENB}). See the *TPS543B22 4-V to 18-V Input, 20-A Synchronous SWIFT™ Step-Down Converter with Internally Compensated Advanced Current Mode Control* data sheet for detailed instructions for setting the external UVLO.

The undervoltage lockout (UVLO) for U1 is adjusted externally using R55 (R_{ENT}) and R57 (R_{ENB}).

3 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS543B22EVM evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start-up, and current limit modes. Measurements are taken with the following conditions unless otherwise noted.

- 12-V input
- Room temperature (20°C to 25°C)
- U1 with the default setting output voltage of 1.2 V, switching frequency of 2200 kHz, and maximum current limit setting
- With the other converter disabled

3.1 Input/Output Connections

The TPS543B22EVM is provided with input connectors, output connectors, and test points as shown in Table 3-1 and Table 3-2.

To support the minimum input voltage with the full rated load on both outputs with the default EVM, a power supply capable of supplying greater than 20 A must be connected to J1 through a pair of 18-AWG wires or better.

For U2, the load must be connected to J2 and for U1, the load must be connected to J14. Two pair of 18-AWG wires or better must be used for each connection. With the maximum current limit setting, the maximum load current capability is near 20 A before the TPS543B22 goes into current limit. Wire lengths must be minimized to reduce losses in the wires.

Test point TP30 provides a place to monitor the V_{IN} input voltage with TP33 providing a convenient ground reference for U1. Test point TP2 provides a place to monitor the V_{IN} input voltage with TP9 providing a convenient ground reference for U2. TP31 is used to monitor the output voltage of U1 with TP36 as the ground reference. TP1 is used to monitor the output voltage of U2 with TP16 as the ground reference.

If modifications are made to the TPS543B22EVM, then the input current can change. The input power supply and wires connecting the EVM to the power supply must be rated for the input current.

Note

For the FSEL pin of the TPS543B22 to correctly detect the resistor value connected to ground, the buffers on the EVM need to be provided a VCC voltage of 2 V to 5.5 V to go high impedance.

Table 3-1. Connectors and Jumpers

REFERENCE DESIGNATOR	NAME	RELATED IC	FUNCTION
J1	VIN	Both	VIN screw terminal to connect input voltage (see Table 1-1 for V_{IN} range).
J2	VOUT_P2	U2	VOUT screw terminal to connect load to output.
J3	VOUT Select	U2	VOUT selection header. Use shunt to set output voltage. See Table 2-1.
J4	ENSYNC_P2	U2	2-pin header to connect U2 buffer output enable to ground. Populate shunt to enable output of buffer. Remove shunt to make buffer output high impedance.
J6	VO_2NDSTG	U2	Output Second Filter.
J7	FSEL Select	U2	FSEL selection header. Use shunt to select FSEL resistor. See Table 2-2.
J8	FSEL Test	U2	Test mode 1-2 use pin strap resistors. 2-3 I2C test mode.
J9	MODE Select	U2	MODE selection header. Use shunt to select MODE resistor. See Table 2-3.
J10	MODE Test	U2	Test mode 1-2 use pin strap resistors. 2-3 I2C test mode.
J14	VOUT_P1	U1	VOUT screw terminal to connect load to output.
J15	EN_OFF_P1	U1	2-pin header for enable. Add shunt to connect EN to ground and disable device.
J16	ENSYNC_P1	U1	2-pin header to connect U4 buffer output enable to ground. Populate shunt to enable output of buffer. Remove shunt to make buffer output high impedance.

Table 3-2. Test Points

REFERENCE DESIGNATOR	NAME	RELATED IC	FUNCTION
TP1	VOUT_P2	U2	VOUT test point. Use this for efficiency, output regulation, and bode plot measurements.
TP2	VIN_P2	U2	VIN test point. Use this for efficiency measurements.
TP3	SW_P2	U2	SW node solder mask opening.
TP4	VDRV_P2	U2	VDRV node test point.
TP5	SW_P2	U2	SW node test point.
TP6	PGOOD_P2	U2	PGOOD test point.
TP7	MSEL_P2	U2	MODE test point.
TP8	AGND_P2	U2	AGND test point.
TP9	PGND_P2	U2	PGND test point.
TP10	VCC_BUF_P2	U2	VDRV Voltage Supply to Buffer.
TP11	GOSNS	U2	Remote Sense for U2.
TP12	FSEL_P2	U2	FSEL test point.
TP13	PGND	U2	Ground near P2 SYNC input.
TP14	BODE-_P2	U2	Test point between voltage divider network and output voltage. Used for Bode plot measurements.
TP15	BODE+__P2	U2	Used for Bode plot measurements.
TP16	PGND_VO2_P2	U2	PGND test point. Use this for efficiency measurements.
TP17	EN__P2	U2	EN test point. If user is applying an external voltage, then the external voltage must be kept below the absolute maximum voltage of the EN pin of 6 V.
TP18	SYNC_P2	U2	SYNC test point. Supply an external clock to this test point to synchronize U1 regulators.
TP19	VO_2NDSTG	U2	SMB connector to measure output voltage after second stage filter if added to EVM. When using this test point, the scope must be set for 1-MΩ termination. When using 50-Ω termination, a 2:1 divider is created.
TP20	VO2_PGND	U2	Ground for second stage filter output.
TP21	ISNS	Both	Test point to measure current in load transient circuit. Gain is 20 A/V.
TP22	FGEN	Both	Test point to connect function generator to load transient circuit. Slowly increase amplitude and vary slew rate of function generator for desired load step.
TP23	ISNS	Both	Test point to measure current in load transient circuit. Gain is 20 A/V.
TP24	SW_P2	U2	SMB connector to measure SW node. When using this test point, the scope must be set for 50-Ω termination. The combination of 50-Ω termination and 450-Ω series resistance creates a 10:1 attenuation.
TP25	VOUT_P2	U2	SMB connector to measure output voltage. When using this test point, the scope must be set for 1-MΩ termination. When using 50-Ω termination, a 2:1 divider is created.
TP26	VO_2NDSTG	U2	Test point to measure output voltage after second stage filter if added to EVM.
TP27	PGND	Both	PGND test point for load transient circuit.
TP29	VOUT_P1	U1	SMB connector to measure output voltage. When using this test point, the scope must be set for 1-MΩ termination. When using 50-Ω termination, a 2:1 divider is created.
TP30	VIN_P1	U1	VIN test point. Use this for efficiency measurements.
TP31	VOUT_P1	U1	VOUT test point. Use this for efficiency, output regulation, and bode plot measurements.
TP32	EN_P1	U1	EN test point. If applying an external voltage, then the external voltage must be kept below the absolute maximum voltage of the EN pin of 6 V.
TP33	PGND_P1	U1	PGND test point.
TP34	PGOOD_P1	U1	PGOOD test point.
TP35	AGND_P1	U1	AGND test point.
TP36	PGND_P1	U1	PGND test point. Use this for efficiency measurements.
TP37	VO_SNS	U1	Used for Bode plot measurements.
TP38	BODE-_P1	U1	Test point between voltage divider network and output voltage. Used for Bode plot measurements.
TP39	VCC_BUF_P1	U1	VDRV Voltage Supply to Buffer.
TP40	PGND_P1	U1	PGND test point.
TP41	SYNC_P1	U1	SYNC test point. Supply an external clock to this test point to synchronize U4 regulators.

3.2 Efficiency

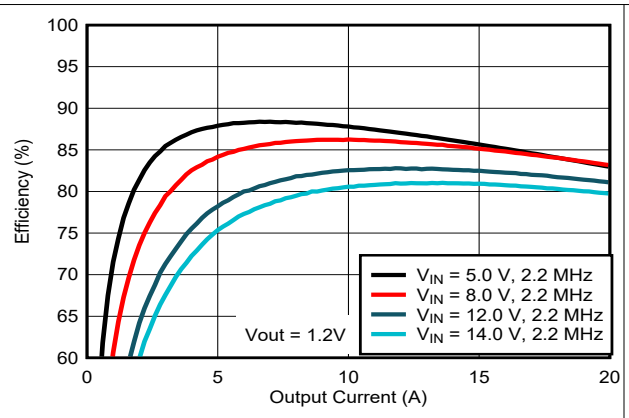
Figure 3-1 and Figure 3-2 show the efficiency for both designs on the TPS543B22EVM. The test points listed in Table 3-3 are used for the efficiency measurement. Use these test points to minimize the contribution of PCB parasitic power loss to the measured power loss.

Some additional test setup considerations to minimize external sources of power dissipation are listed below.

- Disable the other regulator to avoid including the switching quiescent current of the other regulator in the efficiency measurement.
- Do not measure the SW pin of P2 with TP24 while measuring the efficiency of P2. Measuring the SW pin with this test point loads this node with 500 Ω and the efficiency measurement includes the power lost in this external resistance.
- Remove the shunt from J8 to use default start voltage for P2.

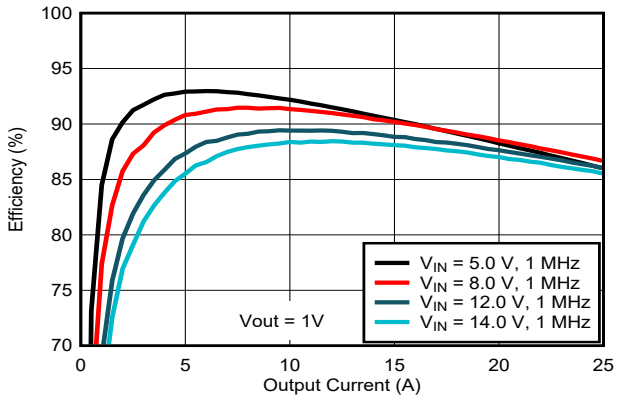
Table 3-3. Efficiency Measurement Test Points

RELATED IC	TEST POINT NAME	REFERENCE DESIGNATOR	FUNCTION
U1	VIN_P1	TP30	Input voltage test point connected near pins of P1
	VOUT_P1	TP31	Output voltage test point near output inductor of P1
	PGND_EFF_P1	TP36, TP33	PGND reference test point for both input and output voltages Kelvin connected near P1
U2	VIN_P2	TP2	Input voltage test point connected near pins of P2
	VOUT_P2	TP1	Output voltage test point near output inductor of P2
	PGND_EFF_P2	TP9,TP16	PGND reference test point for both input and output voltages Kelvin connected near P2



V_{OUT} = 1.2V f_{SW} = 2200 kHz

Figure 3-1. P1 Efficiency



V_{OUT} = 1 V f_{SW} = 1000 kHz

Figure 3-2. P2 Efficiency – Default Configuration

3.3 Output Voltage Regulation

Figure 3-3 and Figure 3-4 show the load and line regulation for U1. Figure 3-5 and Figure 3-6 show the load and line regulation for U2.

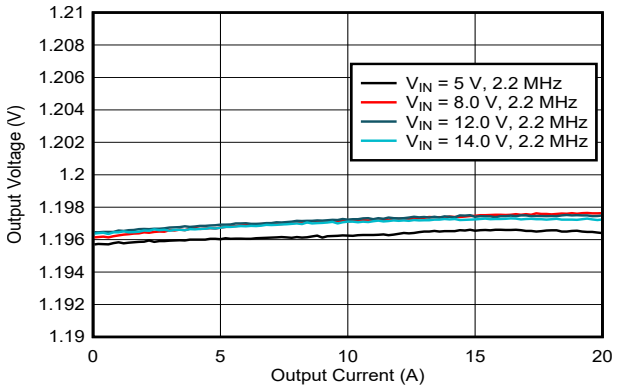


Figure 3-3. U1 Load Regulation

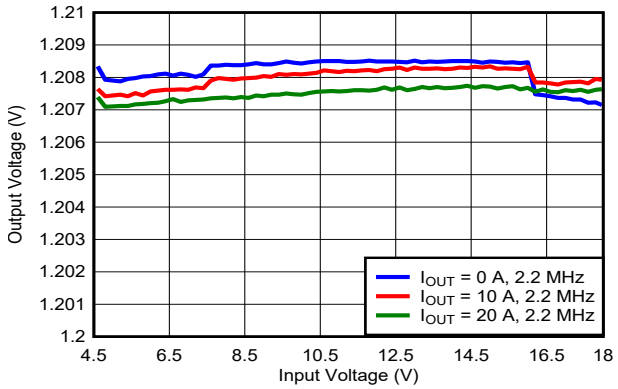


Figure 3-4. U1 Line Regulation

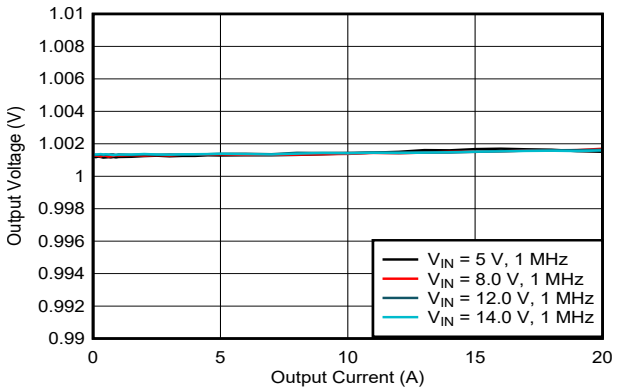


Figure 3-5. U2 Load Regulation

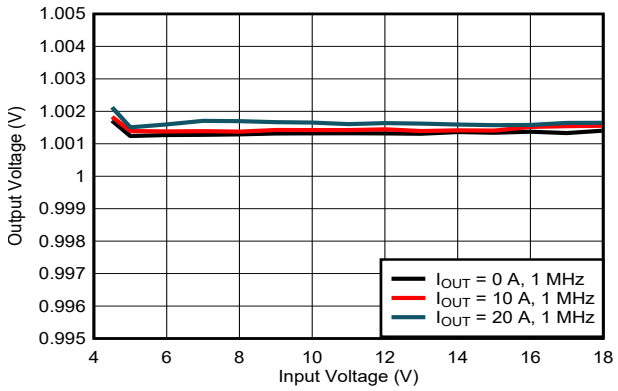


Figure 3-6. U2 Line Regulation

3.4 Load Transient and Loop Response

Figure 3-7 and Figure 3-8 show the response to load transients for both designs. The current step is from 0-A to 10-A and the current step slew rate is 1 A/µs. An electronic load is used to provide a DC 0-A load and the load transient circuit on the EVM is used to provide a 10-A step. The VOUT voltage is measured using TP10 for U1 and TP29 for U2.

When using the load transient circuit included on the TPS543B22EVM, slowly increase amplitude of function generator for desired load step amplitude then vary the rise and fall times for the desired slew rate. The current for the load step can be sensed with the ISNS test point. The default resistors on the EVM provide a gain of 66.66 A/V. With this gain, a 10-A step results in 150-mV at the ISNS test point.

Note

To use the load transient circuit with U1, move R27 to R28.

Figure 3-9 and Figure 3-10 show the loop characteristics for both designs. Gain and phase plots are shown for V_{IN} voltage of 12 V and a 20-A load.

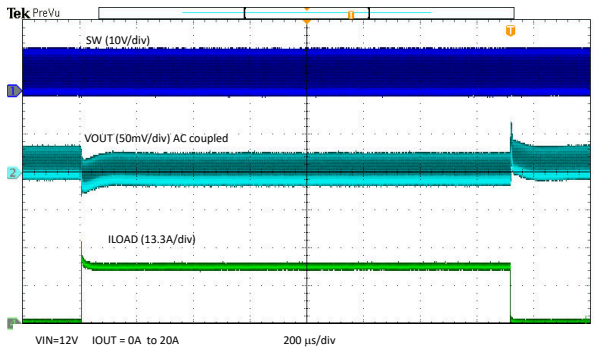


Figure 3-7. U1 Transient Response

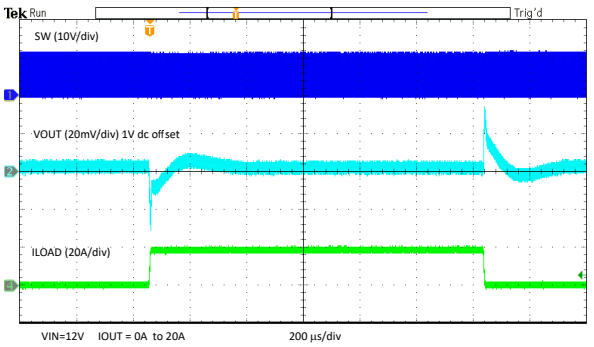


Figure 3-8. U2 Transient Response

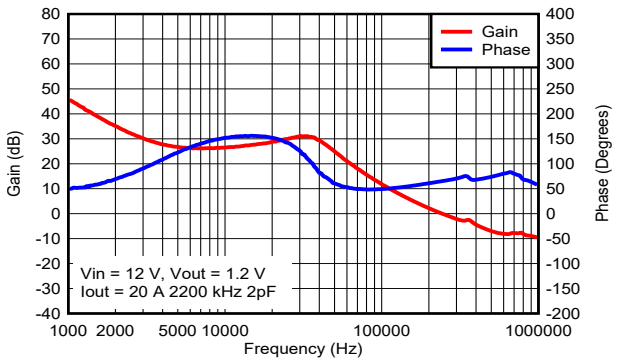


Figure 3-9. U1 Bode Plot

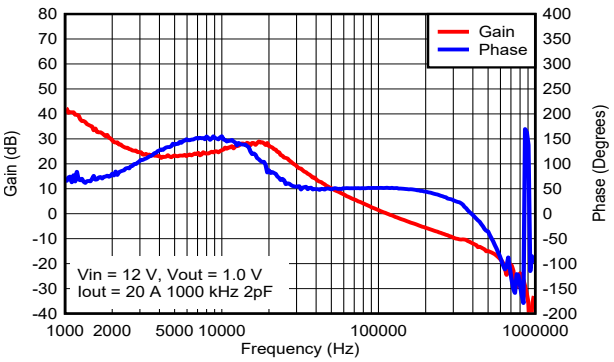


Figure 3-10. U2 Bode Plot

3.5 Output Voltage Ripple

Figure 3-11 through U2 Output Ripple - 20A show the TPS543B22EVM output voltage ripple. The load currents are no load and 20 A. V_{IN} = 12 V. The VOUT voltage is measured using TP29 for U1 and TP25 for U2.

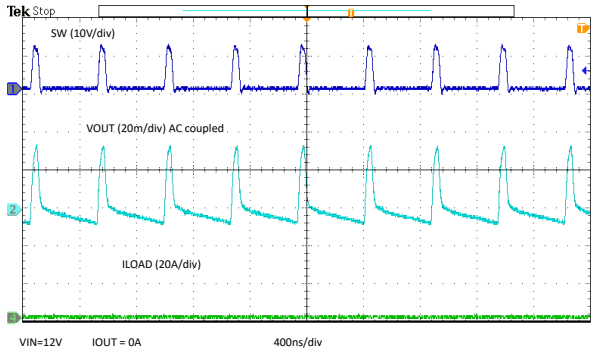


Figure 3-11. U1 Output Ripple – No Load

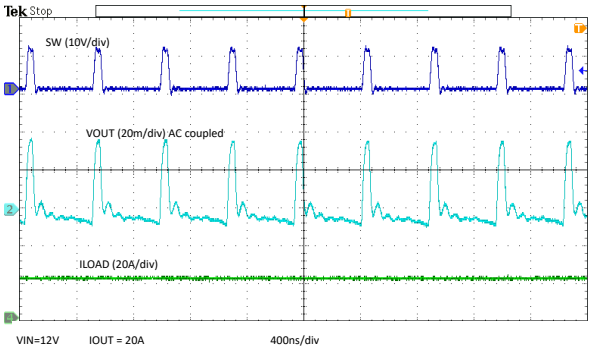


Figure 3-12. U1 Output Ripple – 20 A Load

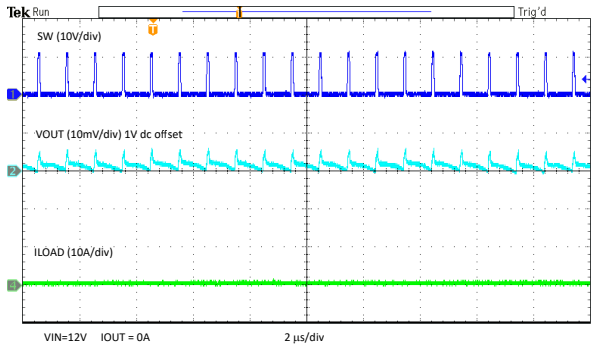


Figure 3-13. U2 Output Ripple – No Load

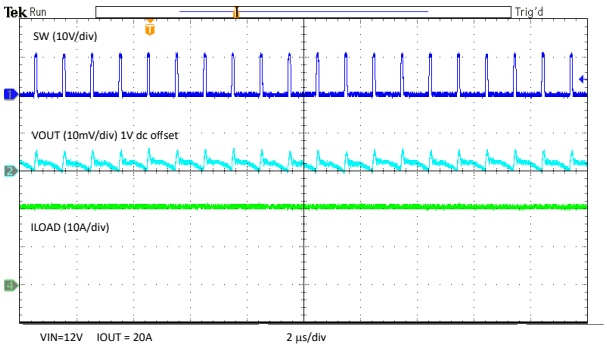


Figure 3-14. U2 Output Ripple – 20 A Load

3.6 Input Voltage Ripple

Figure 3-15 through U2 Input Ripple - 20 A Load show the TPS543B22EVM input voltage ripple. The load currents are no load and 20 A. V_{IN} = 12 V. The ripple voltage is measured across C40 for U1 and measured across C13 for U2.

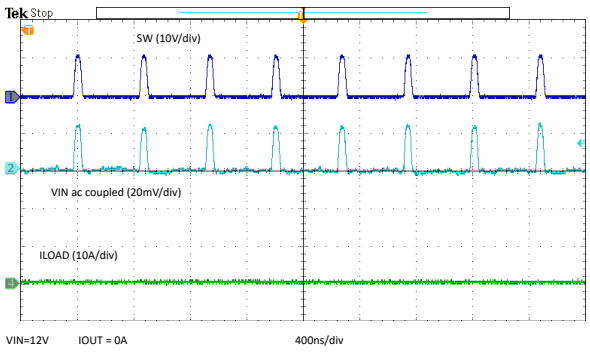


Figure 3-15. U1 Input Ripple – No Load

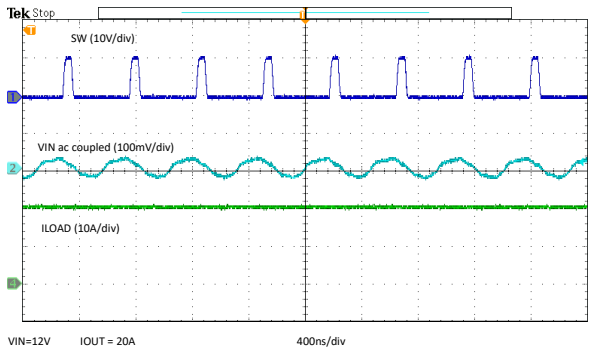


Figure 3-16. U1 Input Ripple – 20 A Load

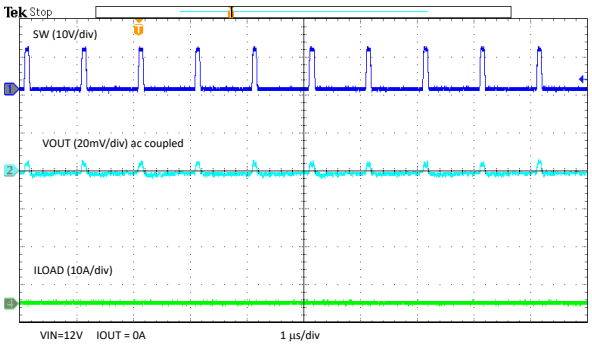


Figure 3-17. U2 Input Ripple – No Load

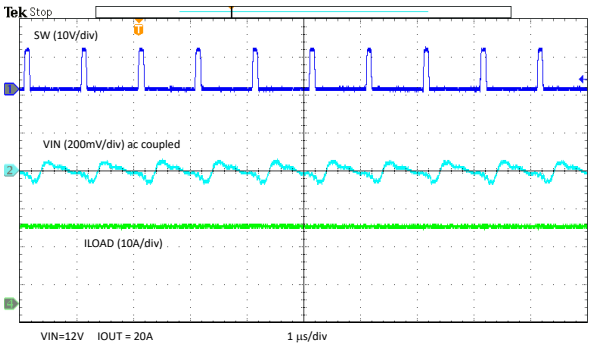


Figure 3-18. U2 Input Ripple – 20 A Load

3.7 Synchronizing to a Clock

Figure 3-19 shows U1 and U2 synchronized to an external clock of 1.25 MHz at the SYNC test point. To synchronize to the clock at the SYNC test point, place a shunt on the ENSYNC_U1 or ENSYNC_U2 jumper or jumpers to enable the output of the buffers.

Figure 3-20 shows the transitions to and from synchronizing to an external clock with 20-A load. 16 pulses with a frequency of 1-MHz were sent to the SYNC testpoint on the EVM. In this waveform, after four pulses, the TPS543B22 begins synchronizing to the clock. After the clock goes away, the TPS543B22 switches at 70% of the internal clock frequency for four pulses then transitions back to the normal internal clock frequency. There is only a small variation in the output voltage during these transitions.

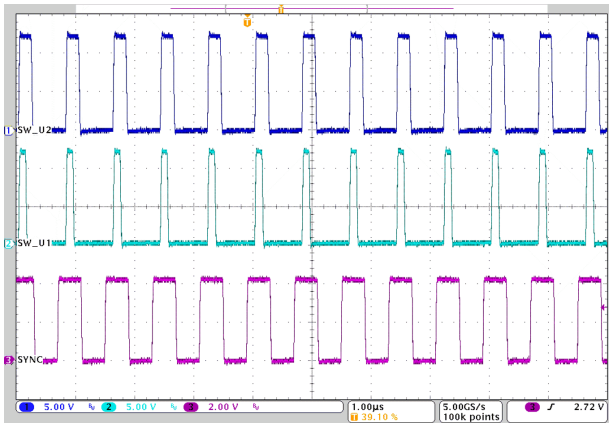


Figure 3-19. U1 and U2 Synchronized to a Clock

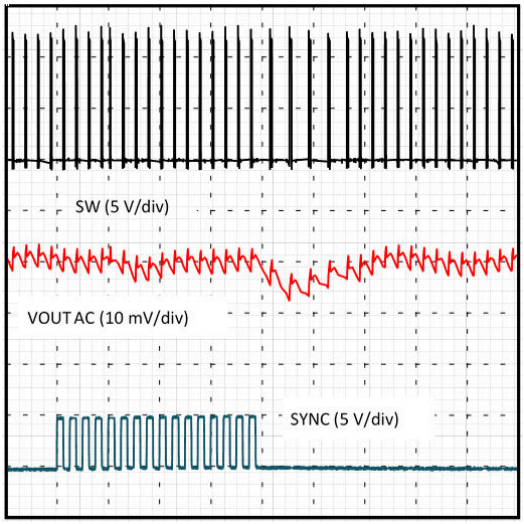


Figure 3-20. U2 Clock Synchronization Transitions

3.8 Start-up and Shutdown with EN

Figure 3-21 and Figure 3-22 show the start-up and shutdown waveforms for U2 with EN. In Figure 3-21, the input voltage is initially applied and the output is inhibited by pulling EN to GND using an external function generator. When the EN voltage is increased above the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value. In Figure 3-22, the external function generator pulls EN to ground and the TPS543B22 shuts down.

Figure 3-23 shows the VDRV internal LDO start-up relative to the EN pin.

A shunt on the ENOFF_U1 jumper or RDIV_VIN can be used to test the EN start-up of U1 and U2, respectively. When the shunt is removed from ENOFF_U1, EN is released and the start-up sequence begins for U1. When the shunt is placed on RDIV_VIN, EN is pulled to the input voltage through the resistor divider and the start-up sequence begins for U2.

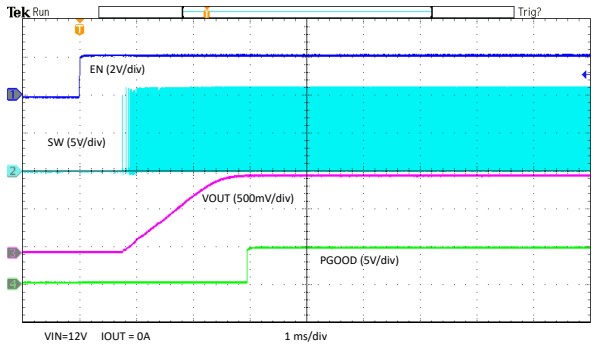


Figure 3-21. U2 Start-up with EN – No Load

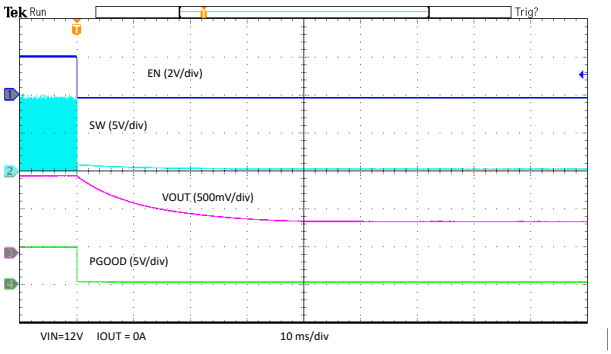


Figure 3-22. U2 Shutdown with EN – No Load

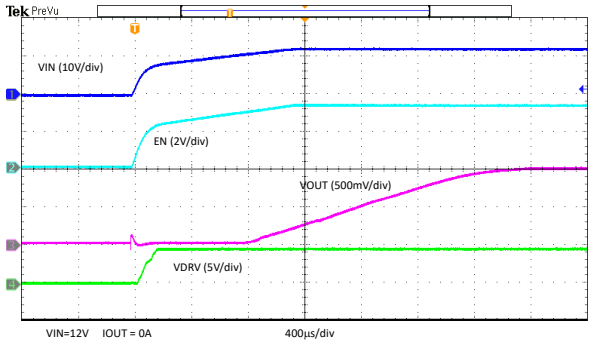


Figure 3-23. U2 Startup with EN – No Load and Measuring VDRV

3.9 Start-up and Shutdown with VIN

U2 Start-Up with VIN and U2 Shutdown with VIN show the start-up and shutdown waveforms for U2 with VIN. In U2 Start-Up with VIN, the VIN voltage ramps up and output voltage ramps up after the input and EN pin voltages reach their respective UVLO threshold. In U2 Shutdown with VIN, the VIN voltage ramps down and the TPS543B22 shuts down when the input or EN pin voltage reach their respective UVLO threshold. The rate at which VIN ramps down changes as soon as the TPS543B22 is disabled because the device is no longer loading the input supply.

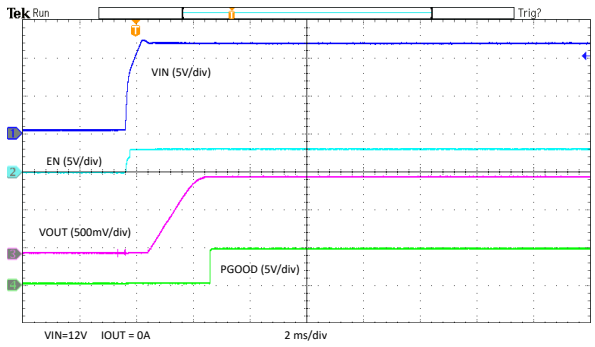


Figure 3-24. U2 Start-up with VIN

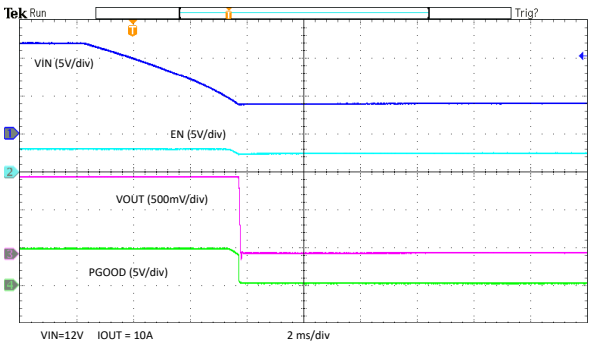


Figure 3-25. U2 Shutdown with VIN

3.10 Start-up Into Pre-Bias

Figure 3-26 shows the EN start-up of U2 into a pre-biased output. The output voltage is pre-biased by toggling the EN pin low then high at a rate such that the output voltage does not fully discharge before EN goes high again.

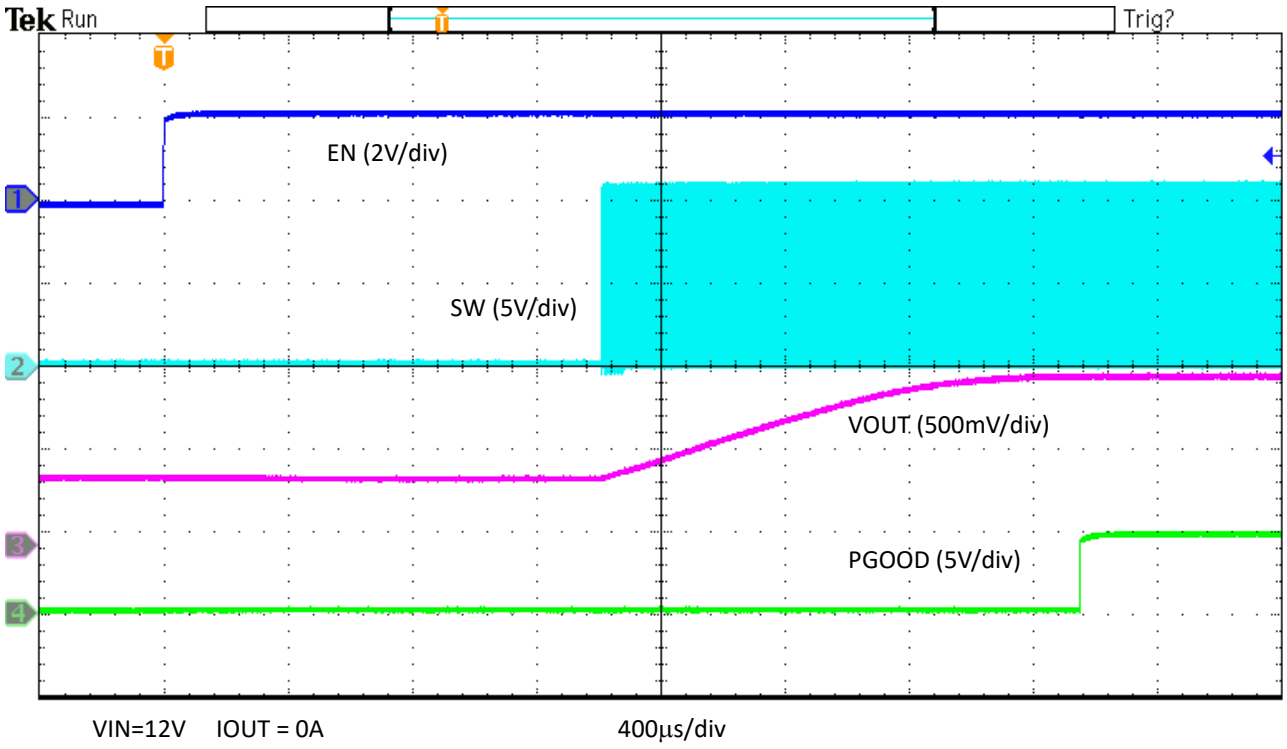


Figure 3-26. U2 Start-up Into 0.5-V Pre-Bias

3.11 Hiccup Current Limit

These waveforms show the TPS543B22 entering hiccup with an overload. The TPS543B22 tries to restart after the Hiccup wait time period but the overload was still present on the output.

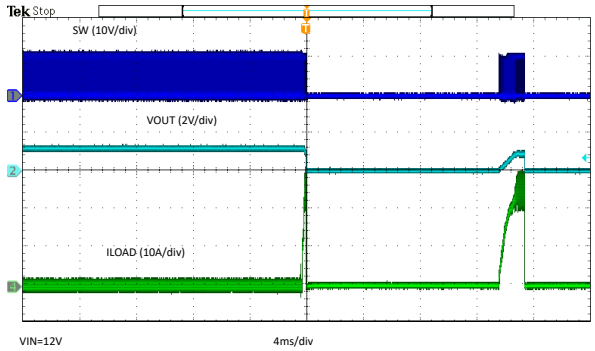


Figure 3-27. U1 Output Overcurrent Protection – Overload

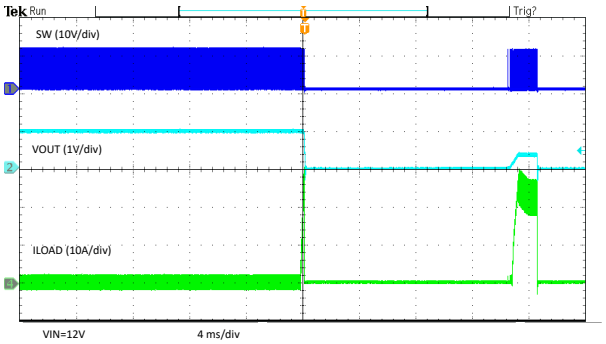


Figure 3-28. U2 Output Overcurrent Protection – Overload

3.12 Thermal Performance

Figure 3-29 through Figure 3-32 show the temperature rise of the TPS543B22 ICs at full 20-A load. Figure 3-29 and Figure 3-30 have only one TPS543B22 on and loaded. Figure 3-31 and Figure 3-32 have both TPS543B22s loaded. A minimum of a 10 minute soak time was used before taking each measurement.

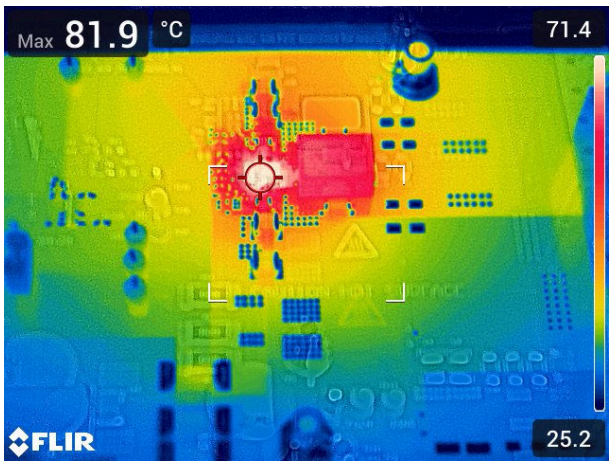


Figure 3-29. U1 Thermal Performance – 20-A Load and U2 Off

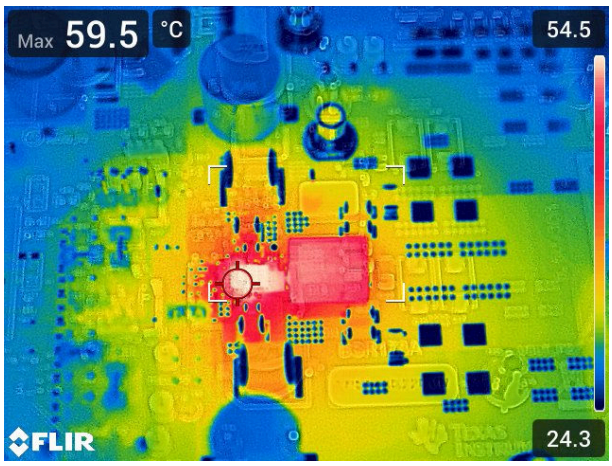


Figure 3-30. U2 Thermal Performance – 20-A Load and U1 Off

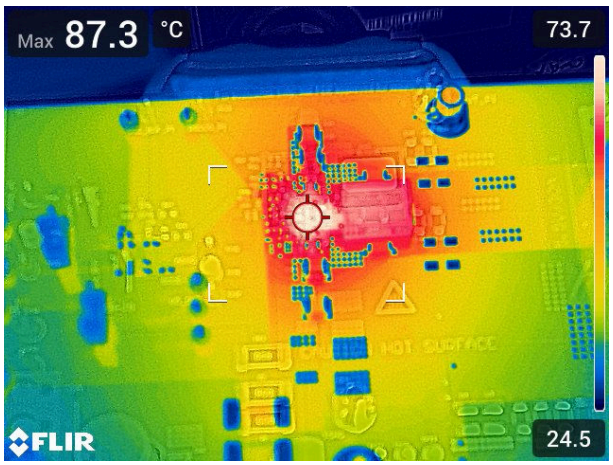


Figure 3-31. U1 Thermal Performance – Both 20-A Load

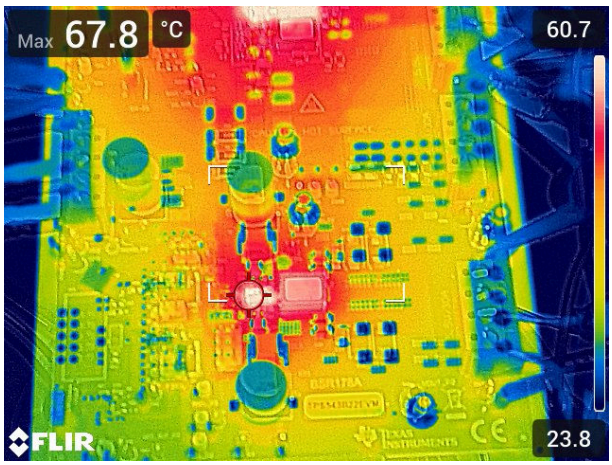


Figure 3-32. U2 Thermal Performance – Both 20-A Load

4 Board Layout

This section provides a description of the TPS543B22EVM board layout and layer illustrations.

4.1 Layout

The board layout for the TPS543B22EVM is shown in Figure 4-1 through Figure 4-12. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper. The small size U1 circuit takes up an area of only approximately 275 mm^2 as shown on the silkscreen.

All of the required components for the TPS543B22 are placed on the top layer for U1. The input decoupling capacitors, VDRV capacitor, VCC capacitor, and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage set point resistor divider components are kept close to the IC. An additional input bulk capacitor is used near the input terminal to limit the noise entering the converter from the supply used to power the board. Critical analog circuits such as the voltage set point divider, EN resistor, MODE resistor, and FSEL resistor are kept close to the IC and terminated to the quiet analog ground (AGND) island on the top layer.

The top layer contains the main power traces for VIN, VOUT, and SW. The top layer power traces are connected to the planes on other layers of the board with multiple vias placed around the board. There are multiple vias near the PGND pins of the IC to help maximize the thermal performance. Each TPS543B22 circuit has their own dedicated ground are for quiet analog ground that is connected to the main power ground plane at a single point. This single point connection is done on the internal ground planes. Lastly the voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} area on the top layer.

The mid layer 1 is a large ground plane and an analog ground island for the MSEL and FSEL resistor and VCC capacitor to connect to by vias. minimize cuts in the ground plane. The U1 V_{OUT} has a large copper pour for carrying the output current. The input bus for the 2nd filter connects on the mid layer 1 from the V_{OUT} of U2 to the 2nd stage filter using vias.

The mid layer 2 has VIN copper area beneath each IC to connect the VIN pins together with a low impedance connection. Lastly, the remaining area of this layer is filled in with PGND and additional copper plane for the 2nd stage filter. The mid layer 3 and mid layer 4 is mostly a power ground plane with minimal trace and cuts.

The bottom layer is primarily used for another ground plane. This layer also has an additional VOUT copper area for the U2 circuit. Lastly, the load transient circuit is placed on this side of the EVM.

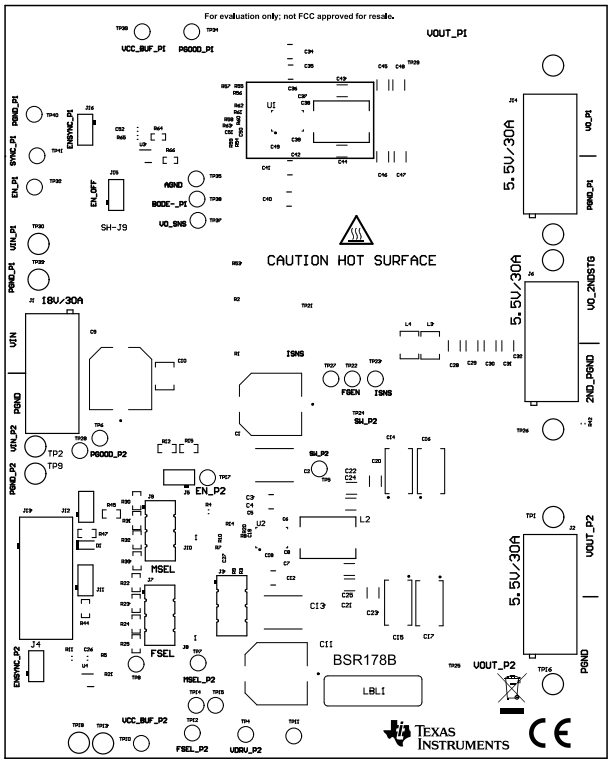


Figure 4-1. Top Overlay

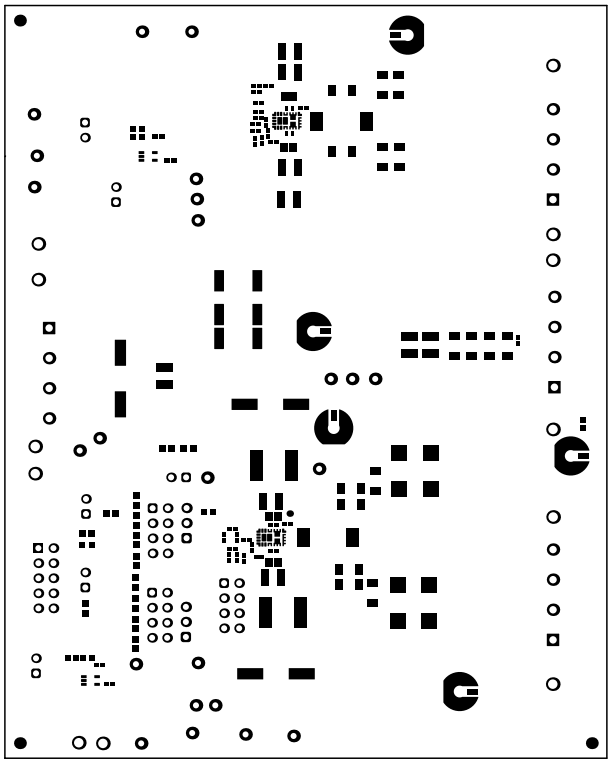


Figure 4-2. Top Solder

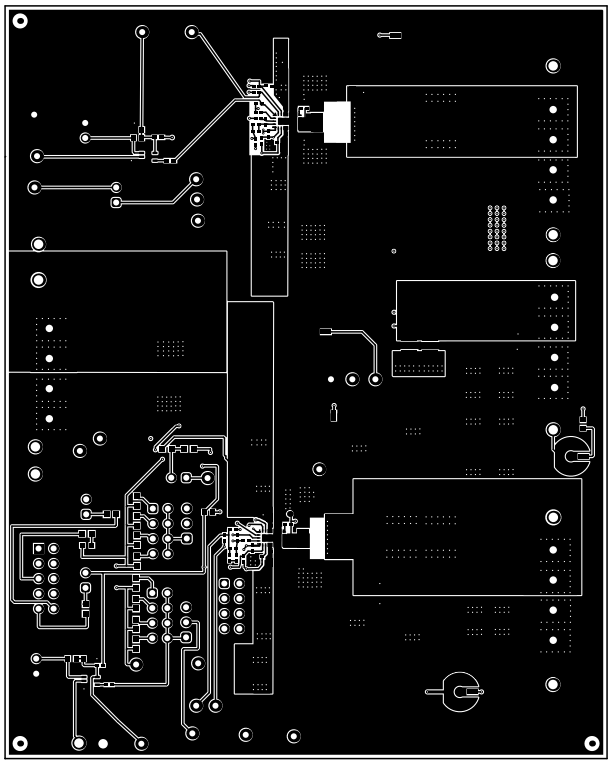


Figure 4-3. Top Layer

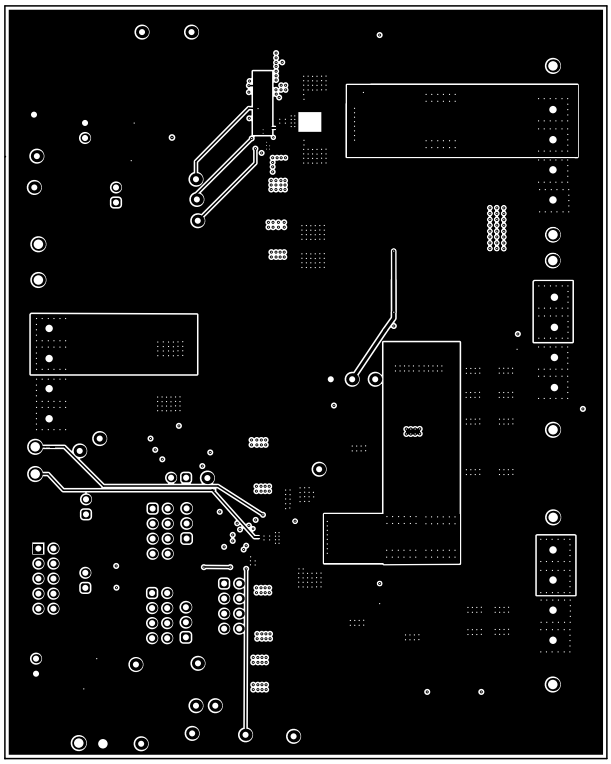


Figure 4-4. Signal 1

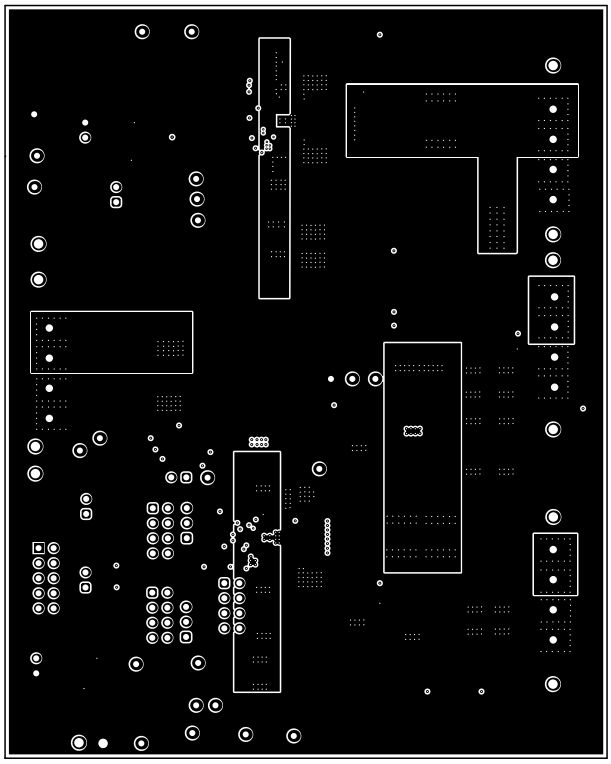


Figure 4-5. Signal 2

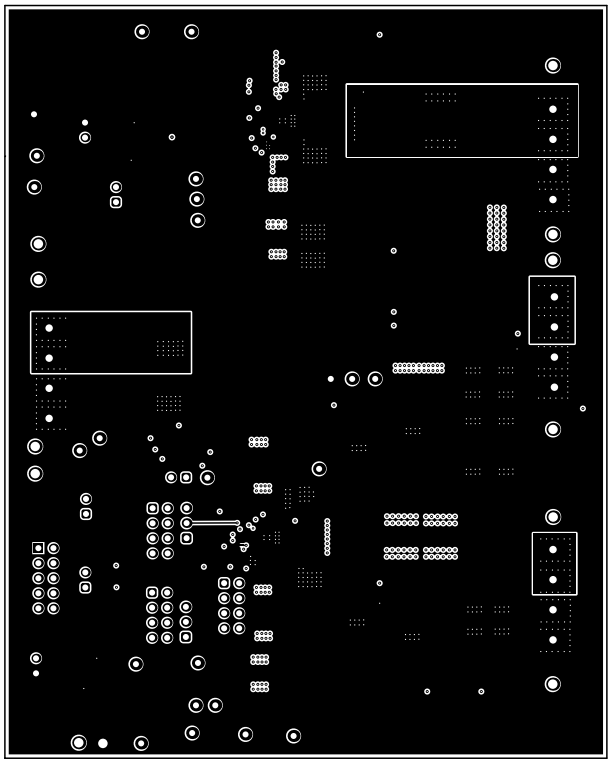


Figure 4-6. Signal 3

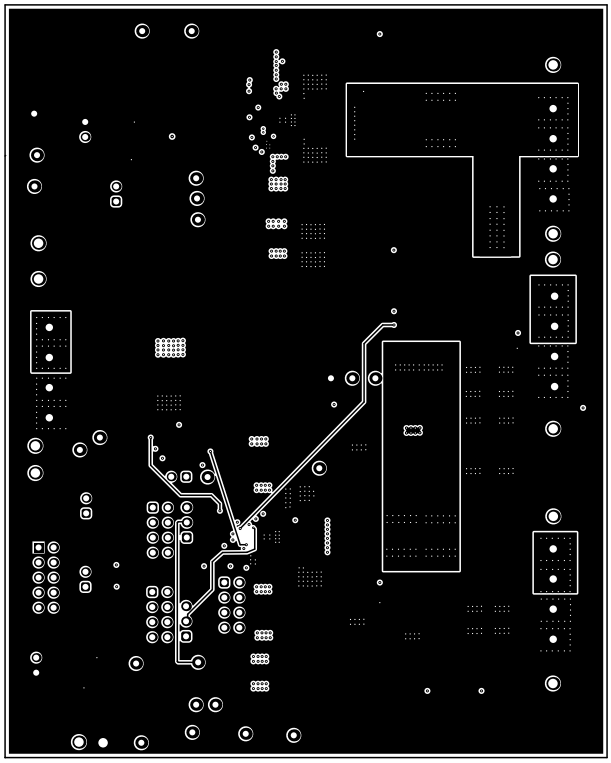


Figure 4-7. Signal 4

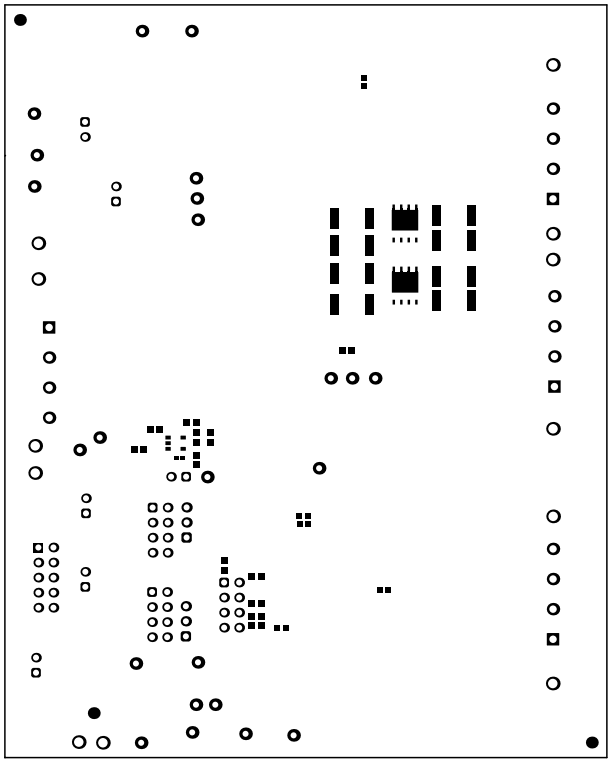


Figure 4-8. Bottom Solder

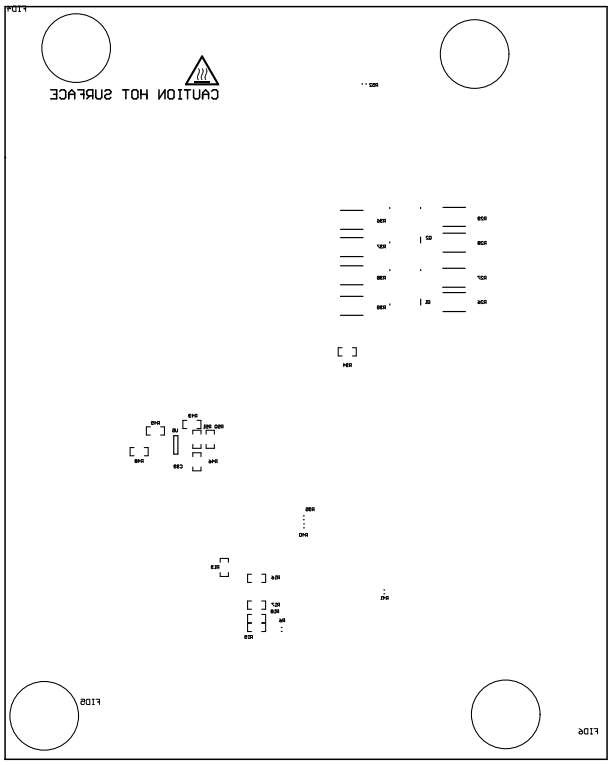


Figure 4-9. Bottom Overlay

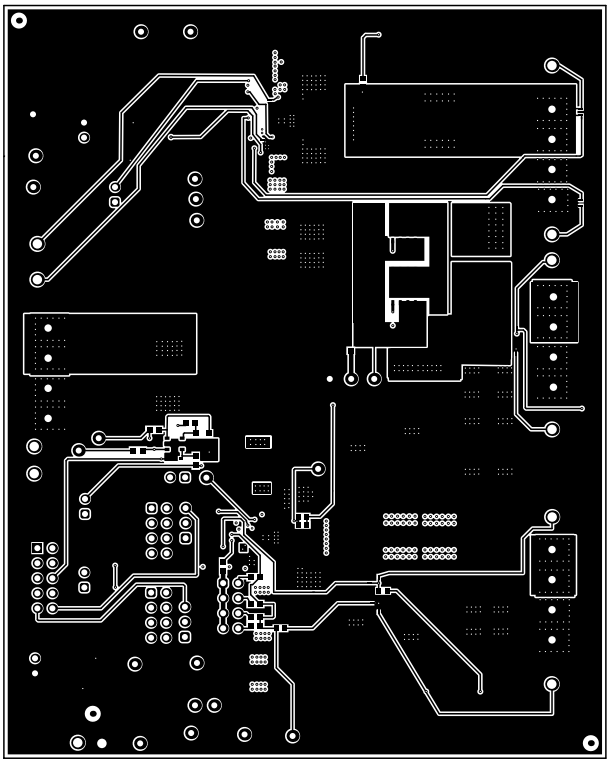


Figure 4-10. Bottom Layer

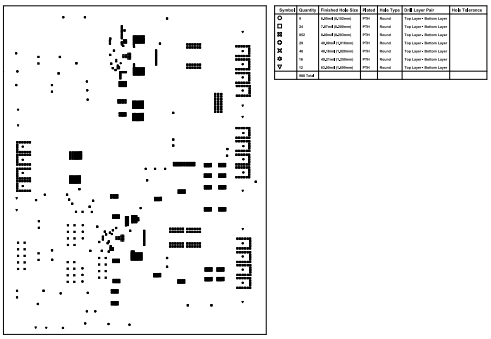


Figure 4-11. Drill Drawing

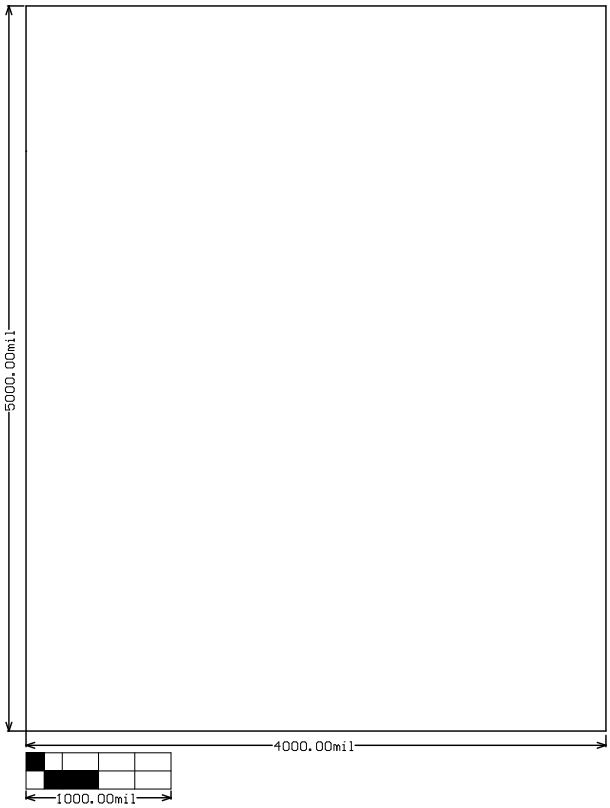


Figure 4-12. Board Dimensions

5 Schematic and Bill of Materials

This section presents the TPS543B22EVM schematic and bill of materials.

5.1 Schematic

Figure 5-1 is the schematic for U1. Figure 5-2 is the schematic for U2.

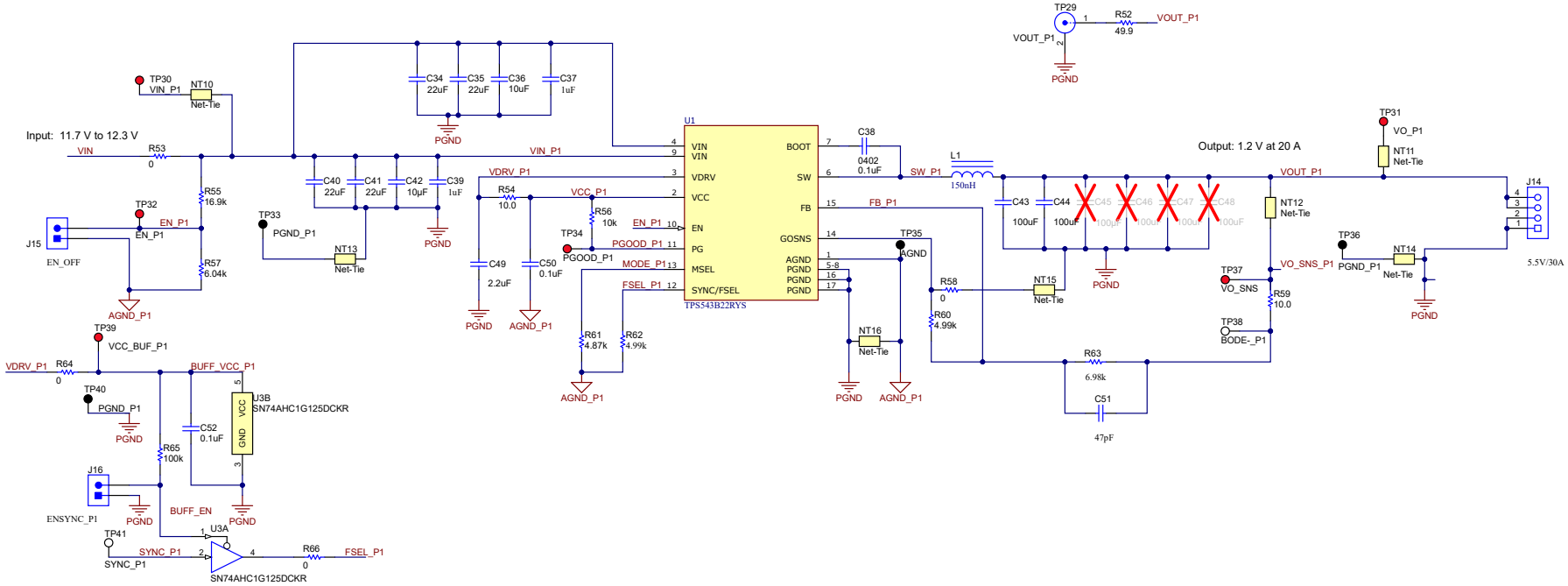


Figure 5-1. U1 schematic

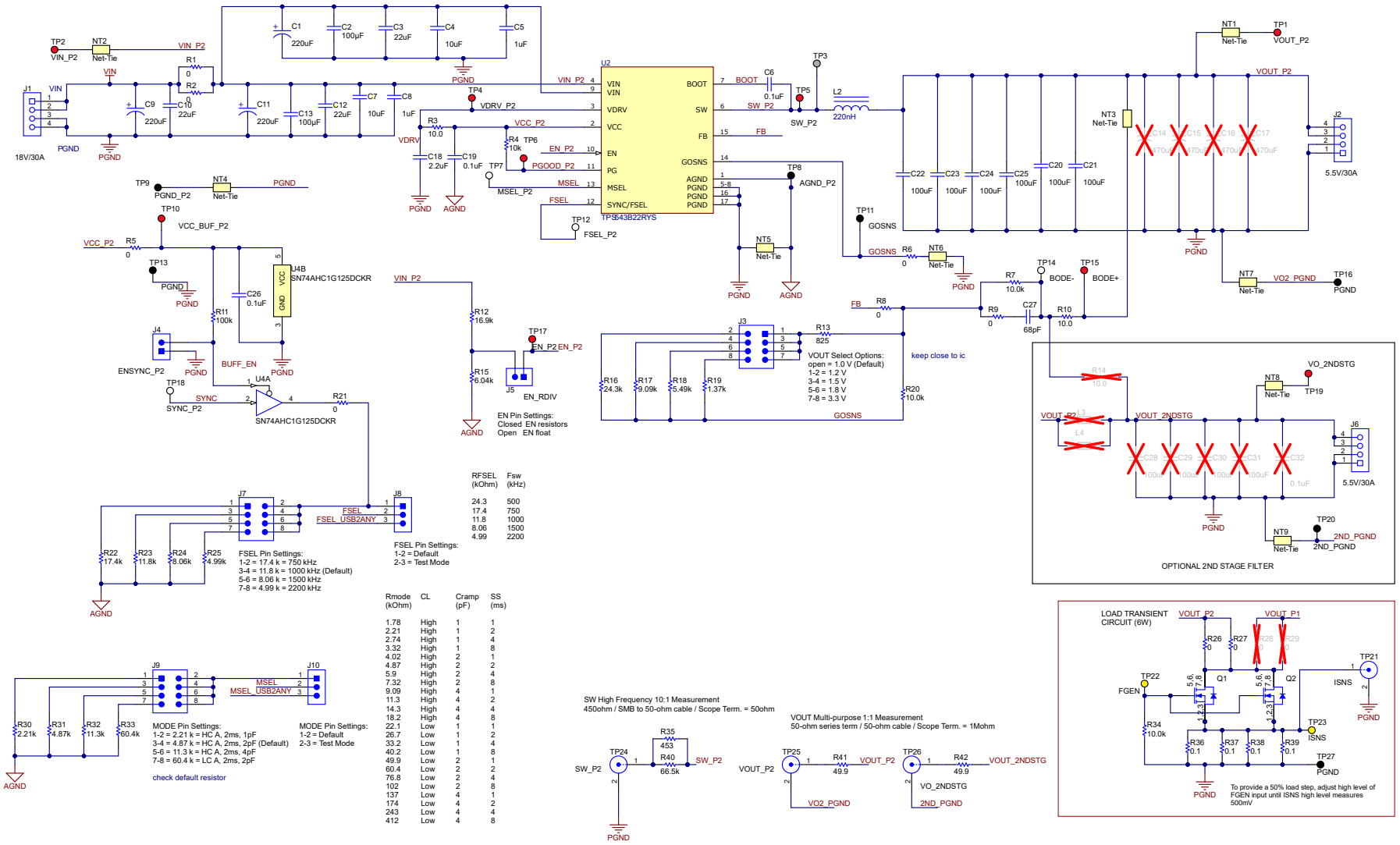


Figure 5-2. U2 schematic

5.2 Bill of Materials

Table 5-1 presents the bill of materials for the TPS543B22EVM.

Table 5-1. TPS543B22EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		BSR178	Any
C1, C9, C11	3	220 µF	220 µF 35 V Aluminum - Polymer Capacitors Radial, Can - SMD 22mOhm 2000 Hrs @ 105°C	SMT_ECAP_10MM3_10MM3	8.75076E+11	Wurth Electronics
C2, C13	2	100uF	CAP, CERM, 100 µF, 25 V,+/- 20%, X7R, 6x5x5mm	6x5x5mm	CKG57NX7R1E107M500JH	TDK
C3, C10, C12, C34, C35, C40, C41	7	22uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X7R, 1210	1210	GRM32ER71E226KE15L	MuRata
C4, C7	2	10uF	CAP, CERM, 10 uF, 25 V, +/- 20%, X7S, 0805	805	GRM21BC71E106ME11L	MuRata
C5, C8, C37, C39	4	1uF	CAP, CERM, 1 uF, 35 V, +/- 10%, X5R, 0402	402	C1005X5R1V105K050BC	TDK
C6, C19, C38, C50	4	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	402	C1005X7R1H104K050BB	TDK
C18, C49	2	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X5R, 0402	402	C1005X5R1A225K050BC	TDK
C20, C21, C22, C23, C24, C25	6	100uF	CAP, CERM, 100 uF, 6.3 V,+/- 20%, X5R, 1206	1206	C3216X5R0J107M160AB	TDK
C26, C52	2	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet
C27	1	68 pF	CAP, CERM, 68 pF, 50 V, +/- 5%, C0G/NP0, 0402	402	GRM1555C1H680JA01D	MuRata
C36, C42	2	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7S, 0805	805	GRM21BC71E106KE11L	MuRata
C43, C44	2	100uF	CAP, CERM, 100 uF, 10 V, +/- 20%, X5R, 1206_190	1206_190	C3216X5R1A107M160AC	TDK
C51	1	47 pF	CAP, CERM, 47 pF, 50 V, +/- 1%, C0G/NP0, 0402	402	GRM1555C1H470FA01D	MuRata
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J6, J14	4		Terminal Block, 5.08 mm, 4x1, Brass, TH	4x1 5.08 mm Terminal Block	ED120/4DS	On-Shore Technology
J3, J7, J9	3		Header, 2.54mm, 4x2, Gold, TH	Header, 2.54mm, 4x2, TH	TSW-104-08-L-D	Samtec
J4, J5, J15, J16	4		Header, 2.54mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	TSW-102-08-G-S	Samtec
J8, J10	2		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
L1	1	150nH	Inductor, Shielded, Ferrite, 150 nH, 51 A, 0.00039 ohm, SMD	10.2x7mm	SLR1050A-151KEC	Coilcraft
L2	1	220nH	Inductor, Shielded, Ferrite, 220 nH, 35 A, 0.0004 ohm, SMD	10.2x7mm	SLR1050A-221KEB	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
Q1, Q2	2	30 V	MOSFET, N-CH, 30 V, 25 A, DQJ0008A (VSONP-8)	DQJ0008A	CSD17579Q5A	Texas Instruments
R1, R2, R53	3	0	RES, 0, 0%, 1 W, AEC-Q200 Grade 0, Body 6.3x3.2mm	Body 6.3x3.2mm	RMCF2512ZT0R00	Stackpole Electronics Inc
R3, R10	2	10	RES, 10.0, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW040210R0FKED	Vishay-Dale
R4	1	10k	RES, 10 k, 5%, 0.1 W, 0603	603	RC0603JR-0710KL	Yageo
R5, R21, R64, R66	4	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04020000Z0ED	Vishay-Dale
R6	1	0	RES, 0, 5%, 0.1 W, 0603	603	RC0603JR-070RL	Yageo
R7, R20	2	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	402	RC0402FR-0710KL	Yageo America
R8, R9, R58	3	0	RES, 0, 5%, 0.063 W, 0402	402	RC0402JR-070RL	Yageo America
R11, R65	2	100k	RES, 100 k, 5%, 0.1 W, 0603	603	CRCW0603100KJNEAC	Vishay-Dale
R12	1	16.9k	RES, 16.9 k, 1%, 0.1 W, 0603	603	RC0603FR-0716K9L	Yageo
R13	1	825	RES, 825, 1%, 0.1 W, 0603	603	RC0603FR-07825RL	Yageo
R15	1	6.04k	RES, 6.04 k, 1%, 0.1 W, 0603	603	RC0603FR-076K04L	Yageo
R16	1	24.3k	RES, 24.3 k, 1%, 0.1 W, 0603	603	RC0603FR-0724K3L	Yageo
R17	1	9.09k	RES, 9.09 k, 1%, 0.1 W, 0603	603	RC0603FR-079K09L	Yageo
R18	1	5.49k	RES, 5.49 k, 1%, 0.1 W, 0603	603	RC0603FR-075K49L	Yageo

Table 5-1. TPS543B22EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R19	1	1.37k	RES, 1.37 k, 1%, 0.1 W, 0603	603	RC0603FR-071K37L	Yageo
R22	1	17.4k	RES, 17.4 k, 1%, 0.1 W, 0603	603	RC0603FR-0717K4L	Yageo
R23	1	11.8k	RES, 11.8 k, 1%, 0.1 W, 0603	603	RC0603FR-0711K8L	Yageo
R24	1	8.06k	RES, 8.06 k, 1%, 0.1 W, 0603	603	RC0603FR-078K06L	Yageo
R25	1	4.99k	RES, 4.99 k, 1%, 0.1 W, 0603	603	RC0603FR-074K99L	Yageo
R26, R27	2	0	RES, 0, 5%, 1 W, AEC-Q200 Grade 0, 2512	2512	CRCW25120000Z0EG	Vishay-Dale
R30	1	2.21k	RES, 2.21 k, 1%, 0.1 W, 0603	603	RC0603FR-072K21L	Yageo
R31	1	4.87k	RES, 4.87 k, 1%, 0.1 W, 0603	603	RC0603FR-074K87L	Yageo
R32	1	11.3k	RES, 11.3 k, 1%, 0.1 W, 0603	603	RC0603FR-0711K3L	Yageo
R33	1	60.4k	RES, 60.4 k, 1%, 0.1 W, 0603	603	RC0603FR-0760K4L	Yageo
R34	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	603	ERJ-3EKF1002V	Panasonic
R35	1	453	RES, 453, 1%, 0.1 W, 0603	603	RC0603FR-07453RL	Yageo
R36, R37, R38, R39	4	0.1	RES, 0.1, 1%, 3 W, 2512	2512	CRA2512-FZ-R100ELF	Bourns
R40	1	66.5k	RES, 66.5 k, 1%, 0.1 W, 0603	603	RC0603FR-0766K5L	Yageo
R41, R42, R52	3	49.9	RES, 49.9, 1%, 0.1 W, 0603	603	RC0603FR-0749R9L	Yageo
R54, R59	2	10	RES, 10.0, 1%, 0.063 W, 0402	402	CRCW040210R0FKED	Vishay-Dale
R55	1	16.9k	RES, 16.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW040216K9FKED	Vishay-Dale
R56	1	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	402	ERJ-2GEJ103X	Panasonic
R57	1	6.04k	RES, 6.04 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04026K04FKED	Vishay-Dale
R60	1	4.99k	RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	402	ERJ-2RKF4991X	Panasonic
R61	1	4.87k	RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04024K87FKED	Vishay-Dale
R62	1	4.99k	RES, 4.99 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04024K99FKED	Vishay-Dale
R63	1	6.98k	RES, 6.98 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04026K98FKED	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9	9	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP19, TP30, TP31	5		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP4, TP5, TP6, TP10, TP15, TP17, TP32, TP34, TP37, TP39	10		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP7, TP12, TP14, TP38, TP41	5		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
TP8, TP11, TP27, TP35, TP40	5		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP9, TP13, TP16, TP20, TP33, TP36	6		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
TP18	1		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone
TP21, TP24, TP25, TP26, TP29	5		Connector, Receptacle, 50 ohm, TH	SMB Connector	SMBR004D00	JAE Electronics
TP22, TP23	2		Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
U1, U2	2		Synchronous Buck Converter, 4-18V VIN, Adjustable, 0.5-7 V 20 A, VQFN-FCRLF14	VQFN-FCRLF17	TPS543B22RYS	Texas Instruments
U3, U4	2		Single Bus Buffer Gate with 3-State Output, DCK0005A, LARGE T&R	DCK0005A	SN74AHC1G125DCKR	Texas Instruments

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2022) to Revision B (September 2023)	Page
• Added performance charts	7
• Changed Layout figures	21
• Changed schematic figures	25
• Changed *Bill of Materials* table	27

Changes from Revision * (September 2022) to Revision A (January 2023)	Page
• First public release	1

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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