Application Report
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USB Charger Solution Using the TPS40210 SEPIC Converter

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ABSTRACT

This application note discusses a dc-dc single-nded, primary inductance converter (SEPIC) solution for a Universal Serial Bus (USB) charger based on the TPS40210, a 4.5-V to 52-V input current-mode boost controller. This controller is especially optimal for the additional current loop to limit the input and output current. With this loop, the maximum current can be limited to meet the USB loading specifications. This application note also provides a practical design.

1 Introduction

Generally speaking, present portable charger design trends feature a USB power supply as well as an offline ac/dc adapter. Figure 1 shows a typical SEPIC topology for a buck-boost converter with a USB charger.

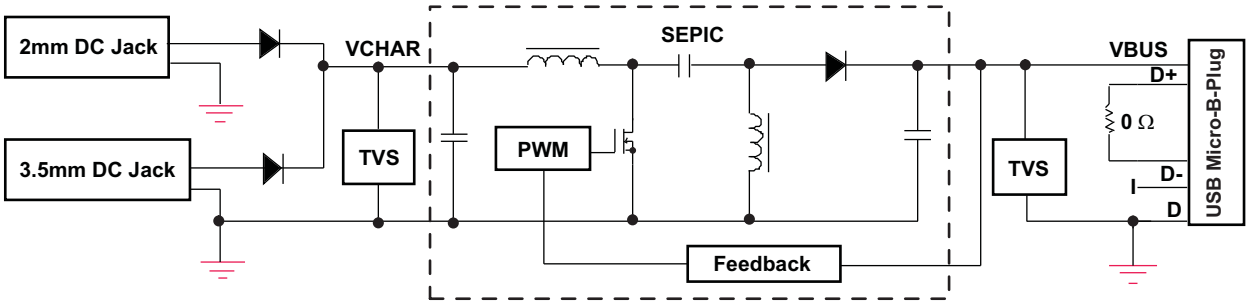

Figure 1. SEPIC Topology for a Buck-Boost Converter with USB Charger

With a common protocol, the cable output (or the USB charger output) could be as high as 9.3 V and as low as 0 V. Consequently, the cable must be able to withstand any voltage within this range. Furthermore, the cable input must be able to survive a 16-V_{DC} input voltage overshoot. The minimum cable output is 300 mA at 5.54-V. The maximum allowed ripple voltage is 800 mV_{PP}. The input voltage may never go below 4.75 V or above 5.25 V. As a result, a buck-boost converter is required for this kind of application, and the cable should have adequate protection to withstand the continuous short of V_{Bus} and ground.

2 Design Considerations

A typical output specification for this USB charger is shown in Figure 2. The U/I of the output should operate in the larger blank area illustrated in Figure 2. Thel operating status should be within this region enveloped by the red line.

Considering the 500-mA input current limit for the USB charger, as well as the 6.4-V output voltage limit, the target power stage should have one current loop as well as one voltage loop to realize the closed-loop

regulation. For the SEPIC topology, we can use the TPS40210 boost controller, which employs an inner peak current mode and an outer voltage mode to realize an output voltage regulation, as well as the cycle-by-cycle peak current limit in a MOSFET. It is clearly easy to limit the output within the maximum 6.4 V requirement. We can use this idea to realize an additional current loop to limit the input current within 500 mA.

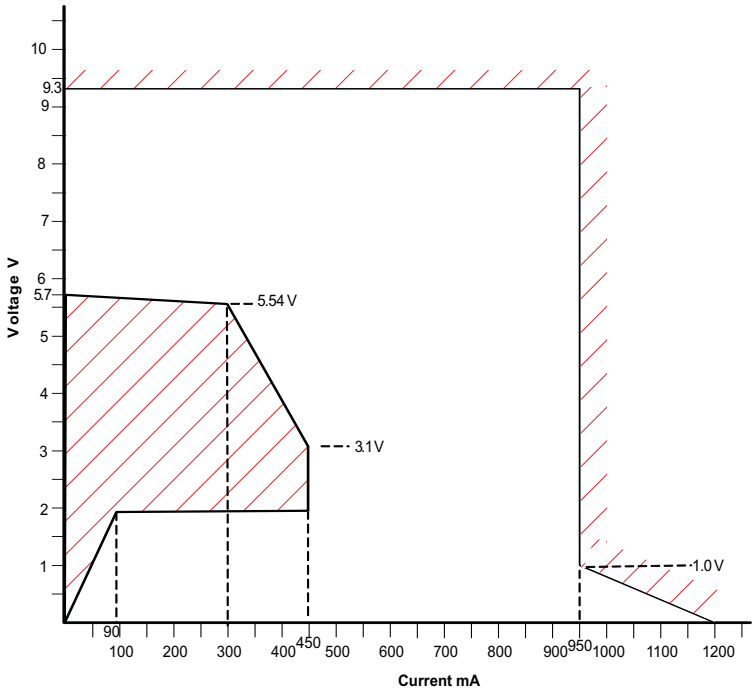

Figure 2. Output U/I Window

2.1 SEPIC Power Stage Analysis

The typical SEPIC topology is shown in Figure 3.

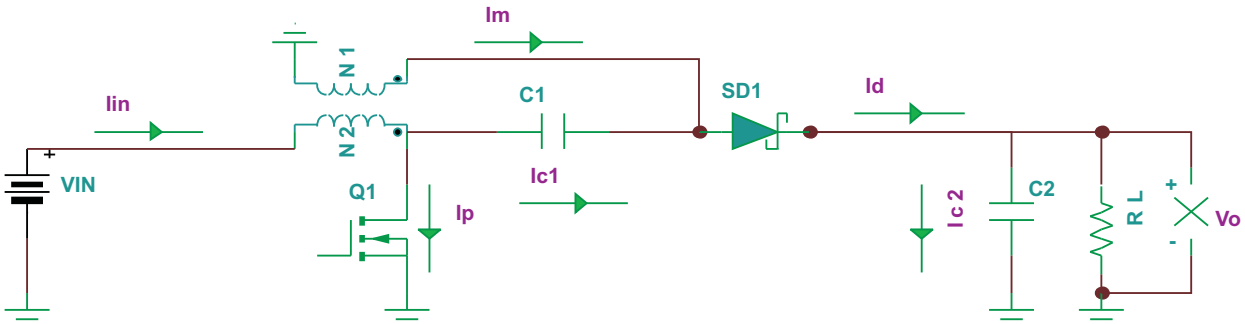

Figure 3. Typical SEPIC Topology

In a SEPIC design, the output voltage can be higher or lower than the input voltage. The SEPIC converter shown in Figure 1 uses two inductors, L1 and L2. The two inductors can be wound on the same core because the same voltages are applied to them throughout the switching cycle, as Figure 3 illustrates. Using a coupled inductor requires less space on the printed circuit board (PCB) and tends to be lower cost than using two separate inductors. Capacitor C1 isolates the input from the output and provides protection against a shorted load. Figure 3 and Figure 4 show the SEPIC converter current flow and switching waveforms. Equation 1 and Equation 2 show the relevant formulas.

$$I_{in} = \frac{Duty}{\left[Eff + (1 - Eff)Duty\right]}\left[I_p - \frac{V_{IN}Duty}{2L_p f} \times (n^2 + 1)\right] \quad (1)$$

$$n = \frac{N_2}{N_1};\ Duty = \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D} \quad (2)$$

Where:

- *Eff* is the efficiency for this converter

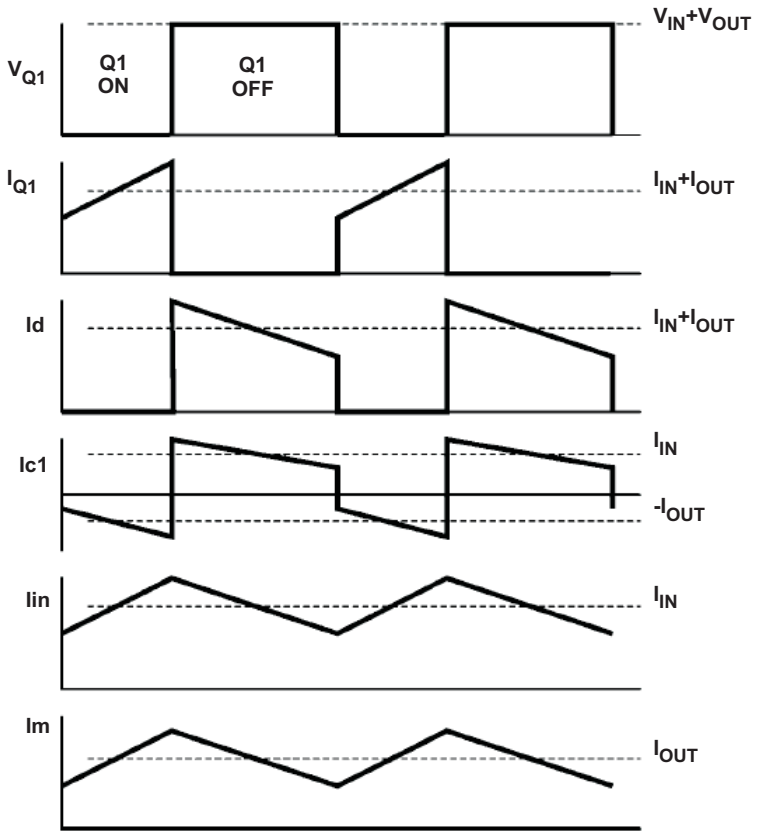

Figure 4. Current and Switching Waveforms for Figure 3 Circuit Design

Restricted Condition 1: The maximum input current limit I_{max} is 0.5 A.

$$I_{IN} \le I_{\max}$$

Let: $$K = \frac{Duty}{Eff + (1 - Eff) \times Duty}$$

Then:

$$L_p \le \frac{V_{IN} \times Duty}{2\left(I_{peaklmt} - \frac{I_{\max}}{K}\right)f} \times (n^2 + 1) \quad (3)$$

Restricted Condition 2: The maximum output power is P_{max}.

$$P_{IN} \geq \frac{P_{\max}}{Eff}$$

Then:

$$L_p \geq \frac{V_{IN} \times Duty}{2\left(I_{peaklmt} - \frac{P_{\max}}{V_{IN} \times Eff \times K}\right)f} \times (n^2 + 1) \quad (4)$$

The power stage design:

Conditions: V_{IN} = 4.75V; V_{OUT} = 5.54 V; $I_{OUT} \geq$ 300 mA; Eff = 0.8; n = 1:1; f = 160 kHz; I_{PLimit} = 1.2A. Then:

$$28.4uH \leq L_p \leq 35.98uH$$

As a result, a transformer with 1:1 turns ratio and 33-µH magnetizing inductor can be used.

Isolated Capacitor C1 Consideration:

The selection of the SEPIC capacitor, C_S, depends on the RMS current, which is given by Equation 5.

$$I_{C1(RMS)} = I_{out}\sqrt{\frac{(V_{out} + V_D)}{V_{IN\min}}} \quad (5)$$

The SEPIC capacitor must be rated for a large RMS current relative to the output power. This property makes the SEPIC architecure much better suited to low-power applications where the RMS current through the capacitor is relatively low (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum and ceramic capacitors are the best choice for SMT, having high RMS current ratings relative to size. Electrolytic capacitors work well for through-hole applications where size is not a factor and they can accommodate the required RMS current rating. The peak-to-peak ripple voltage on C_S (assuming no equivalent series resistance, or ESR) can determine the isolated capacitor, as shown in Equation 6.

$$C_1 = \frac{I_{out} D_{\max}}{\Delta V_{c1} f_{sw}} \quad (6)$$

with: $I_{c1(RMS)} > 0.35A$ **and C1=4.7uF with in = 4.75 ,VD=0.5 , out=5.54 ,fsw=160KHZ,RippleVc1=0.3V**

As a result, a 4.7-µF capacitor with a rating current greater than 0.35 A can be used.

2.2 Input and Output Current Loop Design

In Figure 3, we can derive Equation 7.

$$Avg(I_{in}) - Avg(I_p) = Avg(Ic_1) = 0;\ Avg(I_m) - Avg(I_L) = Avg(Ic_2) - Avg(Ic_1) = 0 \quad (7)$$

As a result, Equation 8 can also be calculated.

$$Avg(I_{in}) = Avg(Ip);\ Avg(I_m) = I_L \quad (8)$$

Therefore, it is critical that we can use the average current of the power MOSFET instead of the input current. One suggestion is that a low-pass filter can eliminate the high-frequency harmonic elements of the MOSFET current; then the average current of MOSFET can be obtained. We can use this average signal to setup a constant-current (CC) mode loop.

In addition, to work with another constant-voltage (CV) mode to regulate the output voltage, the TPS40210 controller requires a solution to automatically switch between the CV and CC modes.

2.3 TPS40210 SEPIC Implementation

Figure 5 shows the internal block diagram of the TPS40210, a wide-input voltage (4.5 V to 52 V), non-synchronous boost controller.

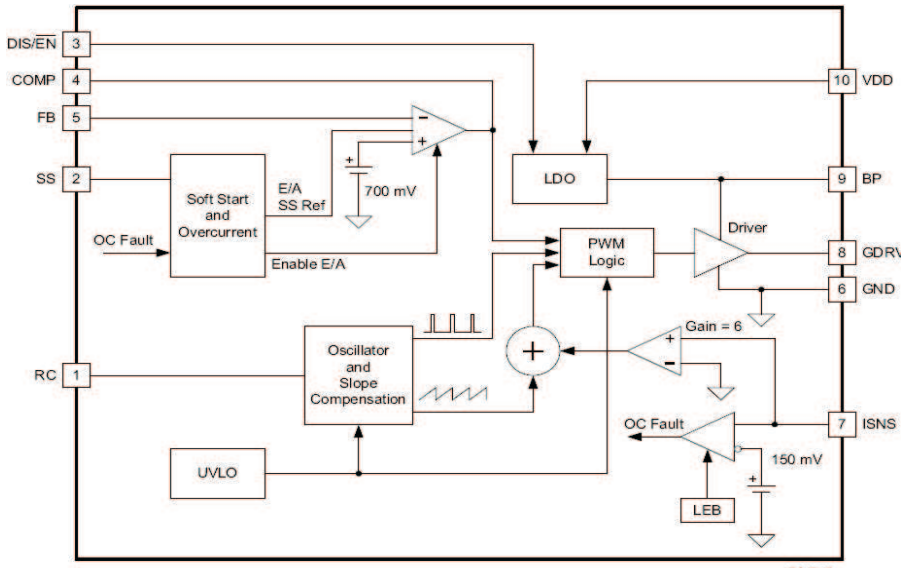

Figure 5. TPS40210 Internal Block Diagram

It is highly suitable for topologies that require a grounded source, N-channel FET including boost, flyback, SEPIC, and various LED driver applications. The TPS40210 features a programmable soft-start, overcurrent protection with automatic retry, and a programmable oscillator frequency. Additionally, current-mode control provides improved transient response and simplified loop compensation.

The overall schematic of the USB charger can be conceptualized as shown in Figure 6, which involves CC and CV mode closed-loop regulation.

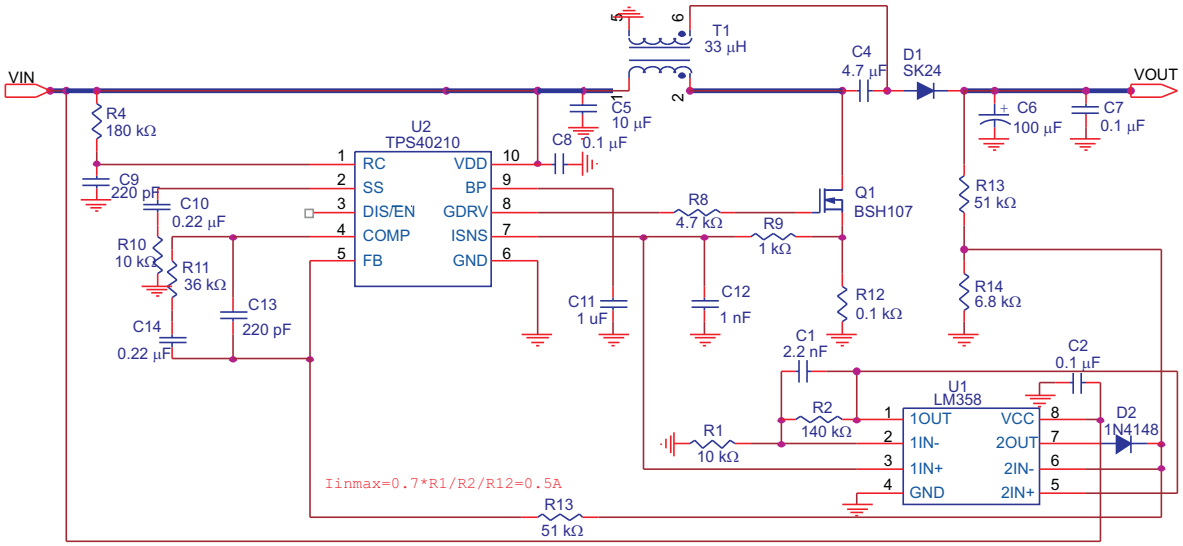

Figure 6. Schematic Design for USB Charger

The operating principle in Figure 6 is summarized by these guidelines:

1. An LM358 amplifier can be used to filter the high-frequency harmonic elements in the voltage across R12, and provide the average voltage signal in the 1OUT pin of the LM358, representing input current.

2. D2 and another internal LM358 amplifier can realize the automatic switching between the CC and CV modes, depending on the value of the 1OUT pin and the 2IN– pin of the LM358. If loading is lower, the 1OUT signal can be also lower than the divided voltage of R13 and R14, which results in a reversed D2; the 2IN– pin used to set up a CV mode control. If loading is higher, the 1OUT signal can be higher than the divided voltage of R13 and R14, which results in a conducting D2; the 2IN– pin can be charged to be the same as the 1OUT signal. then the CC mode take over the TPS40210 closed-loop control.
3. The configuration for input current limit and output voltage limit by the CC current loop and the CV mode can be shown in Equation 9 and Equation 10.

$$I_{in\max} = \frac{0.7 \times R_1}{R_2 R_{12}} = 500mA \tag{9}$$

$$V_{out\max} = 0.7 \times \left(1 + \frac{R_{13}}{R_{14}}\right) = 5.95V \tag{10}$$

2.4 Test Results with Input Current Limit Regulation

Figure 7 and Figure 8 show the measured test results for output voltage versus output current and input current versus output current, respectively.

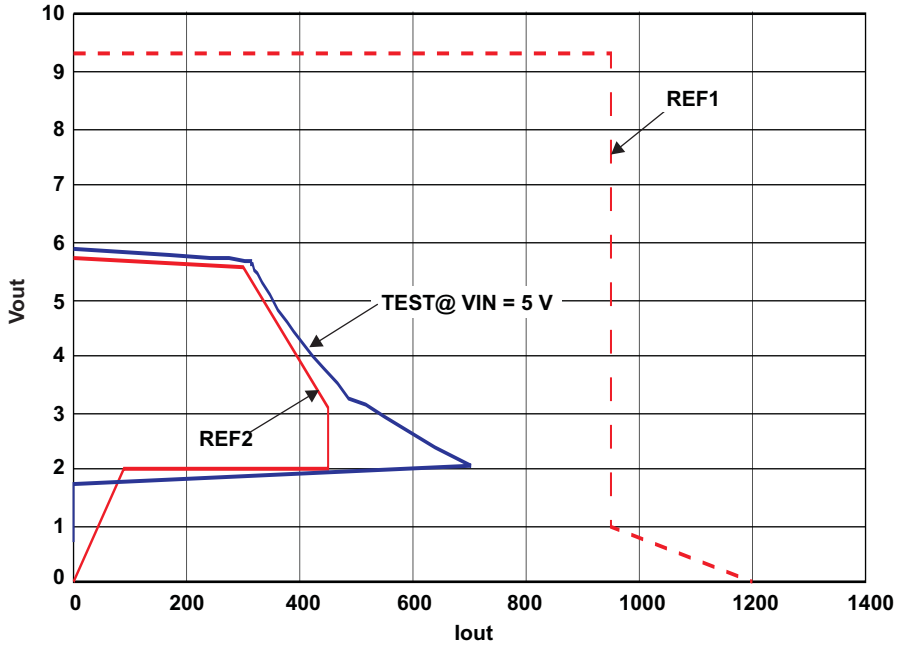

Figure 7. Test Results (V_{OUT} vs I_{OUT}) of the USB Charger Shown in Figure 6

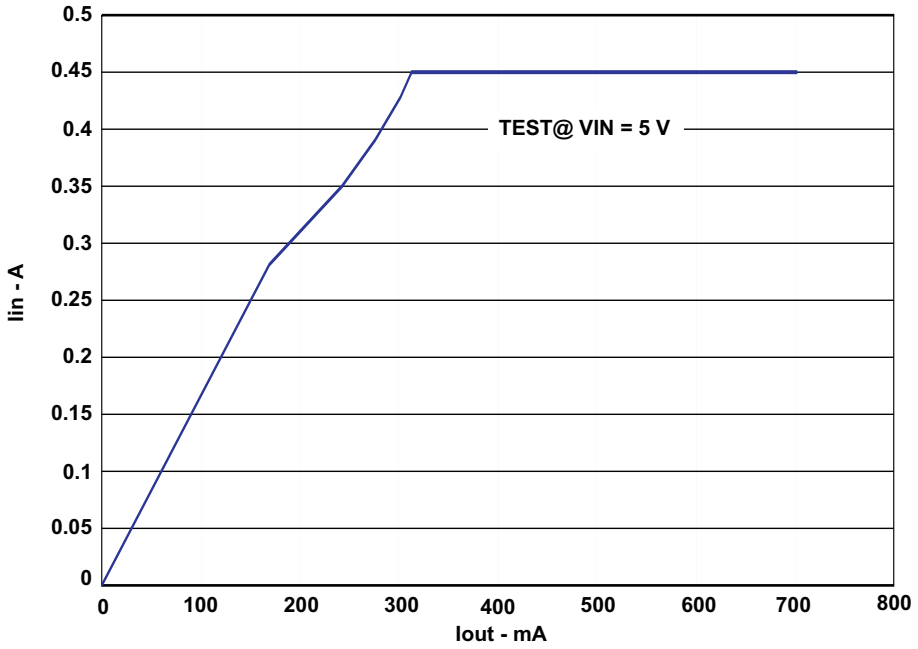

Figure 8. Test Results (I_{IN} vs I_{OUT}) of the USB Charger Shown in Figure 6

2.5 Output Current Limit Regulation

As stated in the design requirements, if the output current must be limited (according to Equation 3), the output current can be sensed in I_m as Figure 6 shows. The maximum output current can be obtained using Equation 11.

$$I_{L-MAX} = Avg(I_m) = \frac{0.7R_2}{R_1R_3} \tag{11}$$

Figure 9 illustrates the recommended solution.

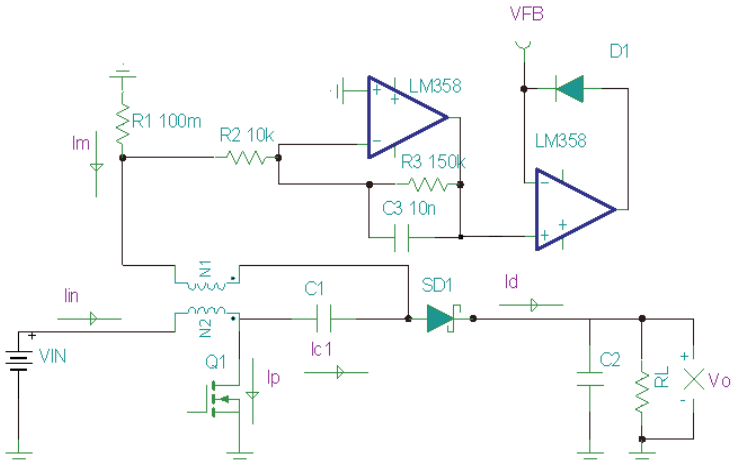

Figure 9. Output Current Limit Regulation Solution

3 Conclusion

With low cost, and fewer external components, the TPS40210 can implement a SEPIC with input and output current regulation, as well as the output voltage regulation. This SEPIC solution is very suitable for the buck-boost charger requirement, and we can limit the input current and output current so that it can be used to power the charger with a USB port.

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