How to Design a Boost Converter With the TPS61170

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Design Example

The following design example helps a user design a 12-V to 24-V power supply using the TPS61170 boost converter integrated circuit (IC). Figure 1 shows the power supply circuit.

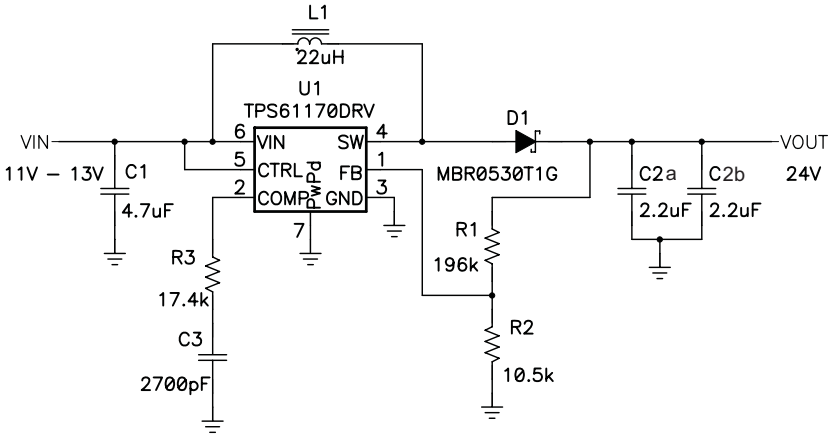

Figure 1. 12-V to 24-V Power Supply

Table 1 gives the performance specifications for the reference design.

Table 1. Performance Specifications for the Reference Design

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
INPUT and AMBIENT CHARACTERISTICS						
V_{IN}	Input voltage		11	12	13	V
F_S	Switching frequency		1.0	1.2	1.5	MHz
T_A	Ambient temperature				60	°C
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage		23	24	25	V
	Load regulation	V_{IN} = 12 V, 10 mA < I_O < 300 mA			1%	$\Delta V_O/\Delta I_O$
V_{RIPPLE}	Output voltage ripple	I_O = 200 mA			50	mVpp
I_O	Output current		1		300	mA
η	Efficiency	I_O = 300 mA		92%		
TRANSIENT RESPONSE						
ΔI_{TRAN}	Load step			250		mA
$\Delta I_{TRAN}/\Delta t$	Load slew rate			0.20		A/µs
ΔV_{TRAN}	V_O undershoot			500		mV

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1. DUTY CYCLE: Use data sheet (SLVS789) Equation 5 to estimate the maximum duty cycle, which occurs at minimum input voltage. This value cannot exceed the IC's maximum duty cycle per the datasheet.

$$D_{(MAX)} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}} = \frac{24\ V - 11\ V}{24\ V} = 55\% \quad (1)$$

2. $I_{OUT(MAX)}$ and $I_{IN(DC)}$: First, use data sheet Equation 4 to determine whether the internally current-limited TPS61170 can provide the desired output current.

   At $I_{OUT(MAX)}$, the current through the switch hits the switch's current limit, I_{LIM}. Expressed mathematically, the maximum average (DC) input current, $I_{IN(DC-MAX)}$, plus 1/2 the peak-to-peak inductor ripple current, IP, equals ILIM, so $I_{IN(DC-MAX)} = I_{LIM} - I_P/2$ at $I_{OUT(MAX)}$. But, for stable power supply operation and to minimize EMI, the I_P must be no more than a fraction, K_{IND} = 20-40%, of $I_{IN(DC)}$, so $I_{IN(DC-MAX)} = I_{LIM} - (K_{IND} \times I_{IN(DC-MAX)}/2$. Solving for $I_{IN(DC-MAX)}$ gives $I_{IN(DC-MAX)} = I_{LIM}/(1 + K_{IND}/2)$ at $I_{OUT(MAX)}$. Assuming estimated efficiency η_{est} = 92% at $V_{IN(MIN)}$ = 11 V and K_{IND} = 0.4,

$$I_{OUT(max)} = \frac{V_{IN} \times I_{LIM} \times \eta_{est}}{(1 + K_{IND}/2) \times V_{OUT}} = \frac{11\ V \times 0.96\ A \times 92\%}{(1 + 0.4/2) \times 24} = 337\ mA \quad (2)$$

   Because the application does not require the maximum output current computed by Equation 2, simply use data sheet Equation 6 to find $I_{IN(DC)}$ at the estimated efficiency and desired output current, I_{OUT}.

   $I_{IN(DC)} = V_{OUT} \times I_{OUT} / (V_{IN(min)} \times 0.92) = 24\ V \times 0.3\ A / (11\ V \times 0.92) = 0.71\ A$

3. INDUCTOR: After solving data sheet Equation 3 for L , the designer substituted $f_{S(MIN)}$ = 1 MHz, the Schottky diode's forward voltage, Vf =0.5 V, Equation 3, $V_{IN(MIN)}$ = 11 V and $I_P = 0.4 \times 0.6$ A to find the minimum L required to keep $I_P = K_{IND} \times I_{IN\_DC}$.

$$L \geq \frac{1}{\left[F_S \times \left(\frac{1}{V_{OUT} + V_f - V_{IN(MIN)}} + \frac{1}{V_{IN(MIN)}}\right)\right] \times I_p}$$

$$= \frac{1}{1\ MHz \times \left(\frac{1}{24\ V + 0.5\ V - 11\ V} + \frac{1}{11\ V}\right) \times 0.4 \times 0.71\ A} = 21.3\ \mu H \rightarrow 22\ \mu H \quad (3)$$

   The designer selected the closest standard value, which is 22 µH. When selecting an inductor, the two additional key specifications are its DC resistance (DCR) and its current rating, which is the lower of either its saturation current or its current for 40°C temperature rise. For this lower power converter, choosing an inductor with DCR less than 200 mΩ minimizes these losses. The inductor current rating must be higher than $I_{IN(DC)} + I_P/2$ = 0.71 A + (0.4 × 0.71 A) / 2 = 0.85 A. The designer selected SD6020-220 from Cooper, capable of 0.9 A with 122-mΩ DCR.

4. FEEDBACK RESISTORS: Use data sheet Equation 2 to size the feedback resistors for the required output voltage. Although the data sheet recommends 10 kΩ as an optimum value for R2, larger or smaller values can be used at the risk of noise being injected into FB or higher current lost through the FB resistors, respectively. After first trying 10 kΩ, the designer selected R2 = 10.5 kΩ so that R1 computes close to a standard resistor value:

$$R1 = R2 \times \left(\frac{V_{OUT}}{1.229\ V} - 1\right) = 10.5\ k\Omega \times \left(\frac{24}{1.229\ V} - 1\right) = 195\ k\Omega \rightarrow 196\ k\Omega \quad (4)$$

5. SCHOTTKY DIODE: Even with an ideal printed-circuit board layout containing short traces to minimize stray inductance and capacitance, the switching node of the boost converter may exhibit ringing up to 30% higher than the output voltage. Therefore, the designer selected a 30-V-rated diode to accommodate such ringing. The designer also selected a diode with a thermal rating that is high enough to accommodate its power dissipation, which is approximately $P_{D(DIODE)} = I_{OUT} \times V_f$ = 300 mA × 0.5 V = 150 mW.

6. OUTPUT CAPACITORS: Use data sheet Equation 12 and the transient specification to size the output capacitance.

   Assuming a ceramic output capacitor with negligible ESR and output ripple specification V_{RIPPLE} = 50 mVpp, data sheet Equation 12 indicates that the minimum output capacitance be

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times V_{RIPPLE}} = \frac{(24\ V - 12\ V) \times 0.300\ A}{24\ V \times 1.0\ MHz \times 50\ mV} = 3\ \mu F \quad (5)$$

If a large ESR capacitor is used, then there is additional output ripple equal to $V_{RIPPLE\_ESR} = I_{OUT} \times ESR$. To meet the load transient specification and assuming a control loop bandwidth f_{BW} = 30 kHz, Equation 6 gives

$$C_{OUT} = \frac{\Delta I_{TRAN}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} = \frac{250\ mA}{2 \times \pi \times 30\ kHz \times 500\ mV} = 2.6\ \mu F \quad (6)$$

The loop bandwidth assumption of 30 kHz may have to be modified later. The designer selected C2 = 2 × 2.2 µF, 50-V output capacitors (Figure 1).

7. COMPENSATING THE CONTROL LOOP: Data sheet equations 7 through 11 can be combined to give a simple mathematical model of the power supply's small signal control loop, $G_T(s)$.

$$G_T(s) = \frac{1.229\ V}{V_{OUT}} \times G_{EA} \times 6\ M\Omega \times \frac{V_{IN} \times R_{OUT}}{V_{OUT} \times R_{SENSE} \times 2} \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_Z}\right) \times \left(1 - \frac{s}{2 \times \pi \times f_{RHPZ}}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2 \times \pi \times f_{P2}}\right)}$$

Where

$$f_{P2} = \frac{2}{2\pi \times R_{OUT} \times C2} = \frac{2}{2\pi \times 80\ \Omega \times 2 \times 2.2\ \mu F} = 905\ Hz$$

$$f_{RHPZ} = \frac{R_{OUT}}{2\pi \times L} \times \left(\frac{Vin}{Vout}\right)^2 = \frac{80\ \Omega}{2\pi \times 22\ \mu H} \times \left(\frac{12}{24}\right)^2 = 136\ kHz$$

$$f_{P1} = \frac{1}{2\ \pi \times 6\ M\Omega \times C3}$$

$$f_Z = \frac{1}{2\pi \times R3 \times C3} \quad (7)$$

G_{EA} is the amplifier transconductance and can be found in the data sheet electrical specifications table and $R_{OUT} = V_{OUT}/I_{OUT}$. For current mode boost power supplies, the inductor is not part of the control loop, and the output capacitor sets the dominant pole, f_{P2}. If the RHPZ is high enough in frequency (i.e., L is not too large), simply setting the compensation zero, f_Z equal to the dominant pole, f_{P2}, stabilizes the loop. Assuming R3 = 10 kΩ per the data sheet recommendation and R_{SENSE} = 200 mΩ, its approximate maximum value, setting $f_z = f_{P2}$ gives C3 = 17.6 nF which is replaced by the standard value of 15 nF. Figure 2 shows the Mathcad™ gain and phase of the power stage, $G_T(s)$, with s = j × 2 × π × f.

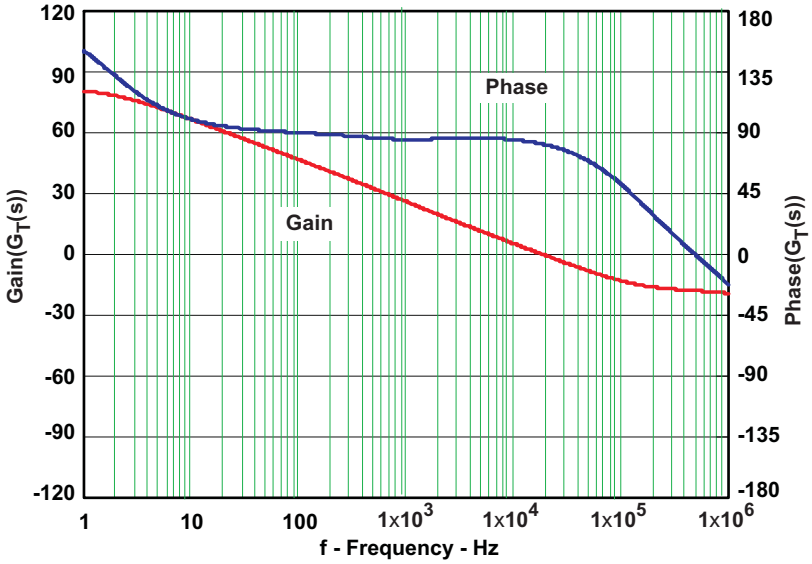

Figure 2. Total Loop Gain and Phase With R3 = 10 kΩ and C3 = 15 nF

Although the loop is stable with almost 90 degrees of phase margin and small signal control loop bandwidth, f_{BW}, of 20 kHz, components R3 and C3 are not optimized to give the highest bandwidth, and therefore the smallest output capacitance to meet the load transient requirement. In fact, maximizing the loop bandwidth using this method requires iteratively increasing R3 and/or decreasing C3 to meet the load transient specification.

By separating the power stage and error amplifier components from data sheet equations 7 through 11, the designer can directly size R3 and C3 for a given f_{BW} without an interactive, trial and error process. G_{PW} gives the power stage small signal transfer function.

$$G_{PW}(s) = \frac{R_{OUT} \times (V_{IN})}{2 \times R_{SENSE} \times V_{OUT}} \times \frac{\left(1 - \frac{s}{2 \times \pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2 \times \pi \times f_{P2}}} \times He(s) \quad (8)$$

Equation 8 ignores the ESR zero, f_Z, because low ESR ceramic output capacitors produce a zero at frequencies above interest. If tantalum or aluminum electrolytic output capacitors are used, then an additional zero created by the output capacitor and ESR must be included in equation 8 in the form $f_{ZESR} = 1+s/(2\times\pi\times ESR\times C2)$. The simplest way to handle this potentially low frequency zero is to cancel it with a pole by connecting an appropriately sized capacitor from COMP to ground. Usually, the stray board capacitance or an actual capacitor in the 10pF range is used to produce a high frequency pole that roles off the loop gain following the RHPZ. But, if this capacitance, C6 on the EVM, is sized such that ESR × C2 ≠ R3 × C6, assuming C6 << C3, then the ESR zero's effect will be nullified and the design method in this application note is still applicable. In rare cases, f_{ZESR} might be low enough in frequency to cancel f_{P2} and eliminate the need for R3 and C3. In all cases, a 0.1uF-10uF ceramic output capacitor in parallel with the large high ESR output capacitor is recommended to reduce the output ripple.

He(s) models the inductor current sampling effect as well as the slope compensation (S_E) effect on the small signal response.

$$He(s) = \frac{1}{1 + \frac{s \times \left[\left(1 + \frac{S_E}{S_N}\right) \times (1 - D) - 0.5\right]}{f_{SW}} + \frac{s^2}{(\pi \times f_{SW})^2}} \quad (9)$$

Where the natural and externally added slopes are

$$S_N = \frac{V_{OUT} + V_F - V_{IN}}{L} \times R_{SENSE} \tag{10}$$

$$S_E = \frac{42000 \frac{A}{F}}{(1 - D)} \tag{11}$$

With R_{OUT} = 24 V/0.300 A = 80 Ω and R_{SENSE} = 200 mΩ, Figure 2 shows the Mathcad™ gain and phase of the power stage, $G_{PW}(s)$, with s = j × 2 × π × f.

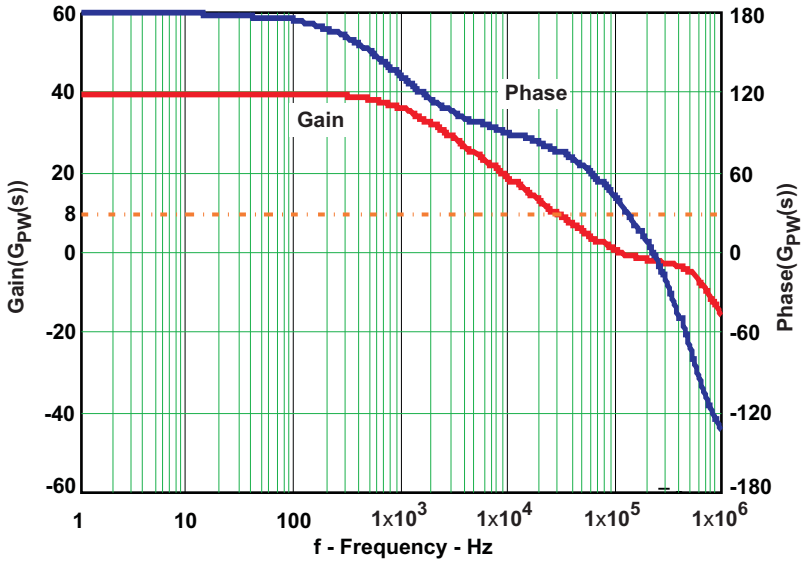

Figure 3. Power Stage Gain and Phase

To prevent switching noise or gain fluctuations due to changes in nonmeasured parameters from causing small signal instability, conventional wisdom recommends that the crossover frequency, f_{BW}, be kept below the lower $F_{S(MIN)}/5$ = 200 kHz or $f_{RHPZ}/3$ = 45.3 kHz. In section 6, the designer chose f_{BW} = 30 kHz. Therefore, the compensation gain, K_{COMP}, and power stage gain at the crossover frequency must be zero, or $K_{COMP}(f_{BW}) + 20\log(G_{PW}(f_{BW})) = 0$, so $K_{COMP}(f_{BW}) = -20\log(G_{PW}(f_{BW}) = –8$ dB as illustrated by the orange dashed line in Figure 2. Using Type II compensation and finding G_{EAmax}= 400 µmho in the data sheet, Equation 12 computes the value of R3 to give $K_{COMP}(f_{BW})$ = –15 dB, rounded up to the closest standard value.

$$R3 \cong \frac{10^{\frac{K_{COMP}(f_C)}{20dB}}}{G_{EA} \times \frac{R2}{R2 + R1}} = \frac{10^{\frac{-9dB}{20dB}}}{400\ \mu mho \times \frac{10.5\ k\Omega}{196\ k\Omega + 10.5\ k\Omega}} = 17.3\ k\Omega \rightarrow 17.4\ k\Omega \tag{12}$$

From Equation 7, the designer set f_Z ~= $f_{BW}/10$ = 3 kHz for maximum phase boost at the crossover point and solved for C3. The answer was rounded down to the closest standard value.

$$C3 \cong \frac{1}{2\pi \times R3 \times f_Z} = \frac{1}{2\pi \times 17.4\ k\Omega \times 3\ kHz} = 3.04\ nF \rightarrow 2700\ pF \tag{13}$$

Figure 4 shows the Mathcad™ plot of $T(s) = G_{PW}(s) \times H_{EA}(s)$

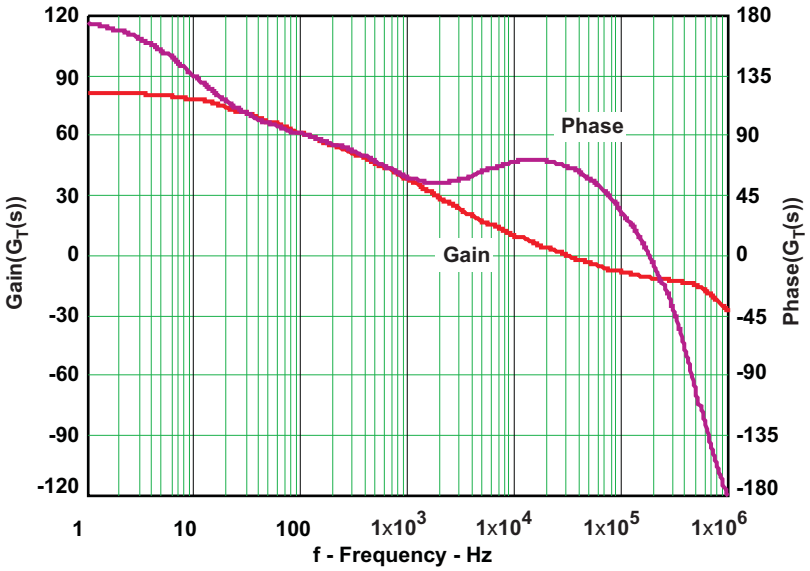

Figure 4. Total Loop Gain and Phase With R3 = 17.4 kΩ and C3 = 2700 pF

Figure 5 shows the loop gain and phase as measured on a Venable Gain Phase Analyzer. The measured f_{BW} is closer to 40 kHz, slightly higher than the designed and simulated 30 kHz. The phase margin is slightly above 60° as expected.

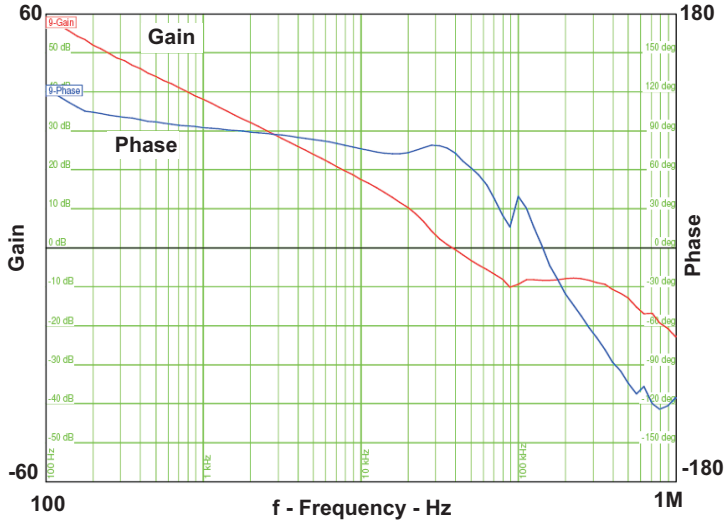

Figure 5. Measured Loop Gain and Phase

Figure 6 shows the transient response for a 250-mA load step. The ΔV_{TRAN} droop of 400 mV is well below the 500 mV specification. This performance is not unexpected due to the over-sized output capacitance and wider than designed loop bandwidth.

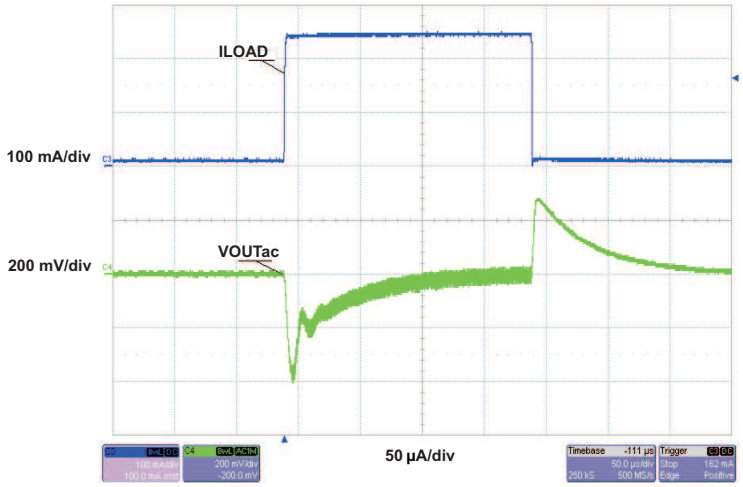

Figure 6. Load Transient Response

Figure 7 shows the efficiency.

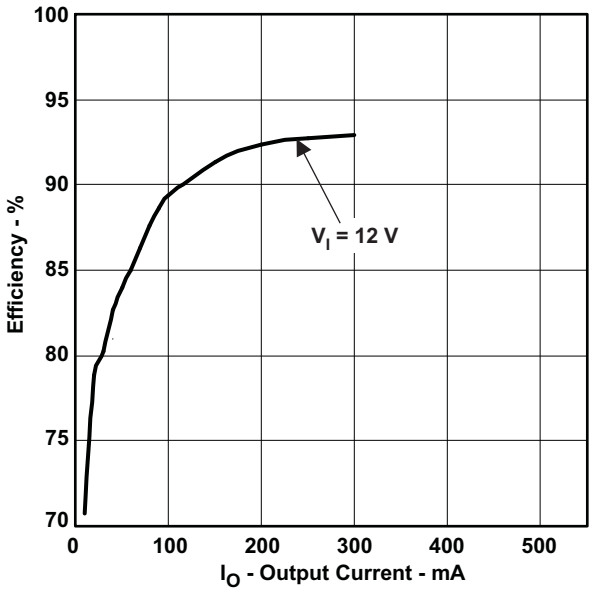

Figure 7. Efficiency

Figure 8 shows the load regulation, which is well within the 1% specification

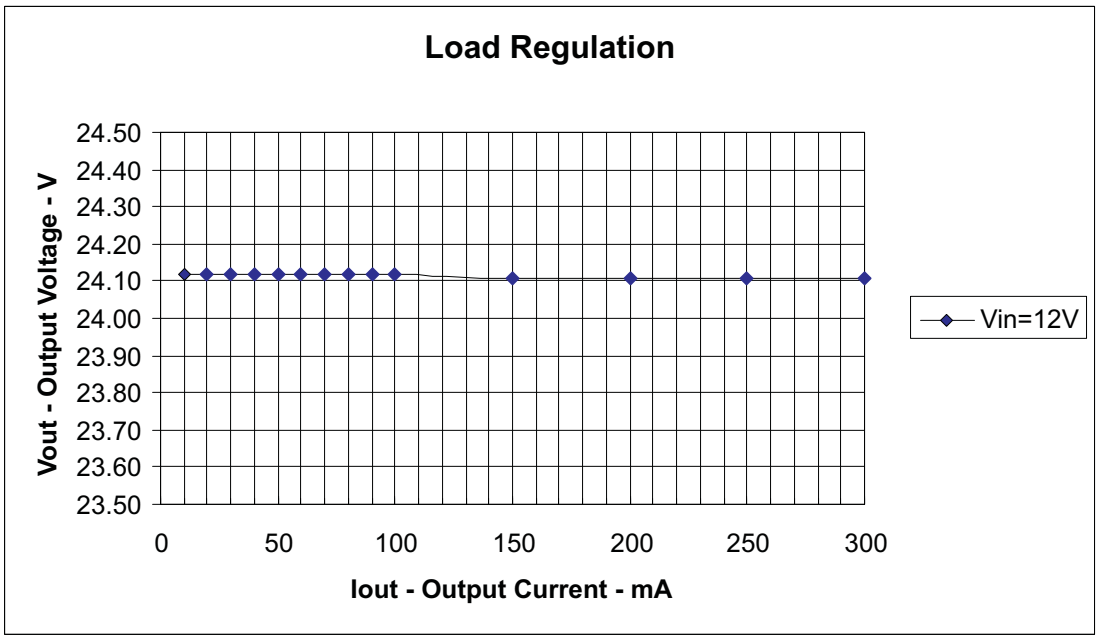

Figure 8. Load Regulation

Figure 9 shows typical operating waveforms.

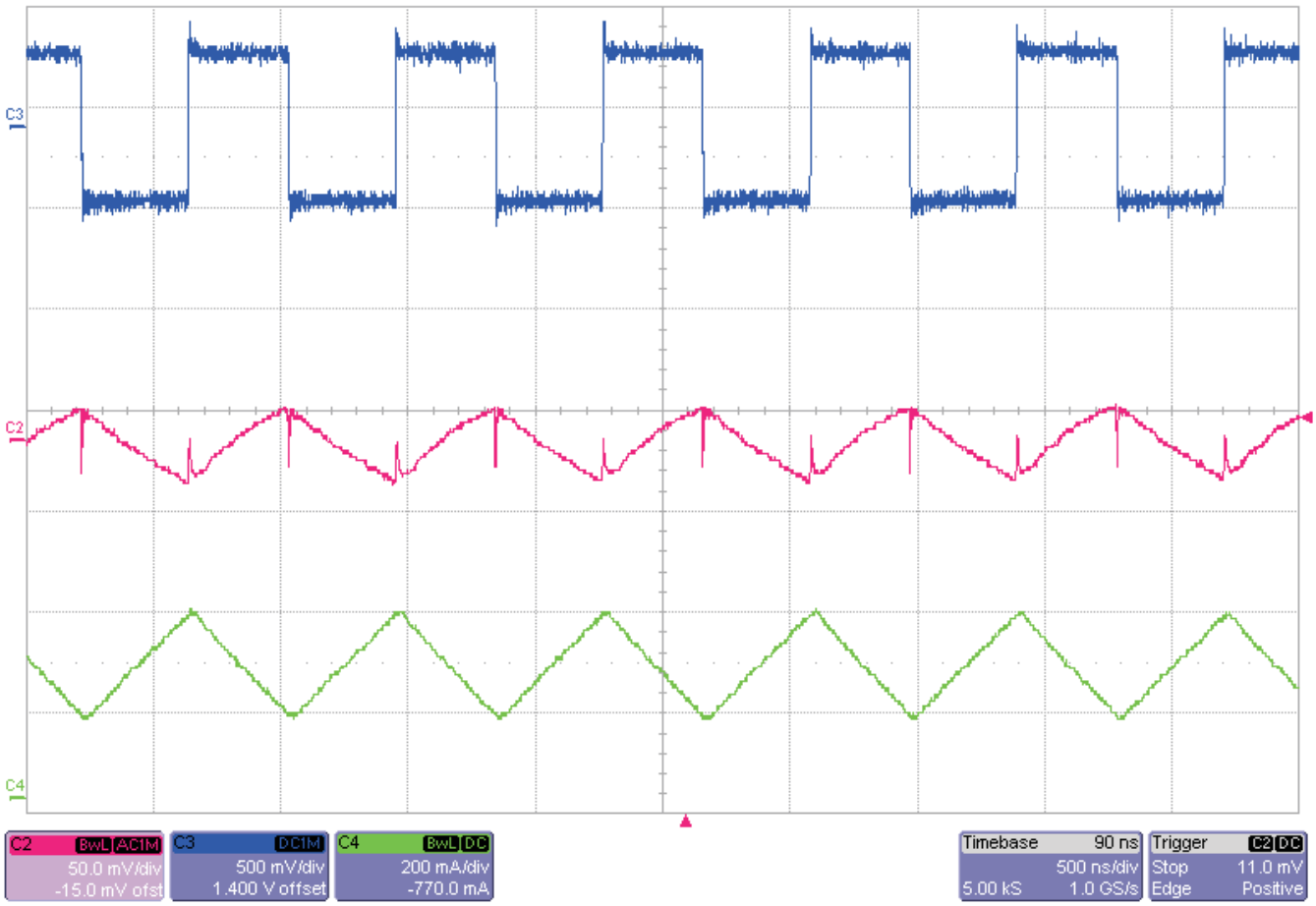

Figure 9. Operation Including V_{RIPPLE} at V_{IN} = 12 V and I_{OUT}=200 mA

The preceding design steps are applicable to any current-mode, control-based boost converter.

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