Creating GSM /GPRS Power Supply from TPS54260

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ABSTRACT

This application report describes how to design power supply for a Global System for Mobile Communications (GSM)/ General Packet Radio Service (GPRS) module.

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1 GSM/GPRS Power Supply Design Requirements

The input voltage supply for the GSM/GPRS module can be from 3.2 V to 4.5 V, with an average power supply current requirement of 400 mA to ~1 A. The power supply must also be able to sustain transmission pulses of 2 A to 3 A, thus considerations for excellent load regulation and low-ripple needs to be taken into account, simultaneously ensuring a highly efficient design.

The average current consumption depends upon the class supported by the module. The most common GPRS classes are Class 8, Class 10 and Class 12. Higher the GPRS class, the faster the data transfer rates and correspondingly it requires more number of timeslots for transmission. Class 8 uses 4 Rx and 1 Tx slot, Class 10 uses 3 Rx and 2 Tx slots and Class 12 uses 1 Rx and 4 Tx slots.

Thus, a GSM/GPRS Module transmits either 1/2/3 time slot(s) of 577us during a 4.6ms period, and receives or remains idle for the rest 4.0ms/3.4ms/2.3ms time depending upon whether it is GSM/GPRS Class 8, Class 10 or Class 12 module. Taking 3 A as the amplitude of transmission bursts, this leads to an average current consumption of about 400mA incase of Class 8 to ~ 1 A in case of Class 12. A power supply design for a GSM/GPRS module should be able to deliver this average current, and also handle intermittent transmission bursts with high current consumption.

Now, for meeting above specifications, a linear regulation solution suffers from following disadvantages:

1. High heat dissipation necessitating the use of a heat sink.
2. Low efficiency in case the unit has to work with higher input voltages.

Thus, use of switched DC-DC converters becomes the right choice. The designs explained below have been optimized for the load transient of 0.1 A - 3 A, and also enable a small footprint, high efficiency and little heat dissipation using TPS54260, a 60V, 2.5 A step down regulator with an integrated high side MOSFET.

The report will go through step-by-step procedure to design the GSM/GPRS power supply with the help of two reference designs implemented using TPS54260. Although this application example presents two examples, the concepts remain identical for other designs as well.

The TP54260 has following features:

- Current mode control: Provides simple external compensation and flexible component selection.
- Pulse skip mode: Reduces no load supply current.
- 250 mΩ High side mosfet provides a cost effective power supply for 2 A to 3 A transient load with a minimum current limit of 3.5 A.
- Under voltage lockout is internally set at 2.5V, but can be increased using the enable pin.
- Slow Start controls the output voltage startup ramp and an also be configured for sequencing/tracking.
- An open drain power good signal indicates the output is within 93% to 107% of its nominal voltage.
- A wide switching frequency range allows efficiency and external component size to be optimized.
- Frequency fold back and thermal shutdown protects the part during an overload condition.

2 Design – 1 Specifications

We start with the following system parameters:

Output Voltage	3.8 V
Transient Response 0 to 3 A load step	ΔVout = 3 %
Output Current	2.5 A (DC)
Transient Current	0.1 A to 3 A GSM Pulse
Input Voltage	12 V nom. 8 V to 40 V
Output Voltage Ripple	1% of Vout
Start Input Voltage (rising VIN)	6V
Stop Input Voltage (falling VIN)	5.5V

NOTE: All the equations given in the following design examples come from TPS54260 (SLVSA86) datasheet. For detailed variable names and assumptions please refer to the datasheet.

2.1 Switching Frequency

The response time of the converter to load transients (in this case, GSM/GPRS Module) depends both on the closed-loop bandwidth of the circuit and the switching frequency. Also, higher switching frequencies enable the use of smaller (and cheaper) output filter components whereas lower switching frequencies tend to have higher efficiencies. In addition, so as to minimize the output ripple on the power supply line to the GSM/GPRS module, the selected frequency should not be too high.

The TPS54260 can be operated at switching frequencies from 100 kHz to 2500 kHz. Following equations impose limits over the maximum switching frequency:

1. To avoid pulse-skipping: As the frequency is increased, the on time for a given duty cycle is decreased ($D = T_{ON} \times f_{sw}$). For consistent switching action without pulse skipping, the on time must be greater than the minimum controllable on time. For the TPS54260, this minimum controllable on time is typically 135 ns.

$$f_{SW(\max skip)} = \frac{1}{t_{ON}} \times \left(\frac{(I_L \times R_{dc}) + V_{out} + V_d}{V_{IN} - (I_L \times R_{ds}) + V_d} \right) \quad (1)$$

Where:

I_L = inductor current
R_{DC} = inductor resistance
V_{INMAX} = maximum input voltage
V_{OUT} = output voltage
V_{OUTSC} = output voltage during short
Vd = diode voltage drop
$R_{DS(on)}$ = switch on resistance
t_{ONmin} = minimum controllable on time

2. Frequency Foldback: During overcurrent conditions, the output voltage decreases as the overcurrent protection is activated. As the foldback voltage at VSENSE decreases below 0.6 V, the switching frequency is reduced by 50% of the nominal value. At a VSENSE voltage of 0.4 V, the switching frequency is reduced to 25%, and finally when the VSENSE voltage falls below 0.2 V, the switching frequency is reduced to 12.5% of the nominal set frequency. This is done so that in any individual switching cycle, sufficient time is available for the inductor current to ramp below the overcurrent threshold. This feature is known as Frequency Foldback.

$$f_{SW(shift)} = \frac{fdiv}{t_{ON}} \times \left(\frac{(I_L \times R_{dc}) + V_{outsc} + V_d}{V_{IN} - (I_L \times R_{ds}) + V_d} \right) \quad (2)$$

Where:

I_L = inductor current
R_{DC} = inductor resistance
V_{INMAX} = maximum input voltage
V_{OUT} = output voltage
V_{OUTSC} = output voltage during short
I_{OUTS} = output short circuit current
Vd = diode voltage drop
$R_{DS(on)}$ = switch on resistance
t_{ONmin} = minimum controllable on time
$f$div = frequency division factor (1, 2, 4, or 8)

Using Equation 1 and Equation 2, the maximum skip and shift frequencies are 2.77 MHz and 4.89 MHz, thus the switching frequency should be less than 2.77 Mhz (the lesser value of maximum skip and shift frequencies).

This design uses a nominal switching frequency of 500 kHz to allow for high efficiency as well as good response time. The switching frequency is set by placing a resistor, R5, from the RT/CLK pin to ground. The value of the R5 is calculated by:

$$R5\ (kOhm) = \frac{206033}{f sw\ (kHz)^{1.0888}} \quad (3)$$

For 500 kHz – switching frequency, R5 must be 237 kΩ.

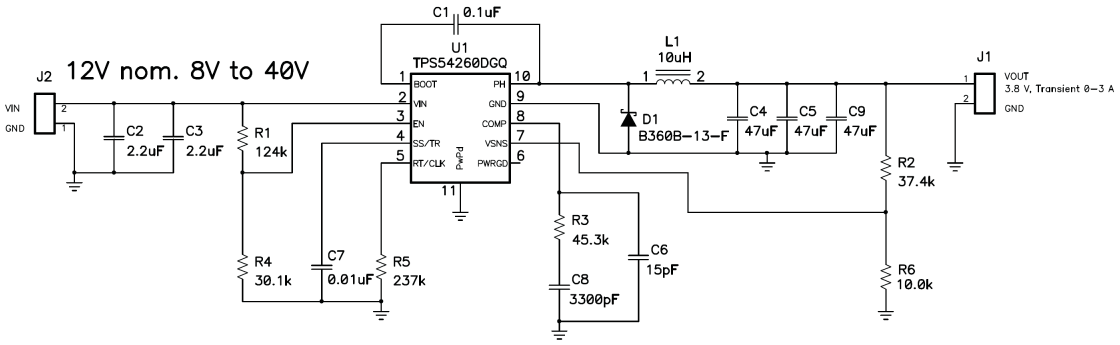

Figure 1. 3.8V Output TPS54260 Design Example

2.2 Output Inductor Selection

The output inductor is typically selected so that the peak-to-peak ripple current is 30% of the output current. Verify that the RMS and saturation current ratings for the inductor exceed application specifications.

$$L1\ min = \frac{Vinmax - Vout}{Io \times K_{IND}} \times \frac{Vout}{Vinmax \times fsw} \quad (4)$$

Once the inductor is chosen, the peak-to-peak inductor current can be calculated using Equation 5.

$$I_{RIPPLE} = \frac{Vout \times (Vinmax - Vout)}{Vinmax \times L1 \times fsw} \quad (5)$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from:

$$I_{L(rms)} = \sqrt{(Io)^2 + \frac{1}{12} \times \left(\frac{Vout \times (Vinmax - Vout)}{Vinmax \times L1 \times fsw} \right)^2} \quad (6)$$

$$ILpeak = Iout + \frac{Iripple}{2} \quad (7)$$

The required minimum inductor is calculated to be 9.17 μH. The nearest standard value inductor is 10 μH.

The calculated peak-to-peak, rms, and peak currents are 0.687 A, 2.50 A, and 2.84 A. For this design, a 10-μH Coilcraft MSS1260-103ML_ is used. The rms current rating is 4 A, and the saturation current rating is 6.92 A.

2.3 Output Capacitor

The output capacitor determines the modulator pole, the output voltage ripple, and response of the regulator to a large change in load current. It needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor (Cout = C4 || C5 || C9) needs to supply the load with current when the regulator can not.

$$Cout > \frac{2 \times \Delta Iout}{fsw \times \Delta Vout} \quad (8)$$

For this example, the transient load response is specified as a 3% change in Vout for a load step from 0.1 A to 3 A. Thus, ΔIout = 2.9 A and ΔVout = 0.03 × 3.8 = 0.114 V. Using these numbers gives a minimum capacitance of 100μF.

When the load current rapidly decreases, the stored energy in the inductor produces an output voltage overshoot. To absorb this energy, the output capacitor needs to be sized properly, thereby maintaining the desired output voltage during these transient periods. Following equation is used to calculate the minimum capacitance required to keep the output voltage overshoot to a desired value.

$$Cout > Lo \times \frac{\left(Ioh^2 - Iol^2\right)}{\left(Vf^2 - Vi^2\right)} \quad (9)$$

Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the final peak output voltage, and V_i is the initial capacitor voltage. For this example, the worst case load step will be from 3 A to 0.1 A. The output voltage will increase during this load transition and the stated maximum in our specification is 3 % of the output voltage. This will make Vf = 1.03 × 3.8 = 3.914. Vi is the initial capacitor voltage which is the nominal output voltage of 3.8 V. Using these numbers in Equation 10 yields a minimum capacitance of 70 μF.

$$Cout > \frac{1}{8 \times fsw} \times \frac{1}{\frac{V_{ORIPPLE}}{I_{RIPPLE}}} \quad (10)$$

Equation 11 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, $V_{ORIPPLE}$ is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. It yields 5.73µF.

The maximum ESR an output capacitor can have to meet the output voltage ripple specification is calculated using following:

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} \tag{11}$$

Equation 11 indicates the ESR should be less than 43.6 mΩ.

The most stringent criterion for the output capacitor is found to be 100 µF of capacitance to keep the output voltage in regulation during a load transient.

Additional capacitance de-ratings for aging, temperature and dc bias should be factored which will increase this minimum value. For this example, 3 × 47 µF, 10 V ceramic capacitors with 7 mΩ of ESR are used. The de-rated capacitance would be above the minimum required capacitance of 100 µF.

Using the following equation the total rms current in the output capacitors is calculated. For this application, following equation yields 198 mA.

$$\text{Icorms} = \frac{\text{Vout} \times (\text{Vinmax} - \text{Vout})}{\sqrt{12} \times \text{Vinmax} \times \text{Lo} \times f\text{sw}} \tag{12}$$

The total rms current in the output capacitor is 0.2A. The ceramic capacitor used has an rms current rating of 3A.

2.4 Catch Diode

The selected diode must have a reverse voltage rating equal to or greater than Vinmax. The peak current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage.

For the example design, the B360B-13-F Schottky diode with 60V reverse voltage is selected for its lower forward voltage and it comes in a larger package size which has good thermal characteristics over small devices. The typical forward voltage of the B360B-13-F is 0.70 volts.

During the converter on time, the output current is provided by the internal switching FET. During the off time, the output current flows through the catch diode. The average power in the diode is given by Equation 13:

$$\text{Pd} = \frac{(\text{Vinmax} - \text{Vout}) \times \text{Iout} \times \text{V}f\text{d}}{\text{Vinmax}} + \frac{\text{Cj} \times f\text{sw} \times \left(\text{Vin}^2 + \text{V}f\text{d}^2\right)}{2} \tag{13}$$

The B360B-13-F has a junction capacitance of 200 pF. The selected diode will dissipate 0.85 W.

2.5 Input Capacitor

The TPS54260 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 3µF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54260. The input ripple current can be calculated using Equation 14:

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{\text{Vout}}{\text{Vinmin}} \times \frac{(\text{Vinmin} - \text{Vout})}{\text{Vinmin}}} \tag{14}$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15:

$$\Delta\text{Vin} = \frac{\text{Ioutmax} \times 0.25}{\text{Cin} \times f\text{sw}} \tag{15}$$

2.6 Slow Start Capacitor

The slow start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Using the slow start time as 3.5ms, the value of slow start capacitor is computed with the help of following equation to be 8.75 nF. For this design, the next larger standard value of 10 nF is used.

$$Tss > \frac{Cout \times Vout \times 0.8}{Issavg} \quad (16)$$

Where:

Issavg = Average slow start current
Tss = Minimum slow start time

2.7 Bootstrap Capacitor Selection

A 0.1-μF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. The capacitor should have a 10V or higher voltage rating.

2.8 Under Voltage Lock Out Set Point

The programmable UVLO and enable voltages are set using the resistor divider of R1 and R4 between Vin and ground to the EN pin. Equation 17 and Equation 18 can be used to calculate the necessary resistance values.

For the example application, a 124 kΩ between Vin and EN (R1) and a 30.1 kΩ between EN and ground (R4) are required to produce the 6.0 V and 5.5 V start and stop voltages.

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (17)$$

$$R4 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1} \quad (18)$$

2.9 Output Voltage and Feedback Resistors Selection

For the example design, 10.0 kΩ was selected for R6 and R2 was calculated to be 37.4 kΩ using following equation:

$$R2 = R6 \times \frac{Vout - 0.8V}{0.8V} \quad (19)$$

2.10 Compensation

To stabilize the closed-loop circuit, a compensation network is required. The compensation components are connected from the COMP pin to GND. For this example, some simplifying assumptions are made so as to ease the design procedure.

To properly compensate the closed-loop circuit, the gain characteristics of the power stage must be determined. In general, the power stage pole, and the power stage zero frequency must be known. These terms are defined as follows:

$$fp\ mod = \frac{Ioutmax}{2 \times \pi \times Vout \times Cout} \quad (20)$$

$$fz\ mod = \frac{1}{2 \times \pi \times Resr \times Cout} \quad (21)$$

For Cout, a de-rated value of 100 μF is used.

Use Equation 22 and Equation 23, to estimate a starting point for the crossover frequency, fco, to design the compensation.

For the example design:

fpmod is 1.04 kHz {V_{OUT} = 3.8 V, I_{OUT} = 2.5 A, C_{OUT} = 100 µF}

fzmod is 682.1 kHz {Resr = 7 mΩ / 3 = 2.33 mΩ , C_{OUT} = 100 µF}

Equation 22 is the geometric mean of the modulator pole and the ESR zero and Equation 23 is the mean of modulator pole and the switching frequency.

$$f_{CO} = \sqrt{f_p mod \times f_z mod} \tag{22}$$

$$f_{CO} = \sqrt{f_p mod \times \frac{f_{SW}}{2}} \tag{23}$$

Equation 22 yields 26.7 kHz and Equation 23 gives 16.1 kHz. Use the lower value of Equation 22 or Equation 23 for an initial crossover frequency. For this example, a higher fco is desired to improve transient response. The target cross-over frequency(f_{co}) is 49 kHz.

Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

To determine the compensation resistor, R3, use Equation 24.

$$R3 = \left(\frac{2 \times \pi \times f_{co} \times Cout}{gmps}\right) x \left(\frac{Vout}{V_{ref} \text{ x } gmea}\right) \tag{24}$$

Assume the power stage transconductance, gmps, is 10.5A/V. The output voltage, Vo, reference voltage, VREF, and amplifier transconductance, gmea, are 3.3V, 0.8V and 310 µA/V, respectively.

R3 is calculated to be 44.9 kΩ, use the nearest standard value of 45.3 kΩ. Use Equation 25 to set the compensation zero to the modulator pole frequency. Equation 25 yields 3360 pF for compensating capacitor C5, a 3300 pF is used for this design.

$$C8 = \frac{1}{2 \times \pi \times R3 \times f_p \text{ mod}} \tag{25}$$

A compensation pole can be implemented if desired using an additional capacitor C6 in parallel with the series combination of R3 and C8. Use the larger value of Equation 26 and Equation 27 to calculate the C6, to set the compensation pole. 15 pF is selected for C6.

$$C6 = \frac{C_o \times Resr}{R3} \tag{26}$$

$$C6 = \frac{1}{R3 \times f_{sw} \times \pi} \tag{27}$$

2.11 Experimental Results Design – 1

Figure 2 to Figure 20 show the experimental test results of the Figure 1 design.

The discontinuous conduction mode (DCM) to continuous conduction mode (CCM) boundary is at an output current of 237mA. The pulse skip mode (PSM) boundary is at an output current of 21mA. The input current draw at no load at 21V input voltage is 0.25mA.

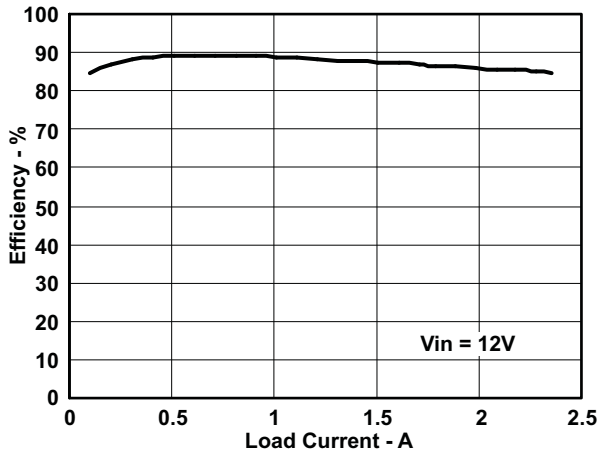

Figure 2. Efficiency vs Load Current

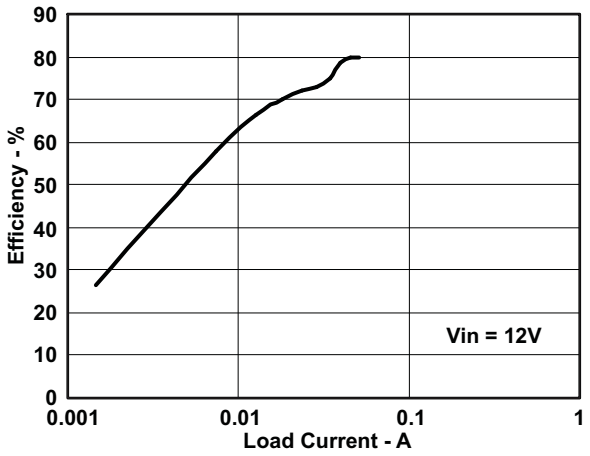

Figure 3. Light Load Efficiency vs Load Current

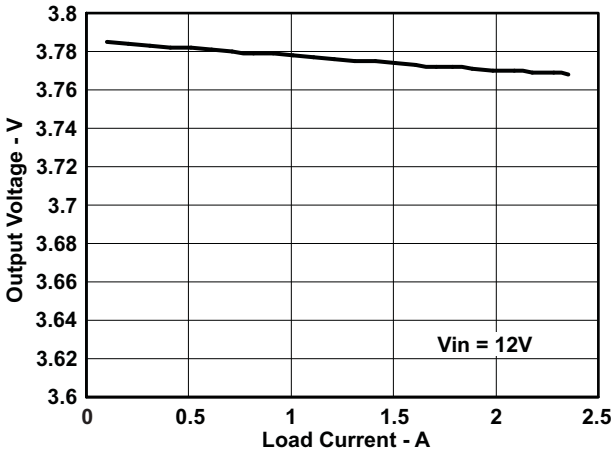

Figure 4. Output Voltage vs Load Current

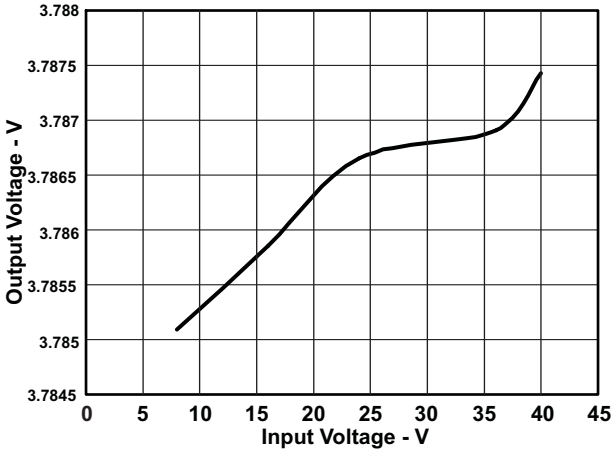

Figure 5. Output Voltage vs Input Voltage

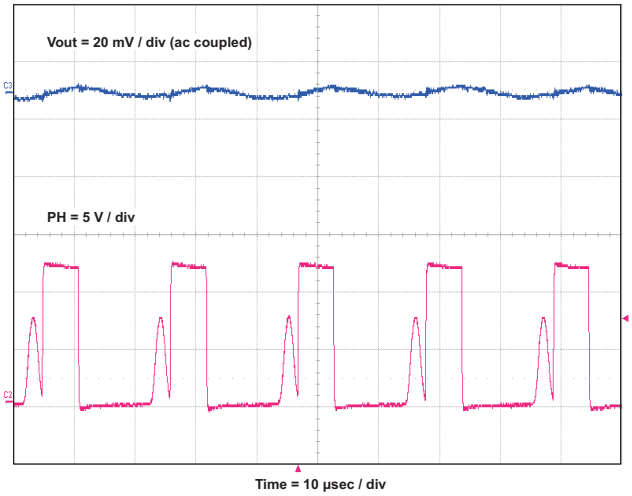

Figure 6. Output Voltage Ripple at DCM

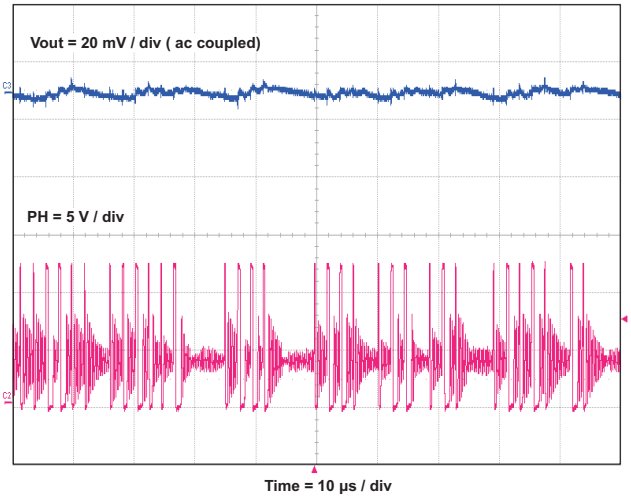

Figure 7. Output Voltage Ripple at PSM

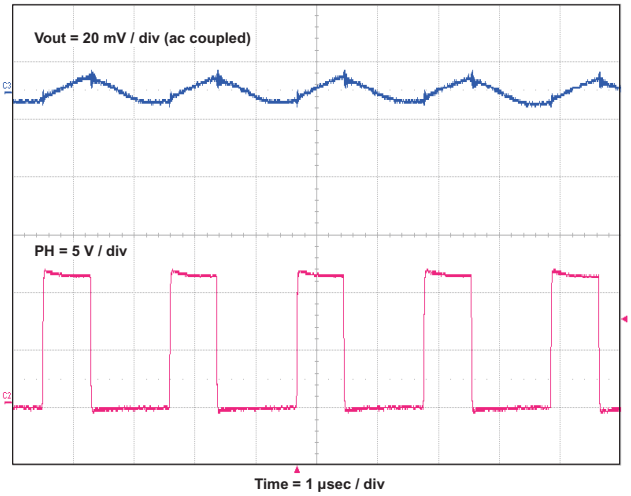

Figure 8. Output Voltage Ripple, Iout = 2.5 A

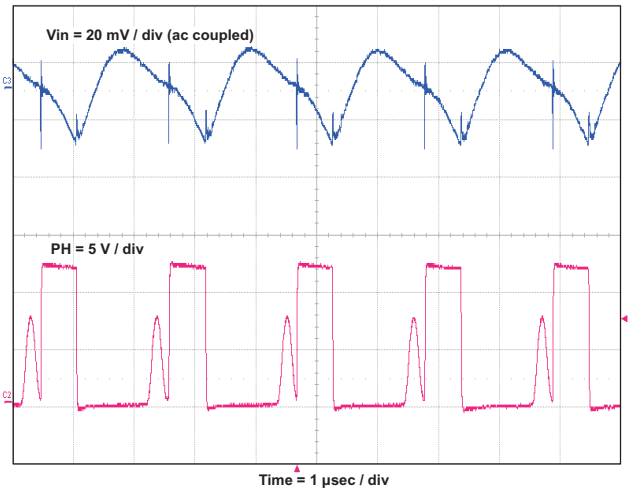

Figure 9. Input Voltage Ripple at DCM

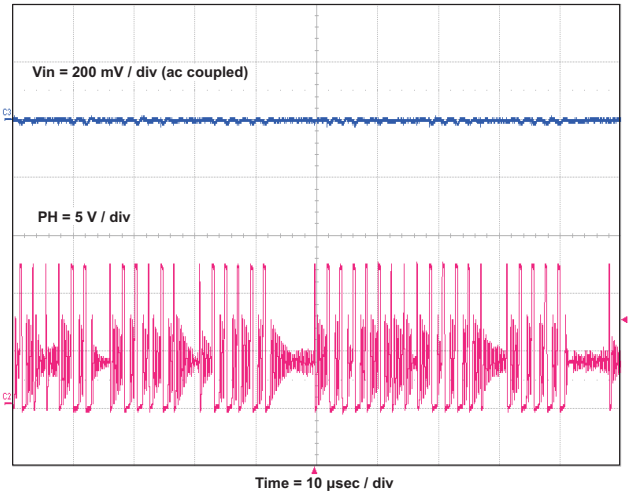

Figure 10. Input Voltage Ripple at PSM

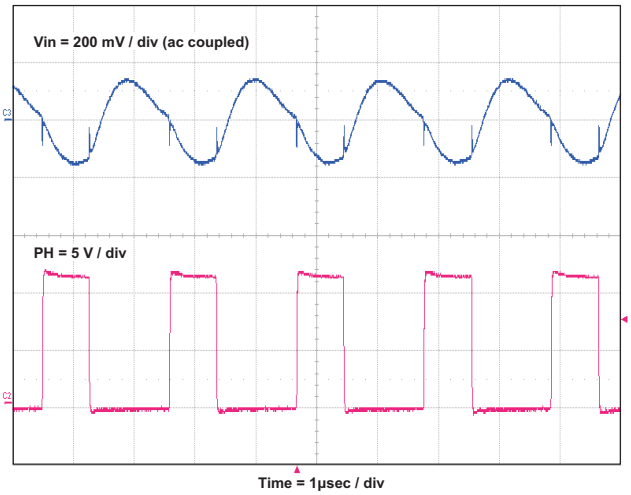

Figure 11. Input Voltage Ripple, Iout = 2.5 A

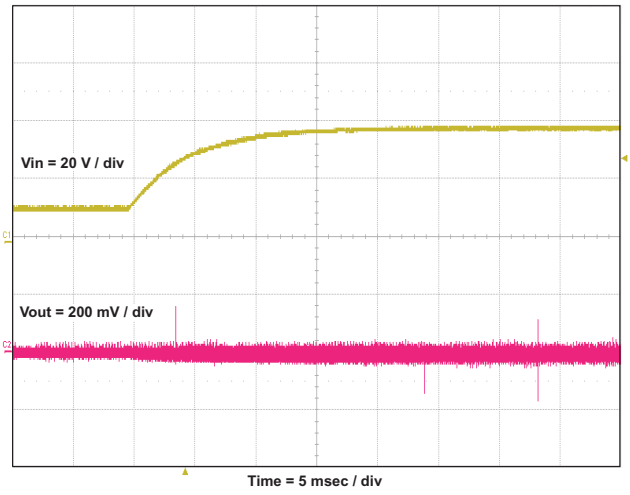

Figure 12. Line Transient, Vin step 8V-40V

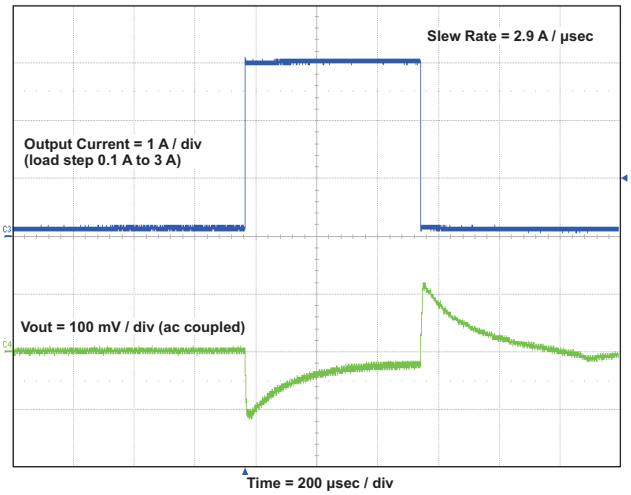

Figure 13. Load Transient 0.1 to 3A Step

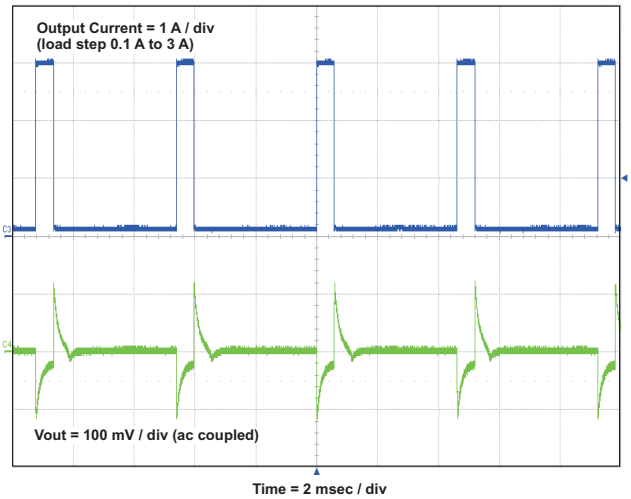

Figure 14. Load Transient 0.1 to 3A Multiple Steps

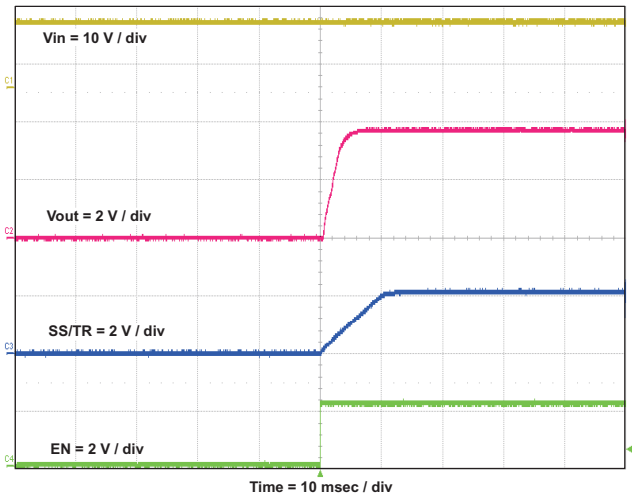

Figure 15. Startup Relative to EN

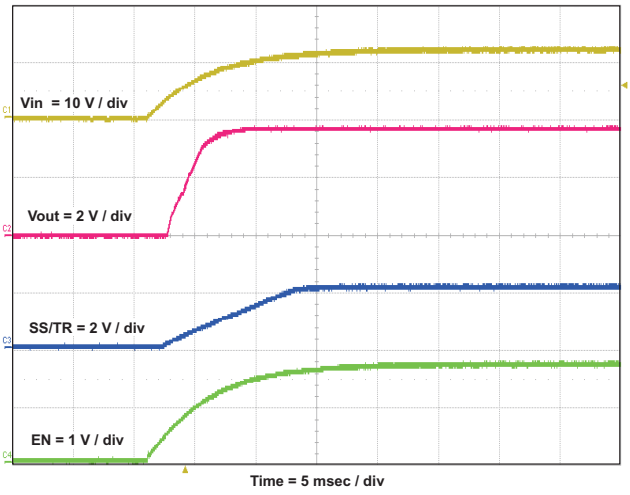

Figure 16. Startup Relative to VIn

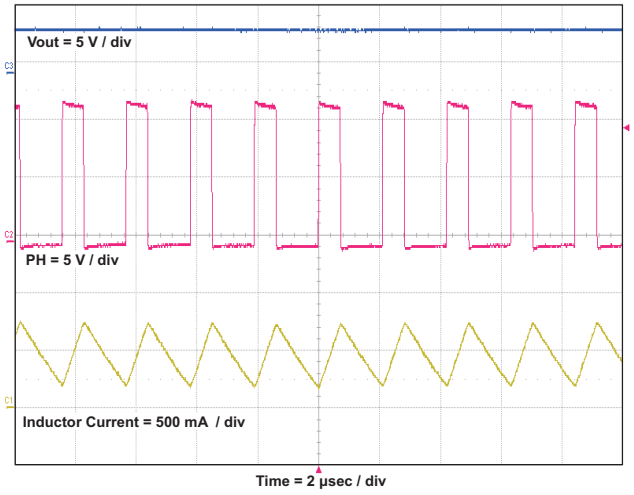

Figure 17. Vout, Inductor Current and PH, CCM

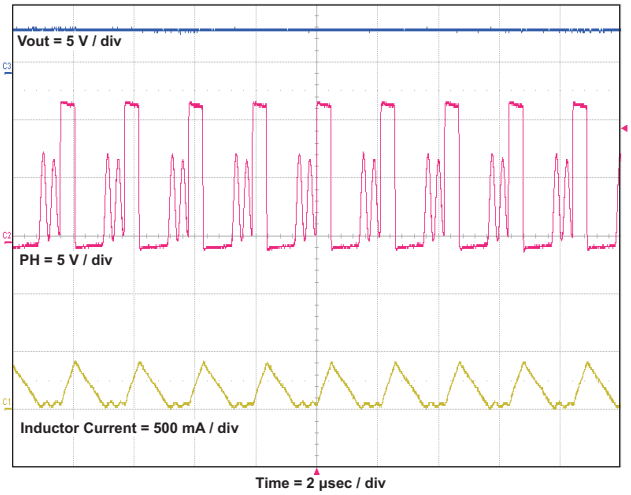

Figure 18. Vout, Inductor Current and PH, DCM

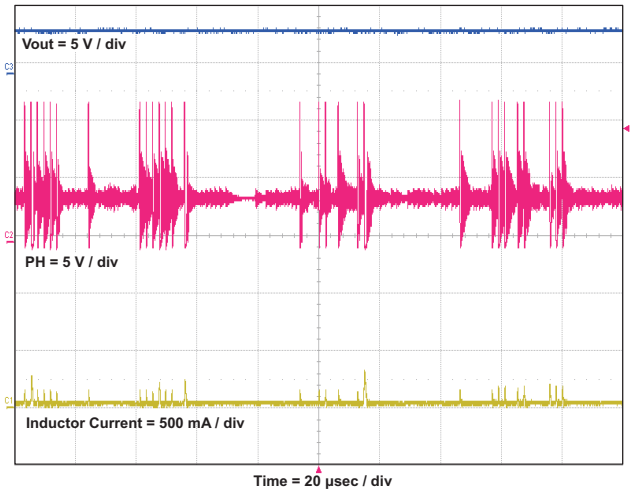

Figure 19. Vout, Inductor Current and PH, Skip Mode

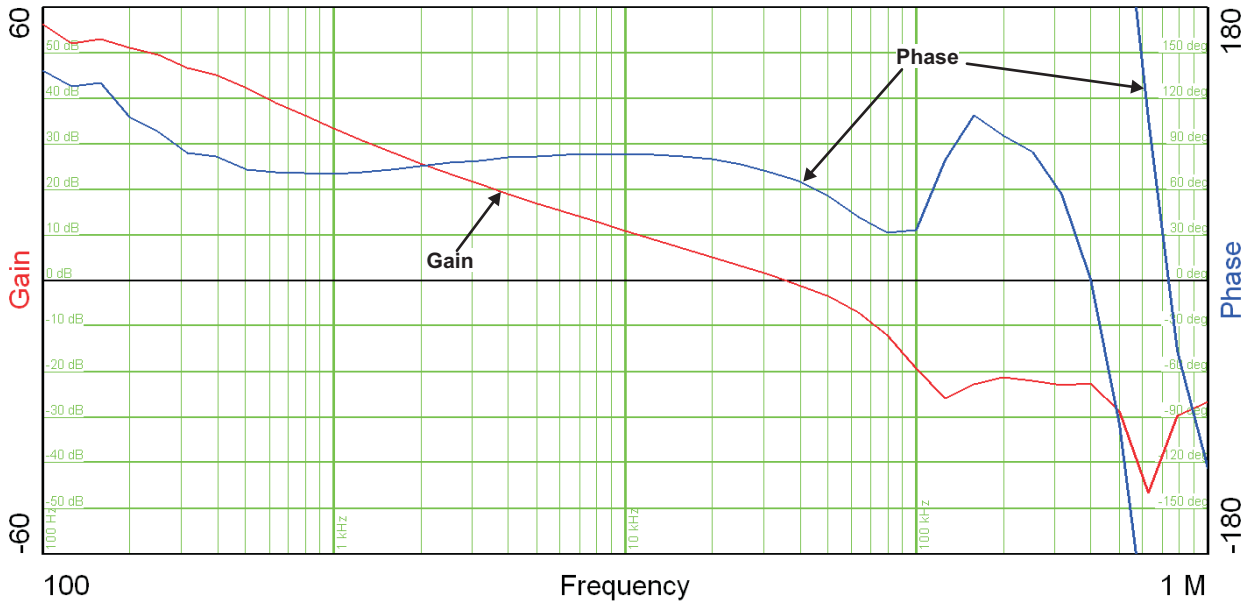

Figure 20. Overall Loop Frequency Response

3 Board Layout for Design – 1

This section provides a description of the board layout and layer illustrations. The board layout for the reference designs is shown in Figure 21 through Figure 23. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for VIN, VOUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54260 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including six vias directly under the TPS54260 device to provide a thermal path from the top-side ground area to the bottom-side ground plane. The input decoupling capacitors (C2 and C3) and bootstrap capacitor (C1) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper VOUT trace past the output capacitors (C4 incase of 4.2 V design and C4, C5, and C9 in case of 3.8 V design). For the TPS54260, an additional input bulk capacitor may be required (C1), depending on the EVM connection to the input supply.

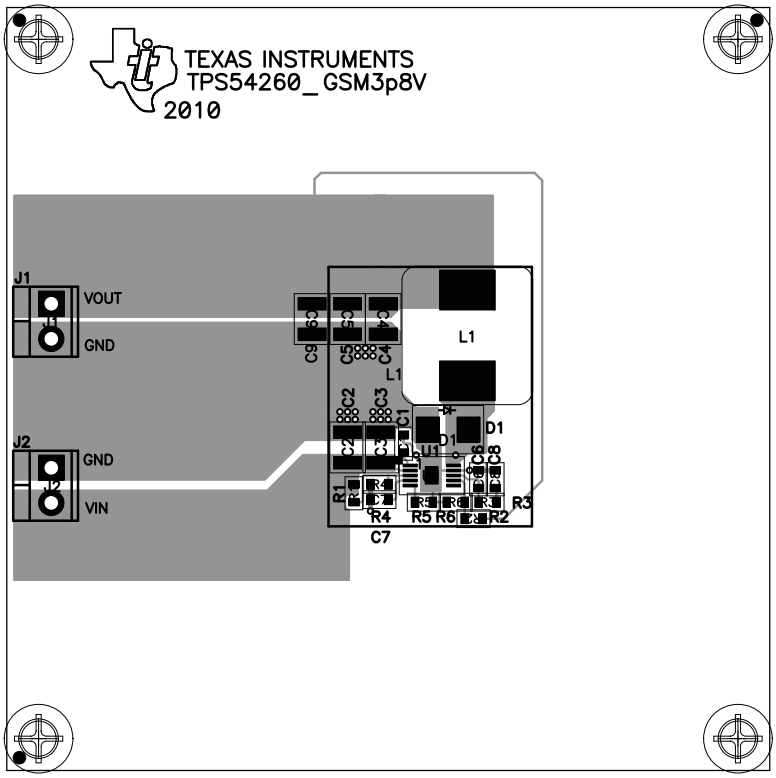

Figure 21. TPS54260_GSM3p8V Top-side Assembly

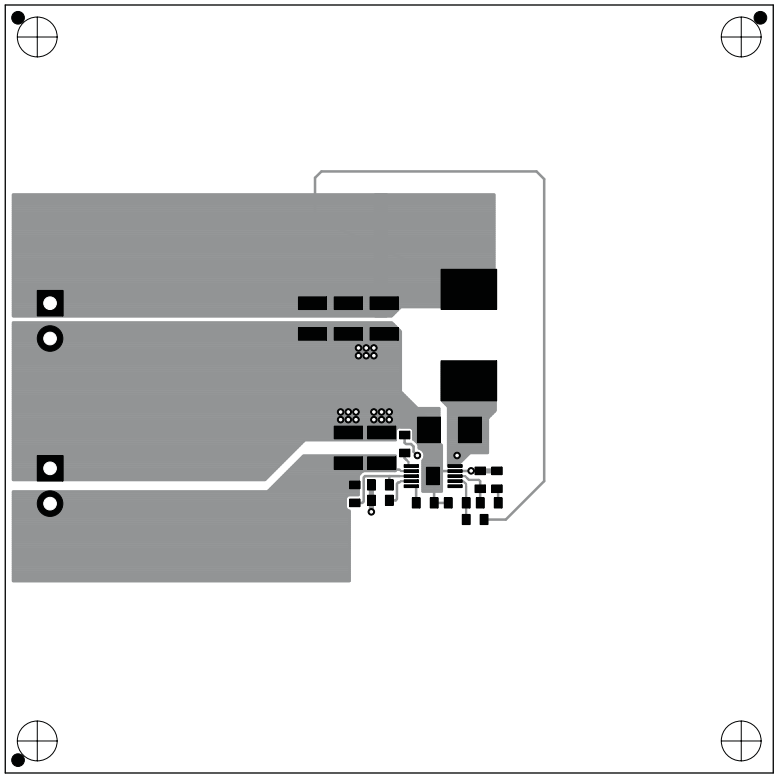

Figure 22. TPS54260_GSM3p8V Top-side Layout

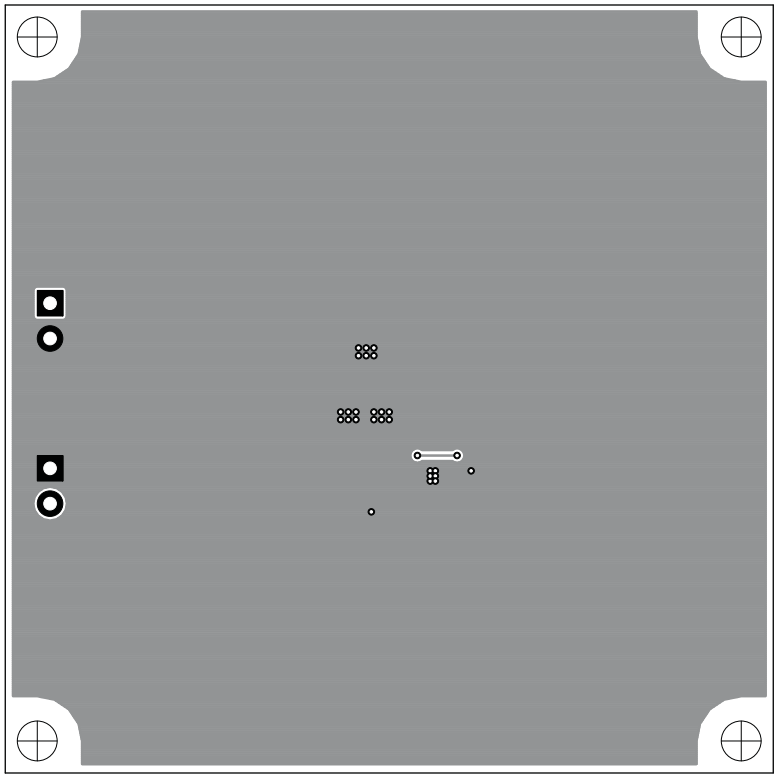

Figure 23. TPS54260_GSM3p8V Bottom-side layout

Table 1. Bill of Materials for Design – 1

Count	RefDes	Value	Description	Size	Part Number
1	C1	0.1uF	Capacitor, Ceramic, 10V, X5R	0603	Std
2	C2, C3	2.2uF	Capacitor, Ceramic, 100V, X5R	1210	Std
3	C4, C5, C9	47uF	Capacitor, Ceramic, 10V, X5R	1210	Std
1	C6	15pF	Capacitor, Ceramic, 25V, NPO, 5%	0603	Std
1	C7	0.01uF	Capacitor, Ceramic, 25V, X5R, 20%	0603	Std
1	C8	3300pF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std
1	D1	B360	Diode, Schottky, 1A, 60V	SMB	B160
2	J1, J2	ED1514	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED1514
1	L1	10uH	MSS1260-103 Inductor, Power, 7.4A, 21milliohm	0.484 x 0.484 inch	MSS1260-103_
1	R1	124k	Resistor, Chip, 1/16W, 1%	0603	Std
1	R2	37.4k	Resistor, Chip, 1/16W, 1%	0603	Std
1	R3	45.3k	Resistor, Chip, 1/16W, 1%	0603	Std
1	R4	30.1k	Resistor, Chip, 1/16W, 1%	0603	Std
1	R5	237k	Resistor, Chip, 1/16W, 1%	0603	Std
1	R6	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std
1	U1	TPS54260DGQ	IC, DC-DC Converter, 3.3V, 2.5A	MSOP-10	TPS54260DGQ

4 Design – 2 Specifications

Using a similar method, Design – 2 is achieved with the following specifications.

Output Voltage	4.2 V
Transient Response 0 to 3A load step	ΔVout = 3 %
Output Current	2.5 A (DC)
Transient Current	0.1 A to 3 A GSM Pulse
Input Voltage	24 V nom. 18 V to 60 V
Output Voltage Ripple	1% of Vout
Start Input Voltage (rising VIN)	17V
Stop Input Voltage (falling VIN)	16V

The schematic and experimental results for the same are shown below:

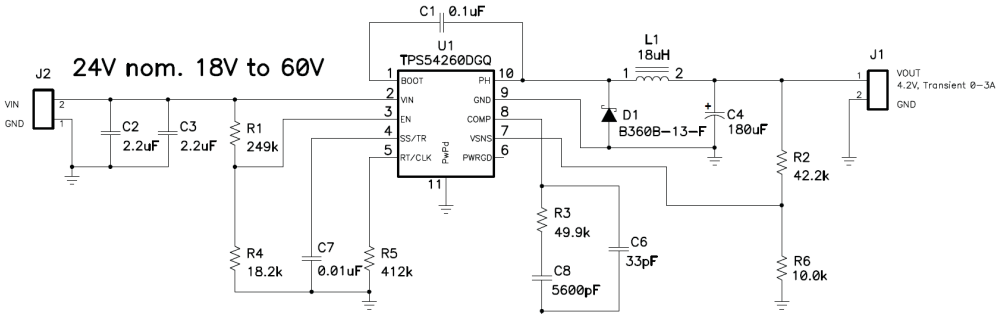

Figure 24. 4.2V Output TPS54260 Design Example

4.1 Experimental Results Design – 2

Figure 25 to Figure 43 show the experimental test results of the Figure 24 design.

The discontinuous conduction mode (DCM) to continuous conduction mode (CCM) boundary is at an output current of 269mA. The pulse skip mode (PSM) boundary is at an output current of 19mA. The input current draw at no load at 24V input voltage is 0.259mA.

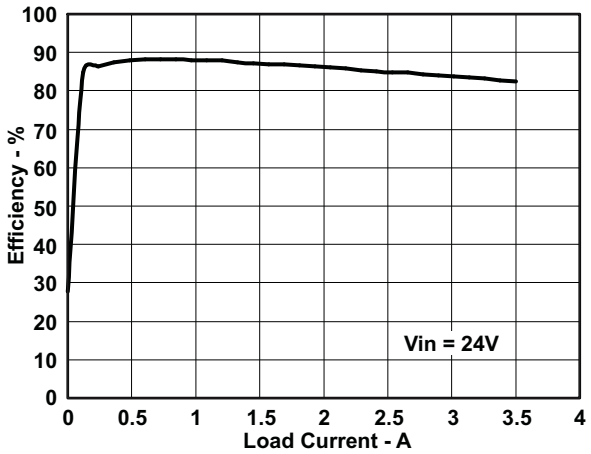

Figure 25. Efficiency vs Load Current

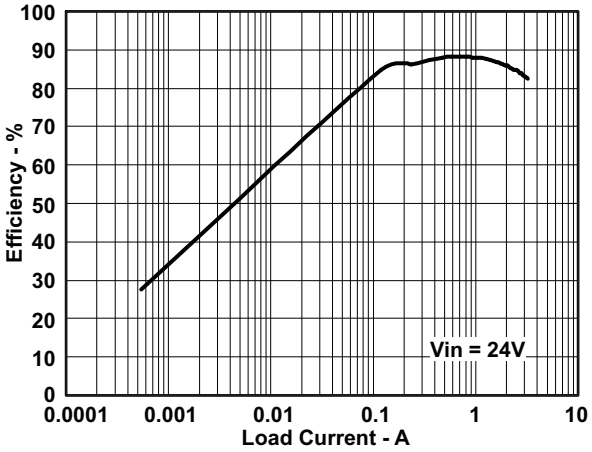

Figure 26. Light Load Efficiency vs Load Current

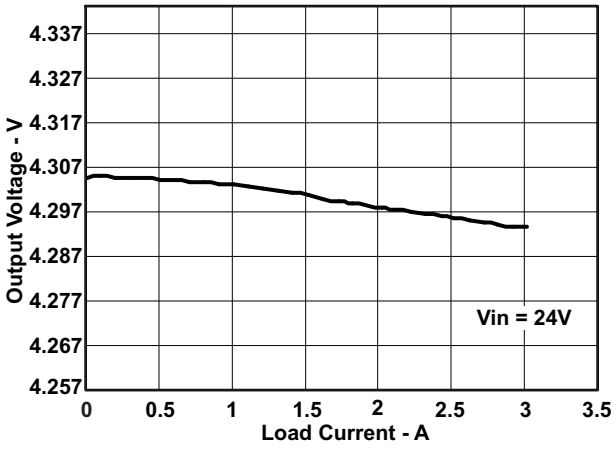

Figure 27. Output Voltage vs Output Current

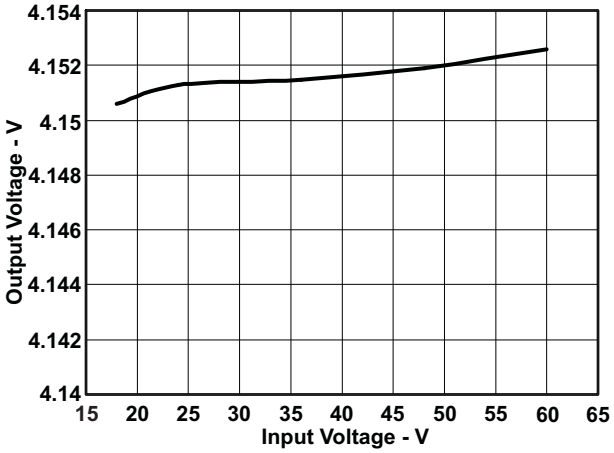

Figure 28. Output Voltage vs Input Voltage

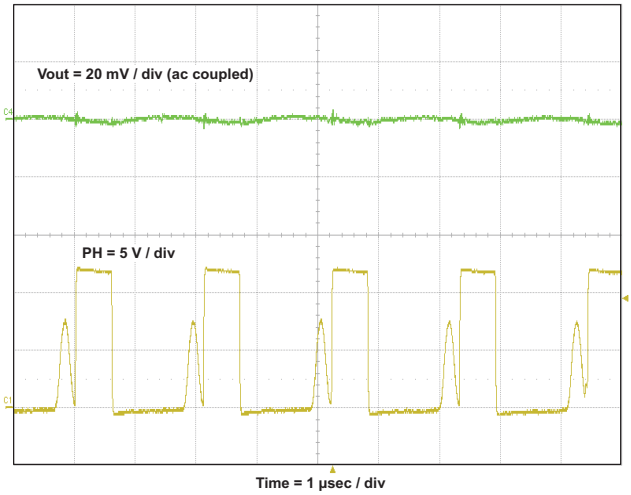

Figure 29. Output Voltage Ripple at DCM

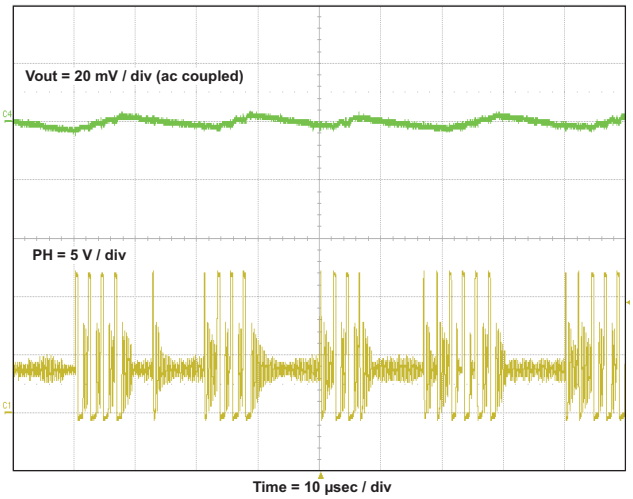

Figure 30. Output Voltage Ripple at PSM

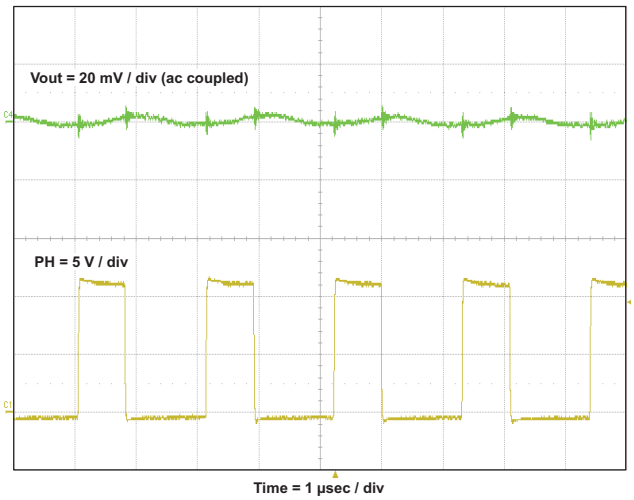

Figure 31. Output Voltage Ripple at 2.5 A

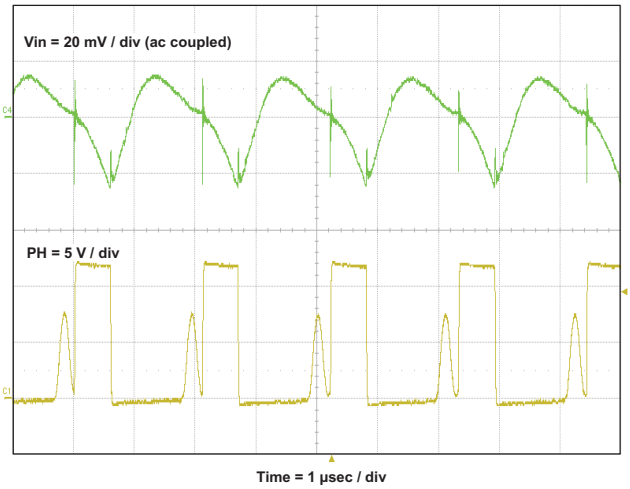

Figure 32. Input Voltage Ripple at DCM

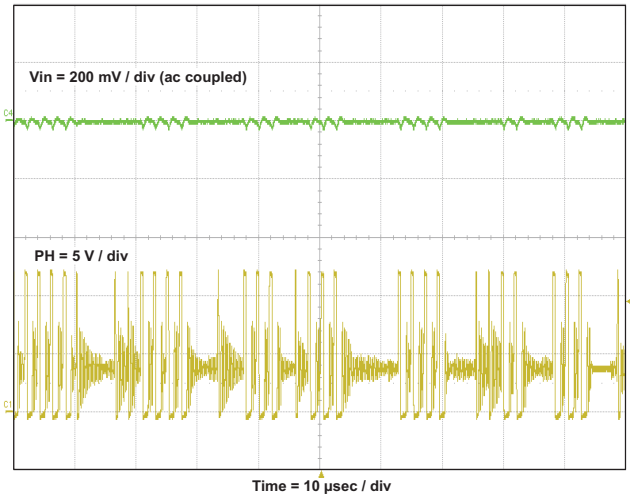

Figure 33. Input Voltage Ripple at PSM

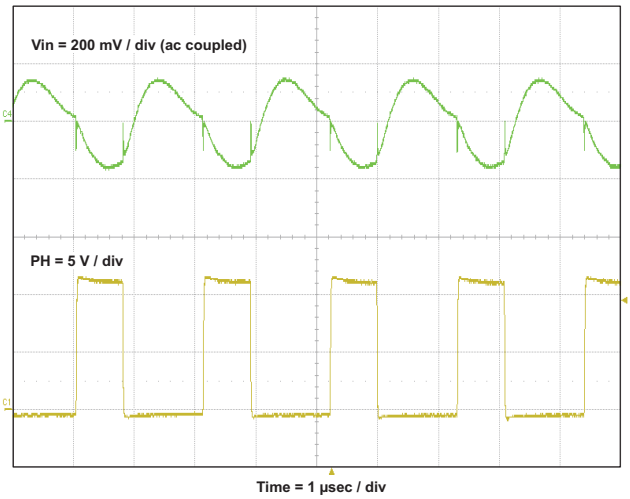

Figure 34. Input Voltage Ripple at 2.5 A

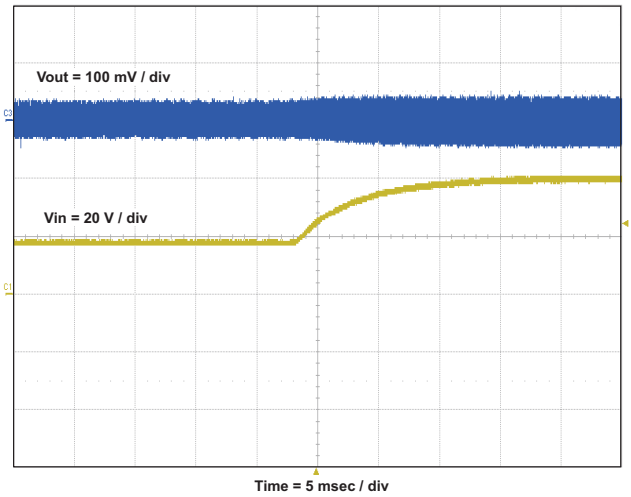

Figure 35. Line Transient, Vin Step 8 v – 40 V

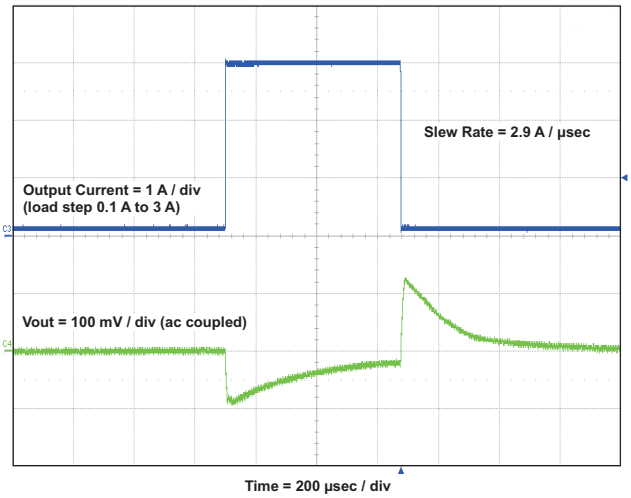

Figure 36. Load Transient, 0.1 to 3 A Step

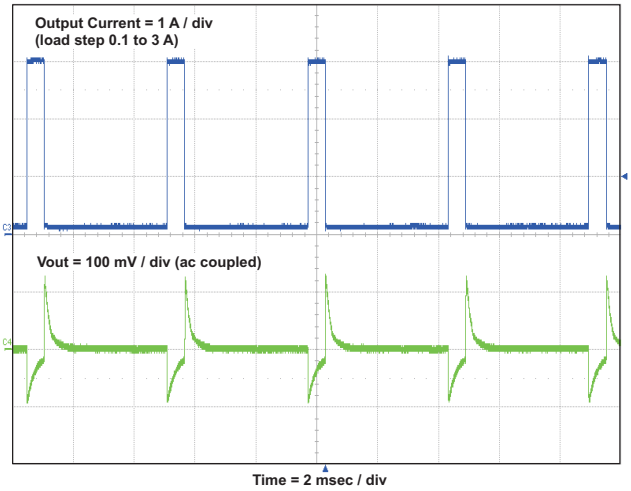

Figure 37. Load Transient, 0.1 to 3 A Multiple Steps

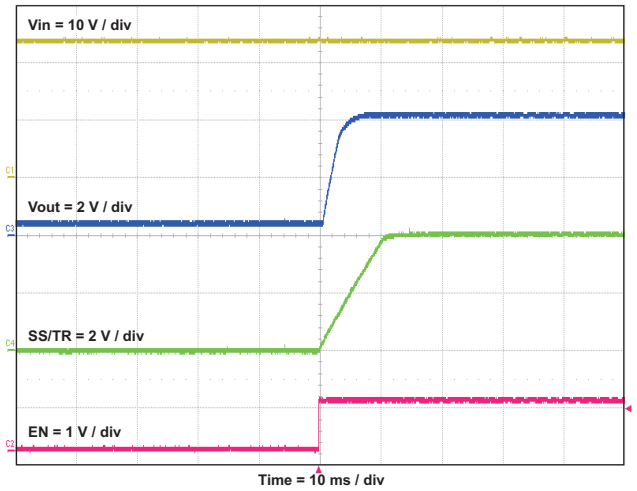

Figure 38. Startup Relative to EN

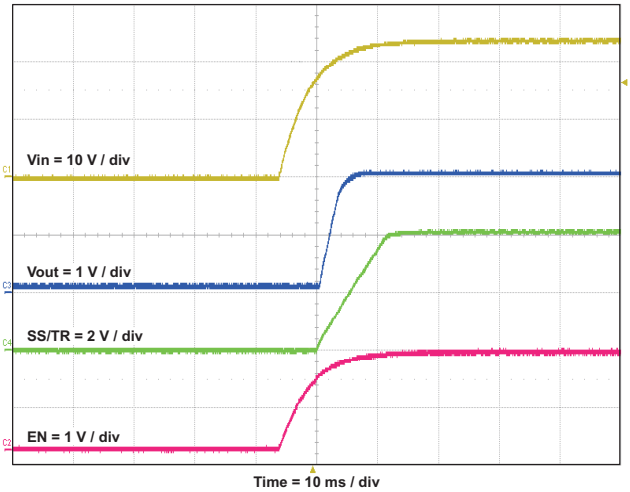

Figure 39. Startup Relative to Vin

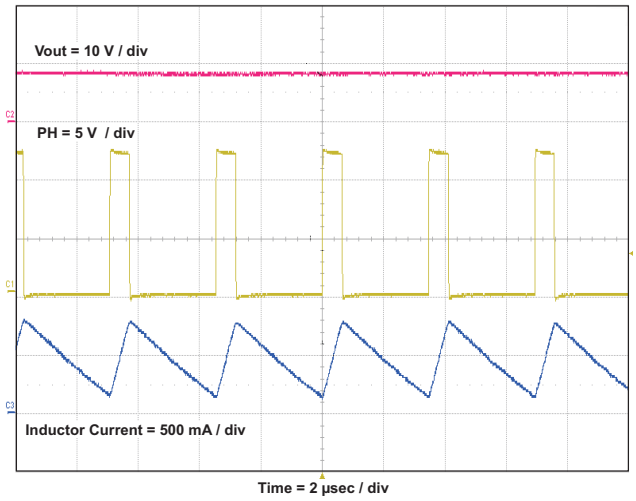

Figure 40. Vout, Inductor Current and PH, CCM

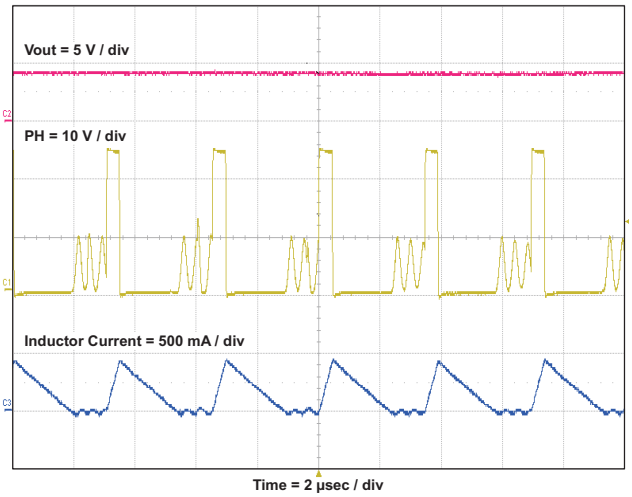

Figure 41. Vout, Inductor Curent and PH, DCM

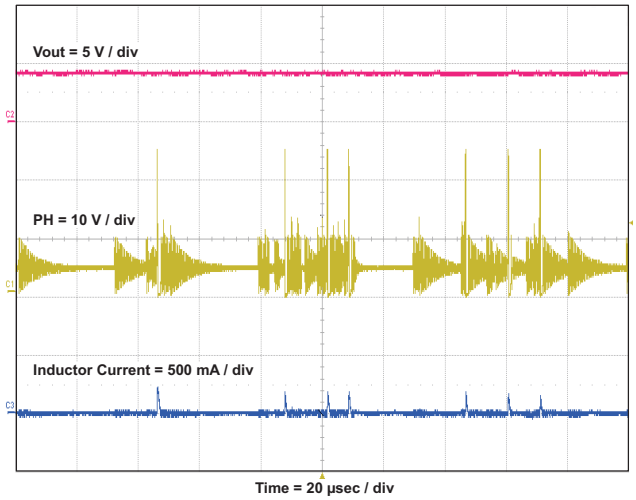

Figure 42. Vout, Inductor Current and PH, PSM

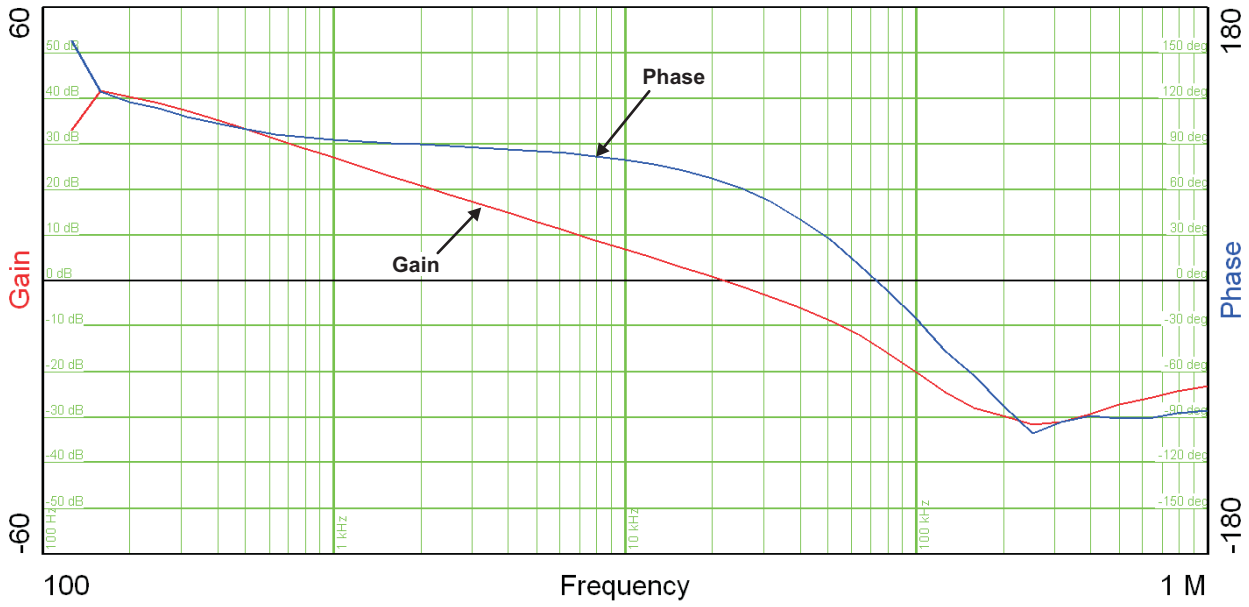

Figure 43. Overall Loop Frequency Response

5 Board Layout for Design – 2

This section provides a description of the board layout and layer illustrations. The board layout for the reference designs is shown in Figure 44 through Figure 46. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for VIN, VOUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54260 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including six vias directly under the TPS54260 device to provide a thermal path from the top-side ground area to the bottom-side ground plane. The input decoupling capacitors (C2 and C3) and bootstrap capacitor (C1) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper VOUT trace past the output capacitors (C4 incase of 4.2 V design and C4, C5, and C9 in case of 3.8 V design). For the TPS54260, an additional input bulk capacitor may be required (C1), depending on the EVM connection to the input supply.

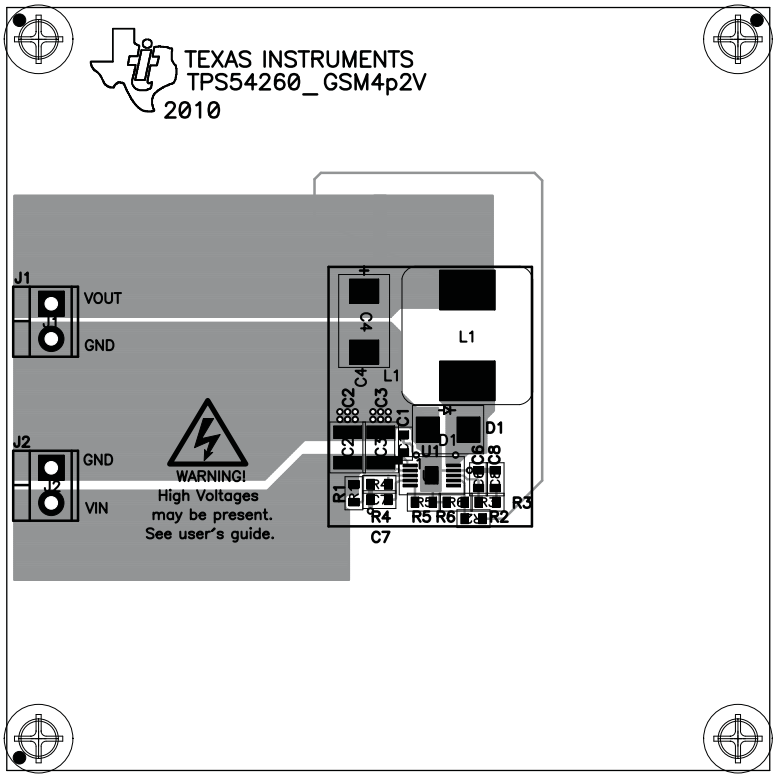

Figure 44. TPS54260_GSM4p2V Top-side Assembly

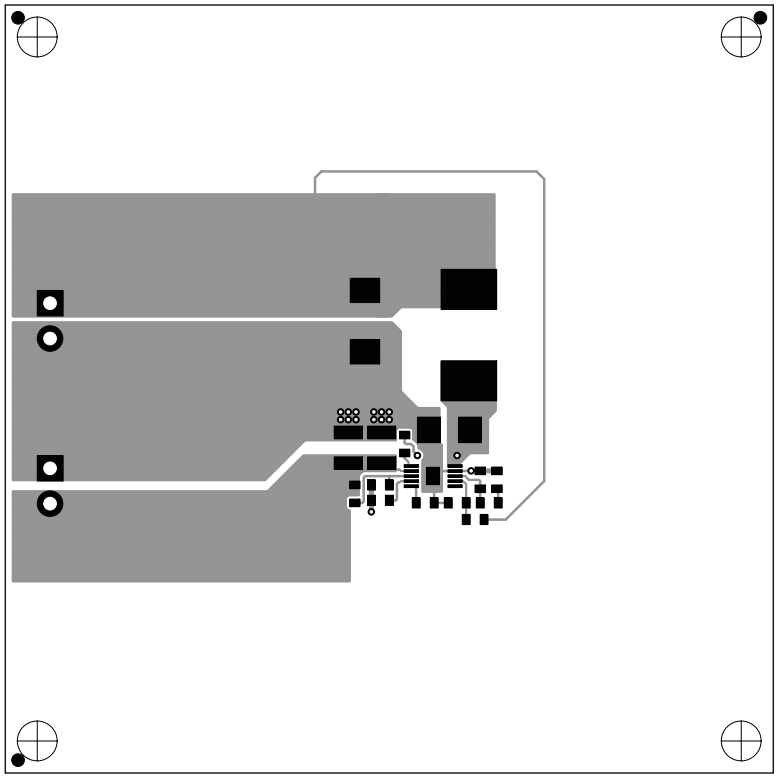

Figure 45. TPS54260_GSM4p2V Top-side Layout

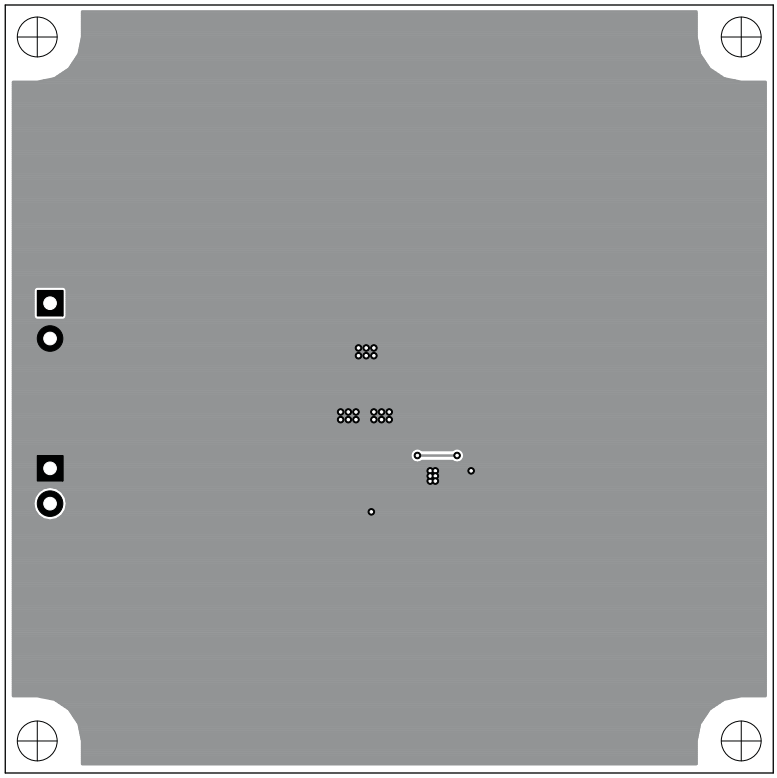

Figure 46. TPS54260_GSM4p2V Bottom-side Layout

Table 2. Bill of Materials for Design – 2

Count	RefDes	Value	Description	Size	Part Number
1	C1	0.1uF	Capacitor, Ceramic, 10V, X5R	0603	Std
2	C2, C3	2.2uF	Capacitor, Ceramic, 100V, X5R	1210	Std
1	C4	180uF	Capacitor, Ceramic, 10V, X5R	1210	Std
1	C6	33pF	Capacitor, Ceramic, 25V, NPO, 5%	0603	Std
1	C7	0.01uF	Capacitor, Ceramic, 25V, X5R, 20%	0603	Std
1	C8	5.6nF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std
1	D1	B360	Diode, Schottky, 1A, 60V	SMB	B160
2	J1, J2	ED1514	Terminal Block, 2-pin, 6-A, 3.5mm MSS1260-183	0.27 x 0.25""	ED1514
1	L1	18uH	Inductor, Power, 5.62 A, 35milliohm	0.484 x 0.484 inch	MSS1260-183_
1	R1	249kΩ	Resistor, Chip, 1/16W, 1%	0603	Std
1	R2	42.2kΩ	Resistor, Chip, 1/16W, 1%	0603	Std
1	R3	49.9kΩ	Resistor, Chip, 1/16W, 1%	0603	Std
1	R4	18.2KΩ	Resistor, Chip, 1/16W, 1%	0603	Std
1	R5	412kΩ	Resistor, Chip, 1/16W, 1%	0603	Std
1	R6	10.0kΩ	Resistor, Chip, 1/16W, 1%	0603	Std
1	U1	TPS54260DGQ	IC, DC-DC Converter, 3.3V, 2.5A	MSOP-10	TPS54260DGQ

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