Application Report
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Isolated Continuous Conduction Mode Flyback Using the TPS55340

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ABSTRACT

Some systems require an auxiliary supply with galvanic isolation between the input power source and output load. This may be a requirement to meet safety ratings such as those defined by UL or the IEC, or to provide a bias supply referenced to a high potential rail. A boost converter with an integrated low-side FET can be used in a flyback topology to make a small solution size isolated power supply. The TPS55340 includes an integrated 40-V, 5-A low-side MOSFET switch for boost, SEPIC or flyback applications. This example design demonstrates the TPS55340 in a flyback topology. An opto-coupler provides feedback to the primary side for highest performance.

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1 Design Specifications

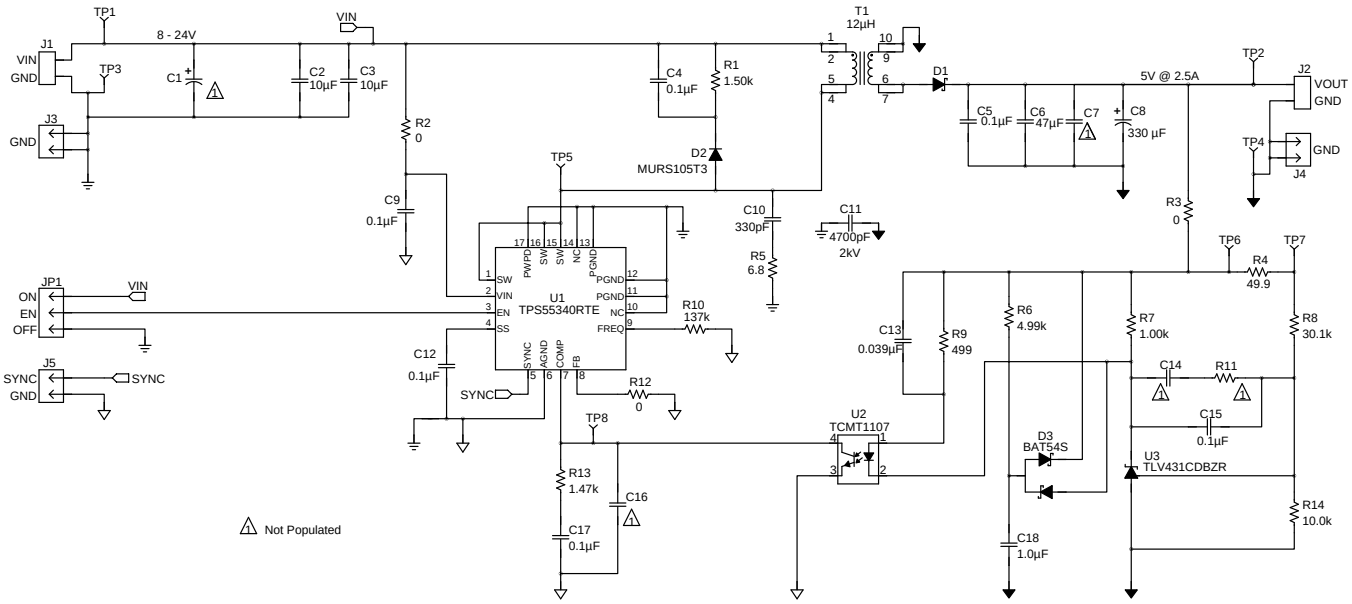

Figure 1. Reference Design Schematic

Table 1. Reference Design Performance Specifications

Parameter	Conditions	MIN	TYP	MAX	Units
Input Characteristics					
Input Voltage Range, V_{IN}		8	12	24	V
Switching Frequency, f_{SW}			350		kHz
Output Characteristics					
Output Voltage, V_{OUT}			5		V
Output Current, I_{OUT}		0		2.5	A
Output Voltage Ripple, V_{RIPPLE}	V_{IN} = 8 V, I_{OUT} = 2.5 A		100		mVpp
Conservative Efficiency Estimate, η_{EST}	V_{IN} = 8 V, I_{OUT} = 2.5 A	80%			
Load Step, ΔI_{STEP}			1.25		A
Transient V_{OUT} Deviation, ΔV_{OUT}			200		mV
Isolation Voltage		1500			V

Table 1 gives the performance specification of the example design presented. Figure 1 shows the final application schematic. A CCM flyback was selected for this application for improved efficiency, reduced component stress and reduced filter size. A flyback operated in CCM reduces peak currents, RMS currents, and MOSFET turn-off loss. However the main disadvantage of a CCM flyback is the lower control loop bandwidth required to compensate for the presence of a right-half plane zero (RHPZ).

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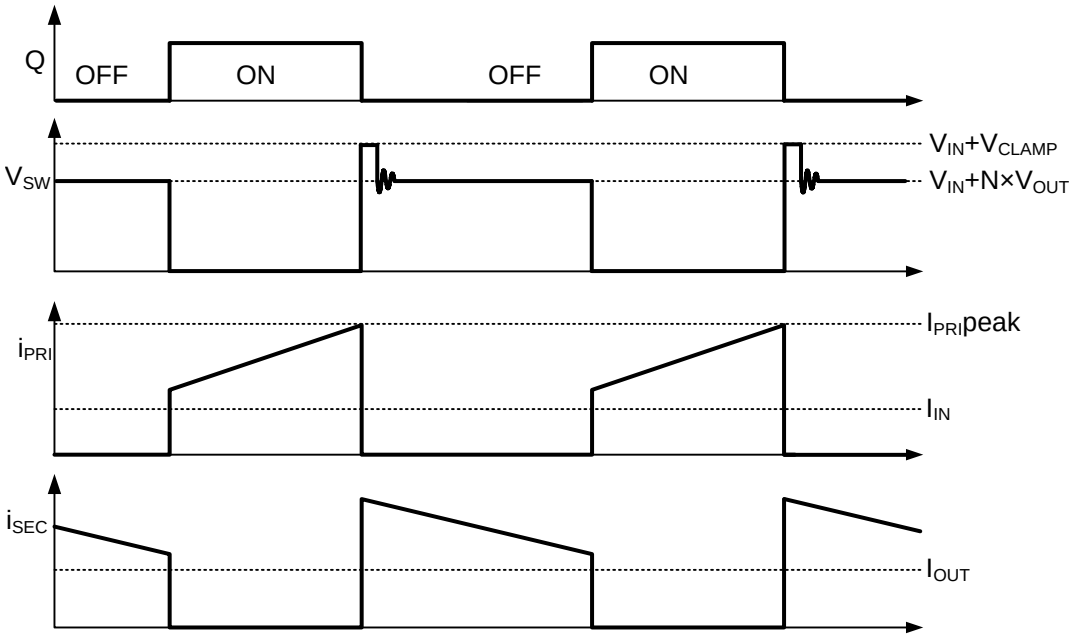

Figure 2. CCM Flyback Voltage and Current Waveforms

Figure 2 shows the current and voltage waveforms of a CCM flyback during the on-time and off-time of the internal switch (Q). While the switch is turned on, the input voltage is applied across the transformer primary winding energizing the transformer inductance. When Q is turned off, the drain to source voltage flies high due to primary leakage inductance and is clamped at V_{IN} + V_{CLAMP} by an external clamp circuit. The energy stored in the transformer during the on-time of the switch is delivered to the load by the secondary winding during the switch off time.

2 Calculations and Component Selection

2.1 Switching Frequency (R10)

The first step in the design process is to choose a switching frequency for the power supply. As with any switching regulator, the tradeoff is between higher efficiency and smaller solution size. High switching frequencies allow for lower primary inductance and smaller output capacitors reducing solution size when compared to a converter switching at a lower frequency. However, higher switching frequency increases switching losses hurting the converter's efficiency and thermal performance.

The efficiency of a flyback converter is particularly sensitive to switching frequency. Due to leakage inductance in the transformer, not all energy is transferred from the primary winding to the secondary winding. When the switch is turned off, a large voltage overshoot on the SW pin must be clamped below the drain to source the voltage rating of the internal 40-V MOSFET. The effect of the clamp when the switch turns off is shown in the V_{SW} waveform in Figure 1. The clamping circuit limits V_{SW} to the voltage V_{IN} + V_{CLAMP}. The clamping circuit absorbs the leakage inductance energy during each switching period. Therefore, a higher switching frequency increases the power lost to the primary-side voltage clamp. A switching frequency of 350 kHz near the low end of the TPS55340 operating range is chosen.

Designs operating below 300 kHz may experience a collapsed output condition if the switch peak current reaches the overcurrent limit threshold. The collapsed output condition is associated with frequency fold-back overload protection. When current limit is exceeded, the device enters frequency fold-back and the switching frequency reduces to ¼ the nominal value set by R_{FREQ}. At switching frequencies less than 75 kHz, the peak current limit threshold of the device also decreases. The output voltage must return to regulation before the switching frequency returns to the pre-set value. However, with the reduced current

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limit threshold, the output voltage will remain below the regulation level until the load current is reduced. The converter can be restarted from this overload condition by cycling the input power, cycling the EN pin or removing the output load. The resistance required to set the switching frequency is calculated with Equation 1 from the product data sheet. For a 350-kHz switching frequency, the calculated resistance is 137.8 kΩ. The nearest standard value of 137 kΩ is used.

$$R_{FREQ}(k\Omega) = 57500 \times f_{SW}(kHz)^{-1.03} = 57500 \times 350(kHz)^{-1.03} = 137.8k\Omega \quad (1)$$

2.2 Transformer - Turns Ratio and CCM Duty Cycle

When designing a flyback the most important component is the transformer. Typically the first specification selected is the turns ratio. The turns ratio is chosen to limit the duty cycle to a maximum of 50% (Dlim). There are two reasons to do this. First, it reduces stress on the rectifying diode and output capacitors. Second, it avoids the possibility of sub-harmonic oscillation inherent to current mode control. The TPS55340 provides internal slope compensation and can be stable with duty cycles greater than 50%. The maximum primary to secondary turns ratio (Np2s) is calculated with Equation 2. This includes an estimated 0.5 V drop of the rectifying diode (V_D).

$$Np2s = \frac{V_{IN}\min \times Dlim}{(V_{OUT} + V_D) \times (1 - Dlim)} = \frac{8V \times 0.5}{(5V + 0.5V) \times (1 - 0.5)} = 1.45 \quad (2)$$

The calculated maximum Np2s is 1.45. The transformer used in the example has 12 primary turns and 10 secondary turns giving an Np2s of 1.2. After selecting the turn's ratio it should be verified the 40-V internal MOSFET of the TPS55340 is sufficient for the voltage stress in the design. In a flyback topology the drain-to-source voltage across the low-side MOSFET is the input voltage plus the output voltage reflected to the transformer primary. At least a 20% margin is recommended to account for voltage overshoot due to the leakage inductance of the transformer and any ringing caused by PCB parasitics. The voltage stress on the MOSFET is calculated with Equation 3 where the 0.8 factor in the denominator provides the 20% voltage margin. With the selected turns ratio the estimated voltage stress on the MOSFET is 38.2 V.

$$V_{FET} = \frac{V_{IN}\max + (V_{OUT} + V_D) \times Np2s}{0.8} = \frac{24V + (5V + 0.5V) \times 1.2}{0.8} = 38.2V \quad (3)$$

After selecting the turns ratio, the duty cycle in CCM can be estimated with Equation 4. This includes the forward voltage drop of the rectifying diode. With the minimum input voltage (V_{IN} min), Dmax equals 45.2% and with the maximum input voltage (V_{IN}max), Dmin equals 21.6%.

$$D_{CCM} = \frac{(V_{OUT} + V_D) \times Np2s}{V_{IN} + (V_{OUT} + V_D) \times Np2s} = \frac{(5V + 0.5V) \times 1.2}{8V + (5V + 0.5V) \times 1.2} = 0.452 \quad (4)$$

2.3 Transformer - Primary Inductance

The desired primary inductance is the next important specification to select for the transformer. The two main concerns when specifying the inductance are the current ripple and the RHPZ. A higher inductance reduces the current ripple which can lower EMI and noise. However, larger inductance increases physical size and limits the bandwidth of the loop due to a lower frequency RHPZ. On the other hand, a lower inductance increases the current ripple, increasing EMI, noise and RMS currents while supporting a smaller solution size and faster control loop bandwidth.

One method to choose the inductance is to limit the current ripple to a percentage of the average current through the primary winding during the on time of the switch. A fair tradeoff between size and efficiency is achieved with a percent ripple (RIP%) between 60% and 90%. The average primary current is calculated using Equation 5. The recommended inductance is then calculated with Equation 6. Both equations are evaluated at the maximum input voltage when the peak to peak current ripple is greatest.

$$I_{RIPPLE} = RIP\% \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}\max \times D\min} = 0.6 \times \frac{5V \times 2.5A}{24V \times 0.216} = 1.45A \quad (5)$$

$$L_{PRI} = \frac{V_{IN}\max \times D\min}{I_{RIPPLE} \times f_{SW}} = \frac{24V \times 0.216}{1.45A \times 350kHz} = 10.2\mu H \quad (6)$$

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With a RIP% of 60%, the target I_{RIPPLE} is 1.45 A and the inductance is 10.2 µH. The selected primary inductance is 12 µH. Using this inductance with Equation 5 and Equation 6 produces a current ripple of 1.23 A. The RHPZ frequency is estimated with Equation 7 ignoring the resistance of the windings. This is evaluated when the frequency of the RHPZ is lowest, at the minimum input voltage and the maximum output current. For a stable design it is recommended to limit the loop bandwidth (f_{BW}) at the minimum input voltage to 1/3 the RHPZ frequency. The RHPZ is calculated at 25.4 kHz and the maximum recommended loop bandwidth is 8.5 kHz.

$$f_{RHPZ} = \frac{\frac{V_{OUT}}{I_{OUT}} \times (1 - Dmax)^2}{2\pi \times \frac{L_{PRI}}{Np2s^2} \times Dmax} = \frac{\frac{5V}{2.5A} \times (1 - 0.452)^2}{2\pi \times \frac{12\mu H}{1.2^2} \times 0.452} = 25.4kHz \tag{7}$$

With the primary inductance selected the maximum output current is estimated based on the current ripple and estimated efficiency using Equation 8. The maximum output current is estimated at 2.79 A.

$$I_{OUT}\,max = \left(I_{LIM}\,min - \frac{I_{RIPPLE}}{2}\right) \times \frac{V_{IN}\,min \times Dmax \times \eta_{EST}}{V_{OUT}} = \left(5.25A - \frac{1.23A}{2}\right) \times \frac{8V \times 0.452 \times 80\%}{5V} = 2.79A \tag{8}$$

In a flyback topology the supply enters DCM when all power stored in the transformer during the on-time of the switch is transferred to the load before the end of the switching period, leaving no residual energy in the transformer. The current at which CCM operation begins is estimated with Equation 9. This estimation is typically high because efficiency is not included. The critical current to enter DCM is estimated at 310 mA with an 8-V input voltage and 640 mA with a 24-V input voltage. Lastly the DCM duty cycle is estimated with Equation 10. This shows the dependence on the switching frequency, primary inductance and output current.

$$I_{OUT}crit = \frac{V_{IN}^2 \times D_{CCM}^2}{2 \times L_{PRI} \times f_{SW} \times V_{OUT}} = \frac{8V^2 \times 0.452^2}{2 \times 12\mu H \times 350kHz \times 5V} = 310mA \tag{9}$$

$$D_{DCM} = \sqrt{\frac{2 \times I_{OUT} \times f_{SW} \times L_{PRI} \times (V_{OUT} + V_D)}{V_{IN}\,min^2}} \tag{10}$$

2.4 Transformer - Ratings and Other Specifications

After selecting the inductance and turns ratio some other necessary ratings for the transformer must be specified. The most important is to minimize the leakage inductance. As mentioned previously, leakage inductance related to imperfect coupling between the primary and secondary windings causes power loss in the primary switch clamp circuit. A good rule is to target the leakage inductance below 2% the selected primary inductance.

The saturation current rating of the transformer must also be specified. Magnetics vendors typically describe this as the current in primary winding when the primary inductance decreases to 20% of the nominal value. Conservative designs will use the 6.6-A typical peak current limit of the TPS55340 as the saturation current. The minimum recommended saturation current rating is 20% higher than the calculated peak current under full load. Equation 11 estimates the peak current. With the selected primary inductance in this design, the peak current is 4.75 A and the minimum recommended saturation current rating is 5.94 A.

$$I_{PRI}peak = \frac{V_{OUT} \times I_{OUT}}{V_{IN}\,min \times Dmax \times \eta_{EST}} + \frac{I_{RIPPLE}}{2} = \frac{5V \times 2.5A}{8V \times 0.452 \times 80\%} + \frac{1.23A}{2} = 4.75A \tag{11}$$

The DC resistance (DCR) of the windings should also be minimized to reduce conduction power losses. The RMS current in the primary winding is estimated with Equation 12, the RMS current in the secondary winding with Equation 13 and the conduction power loss with Equation 14. In the example using V_{IN} of 8 V, the primary RMS current is 2.92 A and the secondary RMS current is 1.9 A.

$$I_{PRI}rms = \sqrt{D \times \left(\left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times D}\right)^2 + \frac{I_{RIPPLE}^2}{3}\right)} = \sqrt{0.452 \times \left(\left(\frac{5V \times 2.5A}{8V \times 0.452}\right)^2 + \frac{0.86A^2}{3}\right)} = 2.92A \tag{12}$$

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$$I_{SEC}rms = \sqrt{(1-D)\times\left(I_{OUT}^2 + \frac{(I_{RIPPLE}\times Np2s)^2}{3}\right)} = \sqrt{(1-0.452)\times\left(2.5A^2 + \frac{(0.86A\times 1.2)^2}{3}\right)} = 1.9A \quad (13)$$

$$P_T cond = I_{PRI}rms^2 \times DCR_{PRI} + I_{SEC}rms^2 \times DCR_{SEC} \quad (14)$$

Lastly, the transformer should be rated for the voltage isolation or safety requirements. Table 2 summarizes the target transformer specifications and the tested ratings of the custom transformer provided by CoilCraft® for this design.

Table 2. Reference Design Transformer Specifications

Specification Name	Design Values for Specifications	NA5889-AL Tested Ratings
Input Voltage Range (V)	8 – 24	
Output Voltage (V)	5	
Output Current (A)	2.5	
Operating Mode	CCM	
Duty Cycle Range (%)	21% to 45%	
Turns Ratio (N_{PRI}:N_{SEC})	1.2	1.2
Switching Frequency (kHz)	350	200
Primary Inductance (µH)	12	12
Leakage Inductance (µH)	.24	.179
Peak Current (A)	5.94 A	5% drop at 5.5 ADC
DCR		PRI = 25 mΩ, SEC = 16.5 mΩ
Insulation Requirements	Functional, Basic, Reinforced	
Regulatory Agencies/Specification	UL, IEC	
Dielectric Withstand Voltage	1500 V	1500 V

2.5 Resistor-Capacitor-Diode (RCD) Clamp (C4, D2, R1) and RC Snubber (C10, R5)

A primary switch RCD clamp is needed to limit the voltage on the SW pin and absorb energy stored in leakage inductance of the transformer. The clamp components were selected by first setting the capacitance of C4 to 0.1 µF. The capacitor is selected to limit voltage ripple in the RCD clamping circuit. The ripple is typically limited to 5%-10% of the clamp voltage. The resistance is then selected to set the voltage clamp level. It is recommended to start with a relatively low resistance for R1 of 1.0 kΩ for a lower clamp voltage. After testing the converter, the resistor may be increased to increase the clamping voltage and reduce power loss. D2 should be an ultra-fast, forward-recovery diode with short forward recovery time allowing the clamping circuit to activate as soon as possible. The selected MURS105T3G is rated at 25 ns. Overshoot that occurs during the diode turn on time can be clamped using an RC snubber. The snubber components are selected using SLVA255 and the values used are C10 = 330 pF, R5 = 6.8 Ω.

After the snubber is added, the resistance in the RCD clamp was tuned during bench testing. For best efficiency it is desired to have the highest allowable clamping voltage while still limiting the maximum voltage on the SW pin below the absolute max of the TPS55340. A larger resistance increases the clamping voltage and a smaller resistance decreases the clamping voltage. The target clamping voltage (V_{CLAMP}) is equal to the SW pin maximum operating rating of 38 V minus V_{IN} max which yields 14 V. In this design the final resistance used to meet this clamping voltage was R1 = 1.5 kΩ.

The components in both the RCD clamp and RC snubber must have the proper power ratings. The clamping voltage (V_{CLAMP}) varies with input voltage and is largest at the minimum input voltage. The capacitor and diode voltage rating should be at least V_{CLAMP}. The diode must be rated at least for the current through R_{CLAMP} of V_{CLAMP} / R_{CLAMP} = 8 mA and the primary peak current of 4.75 A. The power lost in the RCD resistor is estimated with Equation 15 to be 96 mW. The power lost in the RC snubber resistor (R_{SNUB}) is estimated with Equation 16 to be 92 mW. The voltage rating of the snubber capacitor (C_{SNUB}) is must be at least the 40 V maximum voltage at the SW.

$$P_{Rclamp} = \frac{V_{CLAMP}^2}{R1} = \frac{12V^2}{1.5k\Omega} = 96mW \quad (15)$$

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$$P_{Rsnub} = \frac{1}{2} \times f_{SW} \times C_{SNUB} \times V_{SW}^2 = \frac{1}{2} \times 350kHz \times 330pF \times 40V^2 = 92mW \quad (16)$$

2.6 Rectifying Diode (D1)

A rectifying diode is used on the secondary side and must meet the ratings for the application. The diode conducts the current in the secondary winding of the transformer. The average current rating must be at least the DC output current. The reverse breakdown voltage rating must be higher than V_{BR} calculated in Equation 17. This is the sum of the output voltage and the reflected input voltage from the primary. Lastly the package of the selected diode must be capable of handling the power dissipation estimated with Equation 18. With a higher output current, most of the power loss is dissipated in the diode.

$$V_{BR} = V_{OUT} + V_{IN}\,max \times Np2s = 5 + 24 \times 1.45 = 39.9V \quad (17)$$

$$P_D = I_{OUT} \times V_D = 2.5A \times 0.5V = 1.25W \quad (18)$$

2.7 Output Capacitor (C5–C6, C8)

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the supply responds to a large change in load current. The output capacitor needs to be selected based on the most stringent of these criteria.

The output capacitor must supply the output current when the internal MOSFET is turned on and current is flowing in the primary winding. It must also supply increased load current until the regulator responds to a load step. The output capacitance is selected to meet the requirements for the output voltage ripple and voltage change during a load step.

The output voltage ripple is determined by the capacitance and equivalent series resistance (ESR) of the output capacitor. The minimum capacitance for a given ripple is calculated with Equation 19 to be 32.3 µF. When using a high ESR capacitor the maximum ESR is calculated with Equation 20 to be 22 mΩ. When using ceramic capacitors the ESR ripple can be neglected but it must be considered if for example tantalum or electrolytic capacitors are used. Due to simplifications in these equations, when using mixed type output capacitors that have high ESR, it is best to test or simulate the output voltage ripple.

The minimum output capacitance needed to meet a load transient requirement is calculated with Equation 21, with f_{BW} of 6.0 kHz, to be 166 µF. Lastly the output capacitor needs to be rated for the RMS current calculated with Equation 22 to be 2.27 A.

The selected output capacitors are a 0.1-µF ceramic to filter high frequency noise, a 47-µF, 10-V X5R ceramic to help filter the ripple current and reduce the output voltage ripple, and a bulk 330-µF, 25-mΩ POSCAP (10TPE330M) to reduce voltage change during a load step.

$$C_{OUT} > \frac{I_{OUT} \times Dmax}{V_{RIPPLE} \times f_{SW}} = \frac{2.5A \times 0.452}{0.1V \times 350kHz} = 32.3\mu F \quad (19)$$

$$ESR < \frac{V_{RIPPLE} \times (1 - Dmax)}{I_{OUT}} = \frac{0.1V \times (1 - 0.452)}{2.5A} = 22m\Omega \quad (20)$$

$$C_{OUT} > \frac{\Delta I_{STEP}}{2\pi \times \Delta V_{OUT} \times f_{BW}} = \frac{1.25A}{2\pi \times 200mV \times 6kHz} = 166\mu F \quad (21)$$

$$I_{CO}rms = I_{OUT}\sqrt{\frac{Dmax}{(1 - Dmax)}} = 2.5A\sqrt{\frac{0.452}{(1 - 0.452)}} = 2.27A \quad (22)$$

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2.8 Input Capacitor (C2-C3)

As described on the TPS55340 data sheet at least 4.7-µF ceramic input capacitance is recommended. More input capacitance can be used to limit voltage ripple on the input supply. In a flyback topology the input current is discontinuous so more capacitance is typically needed than in a boost topology. The average input current is first estimated with Equation 23 to be 1.95 A. Using Equation 24, the minimum input capacitance to limit the voltage ripple to 10%, the minimum input voltage, is 15.4 µF. Using Equation 25, the input capacitors RMS current rating must be at least 2.15 A. Two 10-µF, 50-V, X5R input capacitors are used for the input capacitors.

$$I_{IN}DC = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta_{EST}} = \frac{5V \times 2.5A}{8V \times 0.8} = 1.95A \tag{23}$$

$$C_{IN} > \frac{I_{IN}DC}{Dmax \times f_{SW} \times 0.01 \times V_{IN}min} = \frac{1.95A}{0.452 \times 350kHz \times 0.01 \times 8V} = 15.4\mu F \tag{24}$$

$$I_{CI}rms = I_{IN}DC\sqrt{\frac{(1-Dmax)}{Dmax}} = 1.95A\sqrt{\frac{(1-0.452)}{0.452}} = 2.15A \tag{25}$$

2.9 IC Power Dissipation

The power dissipation in the TPS55340 is dominated by the conduction losses and switching loss of the power MOSFET. The power loss must not exceed the limitations of the package. Estimate the conduction and switching losses with Equation 26. The conduction loss is a function of the duty cycle, inductor RMS current, and the MOSFET on resistance. The switching losses are a function of the rise and fall times, switching frequency, primary ripple current, and input and output voltages. The rise and fall times are estimated based on an approximate 3 V/ns slew rate. The estimated power dissipation in the TPS55340 is 0.533 W.

$$\begin{aligned} Pdevice &= Rdson \times I_{PRI}rms^2 + \left(V_{IN} + Np2s \times \left(V_{OUT} + V_D\right)\right)^2 \times \frac{I_{IN}DC}{Dmax} \times f_{SW} \times \frac{10^{-9}s}{3V} \\ &= 0.60\Omega \times 2.92A^2 + \left(8V + 1.2 \times \left(5V + 0.5V\right)\right)^2 \times \frac{1.95A}{0.452} \times 350kHz \times \frac{10^{-9}s}{3V} = 0.533W \end{aligned} \tag{26}$$

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2.10 Output Voltage Regulation

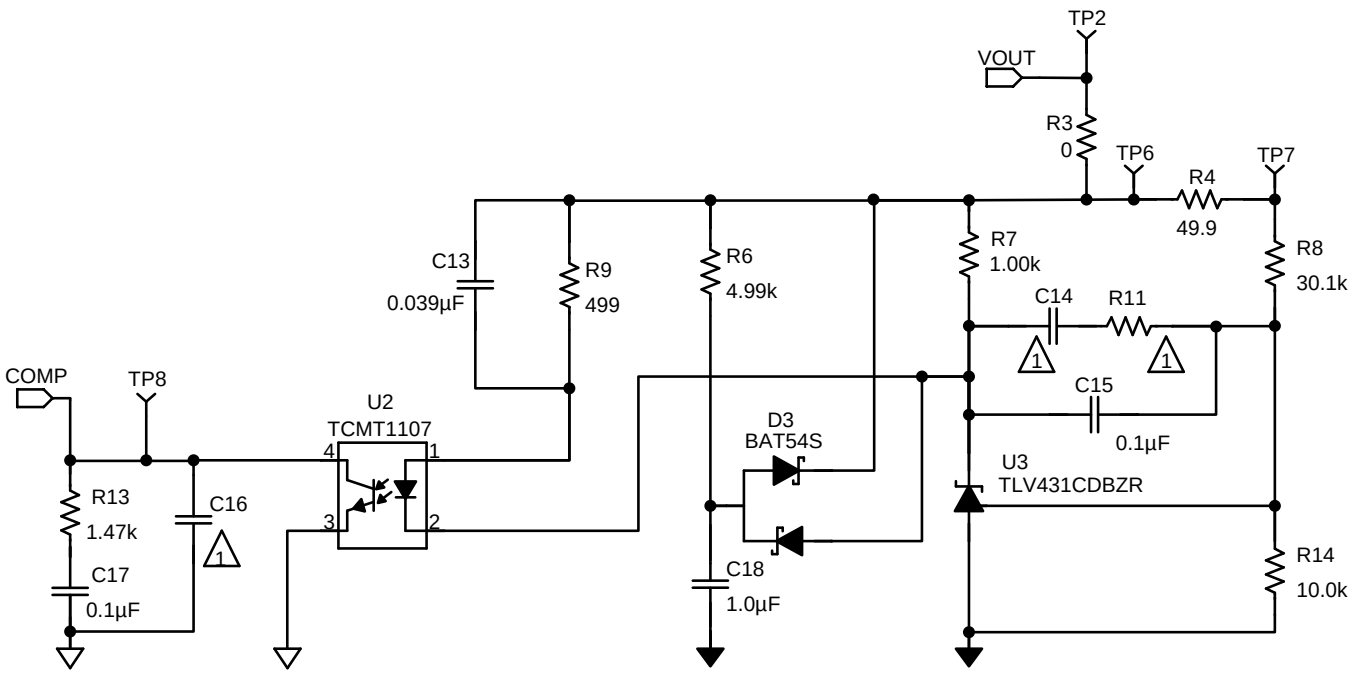

Figure 3. Opto-Coupler and Feedback Circuitry

For the best output voltage accuracy, this design uses secondary-side regulation with a shunt regulator driving an opto-coupler to control the COMP pin voltage of the TPS55340. The FB pin of the TPS55340 is grounded, turning the COMP pin into a constant current source of 42 µA, typical. When current flows in the diode of the opto-coupler, the BJT of the opto-coupler turns on, then based on the CTR of the opto-coupler, current flows from the COMP pin to ground regulating the operating duty cycle of the TPS55340.

The TLV431 (U3) is a shunt regulator with a reference of 1.24 V and a 6-V maximum cathode voltage. For higher output voltages the TL431 is recommended. The resistor divider created by R8 and R14 is used to set the output voltage. Keeping R8 fixed at 30.1 kΩ, R14 is calculated with Equation 27 to be 9.92 kΩ (10-kΩ standard value). When adjusting the output voltage by changing the resistance of R14, there is minimal change in the loop response. However, if the output voltage is adjusted by changing the resistance (R8) the loop response may be reevaluated.

$$R14 = \frac{R8}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)} = \frac{30.1k\Omega}{\left(\frac{5V}{1.24V} - 1\right)} = 9.92k\Omega \tag{27}$$

A bias resistor (R7) is also added to the shunt regulator keeping the Cathode current within the recommended operating conditions for the TLV431 of 0.1 to 15 mA. A value of 1 kΩ is used setting the current to approximately 3.8 mA. Calculate the bias current with Equation 28.

$$I_{BIAS} = \left(\frac{V_{OUT} - V_{REF}}{R7}\right) = \left(\frac{5V - 1.24V}{1k\Omega}\right) = 3.8mA \tag{28}$$

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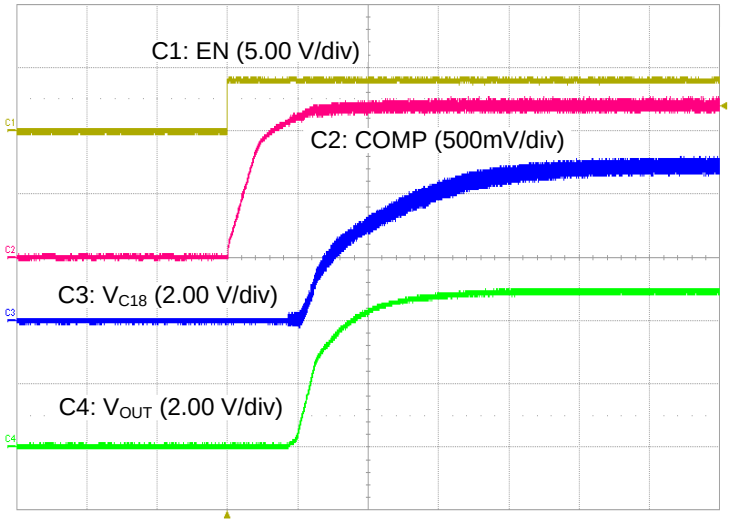
2.11 Slow-Start

In addition to the SS pin of the TPS55340, a slow-start circuit on the secondary side is required for a smooth output voltage ramp during start up. The capacitor (C12) on the primary side, connected to the SS pin of the TPS55340, allows a controlled rise rate of the COMP voltage. When switching begins, there is no bias voltage on the secondary to power the shunt regulator and an error signal cannot be sent back to the primary to control the COMP voltage. The primary soft-start circuit should rise at a faster rate than the secondary circuit controlling the operating duty cycle during the first stage of startup. When bias voltage becomes available for the secondary-side shunt regulator to operate, the secondary slow-start circuit takes over and controls the operating duty cycle through the opto-coupler. If the shunt regulator's reference rises too quickly, there can be overshoot on the output voltage.

The secondary-side slow-start circuit is created with components R6, D3, and C18. This gives a controlled startup of the shunt regulator voltage based on the RC time constant of R6 and C18. D3 provides a charge and discharge path for C18. To adjust the time of the secondary-side slow-start circuit, the RC time constant should be increased by either increasing the value of R6 or C18. The values used in this example are 4.99 kΩ for R6 and 1.0 µF for C18. The primary slow-start capacitor (C12) was set equal to 0.1 µF. Larger capacitance increases the primary slow start time and a smaller capacitance decreases it. Figure 4 shows the startup waveforms using EN with a 12-V input and 1-A load.



Time: 5.00 ms/div

Figure 4. Startup Waveforms

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2.12 Small Signal Response

2.12.1 Modulator

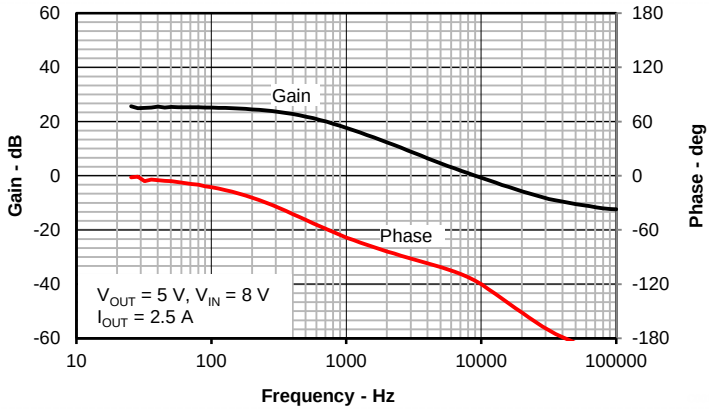

Figure 5. Power Stage Small Signal Response

The flyback power stage has the RHPZ and a pole and zero from the output filter. Equation 7 given in Section 2.3 calculates the RHPZ at a frequency of 25.4 kHz. The pole is due to the output capacitance in parallel with the load resistance and is calculated in Equation 29. This is approximately equal to 226 Hz at the minimum input voltage and full load. The load resistance can be calculated from the output current and output voltage. Equation 30 can be used to calculate the ESR zero. Using the bulk capacitor only this is estimated at 19.3 kHz.

$$f_{Pmod} = \frac{1}{2\pi \times Cout \times Rout} = \frac{1}{2\pi \times 352\mu F \times 2\Omega} = 226Hz \tag{29}$$

$$f_{ZESR} = \frac{1+D}{2\pi \times Cout \times ESR} = \frac{1}{2\pi \times 330\mu F \times 25m\Omega} = 19.3kHz \tag{30}$$

2.12.2 Compensation

As previously mentioned, the internal error amplifier of the TPS55340 is not used. Grounding the FB pin causes the amplifier to source a constant current of 42-µA, nominal, out of the COMP pin. Frequency compensation is implemented around the shunt regulator and opto-coupler. To simplify the compensation of the shunt regulator, a single compensation capacitor (C15) is used. The frequency response of this loop, referred to as the outer loop, includes a pole at the origin and gain set by the value C15 and R8. A C15 value of 0.1 µF is used to give low gain and bandwidth. If a higher gain and bandwidth are used the response of the shunt regulator can influence the inner loop. The response of the outer loop is also influenced by R9 and the characteristics of the opto-coupler. The frequency response of the shunt regulator outer loop is measured by injecting a signal across R4 using TP6 and TP7.

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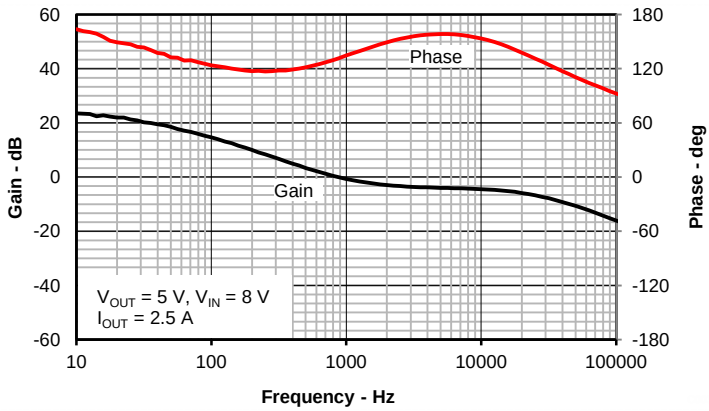

Figure 6. Compensation Small Signal Response

Figure 6 shows the response of the frequency compensation. R9 sets the current through the LED (I_{LED}) of the opto-coupler internally connected from pin 1 to pin 2. At lower output voltages, the maximum resistance value is limited by the voltage drop of the LED and minimum required voltage for the TLV431 reference. The maximum resistance is calculated with Equation 31 based on the desired current through the LED. The current through the LED sets the gain of the opto-coupler by setting the current transfer ratio (CTR). This is typically represented by a curve on the opto-coupler datasheet. R9 also influences the gain of the compensation, where decreasing the CTR will reduce the DC gain and increasing the CTR will increase the DC gain. For a 1-mA LED current and a forward voltage drop of 1 V the maximum resistance of R9 is 2.76 kΩ. A 499-Ω resistor is used setting the LED current at 5.5 mA.

$$R9 = \frac{V_{OUT} - V_{REF} - V_{LED}}{I_{LED}} = \frac{5.0V - 1.24V - 1V}{1mA} = 2.76k\Omega \tag{31}$$

Loop bandwidth is limited by the bandwidth of the opto-coupler. The TCMT1107 in this application begins to impact the loop response at approximately 10 kHz. C13 is added in parallel with R9 adding another zero to the loop. This provides phase boost near crossover to counter the decreasing gain and phase from the opto-coupler. A recommended value for C13 is calculated with Equation 32, placing the zero near target loop bandwidth of 1/3 the RHPZ and the pole of the opto-coupler. The capacitance is calculated to be 0.038 µF and a 0.039-µF capacitor is used adding a zero at 8.2 kHz. R13 and C17 in series add another zero calculated with Equation 33 at 1.08 kHz. R13 also sets the gain of the compensation at the crossover frequency. Higher resistances increase the gain and lower resistances decrease the gain. After setting the gain, C17 should be selected to set the zero between 1/5th and 1/10th the crossover frequency.

$$C13 < \frac{1}{2\pi \times f_{BW} \times R9} = \frac{1}{2\pi \times 8.5kHz \times 499\Omega} = 0.038\mu F \tag{32}$$

$$f_{ZCOMP} = \frac{1}{2\pi \times C17 \times R13} = \frac{1}{2\pi \times 0.1\mu F \times 1.47k\Omega} = 1.08kHz \tag{33}$$

Changing output filter components or the output voltage may require changing the compensation. The targeted loop bandwidth should be kept below 1/3 the RHPZ frequency. If more phase margin is needed, R9 can be adjusted to decrease the CTR of the opt-coupler and gain of the compensation. When changing R9, C13 should be recalculated using Equation 32. If R9 is at the maximum value recommended by Equation 31 and more phase margin is needed, R13 can also be decreased to lower the gain of the compensation. The total loop response is measured by populating R3 with a 49.9-Ω resistor and injecting a signal across it using TP2 and TP6. The loop response is shown in Figure 7.

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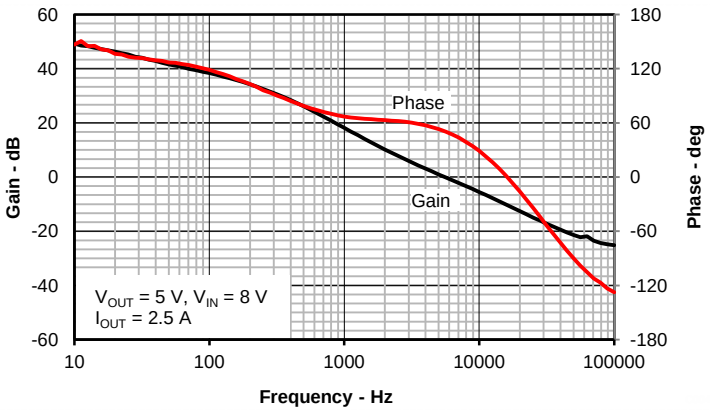

Figure 7. Total Loop Small Signal Response

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3 Evaluation Results

Efficiency and load regulation is shown in Figure 8 and Figure 9. Full evaluation results for this design can be found in the user's guide for the TPS55340EVM-148, SLVU751.

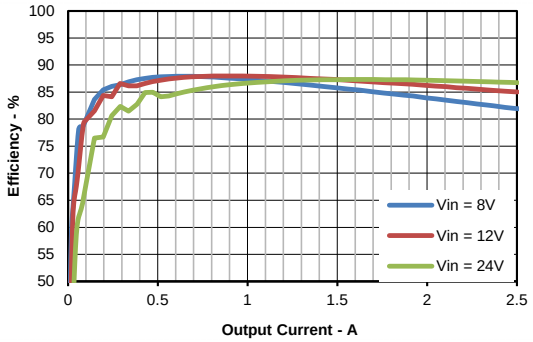

Figure 8. Efficiency

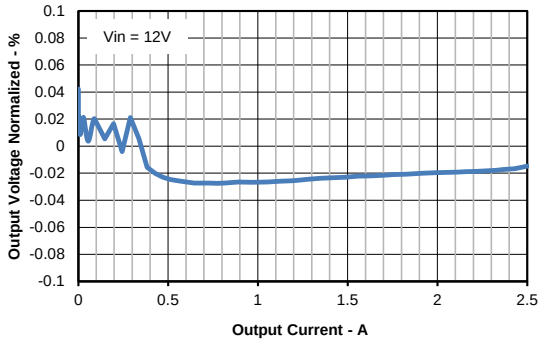

Figure 9. Load Regulation

4 Conclusion

TPS55340 can be used in isolated flyback applications where the 40-V, 5-A rated low-side switch meets the input and output requirements of the design. Using a converter IC with an integrated FET can simplify the design process and reduce the solution size. In addition to the high power and wide input voltage capabilities, the TPS55340 features a low minimum input voltage of 2.9 V. The example design uses opto-coupler feedback for tight regulation and higher performance. If the output does not need to be tightly regulated, a bias winding can be used to drive the FB pin and error amplifier of the TPS55340. Primary-side feedback greatly simplifies the control loop converter design as shown in Figure 10.

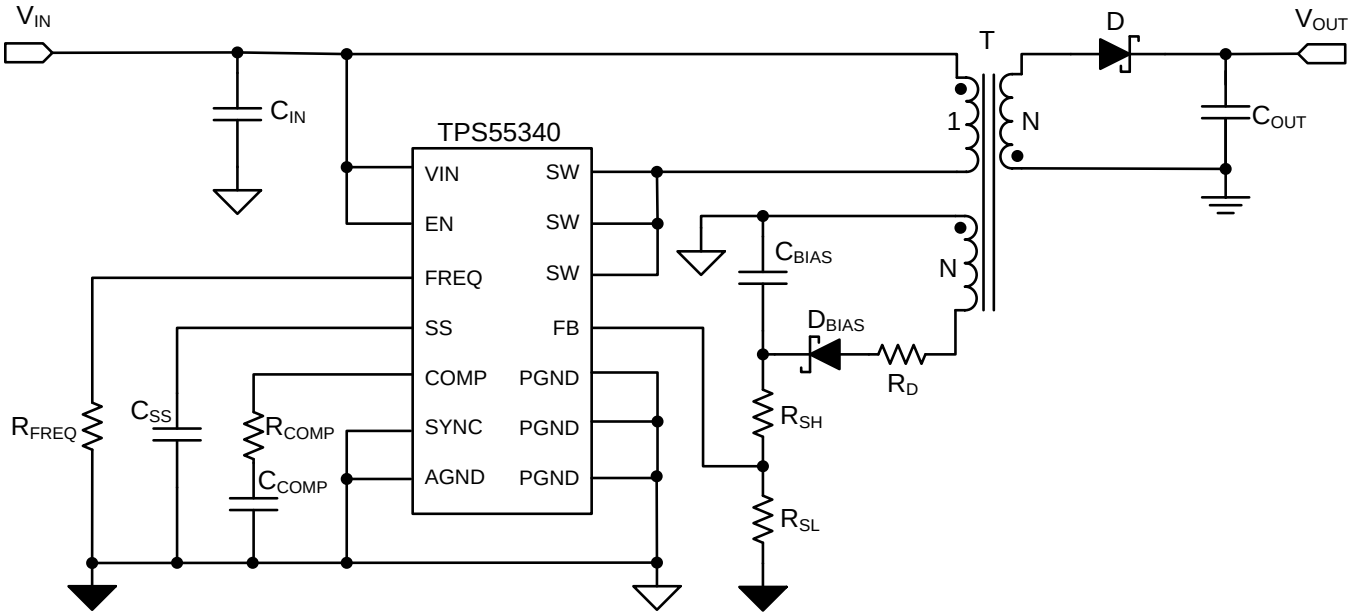

Figure 10. Isolated Flyback with Bias Winding

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5 References

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5. Jean Picard, *Under the Hood of Flyback SMPS Designs* (SLUP261)
6. *AN-1095 Design of Isolated Converters Using Simple Switchers* (SNVA005)

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