Application Report

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Estimating the Power Dissipation in an LCD Level Shifter

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ABSTRACT

The power dissipation in a LCD gate-driving circuit is shared between the level shifter output stages and the parasitic components in the display. The dynamic characteristics of the level shifter output stage and the parasitic component values are frequently unavailable. Thus it is often difficult to estimate the power dissipation. This application note presents a method to evaluate the power dissipation in a typical level shifter application.

Contents

1 Typical Level Shifter Application Description

Figure 1 shows one channel of a level shifter with gate voltage shaping. On the rising edge of IN, Q1 turns on, Q2 and Q3 turn off, and OUT is driven to $V_{(VGH)}$. On the falling edge of FLK, Q1 turns off, Q3 is turned on, and the panel now discharges through Q3 and R_E. On the falling edge of IN, Q2 turns on and Q3 turns off, and OUT is driven to $V_{(VGL)}$. This sequence is repeated in turn for each channel.

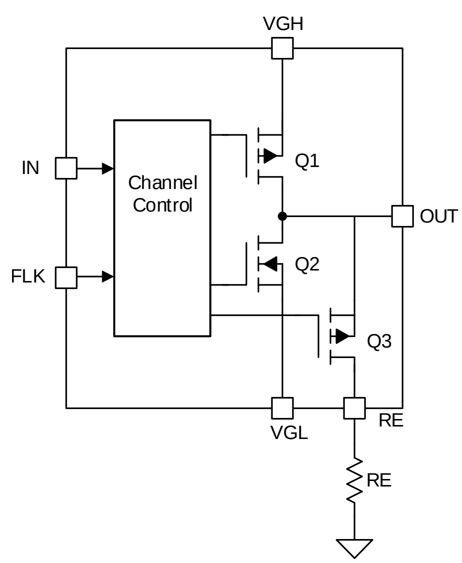


Figure 1. Level Shifter Channel With Gate Voltage Shaping

Level shifters that do not support gate voltage shaping (see Figure 2) are controlled only by the logic level applied to their IN pin. On the rising edge of IN, Q1 turns on, Q2 turns off, and OUT is driven to $V_{(VGH)}$. On the falling edge of IN, Q2 turns on, Q1 turns off, and OUT is driven to $V_{(VGL)}$.

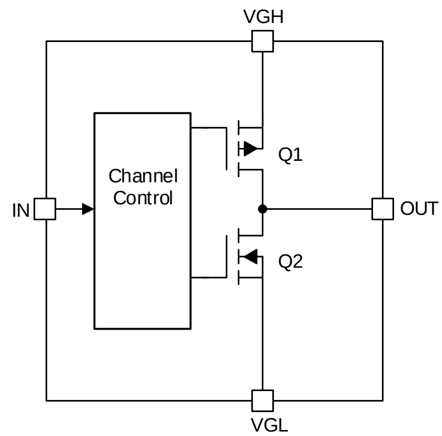


Figure 2. Level Shifter Channel Without Gate Voltage Shaping

2 Power Dissipation Estimation

In a typical level shifter application, the power dissipation is shared between the output stage of the level shifter and the parasitic components, as shown in Figure 3. To calculate the power dissipated in the level shifter, the dynamic characteristic of the output stage and the exact values of the parasitic components must be known. This information is frequently unavailable or not reliable.

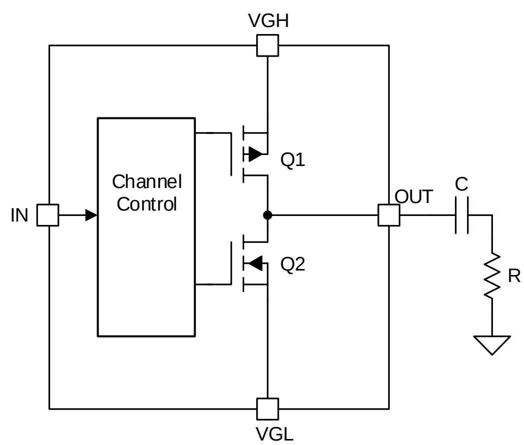


Figure 3. Level Shifter Channel With Load

Section 2.1 and Section 2.2 show a method to calculate the dissipated power in the level shifter without prior knowledge of any particular characteristics of the output stage or the parasitic components. This method works as follows: the voltage and current waveforms are captured with an oscilloscope and then are calculated using a spreadsheet. This is necessary because it is not possible to calculate the power dissipation of the level shifter in real time with an oscilloscope.

An example of the spreadsheet is available on SLVC653.

2.1 Output Voltage and Current Measurements

When capturing the output voltage and current measurements with an oscilloscope, make sure to:

- Capture a whole number of periods (one, two, and so forth). The spreadsheet provided is usable when the capture length covers an exact period.
- Have enough samples. The measurement resolution must be high enough to make sure of an accurate result. The more samples the measurement contains, the more precise the estimated power is.

Two options are available for measuring the current waveform: use a current probe or measure the voltage drop across a sense resistor (see Figure 4 and Figure 5). Measuring the voltage drop is the most convenient way to get the current measurement if a sense resistor is added to the circuit.

A current probe requires the addition of a wire between the output and the load and this adds some parasitic inductance to the circuit.

In Section 3, the current is measured using both methods to show how each impact the result.

The last step in the measurement process is to export the data into a CSV file for the post-processing operation.

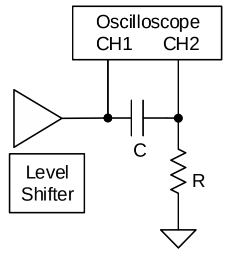


Figure 4. Measurement Setup With Voltage Probes

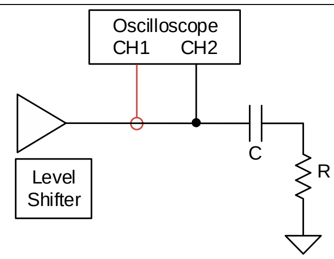


Figure 5. Measurement Setup With Voltage/Current Probes

2.2 Post-processing with Spreadsheet

The *Power Dissipation Estimation* spreadsheet, SLVC653, is a tool that can calculate the power dissipation in the level shifter and display the graph of the power dissipated over the time. For that, fill in the extracted data (sampling time, $V_{(OUT)}$ and $I_{(OUT)}$) in the dedicated case and also:

- The number of samples
- The values of $V_{(VGH)}$ and $V_{(VGL)}$
- The value of the sense resistor if one was used to measure the output current, otherwise keep this value to the default R = 1 Ω

When this step is completed successfully the power dissipated is finally calculated. For each sample, the voltage and the current are evaluated first. If the output current is measured as a voltage drop across a sense resistor, the current will correspond then to this voltage divided by the resistor value.
The voltage depends on the sign of the output current:

- If the output current is positive the voltage is equal to $V_{(VGH)} – V_{(OUT)}$
- And if it is negative the voltage equals $V_{(VGL)} – V_{(OUT)}$.

But the use of this algorithm increases the inaccuracy of the calculation. Therefore determine the voltage as follows (see Figure 6):

- In area 1, the voltage is equal to $V_{(VGH)} – V_{(OUT)}$
- And in area 2, it is equal to $V_{(VGL)} – V_{(OUT)}$

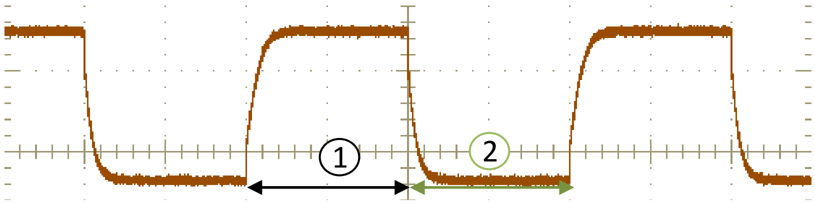


Figure 6. Output Voltage Calculation

After that, the power is calculated for each sample and then the power dissipated will correspond to the average over all samples (see Equation 1).

$$P_D = \frac{1}{n}\sum_{k=1}^{n} v_k i_k$$

where

- P_D is the power
- v_k is the voltage for the sample number k
- i_k is the current for the sample number k
- n is the number of samples (1)

2.2.1 Gate Voltage Shaping

When the level shifter channel supports gate voltage shaping, the calculation of the dissipated power is adapted to take this into account. The waveform of the voltage of the pin RE $V_{(RE)}$ is captured with an oscilloscope in addition to the output voltage and current waveforms. The recommendations in Section 2.1 hold for this operation.

In the spreadsheet, an additional column to fill in is reserved for $V_{(RE)}$. The calculation of the current does not change and for the voltage we can distinguish three cases (see Figure 7):

- In area 1, the voltage is equal to $V_{(VGH)} – V_{(OUT)}$
- In area 2, it equals $V_{(RE)} – V_{(OUT)}$
- And in area 3, it is equal to $V_{(VGL)} – V_{(OUT)}$

The following steps are the same as in the case without gate voltage shaping.

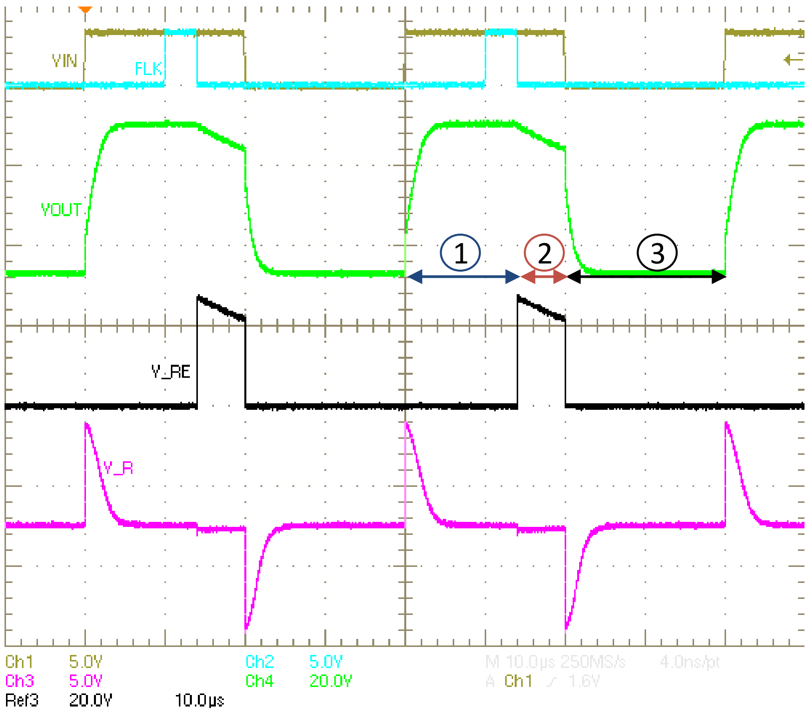
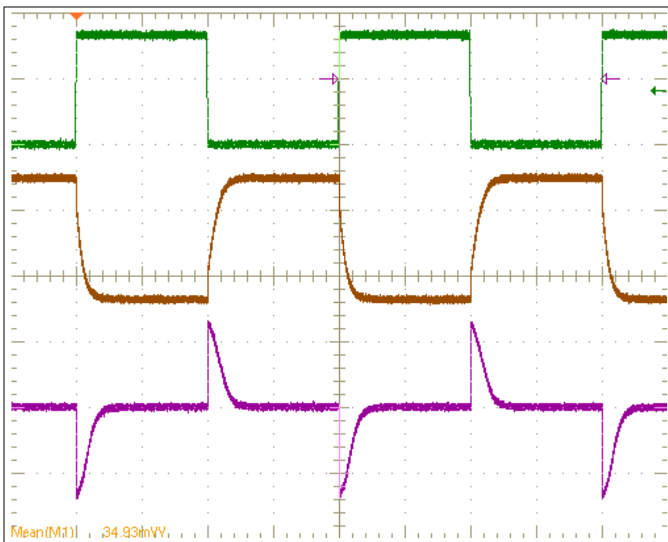


Figure 7. Output Voltage Calculation

3 Application example - TPS65192

The process described in the Section 2.2.1 was used to calculate the dissipated power in the TPS65192 level shifter channel without flicker signal (Figure 3). The output current is measured as a voltage drop across the output resistor. The captured waveforms are shown in Figure 8 and the result in Figure 9.



$V_{(IN)}$ in green $V_{(OUT)}$ in brown $V_R = RI_{(OUT)}$ in purple

Figure 8. Voltage and Current Waveforms

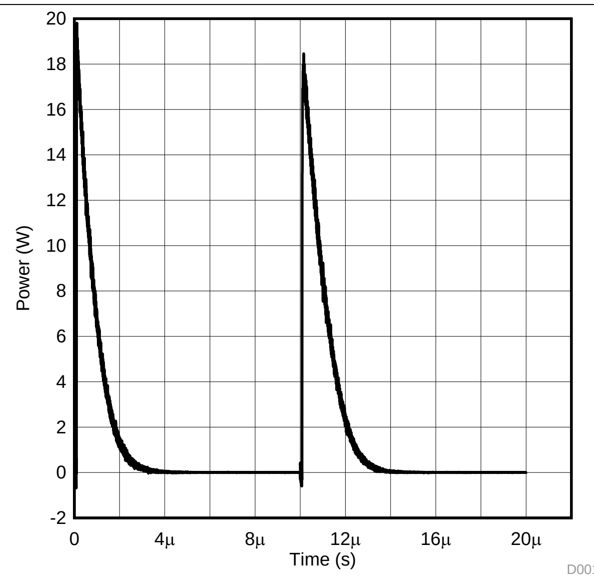


Figure 9. Power Dissipated in Level Shifter

This process was also used to calculate the level shifter power dissipation with different output loads and frequencies in order to make sure that the obtained results are consistent. The different test conditions and the corresponding results are available in Table 1. The total power is calculated with Equation 2.

$$P = fCV^2$$

where

- f is the level shifter's switching frequency
- C is the capacitive load
- V is the voltage swing across the capacitor (2)

Table 1. Test Conditions and Results

Case		Total Power (W)	P_D (W)	Repartition of the power between	
				Level Shifter	Load
1	f = 50 kHz; R = 10 Ω; C = 33 nF	2.26	1.7	75%	25%
2	f = 25 kHz; R = 10 Ω; C = 33 nF	1.13	0.83	73%	27%
3	f = 25 kHz; R = 47 Ω; C = 33 nF	1.13	0.3	23%	77%
4	f = 25 kHz; R = 10 Ω; C = 100 nF	3.4	2.4	70%	30%

These results validate the method used to evaluate the power dissipation in the level shifters. By comparing case 1 and case 2, the results show that the total power has doubled and the level shifter dissipates twice as much power.

The results of cases 2 and 3 indicate that the power dissipated in the level shifter decreases when the load resistor is increased and the capacitance is the same and the power dissipated in the load increases with the resistor as is predicted.

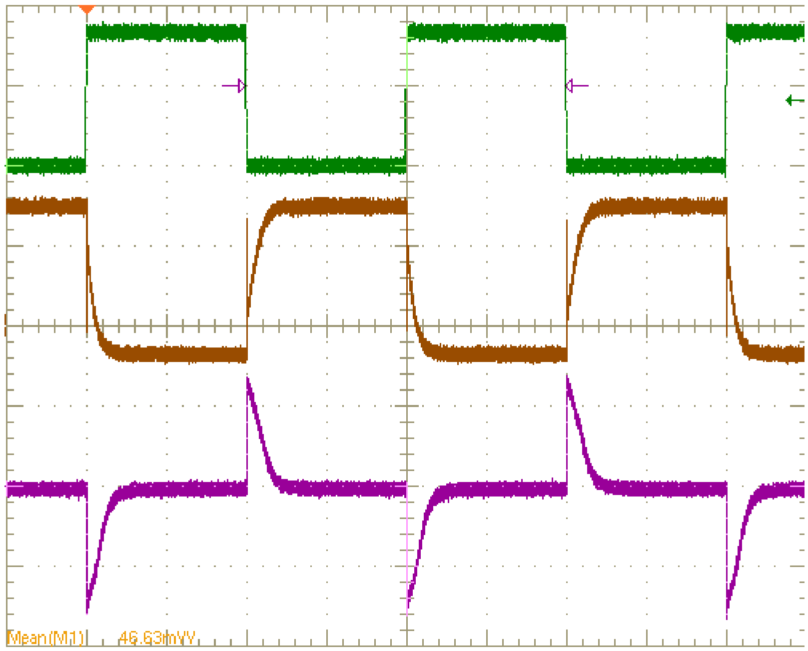
Finally, by comparing cases 2 and 4, the results show that the ratio between the power dissipated in the level shifter and the load is the same when the output resistance is not changed. The output capacitance has effect only on the total power.

3.1 Effect of Parasitic Inductance

To see the impact of the current measurement method in the results, the power dissipation is calculated with the same setup as in case 2 (refer to Table 1), but a current probe is used to measure the output current directly. For that, the shortest possible wire is added between the output and the load. This introduces a parasitic inductance which results in the addition of a spike in the output voltage waveform during transition edges (see Figure 10). The inductor current-voltage relationship (Equation 3) explains this behavior: a variation of the inductor current over time creates a voltage drop across its terminals.

$$V_L = L\frac{di}{dt} \tag{3}$$

The power dissipated in the level shifter is then equal to 0.831 W, which is 1 mW more than before. This indicates that the parasitic inductance does not have an important effect in the result and can thus be neglected.



$V_{(IN)}$ in green $V_{(OUT)}$ in brown $I_{(OUT)}$ in purple

Figure 10. Voltage and Current Waveforms