TEXAS INSTRUMENTS

Application Report
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TPS65311-Q1/TPS65310A-Q1 Monitoring and Diagnostic Mechanism Definitions

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ABSTRACT

TPS65311-Q1 and TPS65310A-Q1 devices are High-Voltage Power-Management Integrated Circuits (ICs) for use in Automotive Applications such as Advanced Driver Assistance Systems (ADAS). To assist safety-related applications, these devices have window watchdog and many diagnostic and detection functions. This application report provides a detailed overview of these features.

Trademarks

1 Introduction

TPS65311-Q1 and TPS65310A-Q1 devices integrate a wide input-voltage buck controller, two low-voltage buck converters, one boost converter, and one linear regulator. These devices are mainly used in automotive Advanced Driver Assistance Systems (ADAS), which require monitoring and diagnostic features in order to help meet certain safety goals at a system level. To assist system safety, the device includes voltage monitoring on all supply rails and a window-watchdog to help monitor the microcontroller unit (MCU) and digital-signal- processor (DSP). Other features include a high-side driver, which drives a warning-lamp (LED), a reference voltage used as analog-to-digital converter (ADC) reference in the MCU or DSP, and a shutdown comparator which, in combination with an external negative temperature coefficient (NTC) resistor, switches off the device at too low ambient temperature. Figure 1 shows the typical application block diagram of TPS65311-Q1 and TPS65310A-Q1 devices.

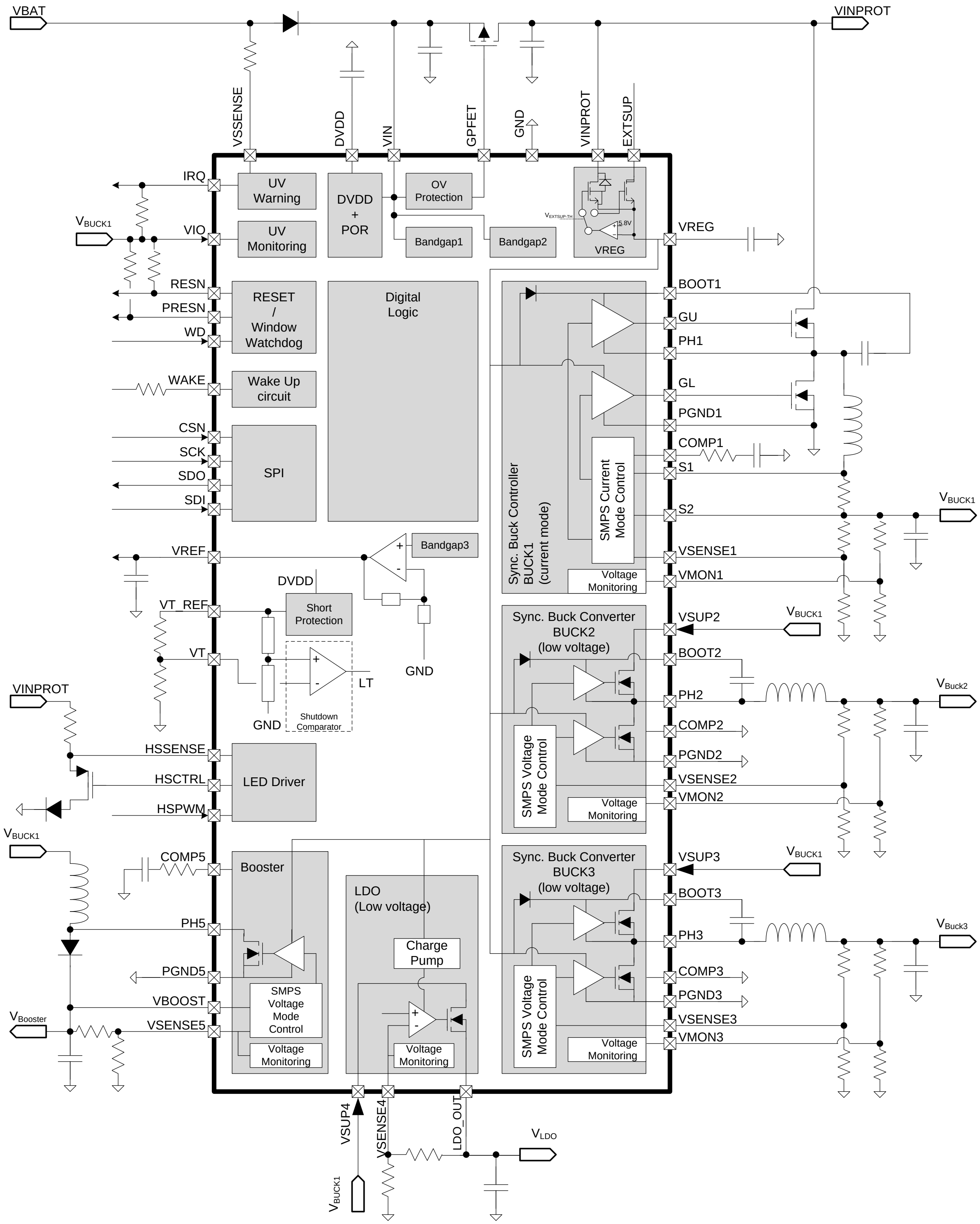

Figure 1. Detailed Block Diagram

Table 1 provides the detailed overview on the monitoring and diagnostic features available in the device. Monitoring functions run frequently or continuously (for example, output driver over current reporting). Diagnostic is a test that is performed periodically (for example, once per ignition cycle, self-test of the independent voltage monitors).

Table 1. TPS65311-Q1 Monitoring and Diagnostic Mechanism Definitions

Monitoring or Diagnostic Definition Number	Circuit Block	Monitoring or Diagnostic Mechanism	Description of Monitoring or Diagnostic Mechanism Inside Device
1	Oscillator	Loss of SMPS clock (or too slow main oscillator)	Detects loss of SMPS clock or SMPS clock is too slow when the main oscillator clock is still available. – During power up, it is detected in VTCHECK state and device enters LPM0 mode – If device is in ACTIVE state, device enters ERROR mode and error counter increments and register bit SMPCLK_ FAIL in SYS_STAT register is set
2	Oscillator	Loss of LPM clock	Device transitions to SHUTDOWN state, power on reset (POR) is generated and complete device is reinitialized – RESN and PRESN are asserted low – POR bit is set in SYS_STAT register
3	Oscillator	Loss of device Main Oscillator (or too slow main oscillator)	If clock is completely off, input power cycling (external power on reset) is needed for the device to enter the known state
4	Internal Power Supplies	Digital Core supply (DVDD)	DVDD is internal digital supply voltage – DVDD supply has independent undervoltage and overvoltage (UV/OV) monitoring – Upon detecting UV/OV condition, POR bit in the SYS_STAT register is set and device enters SHUTDOWN mode
5	Internal Power Supplies	VREG under voltage monitoring	VREG is used as internal supply voltage for BUCK1, BUCK2, BUCK3, Boost, and LDO driver circuits – When detected during power up while device is in the following state: _ INIT state: Device enters TESTSTART state, VREG_FAIL bit set and RESN and PRESN are asserted low _ VTCHECK state: Device enters LPM0 state,VREG_FAIL bit set and RESN and PRESN are asserted low _ RAMP state: Device enters ERROR state, VREG_FAIL bit set and RESN and PRESN are asserted low – When detected during ACTIVE state, the device status bit VREG_FAIL is set and device enters ERROR state – VREG_FAIL bit is cleared after MCU reads the PWR_STAT register and this fail condition is not present anymore
6	Internal Power Supplies	VREG current limit protection	VREG pin has internal current-limit protection, which switches off Vreg when current limit is detected. VREG must not be used to power any external circuits.
7	Internal Power Supplies	VREG Over temperature	– If detected during power up, device enters ERROR state and device error count is incremented. Device RESET remains active as long as this condition exists – If detected during ACTIVE state, device initiates RESET, enters ERROR state and device error count is incremented. Device RESET remains active as long as this condition exists
8	Internal Power Supplies	External Supply (EXTSUP) monitor	- Internal linear VREG regulator regulates output voltage (VREG) from VINPROT input if EXTSUP is not present or EXTSUP is too low. – When EXTSUP is > 4.8 V, the supply for VREG linear regulator automatically switches to EXTSUP only if IC is in Active Mode. This improves the thermal efficiency. – When EXTSUP is < 4.6 V, the supply for VREG linear regulator automatically switches to VINPROT. **NOTE:** BUCK1 can be used as External supply (EXTSUP) if BUCK1 is configured for VBUCK1> 4.8 V, Another option is to use VBOOST output if it is configured for > 4.8 V and has sufficient current budget.
9	Digital Logic	Reaction to Random Power Up State	Digital logic block designed so that all invalid FSM states transition to INIT, all regulators are switched off, and new device start up is forced.

Table 1. TPS65311-Q1 Monitoring and Diagnostic Mechanism Definitions (continued)

Monitoring or Diagnostic Definition Number	Circuit Block	Monitoring or Diagnostic Mechanism	Description of Monitoring or Diagnostic Mechanism Inside Device
10	RESN and PRESN	System and Peripheral reset supervisor	– RESN goes high after successful power-up and indicates that device is ready to receive WD input from microcontroller. – PRESN is latched version of RESN and goes high only after WD signal is detected by the device indicating that it has detected the WD signal and is fully functional – In case of any critical errors detected during start up/ active mode, these signals are driven low, device enters ERROR state and device error count is incremented **NOTE:** External pullup resistors are required on these two pins and must be connected to microcontroller Reset ports
11	SPI	SPI FSI bit	Device sends FSI bit between the falling edge of CSN and rising edge of SCK. This can be used as a software error interrupt to MCU. – Low level of SDO indicates normal operation of the device – If SDO line is high during this time, failure has occurred in the system and MCU must use PWR_STAT to get the details of the failure The following device error status bits drive the FSI bit: – PWR_STAT[7]: BUCK_FAIL, PWR_STAT[6]: VREG_FAIL, PWR_STAT[5]: OT_BUCK,PWR_STAT[4]: OT_LDO,PWR_STAT[3]: OT_BOOST,PWR_STAT[2]: LDO_FAIL, PWR_STAT[1]: BOOST_FAIL, PWR_STAT[0]:HS_OL
12	SPI	SPI_SCK_FAIL	SPI_SCLK_FAIL bit indicates the incorrect number of SCLKs in any SPI transaction – SPI_SCK_FAIL[4]: this bit is set if Number of SCLK cycles > 16 – SPI_SCK_FAIL[3:0]: Number of rising edges on SCK between a falling and a rising edge of CSN minus 1.
13	SPI	SPI_STAT	This register indicates the SPI communication errors – SPI_STAT[2]: Clock_Fail: Between a falling and a rising edge of CSN, the number of SCK does not equal 16 (CLOCK_FAIL) – SPI_STAT[1]: CMD_ID_Fail: Wrong command ID – SPI_STAT[0]: Parity_Fail: Parity error (parity bit odd is correct)
14	SPI	LPM0_CMD	The MCU can use this bit to put the device in LPM0 state – LPM0_CMD[7:0]: 0xAA brings device into LPM0 mode

Table 1. TPS65311-Q1 Monitoring and Diagnostic Mechanism Definitions (continued)

Monitoring or Diagnostic Definition Number	Circuit Block	Monitoring or Diagnostic Mechanism	Description of Monitoring or Diagnostic Mechanism Inside Device

15	Watchdog	Window Watchdog (WD)	Used to monitor the system MCU.
			– After start up, watchdog is enabled by rising edge on WD input, which has to occur within fixed timeout window ($t_{timeout}$,300 ms typical) from RESN rising edge.
			– If starting trigger is not detected within starting timeout window, device error count is incremented and RESN is driven low for $t_{RESNHOLD}$ duration (2 ms typical).
			– After reset extension (after $t_{RESNHOLD}$ is lapsed), device is in active state and waiting for another watchdog enable trigger which has to occur again within $t_{timeout}$ from RESN rising edge.
			– If watchdog enable trigger never occurs, sequence is repeated until device error count reaches NRES value.
			– Once EC reaches NRES, device enters LPM0 mode.
			Once watchdog is enabled, watchdog is triggered by:
			– The rising edge at the WD pin
			– WD signal rising edge must occur within the WD trigger open time window
			– WD input pulse signal (repetitive) period (T_{WD_IN}) must meet the following conditions:
			  – t_{WD} / 4 < T_{WD_IN} < t_{WD}
			  where
			  t_{WD} = Watchdog window time = 20 ms, typical
			  – For example: WD input pulse signal with 10 ms off time and 5 ms on time will work, provided the first WD input pulse rising edge is applied within $t_{timeout}$ after RESN rising edge
			Watchdog reset happens by:
			– A trigger pulse outside the WD trigger open window
			– No trigger pulse during window time
			– Watchdog reset flag is set via WD register bit
			– Watchdog reset causes RESN to be asserted and error counter is incremented
			– When Watchdog Fail Count exceeds NRES value, watchdog reset is asserted (if enabled) and device transitions to LPM0 state

16	Watchdog	Internal FSM state timeout	The timer limits the time during which the device stays in each of the start up modes: TESTSTART, TESTSTOP, VTCHECK, and RAMP. If the device enters one of these start-up modes and fails in any of these modes, the device enters LPM0 after timeout is elapsed if the WAKE pin is low. If WAKE pin is high, device stays in the same mode in which it failed.
17	EEPROM	EEPROM CRC Check	EEPROM CRC Check provides protection against wrong device trim settings (leading to wrong electrical specification parameters) and configuration. – After power on reset, device enters INIT mode. In this mode, device configuration data is loaded from EEPROM. – If EEPROM checksum error is detected, device will not enter TESTSTART mode and will remain in INIT mode until power cycle event occurs.

Table 1. TPS65311-Q1 Monitoring and Diagnostic Mechanism Definitions (continued)

Monitoring or Diagnostic Definition Number	Circuit Block	Monitoring or Diagnostic Mechanism	Description of Monitoring or Diagnostic Mechanism Inside Device
18	Internal Monitoring	Power up Self Test (Diagnostics)	These features provides Diagnostic coverage during power up INIT mode: – VREG comparator undervoltage check TestStart mode: – VT pin voltage check – BUCK1, BUCK2, BUCK3, BOOST, LDO, and VIO comparators UV and OV check The test is implemented such that during this mode all comparators have to deliver a 1 (fail condition). **NOTE:** In case any of the supply rails for BUCK2, BUCK3, LDO, or BOOST are not used in the application, the respective VMON2 and VMON3 or VSENSE4 and VSENSE5 pin of the unused supply must be connected to VMON1. Alternatively, the VSENSE4 pin can also be connected directly to ground in case the LDO is not used. TESTSTOP mode: – BUCK1, BUCK2, BUCK3, BOOST, LDO and VIO comparators OV check in normal operation It is expected that only the UV comparators will give a fail signal. In case there is an OV condition on any rail or one of the rails has an overtemperature, the device stays in TESTSTOP.
19	Vin monitor	Vin overvoltage (OV) monitor (VBAT after reverse battery protection) and GPFET	Vin over voltage (OV) monitor is used to protect internal VREG and external BUCK1 power stages. VREG is used as internal supply voltage for BUCK1, BUCK2, BUCK3, Boost, and LDO driver circuits – As soon as Vin is higher than the set threshold, GPFET switches off the external MOSFET (PMOS). Vin threshold is configurable via register bit: GPFET_OV_HIGH – In case of overvoltage in VTCHECK, RAMP, and ACTIVE mode, the GPFET turns off and the device changes to ERROR mode – GPFET is also turned off in ERROR, LOCKED, POR, INIT, TESTSTART, TESTSTOP or LPM0 modes **NOTE:** Depending on the application, the external PMOS may be omitted as long as VBAT < 40 V

20	Vin monitor	Vin undervoltage (POR) monitoring	Monitoring minimum Vin at which device can stay alive (Vin is VBAT after reverse battery protection)
			When VIN drops below VPOR level:
			– Device power-on reset is generated and device is reinitialized
			– POR flag is set
			– Device transitions to SHUTDOWN state
			When VIN recovers above VPOR level:
			– Device power-on reset is released
			– Device enters INIT state
			    – If WAKE input is still driven high, device starts power-up sequence
			    – If WAKE input is driven low, device transitions to LPM0 state

21	VBAT Monitor	VBAT under voltage monitor	Detects low VBAT voltage condition through VSSENSE pin. It is continuously monitored regardless of device state. – Default threshold can be modified by setting register bit: IRQ_THRES. An integrated filter time avoids false reaction due to spikes on the VBAT line. – Monitoring threshold is above VPOR Rising Vin Max threshold. – When detected, IRQ pin is driven low. The IRQ pin is low as long as PRESN is low. – If PRESN goes high and the battery line is already below the VSSENSETHx threshold, the IRQ pin is forced high for $t_{VSSENSE\_BLK}$ (35 µs max).

Table 1. TPS65311-Q1 Monitoring and Diagnostic Mechanism Definitions (continued)

Monitoring or Diagnostic Definition Number	Circuit Block	Monitoring or Diagnostic Mechanism	Description of Monitoring or Diagnostic Mechanism Inside Device
22	Power Supply	BUCK1 output voltage sense	BUCK1 voltage sense is for BUCK1 regulation loop. – The error between the feedback voltage VSENSE1 and the internal reference produces an error signal at the output of the error amplifier (COMP1), which serves as target for the peak inductor current. – A rise or fall in load current produces a rise or fall in voltage at VSENSE1, which causes COMP1 to rise or fall respectively, thus increasing or decreasing the current through the inductor until the average current matches the load current. In this way, the output voltage VBUCK1 is maintained in regulation. – Maximum value of COMP1 is clamped so that maximum inductor current is limited to a set value.
23	Power Supply	BUCK1 (Controller) thermal shutdown	– BUCK1 has a dedicated temperature sensor – OT_BUCK bit set if error detected (common bit for all the BUCK regulators)
24	Power Supply	BUCK1 (Controller) current limit	– BUCK1 has differential current sense and the controller works using cycle-by-cycle peak current mode control (regulates peak current through the inductor such that output voltage is maintained to its set value) and output of the error amplifier (COMP1 pin) serves as target for the peak inductor current. – The maximum value of COMP1 is clamped so that the maximum current through the inductor is limited to a set value. – BUCK_FAIL register bit set if overcurrent is detected.

25	Power Supply	BUCK1 (Controller) output voltage monitor	Detects the BUCK1 UV and OV conditions
			– BUCK1 output is continuously monitored at the point of load with voltage monitoring independent from BUCK1 regulation circuit
			– When BUCK1 UV/OV is detected:
			  – BUCK_FAIL bit set
			  – RESN is driven low, device transitions to ERROR state, Device error count is incremented

26	Power Supply	BUCK1 (Controller) dead time	Built-in shoot-through protection to prevent the high-side and low-side FET from being turned on simultaneously. This would create a short between VIN and GND. **NOTE:**Blanking time is 25 ns, typical
27	Power Supply	BUCK2 output voltage sense	BUCK2 voltage sense is for BUCK2 regulation loop
28	Power Supply	BUCK2 thermal shutdown	– BUCK2 has dedicated temperature sensor – OT_BUCK bit set if error detected (common bit for all the BUCK regulators)
29	Power Supply	BUCK2 current limit	Cycle-by-Cycle current limit is implemented for BUCK2 – In case of a output short circuit to ground or an overload condition, the integrated cycle-by-cycle current limit turns off the high-side FET when its current reaches $I_{HS\text{-}Limit}$ and the low-side FET is turned on until the end of the given cycle. – When the current limit is reached at the beginning of the cycle for five consecutive cycles, the pulse-width modulation (PWM) is forced low by turning on the LS-FET for sixteen cycles to prevent uncontrolled current build-up. – In case the low-side current limit of ILS-Limit is reached, for example, because of an output short to the VSUP2 and VSUP3 pins, the low-side FET is turned off until the end of the cycle. – If this is detected after the high-low PWM transition (immediately after the low-side overcurrent comparator blanking time), both FETs are turned off for sixteen cycles.

30	Power Supply	BUCK2 output voltage monitor	Detects the BUCK2 UV and OV conditions
			– BUCK2 output is monitored continuously at the point of load with voltage monitoring independent from BUCK2 regulation circuit
			– When BUCK2 UV/OV is detected:
			  – BUCK_FAIL bit is set
			  – RESN is driven low, device transitions to ERROR state, Device error count is incremented

31	Power Supply	BUCK2 dead time	Built-in shoot-through protection to prevent the short between high side and low side MOSFETs **NOTE:** Blanking time is 20 ns, typical
32	Power Supply	BUCK2 Enable	BUCK2_EN bit. Upon reset, BUCK2 is enabled, clearing this bit disables BUCK2
33	Power Supply	BUCK3 output voltage sense	BUCK3 voltage sense is for BUCK3 regulation loop

Table 1. TPS65311-Q1 Monitoring and Diagnostic Mechanism Definitions (continued)

Monitoring or Diagnostic Definition Number	Circuit Block	Monitoring or Diagnostic Mechanism	Description of Monitoring or Diagnostic Mechanism Inside Device
34	Power Supply	BUCK3 thermal shutdown	– BUCK3 has dedicated temperature sensor – OT_BUCK bit set if error detected (common bit for all the BUCK regulators)
35	Power Supply	BUCK3 current limit	Cycle-by-Cycle current limit is implemented for BUCK3 – In case of an output short circuit to ground or an overload condition, the integrated cycle-by-cycle current limit turns off the high-side FET when its current reaches IHS-Limit and the low-side FET turns on until the end of the given cycle. – When the current limit is reached at the beginning of the cycle for five consecutive cycles, the pulse-width modulation (PWM) is forced low by turning on the LS-FET for sixteen cycles to prevent uncontrolled current build-up. – In case the low-side current limit of ILS-Limit is reached, for example, because of an output short to the VSUP2 and VSUP3 pins, the low-side FET is turned off until the end of the cycle. – If this is detected after the high-low PWM transition (immediately after the lowside overcurrent comparator blanking time), both FETs are turned off for sixteen cycles.

36	Power Supply	BUCK3 output voltage monitor	Detects the BUCK3 UV and OV conditions
			– BUCK3 output is monitored continuously at the point of load with voltage monitoring independent from BUCK3 regulation circuit
			– When BUCK3 UV/OV is detected:
			  – BUCK_FAIL bit is set
			  – RESN is driven low, device transitions to ERROR state, Device error count is incremented

37	Power Supply	BUCK3 dead time	Built-in shoot-through protection to prevent the short between high side and low side MOSFETs **NOTE:** Blanking time is 20 ns, typical
38	Power Supply	BUCK3 Enable	BUCK3_EN bit. Upon reset, BUCK3 is enabled, clearing this bit disables BUCK3
39	Power Supply	Boost output voltage sense	Boost voltage sense is for boost regulation loop and UV and OV monitoring function. – Boost output is continuously monitored with voltage monitoring independent from Boost regulation circuit, but with common external voltage divider circuit – When Boost UV/OV is detected, BOOST_FAIL bit is set – BOOST_FAIL flag is cleared if there is no undervoltage and no overvoltage and the flag was transmitted to the master
40	Power Supply	Boost thermal shutdown	– BOOST has dedicated temperature sensor – OT_BOOST bit set if error detected
41	Power Supply	Boost current sense	Cycle-by-Cycle current limit is implemented – In case of an overcurrent, the integrated cycle-by-cycle current limit turns off the low-side FET when its current reaches ICLBOOST until the end of the given cycle. – When the current limit is reached in the beginning of the cycle for five consecutive cycles, the PWM is forced low to turn off low-side-FET for sixteen cycles to prevent uncontrolled current build-up.
42	Power Supply	LDO output voltage sense	– Output voltage is monitored by central independent voltage monitoring circuit with independent bandgap. – LDO_FAIL bit is set if error detected – Overvoltage during VTCHECK & RAMP mode, device enters ERROR mode
43	Power Supply	LDO current limit	Protects against overload and short circuit
44	Power Supply	LDO thermal shutdown	LDO has dedicated temperature sensor and OT_LDO bit is set if error detected
45	Power Supply	VIO under voltage Monitor	– MCU IC supply can be monitored for undervoltage – If VIO (MCU IO supply monitor) falls below UV threshold, reset is generated and the device enters ERROR mode

Table 1. TPS65311-Q1 Monitoring and Diagnostic Mechanism Definitions (continued)

Monitoring or Diagnostic Definition Number	Circuit Block	Monitoring or Diagnostic Mechanism	Description of Monitoring or Diagnostic Mechanism Inside Device

46	Power Supply	GND Loss Detection	– All power grounds PGNDx are monitored.
			– If the voltage difference to GND exceeds VGLTH-low or VGLTH-high:
			  – Device enters ERROR mode
			  – RESN and PRESN are asserted low
			  – The external PMOS (main system switch) is switched off by GPFET
			  – Device Error count (EC) is incremented

47	Reference Voltage	Bandgap	Device has three independent bandgap references (bandgap1, bandgap2, bandgap3) – Bandgap1 is used for reference for voltage regulators – Bandgap2 is used for voltage monitors (VMONx) and over temperature (OT) – Bandgap3 is used for VREF (ADC reference)
48	Reference Voltage	VREF	– VREF has Under Voltage Monitoring and Upon detecting failure, device enters ERROR mode – VREF pin is Short circuit protected by its current limiting function – VREF has independent band gap reference voltage (bandgap3)

49	External Temperature Monitor	Shutdown Comparator	VT_REF and VT pins can be used to interface external NTC to monitor the ECU temperature
			– VT_REF and VT pins are monitored during startup in VTCHECK mode
			  – If VT > VTTH, GPFET is switched off
			  – If VT_REF < VT_REF_TH, device enters ERROR mode if Shutdown comparator is enabled
			– VT_REF pin is short circuit and overvoltage protected
			– This Feature can be disabled using register bit VT_EN

50	LED Driver Module	Open Load Detection	Register bit: HS_OL in PWR_STAT register is set if Open load is detected.
51	LED Driver Module	Over current Detection	– A Counter monitors the overcurrent condition and when this module is active, counter is incremented during overcurrent condition. Once counter reaches the current limit time (THSS_CL), driver turns off, HS_EN register bit clears, and counter resets – Current level can be adjusted using external resistor
52	LED Driver Module	Self-Test of open load comparator	When PWM is low, if VINPROT–HSSENSE does not drop below the threshold, HS_OL flag is set

Revision History

DATE	REVISION	NOTES
November 2016	*	Initial Release