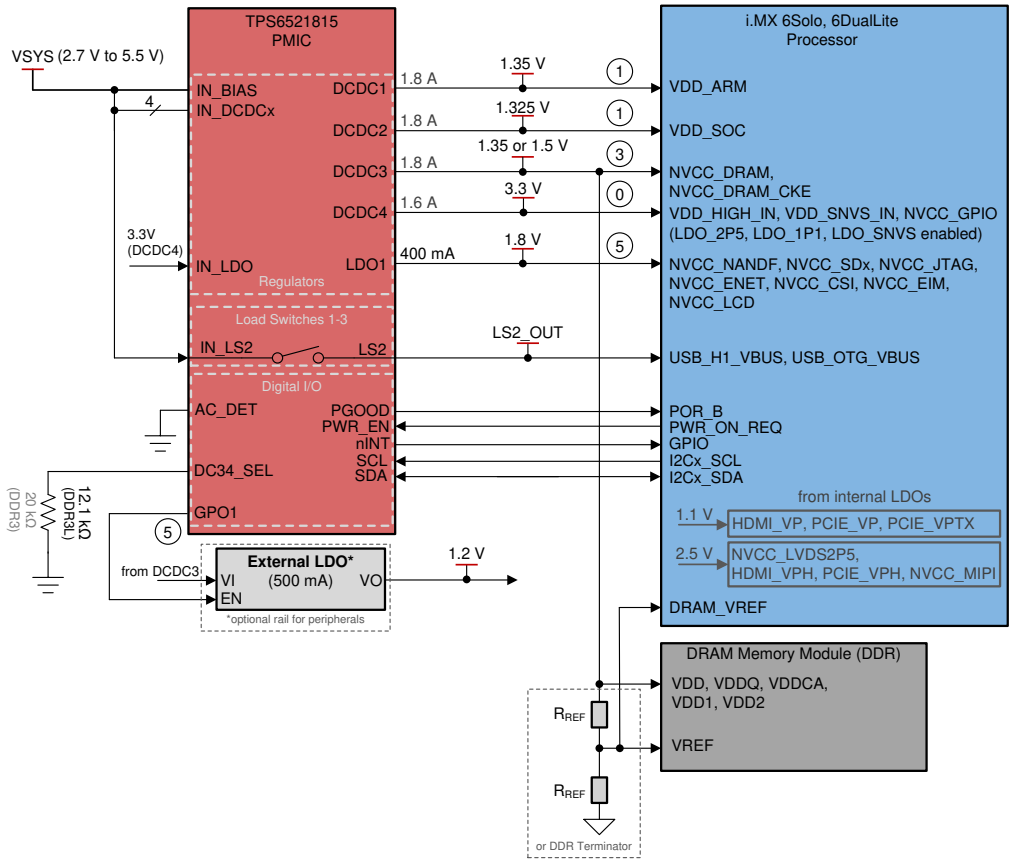
Powering the NXP i.MX 6Solo, 6DualLite with the TPS6521815 PMIC

System Power Block Diagram



Can you change PMICs?

Using a multi-rail power management IC (PMIC) for an applications processor is common, but typically the vendor recommends the PMIC that should be used for each processor. Even if the suggested PMIC is not ideal for the needs of the processor, often the complexity makes it difficult to swap out the PMIC for another solution. The purpose of this tech note is to show that the TPS6521815 PMIC can provide power for the i.MX 6Solo and 6DualLite processors.

Why the TPS6521815?

The TPS6521815 device has an input range from 2.7 to 5.5 V, making it appropriate for system-on-module applications powered from a 3.3-V or 5-V DC supply or a Li-Ion battery. The device has four step-down converters that provide the 1.35-V and 1.325-V power rails required for the ARM® and SoC cores, the 1.35-V (or 1.5-V) rail required for DDR3L (or DDR3) memory, and a 3.3-V rail required for I/Os. A low-dropout (LDO) regulator provides 1.8-V for an SD Card, NAND Flash, and JTAG I/Os. The TPS6521815 automatically sequences these rails in the correct power-up sequence for the i.MX 6Solo and 6DualLite processors.

How do you make the switch?

The TPS6521815 output voltages and sequencing order are determined by an EEPROM-backed register map, which can be programmed using the BOOSTXL-TPS65218 socketed booster pack. Samples of the TPS6521815RSLR can be programmed during the prototype phase of product development and soldered down on the TPS65218EVM-100 or the prototype PCB of the final product to evaluate the performance of the PMIC. To order pre-programmed samples of the TPS6521815RSLR for the NXP i.MX 6Solo, 6DualLite processor that match this tech note, contact the programming services organization at ARROW.

Table 1. i.MX 6Solo and 6DualLite Power Requirements

TPS6521815				i.MX 6Solo/6DualLite		
POWER-UP SEQUENCE	POWER SUPPLY (OUTPUT)	OUTPUT CURRENT [mA]	OUTPUT VOLTAGE [V]	POWER SUPPLY (INPUT)	VOLTAGE RATING [V]	MAX CURRENT [mA]
1	DCDC1	1800	1.35(1)	VDD_ARM	Minimum: 1.275 Maximum: 1.5	1320 (i.MX 6Solo) 844-2200 (i.MX 6DualLite)(2)
1	DCDC2	1800	1.325(1)	VDD_SOC	Minimum: 1.275 Maximum: 1.5	878-1260(2)
3	DCDC3	1800	1.35 (or 1.5)	NVCC_DRAM, NVCC_DRAM_CKE	Minimum: 1.283 Typical: 1.35 Maximum: 1.45	1000
0	DCDC4	1600	3.3	VDD_HIGH_IN, VDD_SNVS_IN, NVCC_GPIO(3)	Minimum: 2.9 Maximum: 3.3	125 + Maximum IO current
5	LDO1	200	1.8	NVCC_NANDF, NVCC_SDx, NVCC_JTAG, NVCC_ENET, NVCC_CSI, NVCC_EIM, NVCC_LCD	Minimum: 1.65 Maximum: 3.6	N/A
5	Ext. LDO(4)	500	1.2	1.2-V peripheral(s)	N/A	N/A
N/A	LS2	100	5	USB_H1_VBUS, USB_OTG_VBUS	Minimum: 4.4 Maximum: 5.25	25

(1) This set-point is based on the use case where VDD_ARM LDO and VDD_SOC are enabled. LDO VDD_ARM and VDD_SOC voltages can be modified by the processor after power-on using I2C, a feature named dynamic voltage scaling (DVS or DVFS) such that VDD_ARM_IN and VDD_SOC_IN are 125 mV greater than the LDO output set-point.

(2) The maximum current for the VDD_ARM and VDD_SOC core rails is determined from the *Use case 1—dual-core Dhrystone benchmark* and *Typical max power* sections in the AN4576 Application Note and the *Maximum Supply Currents* section in the IMX6SDLIEC data sheet.

(3) LDO_2P5, LDO_1P1, and LDO_SNVS internal LDO regulators are enabled to generate voltages for all NVCC power inputs as well as the HDMI_VPH and PCIE_VPH supply voltages.

(4) The external LDO is optional. When needed, it is controlled by an automatically sequenced GPIO of the TPS6521815.

Table 2. Adjacent Tech Notes

Processor	Title
i.MX 7Solo and 7Dual	Powering the NXP i.MX 7 Processor with the TPS6521815 PMIC
i.MX 8M Mini	Powering the NXP i.MX 8M Mini with the TPS6521815 and LP8733-Q1 PMICs

References

Texas Instruments, *TPS6521815 Power Management for ARM® Cortex™-A8/A9 SOCs and FPGAs* Data Sheet

Texas Instruments, *Power Supply Design for NXP i.MX 6 Using the TPS65023* Application Report, SLVA943, Feb. 2018

NXP Semiconductors, *i.MX 6Solo/6DualLite Family of Applications Processors for Industrial Products* Data Sheet (IMX6SDLIEC), Rev. 8, 09/2017

NXP Semiconductors, *i.MX 6DualLite Power Consumption Measurement* Application Note (AN4576), Rev. 1, 3/2013

0.1 Trademarks

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2019) to A Revision	Page
• Updated part number from TPS65248D0 to TPS6521815	1
• Updated Block Diagram based on complete design	1
• Updated i.MX 6Solo and 6DualLite Power Requirements Table based on complete design	2

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