Application Note

Demystifying and Mitigating Power Supply Ripple and Noise Implication on AFE8092

Srinivasan Iyer, Srinivas Murthy

ABSTRACT

Demystifying and Mitigating Power Supply Ripple and Noise Implication on AFE8092 AFE RF performance application note describes the significance of power supply impact on key RF Performance and explains the high-efficiency power topology to meet the same. The application note covers the following key points.

- Understanding Power Supply Ripple Modulation into RF spectrum for AFE8092 and deriving noise and ripple specification.
- Key measurement results showing implication of power supply on RF performance and design consideration for meeting RF metrics is discussed which includes Error Vector Magnitude (EVM), Phase Noise Plot for 5G NR Spectrum.
- The noise sensitive 1.8-V Analog rails of the AFE8092 are supplied using the TPS62913 switching regulators without the need for Low-Dropout Linear Regulators (LDOs) while maintaining the same performance as the original design. The LMK04828 is also supplied by the TPS62913.
- The digital core power rails of 0.9 V and mixed signal 1.2-V rails are powered by the TPS543820 with passive ripple filtering meeting power supply ripple restrictions.
- The design is applicable to the AFE80xx and other AFEs that require low noise power supplies that are size constrained and thermal constrained. Examples of applications are Remote Radio Units (RRU), Active Antenna Systems (AAS), Distributed Antenna Systems (DAS), small cell base stations, and repeaters.

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1 Introduction

High speed RF transceiver's integrated Phase-Locked Loop (PLL)/VCO and DAC supply rail are sensitive to power supply spurious and noise. Load transient ripple on the power supply directly impacts the data converter performance. One such real application example is Time Division Duplex (TDD) mode in which RX and TX channel toggle causes dynamic load transient thus resulting in supply ripple which couples into signal spectrum causing side band multiplicative spurious affecting Spurious Free Dynamic Range (SFDR) and Error Vector Magnitude (EVM).

The most common solution to minimize that ripple and noise is to use linear power supplies cascaded to the DC-DC output rail. LDO based solutions come at the disadvantage of impacting power efficiency losses which becomes more challenging to manage in systems having multiple AFEs.

An alternative approach which is discussed in this application note is powering noise and ripple sensitive rails directly from the DC-DC output by restricting supply ripple within allowed limits.

Compared to a linear supply, there are two big advantages of using a DC-DC converter alone: the reduction in power loss and the size of the power supply. To use a DC-DC converter alone requires careful consideration of the switching supply control topology, as well as the design and layout of the DC-DC converter.

This application note uses the AFE8092 as an example of a high-performance RF sampling transceiver where the 1.8-V and 1.2-V supplies have been changed from a DC-DC converter plus LDO approach to a DC-DC converter-only approach. This methodology can be used for many other noise sensitive applications as well. The TPS62913 low-ripple and low-noise buck converter used in this application note is specifically designed to help engineers design power supplies that meet the noise and ripple requirements for noise sensitive applications.

2 System Description

2.1 AFE80xx Noise and Ripple Requirements

The AFE80xx is a family of high performance, wide bandwidth multi-channel transceivers, integrating eight RF sampling transmitter chains, eight RF sampling receiver chains, and up to two RF sampling digitizing auxiliary chains (feedback paths). The high dynamic range of the transmitter and receiver chains allows the device to generate and receive 3G, 4G, and 5G signals from wireless base stations, while the wide bandwidth capability of the AFE80xx devices is designed for multi-band 4G and 5G base stations.

While the DC supply rail accuracy is specified for the AFE80xx, for ripple and noise specifications power supply to signal modulation (or PSMR) is used. In this application note 1.2-V TXADOUT and 1.8-V PLL is modulated with 100-mV peak to peak sine wave from 100 Hz to 2 MHz (600 kHz for 1.8-V PLL) signal frequency using Power Supply Line Injector to observe RF signal first order inter-modulation spurious amplitude.

To plot PSMR, spurious Root Mean Square (RMS) voltage is calculated using measured value of first harmonic power spectrum as shown in Equation 1 for 50-Ω load.

$$VSPUR_{RMS} = \sqrt{10^{\left(\frac{VSPUR_{dBm}}{10}\right)} \times 50} \tag{1}$$

Than PSMR is than computed using ratio as shown in Equation 2 with RMS of injected supply ripple voltage (35.35 mV).

$$PSMR = 20 \times \log\left(\frac{VSPUR_{RMS}}{SUPPLY\_RIPPLE_{RMS}}\right) \tag{2}$$

As an example shown in Figure 2-1 the 100-mV p-p sine wave signal impacts signal spectrum with undesired multiplicative inter-modulation spurious at offset of ripple frequency and its harmonic which impacts Signal SFDR for occupied bandwidth. This spurious can also corrupt constellation resulting in poor EVM.

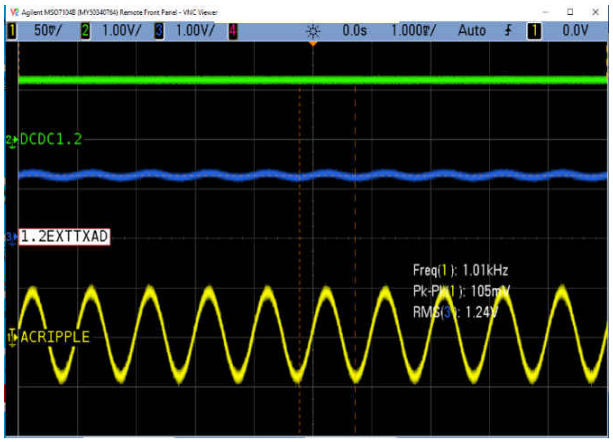

Figure 2-1. Modulated Power Supply 1.2 V

Figure 2-2. TXA Output Spectrum for Single Tone

Consolidated Power Supply Modulation Ratio (or PSMR for 1.2-V TXADOUT and 1.8-V PLL is as shown in Figure 2-3 and Figure 2-4. For 1.2-V TX Supply PSMR indicates sensitivity for low frequency ripple and higher attenuation for power supply switching frequency, thus it is necessary to limit undershoot and overshoot and steady state ripple due to low frequency load transient.

Signal to Noise Ratio (SNR) to EVM can be understood using Modulation Error Rate (MER) which can be related using peak to average power ratio (dB) of modulation scheme and target EVM specification for non-averaged measurement as shown in Equation 3. For 64 Quadrature Amplitude Modulation (QAM) having 3.7-dB peak to average ratio and 0.3% target EVM, the SNR needs to be approximately -47 dB.

$$SNR = \left(3.7 + 20 \times \log\left(\frac{EVM\%}{100\%}\right)\right) \quad (3)$$

For 1.2-V TX DAC supply at 100 Hz for 35.35-mV RMS supply ripple the PSMR magnitude is close to -42 dB resulting in spurious magnitude of -59.96 dBm in power spectrum. For -12-dBm carrier tone and -48-dB allowed power supply spurious magnitude, the load transient ripple on 1.2-V TX supply needs to be below 35.35 mV to achieve desired EVM specification.

For 1.8-V PLL the PSMR plot indicates that supply ripple is amplified up to 200-kHz bandwidth post which the ripple is attenuated, hence the 1.8-V PLL needs to be powered using low noise and ripple free power circuitry.

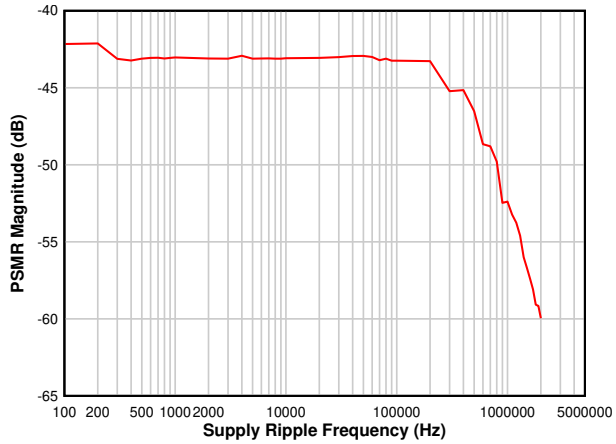

Figure 2-3. PSMR 1.2-V TXADOUT

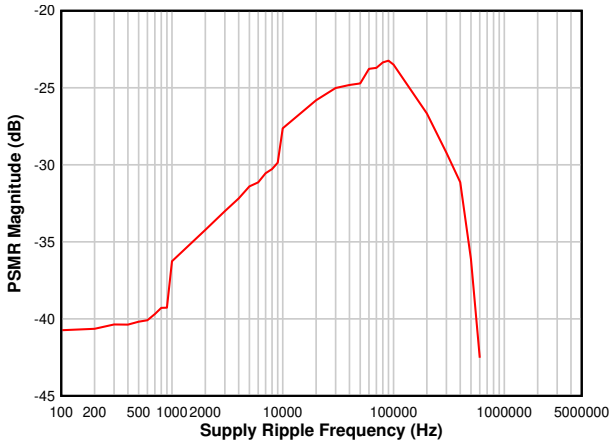

Figure 2-4. PSMR 1.8-V PLL

3-GPP TS 136 104 5G NR standard recommends EVM limit of 8% for 64-QAM modulation and 3.5% for 256 QAM for base station type 1-C and 1-H.

For this application note noise floor below -90 dB and power supply side band inter-modulation spurious magnitude below -46 dB with respect to carrier tone is considered as desired specification to meet below 2% target of first symbol EVM to comply with 5G NR standard requirements.

To meet the above desired specification, fixed frequency control topology is used to maintain steady state switching frequency ripple across load current variation. Second stage filtering is added in DC-DC power path to attenuate switching frequency supply ripple below 1 mV. Step load transient ripple (Overshoot and Undershoot) is maintained below 35.35 mV to achieve below -47-dB target for supply inter-modulation spurious with RF signal tone.

2.2 AFE80xx Supply Settling and EVM for TDD Operations

In TDD mode operation Transmit (TX) and Receive (RX) signals are time multiplexed to operate in same frequency spectrum. The time multiplexing is done as per definition of wireless interface standard.

For defined guard period as per the wireless standard interface between TX and RX switching the DAC supply undergoes load transient which results into overshoot and undershoot ripple. If supply rail is not settled before data is transmitted from AFE TX channel, constellation points will be affected, resulting in poor first symbol EVM.

5G NR TDD 20 MHz, 256.76 MSPS data is transmitted from TX channel with 15-us guard period with RX channel. The hardware data delay of start of pulse and actual start of data is 2.5 us. As 1.2-V DAC supply is not settled at 2.5 us, the first symbol is degraded causing EVM peak around 1.5%.

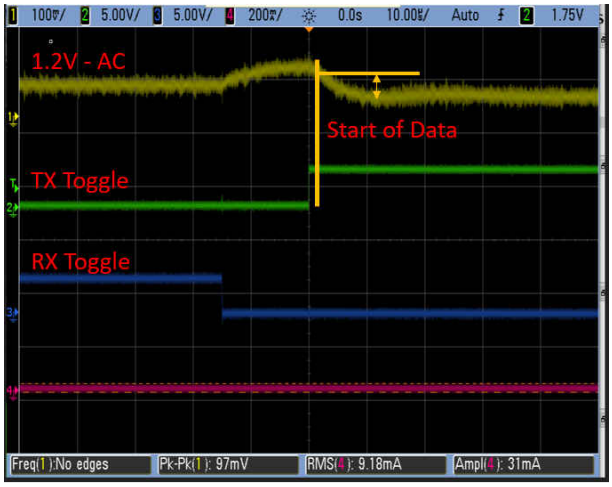

Figure 2-5. 1.2-V Supply Settling

Figure 2-6. 5G NR TDD EVM

5G NR TDD 20 MHz, 256.76 MSPS data is transmitted from TX channel with 10-us guard period with RX channel. The hardware data delay of start of pulse and data is 7 us. As 1.2-V DAC supply is settled at 7 us, hence the first symbol is not degraded showing EVM peak improvement from 1.5% to 1.0%.

In the above example 1.2-V DC is settled approximately to 96% of final steady state of DC supply at start of data thus preventing degradation of first symbol EVM.

To achieve optimized settling of 1.2-V DC rail for load transient, it is necessary to design Buck converter power stage and secondary closed loop L-C filter with good phase margin and settling response.

TI SWIFT™ based DC-DC power device operating in Advanced Current Mode (ACM) control and optimized power stage helps to achieve AFE80xx supply requirements.

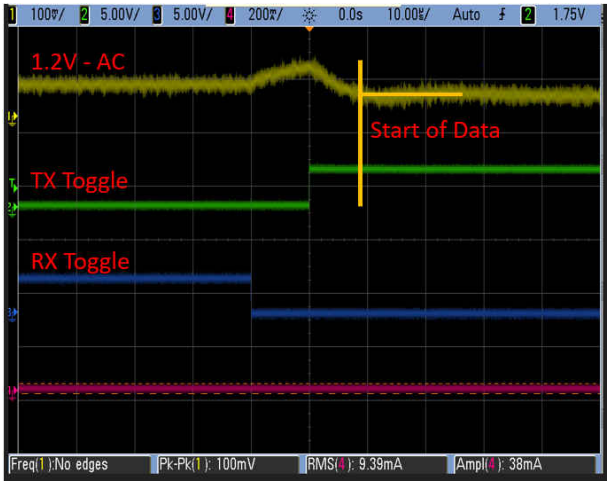

Figure 2-7. 1.2-V Supply Settling

Figure 2-8. 5G NR TDD EVM

2.3 Block Diagram

2.3.1 Proposed Power Architecture

AFE8092 0.9-V, 1.2-V, and 1.8-V groups are powered directly from DC-DC as shown in Figure 2-9. All DC-DC have additional second stage LC filtering using ferrite bead and filter caps. Additionally, each group of power rail is isolated with additional ferrite bead filtering to suppress high frequency noise from either side. Additional ferrite bead filtering with AFE decoupling capacitor should be designed without causing supply ringing during load step and meet settling time as close as DC-DC output response as mentioned in AFE80xx Supply Settling (Section 2.2). See *Section 4.1.4* of TIDA-01579 for ferrite bead filter design with damping resistor. Optimized ferrite LC bead filtering can eliminate cross channel carrier coupling and prevent inter-modulation spurious in RF spectrum.

In Figure 2-9 power design, 1.8-V PLL rail can be powered from dedicated TPS62913 DC-DC power supply to avoid coupling of loads transient ripple from 1.8-V supply into 1.8-V PLL bandwidth of AFE8092 when used for TDD Wireless systems.

For Multichannel AFE architecture a single DC-DC TPS62913 can be used to power up multiple 1.8-V PLL supply rails. 0.9-V and 1.2-V rails of Multichannel AFE architecture (64T64R) can be powered from single or dual TPS543B20 high current synchronous converter.

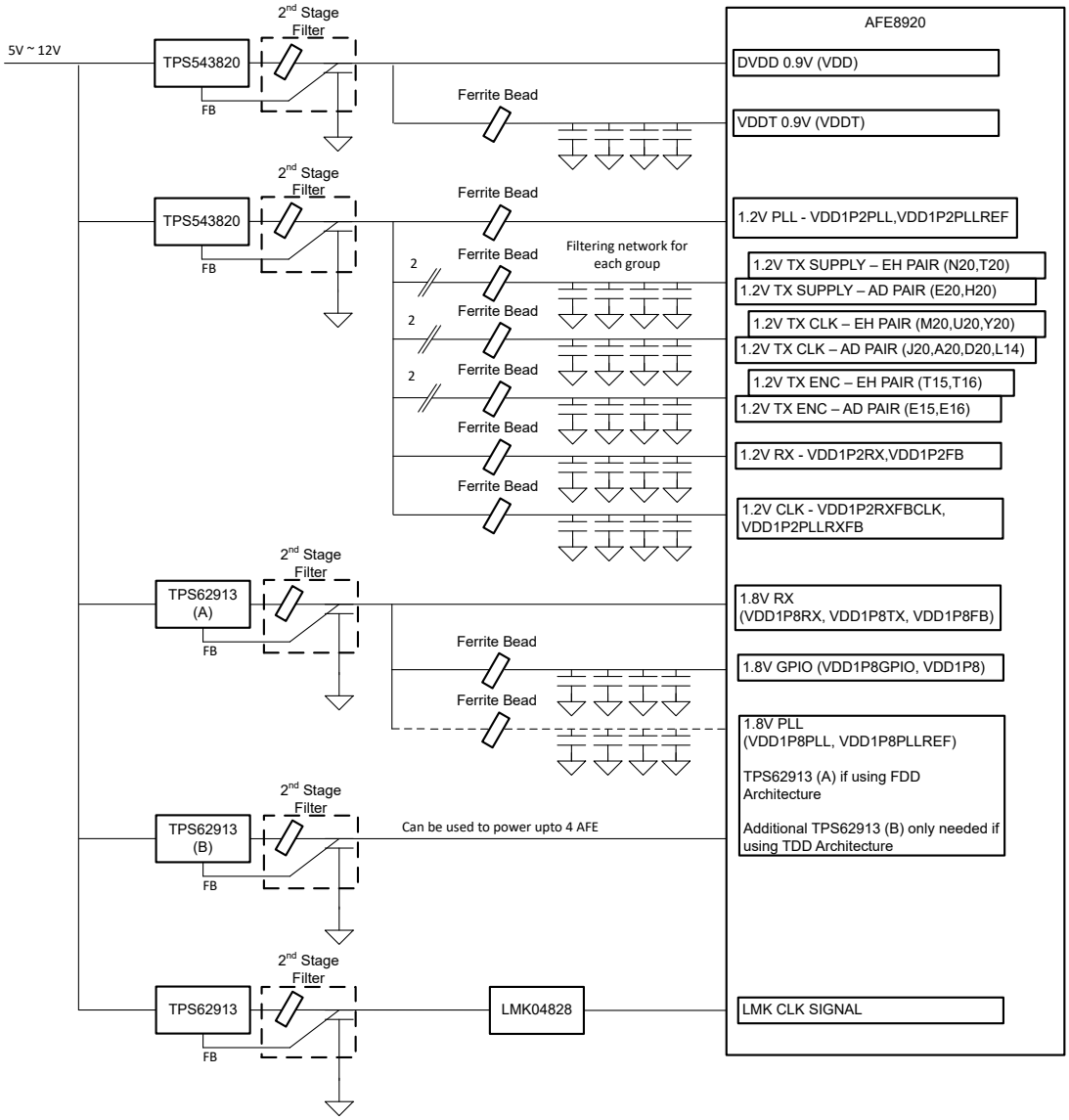

Figure 2-9. Proposed Point of Load Power Architecture

All DC-DC is externally synced with 1-MHz switching clock to eliminate any Beating spurious in RF spectrum. Additional phase shift in clock signal can be added to reduce input ripple current of DC-DC blocks. A low-cost clock sync circuit is proposed as shown in Figure 2-10 using square pulse oscillator using TLV3501 and D flip flop, NAND Gate to generate 90° phase shifted clock pulses.

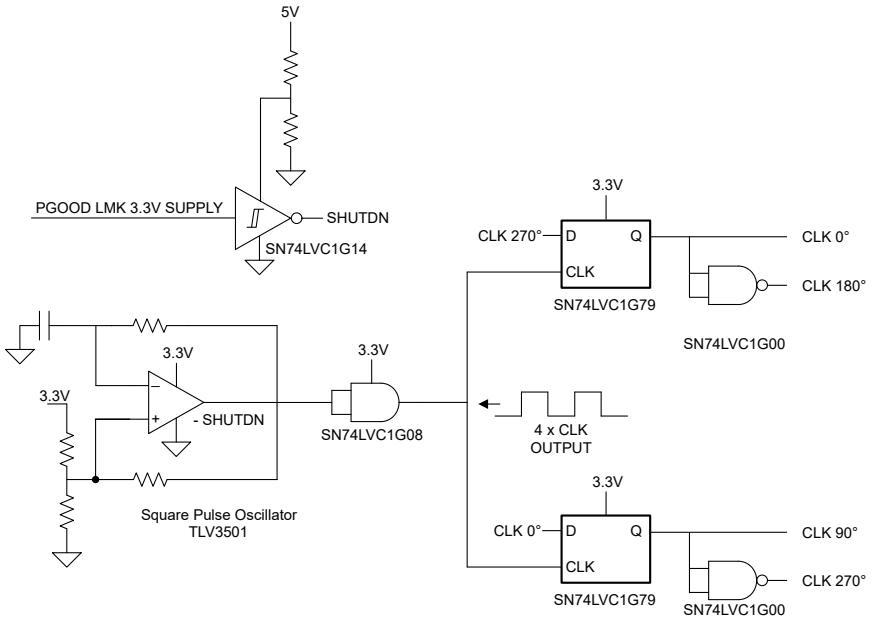

Figure 2-10. External Clock Synchronization

2.3.2 Power Sequencing

In the proposed solution, sequencing is achieved by gating Power Good to Enable pin of DC-DC solution. For this application note for AFE8092 family, the sequencing is implemented using logic gates as shown in Figure 2-11 to meet the timing requirements on power rails as per AFE80xx specification in data sheet. R-C circuit on buffer output can be adjusted for fixed delay time across enable pulses to suppress any power good oscillations and additional soft start for DC-DC.

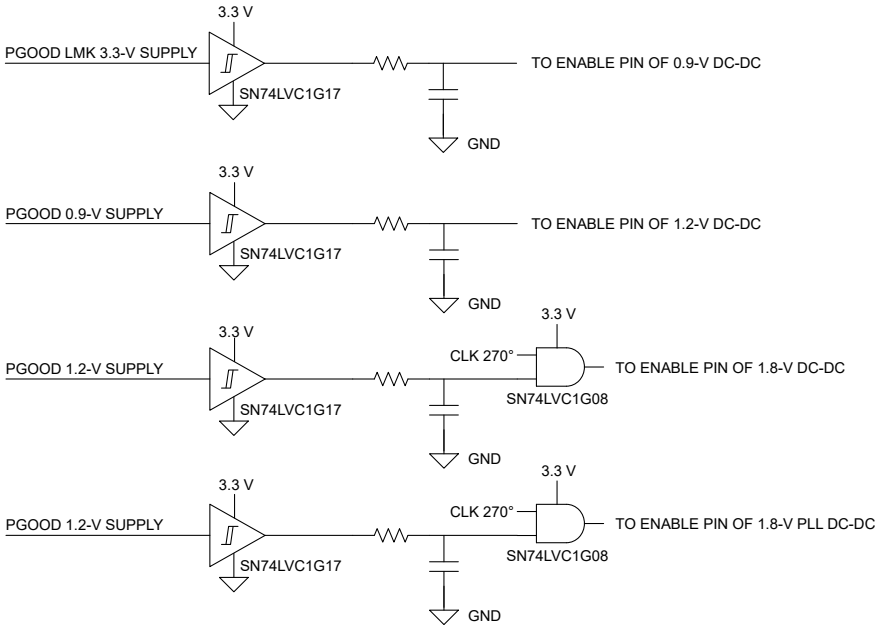

Figure 2-11. DC-DC Sequencing Circuit

2.4 Power Supply Design Consideration

The analog and clock inputs of converter often get most of the scrutiny when it comes to addressing low noise on their inputs. Keep in mind that power supplies are inputs too. Because we think of them as DC biasing circuits we often do not think of them as affecting RF performance. However, this is not true. Spurious performance is dependent on the layout structure. The DC-DC converters are generating switching spurious which can be large.

Switching spurious infiltrate unwanted circuits via conducted paths or radiated paths. Conducted spurious are mitigated with the ferrite bead isolation, supply filtering, and adequate low frequency bypass capacitors. Radiated emissions are more difficult to control.

The primary location for radiated emissions is right at the DC-DC converter itself and the switching inductor. Since the switching spurious are large in amplitude and at low frequency, localized shielding or PCB ground planes do little to attenuate the spurious. Switching spurious penetrate ground planes easily and infect internal, sensitive power traces. As such, keep sensitive routing from running on an internal layer directly underneath the DC-DC converter. Further, no other board with sensitive internal nets should be placed directly above or below. Even physical spacing as much as one inch is not sufficient to reduce the spurious coupling. Instead, the DC-DC switchers should be offset from any sensitive area or other boards so that there is nothing directly above or below the converters that will be contaminated by switching spurious. When designing power supply domains for any high-speed converter, here are some useful tips in maximizing power supply noise immunity:

- Decouple all power supply rails and bus voltages as they come onto the system board near the AFE itself.
- Remember that approximately 20-dB/decade noise suppression is gained for each additional filtering stage.
- Decouple both high and low frequencies, which might require multiple capacitor values.
- Series ferrite beads are commonly used at the power entry point just before the decoupling capacitor to ground. This should be done for each individual supply voltage coming into the system board regardless of whether it comes from an LDO or switching regulator.
- For added capacitance, use tightly stacked power and ground plane pairs (≤ 4-mil spacing). This adds inherent high-frequency (> 500 MHz) decoupling to the PCB design.
- Keep supplies away from sensitive analog circuitry such as the front-end stage of the AFE and clocking circuits if possible.
- Follow the IC manufacture recommendations; if they are not directly stated in the application note or data sheet, then study the evaluation board. These are great vehicles to learn from.

Applying the above points help provide a solid power supply design yielding data sheet performance in many applications.

3 Tests and Results

3.1 Test Methodology

3.1.1 Phase Noise (Transmit) (dBc/Hz)

The phase noise parameter measures the frequency noise or jitter that is related to the sampling clock. Phase noise measurement sweeps from a very low frequency offset (≈100 Hz) out to over 10 MHz relative to the carrier frequency. This measurement examines low frequency spurious and noise that may come from the power supply at the RF transmitter output.

3.1.2 EVM for Frequency Division Multiplexing (FDD) Mode(%)

EVM is measured to plot the deviation of constellation points for 5G NR spectrum configured for FDD mode. Noise, spurious signals, distortion and phase noise degrades the EVM. In FDD mode AFE8092 all 8 transmit and 8 receive pairs are enabled in continuous mode.

3.1.3 EVM for TDD Mode(%)

EVM is measured to plot the deviation of constellation points for 5G NR spectrum configured for TDD mode. Noise, spurious signals, distortion and phase noise degrades the EVM. In TDD mode AFE8092 all 8 transmit and 8 receive pairs are toggled with 10-us guard time period. The TDD toggling causes dynamic load current variations on power supply rail resulting into load transient ripple coupling into signal spectrum.

Along with power supply improvements, AFE80xx features unique programmability to group TX or RX channel time staggering each TX and RX channel by fixed delay thereby reducing the load step to be seen by DC-DC output hence reducing supply overshoot and undershoot magnitude. Additionally, AFE80xx also features internal bias voltage configuration for TX channel to minimize supply modulation into RF DAC output.

3.1.4 Receive (RX) Spectrum (Power Supply Spurious)

The SFDR is the ratio of the RMS value of the signal to the RMS value of the peak spurious spectral component for the analog input frequency that produces the worst result. SFDR is intended to capture the spurious performance due to power supply stage into receive signal spectrum.

3.1.5 Power Efficiency

Powering noise sensitive rails of AFE8092 directly from DC-DC is advantageous to achieve higher power efficiency and low thermal hotspots. In this application note, power efficiency of proposed solution is compared with LDO powered architecture for FDD and TDD mode.

3.2 Test Conditions

AFE8092 is configured for 8T8R mode with approximately 12-GSPS DAC and 3-GSPS ADC sampling rate. Numerical Control Oscillator (NCO) is internally configured for single band 3500 MHz to match the matching network and signal spectrum of 3.5 GHz.

For TDD mode GPIO pin TXATDD1 and RXATDD1 of AFE8092 are driven through FPGA capture card with square pulse signal having 75% and 25% duty ratio.

3.3 Test Results

3.3.1 Phase Noise

Single tone 3.5-GHz transmit output signal of Channel A is monitored using R&S Phase noise analyzer to see implication on ripple and noise coupling from supply rail into signal chain. Internal charge pump current is set to default 1 mA for this test. Charge pump current sets the PLL loop bandwidth, changing the charge current results into changes into PLL loop bandwidth response. Lower values of charge current reduces loop bandwidth of PLL improving rejection at higher frequency. PSMR plot 1.8-V as shown in Figure 2-4 gives relation of overall PLL loop bandwidth response to external supply rail for 1-mA charge pump current. As we see in Figure 3-1 the integrated noise up to 100-MHz bandwidth is -51.7 dBc.

The phase noise plot starts close to -95 dBc at 100-Hz offset which clearly implies that ripple and noise injected from supply post LC filtering is close to noise floor. TPS62913 ultra low noise DC-DC (16.8 uV RMS) powering 1.8-V PLL enables to achieves performance similar to Low Noise LDO powered solution.

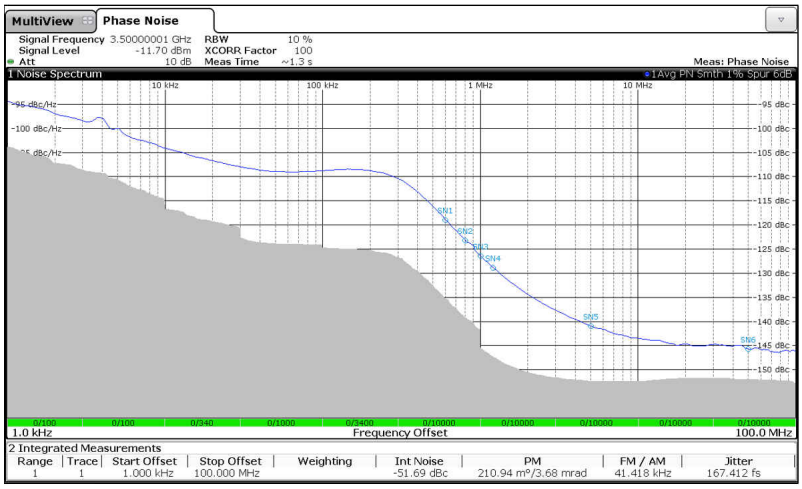

Figure 3-1. TX – Channel A Phase Noise Plot

3.3.2 EVM for FDD Mode

For EVM plot in FDD mode, all transmit and receive pairs are configured for 20-MHz 5G NR Spectrum set at 3.5 GHz. EVM waveform in Figure 3-2 indicates 0.33% average constellation deviation across symbols and first symbol peak deviation close to 1% which is well below the target of 2%. CH1 spectrum also represent in band spurious free spectrum for occupied bandwidth.

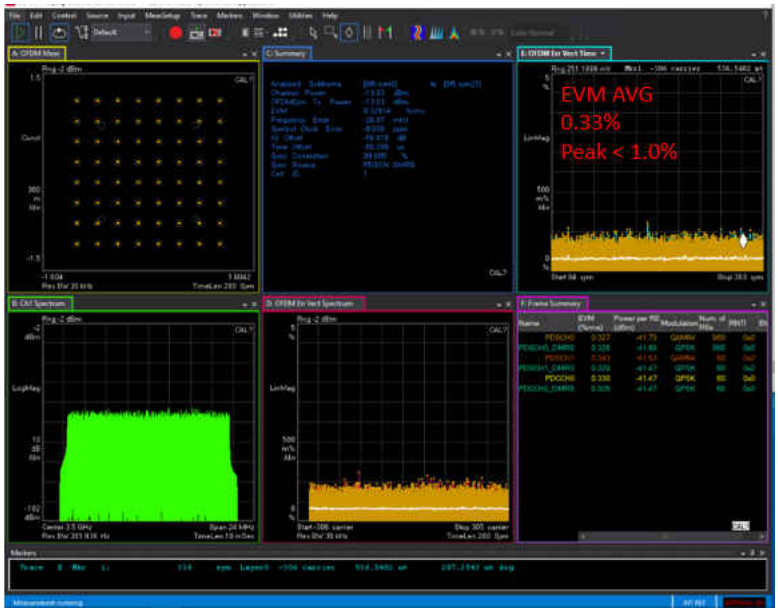

Figure 3-2. EVM for FDD Mode (5G NR Spectrum)

3.3.3 EVM for TDD Mode

For EVM plot in TDD mode all transmit and receive pairs are configured for 20-MHz 5G NR Spectrum set at 3.5 GHz. 75% Receive and 25% Transmit duty period of 100-Hz periodic pulse is generated using FPGA capture card and configured to toggle AFE8092 CPLD pins IO_DIFFIO-L4P and IO_DIFFIO-L4N.

EVM waveform in Figure 3-3 indicates 0.33% average constellation deviation across symbols and first symbol peak deviation close to 1% which is well below target of below 2%. CH1 spectrum also represent in band spurious free spectrum for occupied channel bandwidth.

Figure 3-3. EVM for TDD Mode (5G NR Spectrum)

In complete system applications with external PA, the RX to TX guard time can be adjusted such that the power supply is settled before data is transmitted on output channel.

3.3.4 RX Spectrum

The FFT spectral plot is shown for an input frequency of 3.51 GHz, NCO of 3.5. Figure 3-4 shows the performance of RX Single tone for AFE 89xx powered with DC/DC on all rails. No close-in spurious signal due to power supply switching ripple or beat frequency observed degrading the SNR and SFDR.

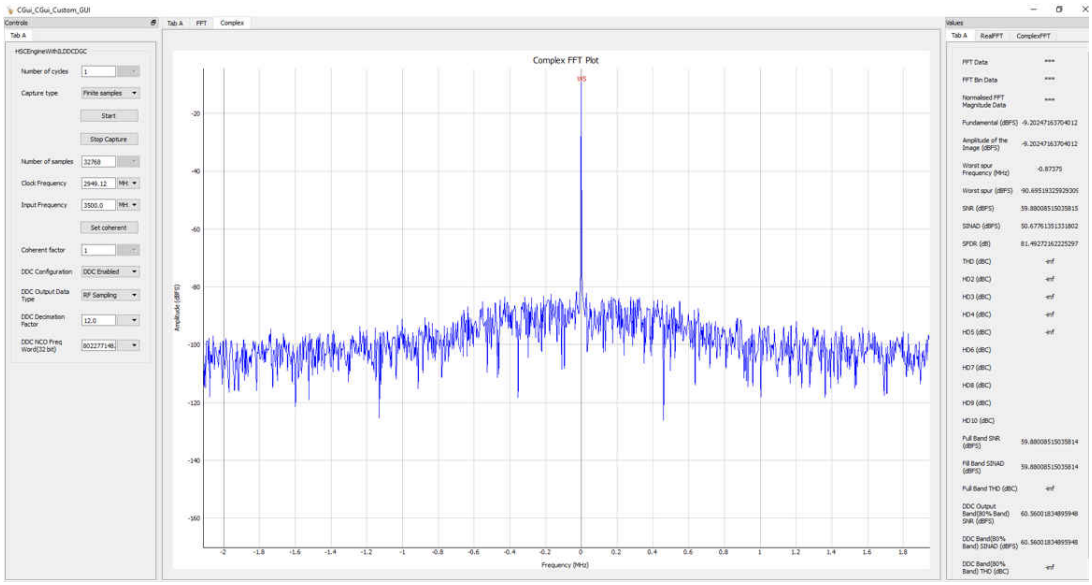

Figure 3-4. RX Single Tone Spectrum

3.3.5 Power Efficiency

To compare efficiency of proposed solution FDD and TDD 5G NR spectrum power consumption is observed using onboard INA226 monitoring bus voltage and group currents for 0.9-V, 1.2-V, 1.8-V and 3.3-V supply.

As shown in Table 3-1 in standby mode for 5-V Input supply the Power efficiency remains close to 92% while for FDD and TDD mode the total power efficiency is at 87.67% and 90%. For 12 V the standby, FDD and TDD modes the total power efficiency is at 85.2%, 87.3%, and 88.17%. With respect to traditional cascaded DC - DC plus LDO topology for all rails, the overall efficiency improvement observed is approximately 20%.

Table 3-1. Power Efficiency

Input voltage(V)	Input current(A)	Input power(W)	Standby/FDD/TDD	Volateg Label	Output voltage(V)	Output current(A)	Output Power (W) (Voltage Group)	Total Power(W)	Proposed DC-DC Solution PoL Efficiency (%)	Cascaded DC-DC + LDO (All Supply Rails) PoL Efficiency (%)
4.98	1.09	5.41	Standby	vcc 0.9	0.91	0.66	0.61	5.02	92.77	74.76
				vcc 3.3	3.29	0.47	1.55			
				vcc 1.2	1.19	0.70	0.83			
				vcc 1.8	1.79	1.06	1.91			
				pll 1.8	1.80	0.07	0.13			
12.04	0.49	5.86	Standby	vcc 0.9	0.91	0.66	0.60	5.01	85.42	71.15
				vcc 3.3	3.29	0.47	1.55			
				vcc 1.2	1.19	0.69	0.82			
				vcc 1.8	1.79	1.06	1.91			
				pll 1.8	1.80	0.07	0.13			
4.95	2.89	14.30	FDD	vcc 0.9	0.96	3.82	3.67	12.78	89.38	73.66
				vcc 3.3	3.29	0.47	1.55			
				vcc 1.2	1.14	3.75	4.28			
				vcc 1.8	1.78	1.76	3.14			
				pll 1.8	1.80	0.07	0.13			
12.00	1.22	14.58	FDD	vcc 0.9	0.97	3.83	3.69	12.81	87.85	65.42
				vcc 3.3	3.29	0.47	1.55			
				vcc 1.2	1.14	3.75	4.29			
				vcc 1.8	1.78	1.77	3.14			
				pll 1.8	1.80	0.07	0.13			
5.02	2.02	10.15	TDD	vcc 0.9	0.94	2.49	2.35	9.25	91.13	68.11
				vcc 3.3	3.29	0.47	1.55			
				vcc 1.2	1.16	2.39	2.79			
				vcc 1.8	1.79	1.36	2.43			
				pll 1.8	1.80	0.07	0.13			
12.03	0.87	10.48	TDD	vcc 0.9	0.94	2.49	2.35	9.27	88.43	67.33
				vcc 3.3	3.29	0.47	1.56			
				vcc 1.2	1.16	2.41	2.80			
				vcc 1.8	1.79	1.36	2.43			
				pll 1.8	1.80	0.07	0.13			

4 Conclusion

Following guidelines of PSMR plot and power supply load transient settling time, first symbol degradation and additional phase noise, Jitter can be minimized to desired specification.

We can summarize with captured waveform and test data that by paring low noise DC-DC TPS62913 and TPS543820 TI power products with TI AFE80xx AFE family, desired RF performance can be achieved.

Pairing AFE80xx with low noise DC-DC operating in fixed frequency mode with ACM (Advance Current Mode) control to achieve fast load transient response and secondary passive L-C closed loop filtering enables a drastic reduction of phase noise jitter and inter modulation spurious in RF spectrum.

5 References

- Texas Instruments, *AFE7920, Four-transmit Four-Receive RF-Sampling Transceiver with Dual-Band DUC/DDC and Two Feedback Paths* data sheet.
- Texas Instruments, *TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter with Integrated Ferrite Bead Filter Compensation* data sheet.
- Texas Instruments, *High-Efficiency, Low-Output Ripple Power Supply Reference Design for Imaging Application*.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2021) to Revision B (November 2021)	Page
• Changed *External Clock Synchronization* figure	6

Changes from Revision * (July 2021) to Revision A (August 2021)	Page
• Updated image and the description	6
• Added an additional reference	13

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