Application Note

Key Register Configuration of BQ25890H for PPS/HVDCP and BC1.2 Power Source

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ABSTRACT

In smart-phone applications, the unit for charging plays a very important role because the charging unit needs to detect a correct charging port such as DCP/SDP/HVDCP to finish a safe and correct charging process. The charging unit includes different charging protocols to identify different charging source, such as BC1.2 and other special fast charging protocol so as to execute correct charging profile in charging control unit. This application note provides a key register configuration to assist software design engineers to drive BQ25890H and BQ25891H efficiently. Besides standard BC1.2, this document also includes a detailed description to drive PPS (Program Power Supply)/HVDCP source so as to realize fast charging with higher efficiency.

Table of Contents

List of Figures

List of Tables

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1 Introduction

Key register configuration for BC1.2 standard AC adapter and PPS AC adapter with higher efficiency. The configuration includes design structure and a sample for reference.

2 DPDM Structure of BQ25890H

2.1 DPDM Block Diagram and Working Flow Chart

Figure 2-1 shows that when DCP is detected, the device initiates adjustable high voltage adapter handshake including MaxCharge™, and so on. The handshake connects combinations of one or more voltage sources and or current sink on D+/D- to signal input source to raise output voltage from 5 V to 9 V/12 V. The adjustable high voltage adapter handshake can be disabled by clearing MAXC_EN and or HVDCP_EN bits.

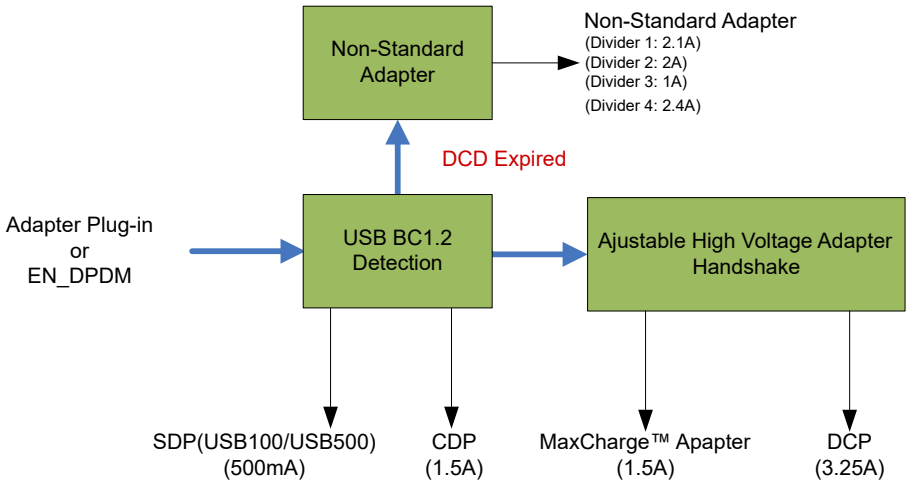

Figure 2-1. DPDM Detection Process

Also, we can get same conclusion from Figure 2-2, HVDCP/MaxCharge detection only happens after DCP/CDP detection, otherwise, it does not trigger HVDCP/MaxCharge detection, such as, if the result of BC1.2 detection is SDP, it cannot move forward to HVDCP/MaxCharge detection process.

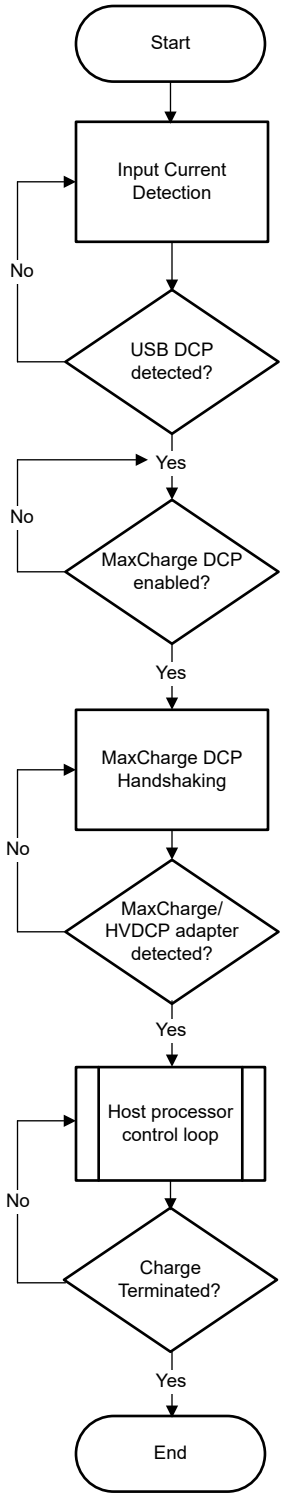

Figure 2-2. DPDM Working Flow Chart

2.2 Key Register Configuration for BC1.2/HVDCP Standard Power Source with DPDT Signal Switch

In Figure 2-3, the description for DPDT switch is highlighted with a RED colored dashed line). Normally, the default connection for DPDT is always connected to AP (Host) side, after external device identification by CC port (assumes USB-Type C® port), such as DFP mode. The DPDT switch will be switched to BQ25890H DPDM side by AP (Host) commanding, then BQ25890H starts charging port identification process.

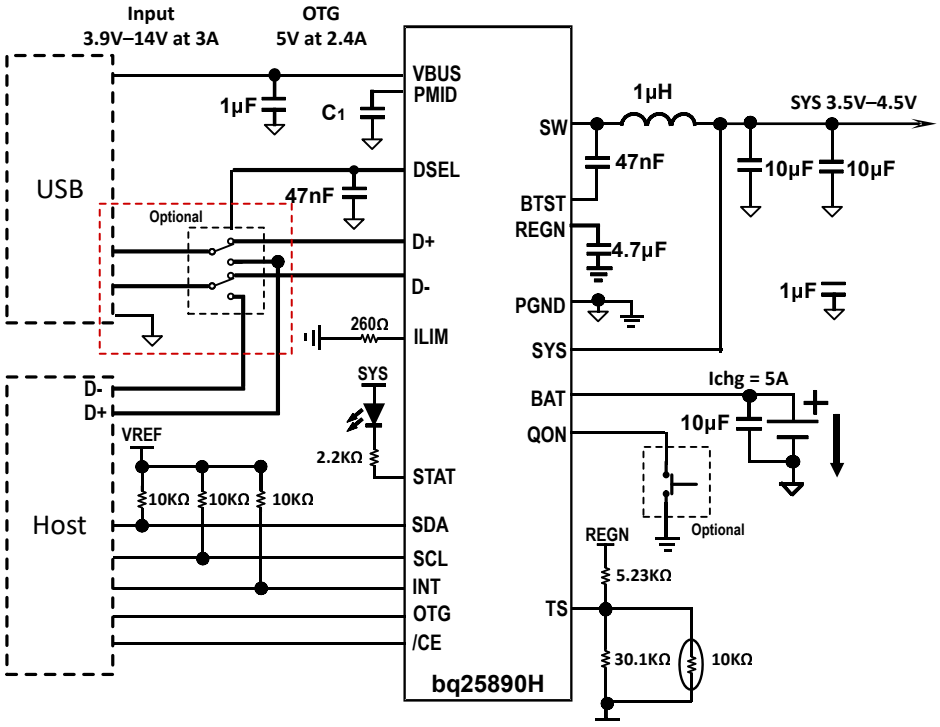

Figure 2-3. Typical Simple Schematic With DPDT Switch

Key register configuration for boot charging:

Step 1:

When external AC adapter is plugged into PD (Portable Device) AP (Host) must be configured

REG02, Bit 0=0, disable Auto DPDM detection

Bit Description:

Bit0: Automatic D+/D- Detection Enable

0 –Disable D+/D- or PSEL detection when VBUS is plugged-in

1 –Enable D+/D- or PEL detection when VBUS is plugged-in (default)

Step 2:

After finishing external device identification such as DFP by CC logic, AP (Host) will drive DPDT switch to connect to BQ25890H DPDM pin, meanwhile, AP (Host) must be configured

REG02, Bit1=1, force DPDM detection

Bit Description:

Force D+/D- Detection

0 – Not in D+/D- or PSEL detection (default)

1 – Force D+/D- detection

Step 3:

After identification, BQ25890H will send out INT to AP(Host), then AP(Host) will receive the type of adapter by reading,

REG0B Bit5 to Bit7

Bit description:

VBUS Status register

000: No Input

001: USB Host SDP

010: USB CDP (1.5A)

011: USB DCP (3.25A)

100: Adjustable High Voltage DCP (MaxCharge) (1.5A)

101: Unknown Adapter (500mA)

110: Non-Standard Adapter (1A/2A/2.1A/2.4A)

111: OTG Note: Software current limit is reported in IINLIM register

Step 4:

AP (Host) will configure BQ25890H charging profile and start charging process according to type of AC adapter.

2.3 Key Register Configuration for BC1.2/HVDCP Standard Power Source Without DPDT Signal Switch

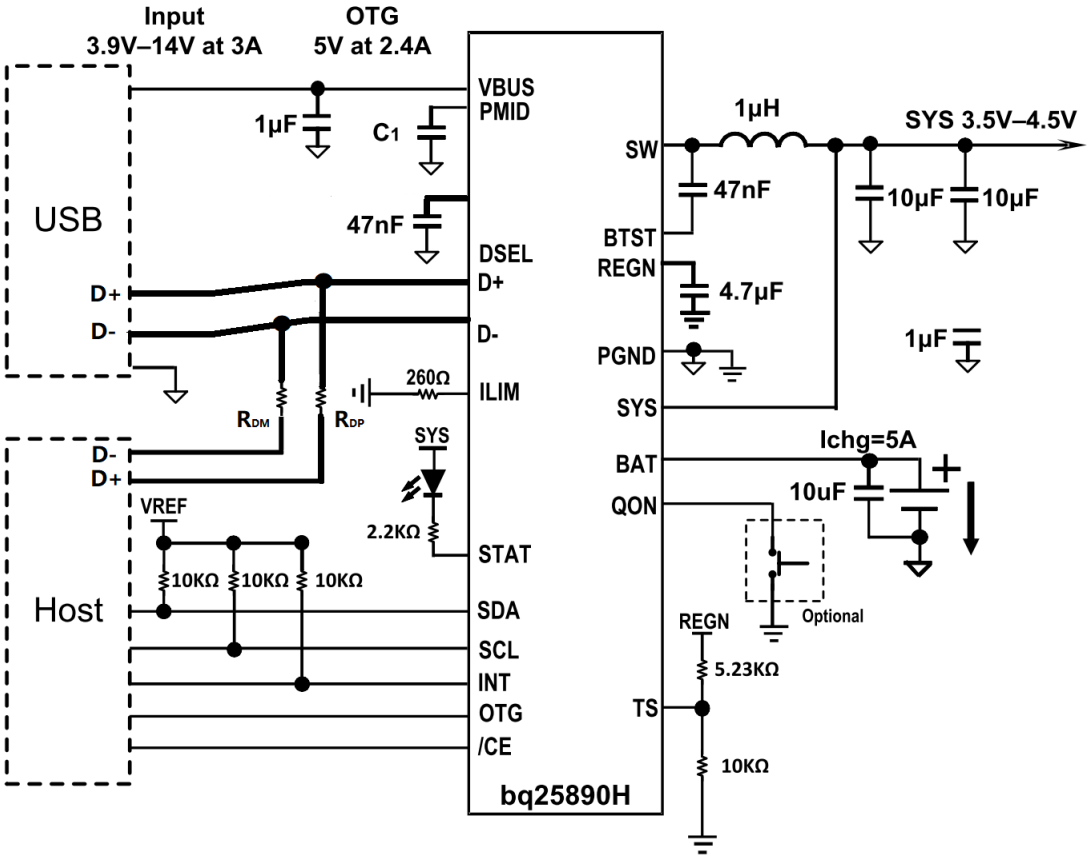

Figure 2-4. Typical Simple Schematic Without DPDT Switch

Sometimes, for lower cost consideration, DPDT switch is saved, so the DPDM pin of BQ25890H will be connected to AP(Host) and USB port by R_{DP} and R_{DM} resistor, please note, the resistance of R_{DP} and R_{DM} must be adjusted according to eye-diagram quality of USB signal.

Step1:

When AC adapter is plugged in PD, BQ25890H can start AC adapter identification process, keep

REG02, Bit 0=1, enable Auto DPDM detection (keep default)

Description:

Bit0: Automatic D+/D- Detection Enable

0 –Disable D+/D- or PSEL detection when VBUS is plugged-in

1 –Enable D+/D- or PEL detection when VBUS is plugged-in (default)

Step2:

After identification, BQ25890H will send out INT to AP, then AP will get type of adapter by reading,

REG0B Bit5 to Bit7

Bit description:

VBUS Status register

000: No Input

001: USB Host SDP

010: USB CDP (1.5A)

011: USB DCP (3.25A)

100: Adjustable High Voltage DCP (MaxCharge) (1.5A)

101: Unknown Adapter (500mA)

110: Non-Standard Adapter (1A/2A/2.1A/2.4A)

111: OTG Note: Software current limit is reported in IINLIM register

Step3:

AP (Host) will configure BQ25890H charging profile and start charging process according to type of AC adapter.

2.4 Fast Charging Configuration for PPS/HVDCP Power Source with BQ25890H

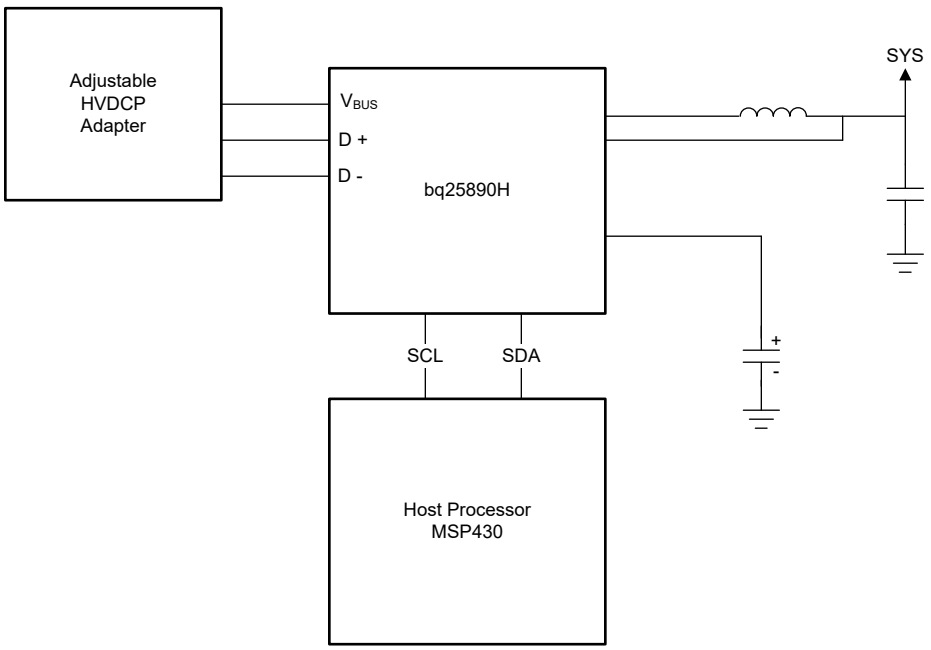

Figure 2-5. Simplified Schematic of BQ25890H for PPS/HVDCP Power Source

2.4.1 Working Mechanism with PPS/HVDCP Source

In general, for higher efficiency and power in fast charging mode, PPS/HVDCP power source would be better candidate compare to fixed 5-V adapter. BQ25890H can support this kind of application by using programmable DPDM interface. Design engineer can monitor the status of IINDPM/VINDPM in BQ25890H to adjust PPS/HVDCP output voltage so as to meet target charging power, such as 18 W or more. IINDPM means, when the output power of PPS/HVDCP adapter cannot reach target charging power, BQ25890H will indicate IINDPM signal to AP, AP will send control command to PPS/HVDCP adapter by DPDM port to ask more power from PPS/HVDCP adapter, or increase the output voltage of PPS/HVDCP adapter until target charging power is satisfied. Meanwhile, higher output voltage of AC adapter can decrease power dissipation on the cable of AC adapter further. Another option is that if IINDPM is not triggered but target charging current is reached, it means the output voltage of adapter would be a little higher than expected, so AP will send command to adapter to decrease voltage of adapter to get higher efficiency (lower differential voltage between input and output in buck charger will get higher efficiency).

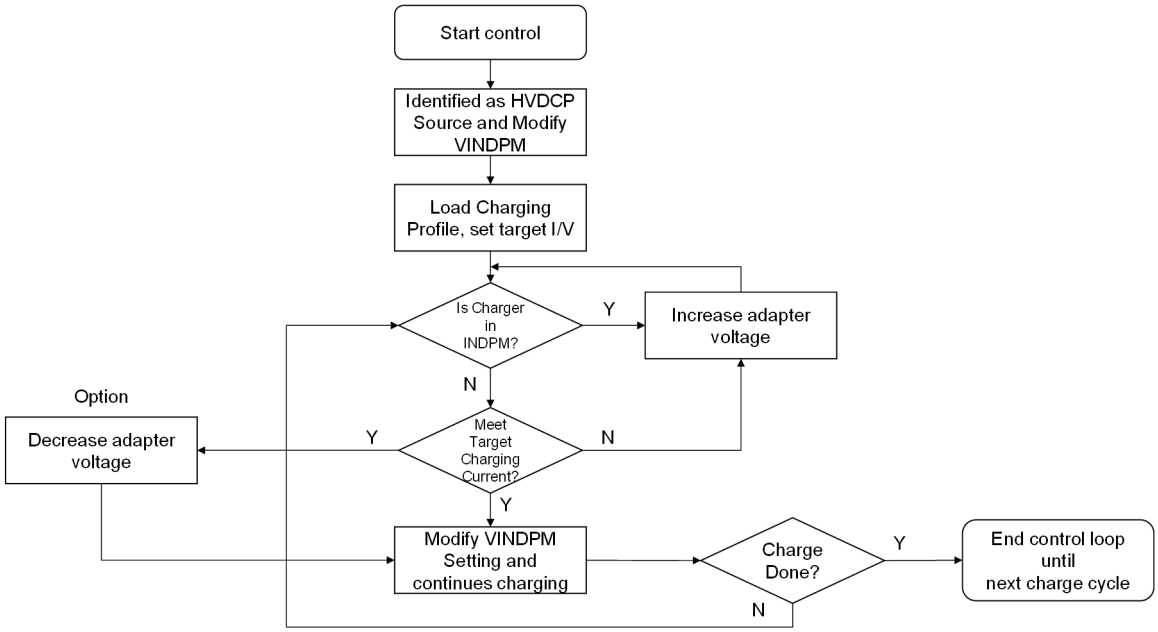

Figure 2-6. HVDCP/PPS Fast Charging Flow Chart

2.4.2 Programmable D+/D– Output Driver Introduction in BQ25890H

The bq25890H allows each of the D+/D– lines to be controlled independently to output one of the preset voltage levels (0 V, 0.6 V, 1.2 V, 2.0 V, 2.7 V, 3.3 V, and HiZ). Each line can be set to one of these presets over I^2C. This allows the implementation of a handshaking protocol between the charger and an adapter with an interface that allows adjusting the voltage, such as the CHY100 and CHY103 interfaces. Since the adapter voltage is controllable, the operating point of the charger can be fine-tuned to ensure high efficiency during charging. In addition, higher voltages allow enabling efficient high-charge currents. As a byproduct, charge time is decreased, making it even more appealing for high-capacity cells. REG01 of the bq25890H includes the bits needed to control the D+/D– output driver. The host processor can communicate through I 2 C to the charger, and modify this register to emulate the relevant adapter interface. This register also includes the bits to enable detection of HVDCP and MaxCharge adapters during the input current detection.

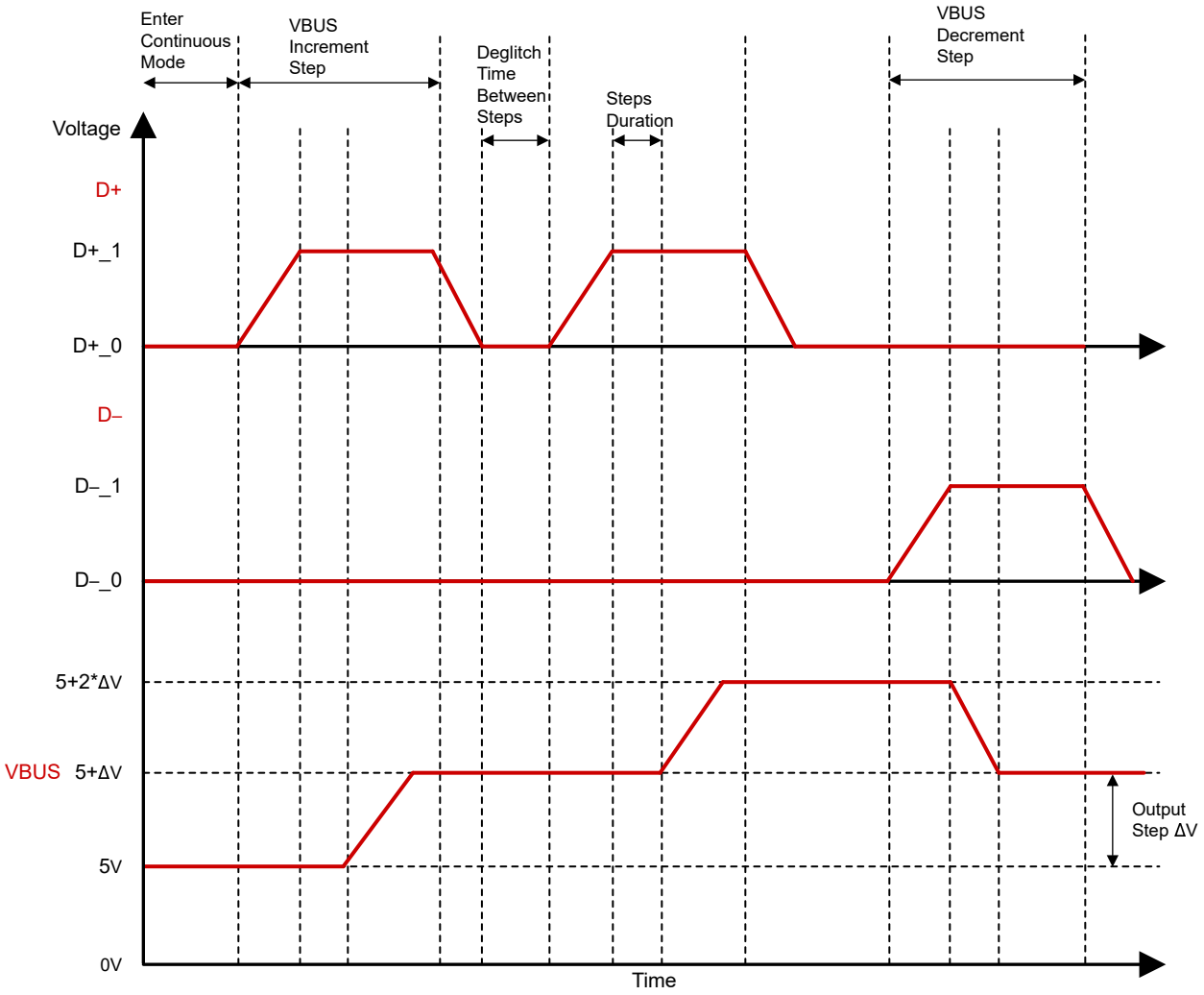

Figure 2-7. Adjustable Adapter Output Step by DPDM Interface

Figure 2-7 represents an example of how this behavior looks after implementing the increase or decrease functions, where Dx_y represents the specific D+ or D- thresholds based on the protocol used and ΔV, the resolution of the output voltage steps. D+/D- can generate multiple pulse signal periodicity through AP configuring. By adopting different D+ and D- pulse signal combination to increase or decrease output of adapter, for example, to adjust output power of adapter dynamically.

Table 2-1. DPDM Bit Adjustment in REG01

Bit	Field	Type	Reset	Description
7	DP_DAC[2]	R/W	by REG_RST	D+ Pin Output Driver 000 – HiZ mode (Default) 001 – 0 V (V_{0P0_VSRC}) 010 – 0.6 V (V_{0P6_VSRC}) 011 – 1.2 V (V_{1P2_VSRC}) 100 – 2.0 V (V_{2P0_VSRC}) 101 – 2.7 V (V_{2P7_VSRC}) 110 – 3.3 V (V_{3P3_VSRC}) 111 – Reserved Register bits are reset to default value when input source is plugged-in and can be changed after D+/D- detection is completed.
6	DP_DAC[1]	R/W	by REG_RST	
5	DP_DAC[0]	R/W	by REG_RST	
4	DM_DAC[2]	R/W	by REG_RST	D- Pin Output Driver 000 – HiZ mode (Default) 001 – 0 V (V_{0P0_VSRC}) 010 – 0.6 V (V_{0P6_VSRC}) 011 – 1.2 V (V_{1P2_VSRC}) 100 – 2.0 V (V_{2P0_VSRC}) 101 – 2.7 V (V_{2P7_VSRC}) 110 – 3.3 V (V_{3P3_VSRC}) 111 – Reserved Register bits are reset to default value when input source is plugged-in and can be changed after D+/D- detection is completed.
3	DM_DAC[1]	R/W	by REG_RST	
2	DM_DAC[0]	R/W	by REG_RST	
1	EN_12V	R/W	by REG_RST	Enable 12 V detection for MaxCharge and HVDCP 0 – Disable 12 V Detection (default) 1 – Enable 12 V Detection
0	VINDPM_OS	R/W	by REG_RST	Input Voltage Limit Offset 0 – 400 mV 1 – 600 mV (default)

3 References

- Texas Instruments, *BQ25890H I2C Controlled Single Cell 5-A Fast Charger with MaxCharge™ Technology for High Input Voltage and Adjustable Voltage USB On-the-Go Boost Mode*, data sheet.
- Texas Instruments, *bq25890EVM, bq25892EVM, bq25895EVM, bq25896EVMand bq25895MEVM(PWR664)*, user's guide.
- Texas Instruments, *Handshaking Between Adjustable HVDCP Adapters and Battery Chargers*, application note.
- Texas Instruments, *DPDM Control Process Evaluation in BQ2589x Family Supporting HVDCP MaxCharge* application note.

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