Application Brief

TPS7H1111-SP Pin Failure Mode Analysis (FMA)

This application brief provides a *Failure Mode Analysis* (FMA) for the pins of the TPS7H1111-SP ultra-low noise, high PSRR, LDO. The failure conditions covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 1)
- Pin short-circuited to V_{IN} supply (see Table 2)
- Pin short-circuited to V_{OUT} supply (see Table 3)
- Pin open-circuited (see Table 4)
- Pin short-circuited to an adjacent pin (see Table 5)

In the tables below, *damage* means there is a possibility of immediate device damage, gradual device damage, or lifetime reductions. It only encompasses damage of the device itself, not upstream or downstream components. *Functional* means the device as a whole behaves as described in the data sheet (although this does not necessarily mean the device is regulating). This analysis was considered for the schematic shown in Figure 3 with a resistive 0.5-A load. See comments in the tables below for details on each situation.

This analysis was considered primarily for the ceramic HBL 14-pin package of the TPS7H1111-SP device. However, most results are also applicable for the plastic PWP 28-pin package of the TPS7H1111-SP and TPS7H1111-SEP devices.

Figure 1 and Figure 2 show the TPS7H1111-SP pin diagrams for the CFP and HTSSOP packages. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7H1111-SP data sheet.

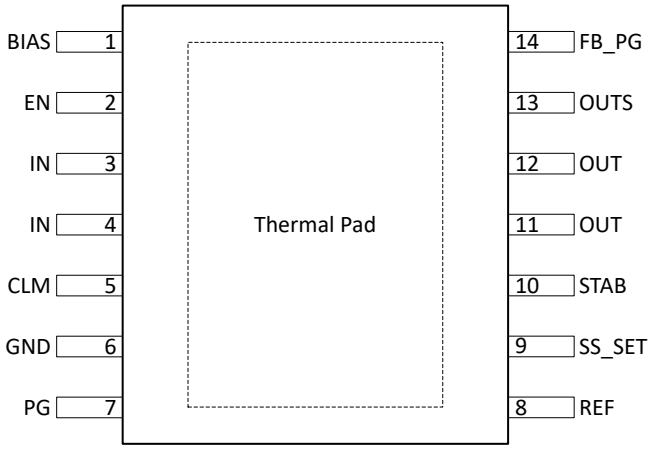

Figure 1. Pin Diagram (CFP) Package

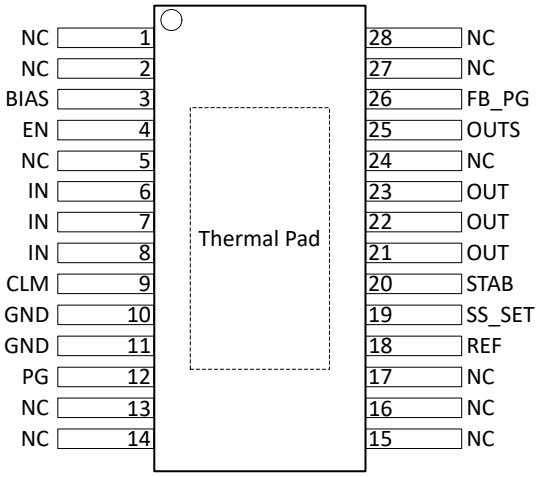

Figure 2. Pin Diagram (HTSSOP) Package

HBL Package
14-Pin CFP
Top View

PWP Package
28-Pin HTSSOP
Top View

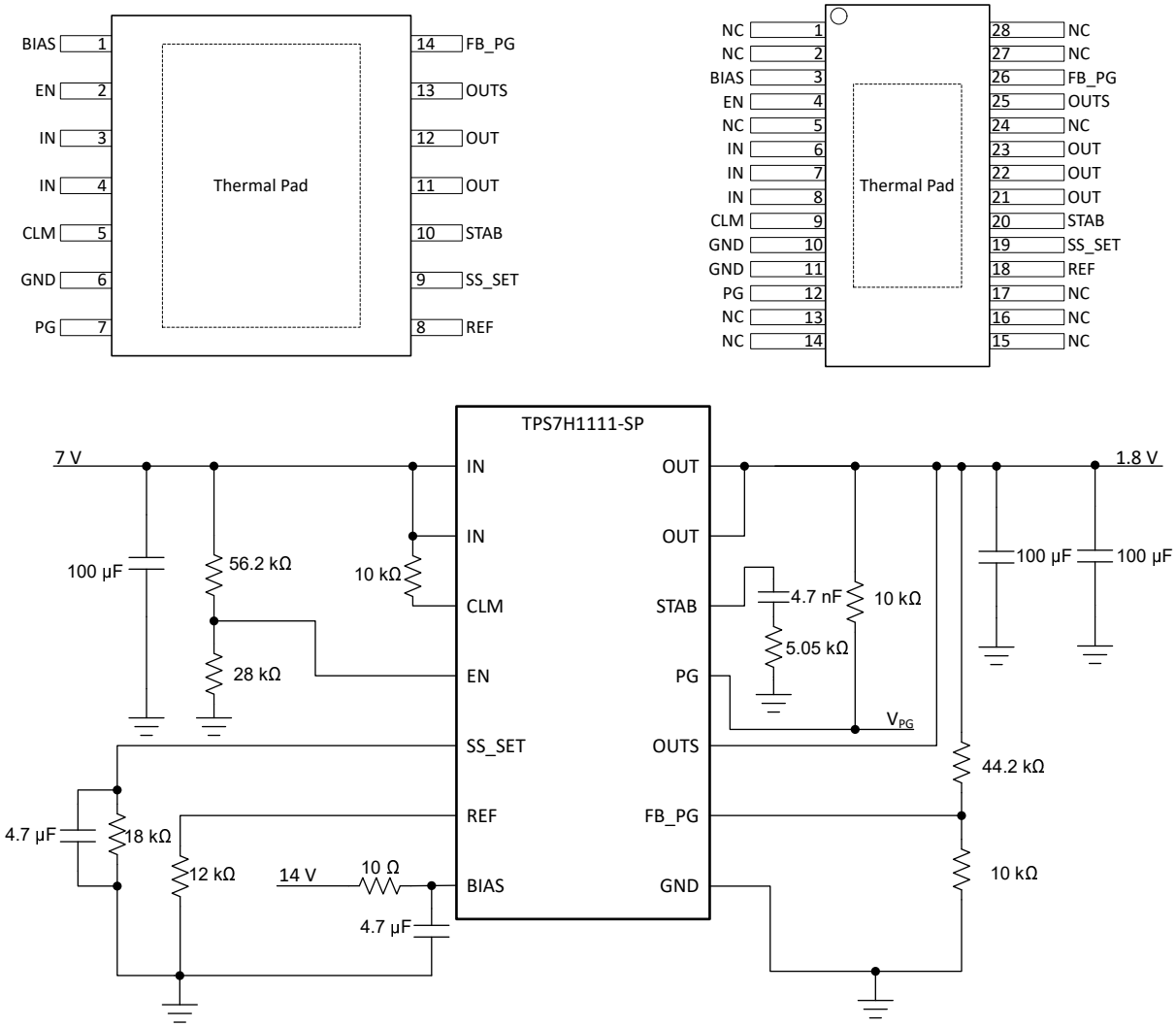

Figure 3. Device Schematic for Pin FEA

Table 1. Pin Short-Circuited to Ground

Pin Name	Pin No.	Damage	Functional	Description of Potential Failure Effects
BIAS	1	No	Yes	Device turns off (enters UVLO).
EN	2	No	Yes	Device turns off (disabled).
IN	3	Yes	Yes	If both IN pins are shorted, the device is below internal UVLO and therefore turns off. If only one is shorted there will be a potentially damaging overcurrent event between the two pins.
IN	4	Yes	Yes	
CLM	5	No	Yes	Normal operation – device configured for turn-off current limit mode. If CLM was previously connected directly to V_{IN} when the short to ground occurs, a short circuit could result, potentially causing damage. As the schematic shows a 10 kΩ pull-up to V_{IN}, damage is not expected.
GND	6	N/A	N/A	N/A
PG	7	No	Yes	Pin remains at 0 V since it is an open-drain pin and doesn't have an internal pull-up voltage.
REF	8	Yes	No	An overcurrent event occurs on the REF pin that could cause damage. Additionally, this may cause improper biasing in other circuits which could cause other failures.
SS_SET	9	No	Yes	Device regulates to 0 V output. If FB_PG falls below $V_{FB\_PG(rising)} – V_{FB\_PG(HYS)}$, the 2-mA current will turn-on and flow out of this SS_SET pin.
STAB	10	No	No	The pass element turns-on which could cause entering of current limit or the output to rise above the programmed SS_SET value. While device damage isn't expected, downstream circuitry may be damaged. Damage would be expected if this short occurred while the device was powered but disabled as STAB is internally driven high. This would cause excessive current on STAB which may cause damage.
OUT	11	Yes	Yes	Short circuit protection activated to prevent immediate damage; not intended for prolonged operation.
OUT	12	Yes	Yes	
OUTS	13	Yes	Yes	The device senses 0 V on the output and therefore will regulate to the maximum voltage possible. However, this 0 V on OUTS causes improper internal biasing which may cause unexpected voltage stresses which may cause damage over time. Additionally, since OUTS is externally connected to OUT, this could cause a high current path externally, potentially causing external damage.
FB_PG	14	Yes	Yes	Device enters soft start mode and outputs 2 mA on the SS_SET pin which causes a higher output voltage. The device itself will be fine unless it reaches current limit and remains in constant current limit for a prolonged period of time.

Table 2. Pin Short-Circuited to V_{IN}

Pin Name	Pin No.	Damage	Functional	Description of Potential Failure Effects
1	BIAS	Yes	Yes	If V_{BIAS} is higher than V_{IN} then the device may stop properly regulating since the proper bias voltage isn't supplied. If V_{IN} is an acceptable bias supply then the device may continue operating properly. If V_{BIAS} is higher than 7 V, the IN pins are overstressed and damage occurs.
2	EN	No	Yes	Device turns on.
3	IN	N/A	N/A	N/A
4	IN	N/A	N/A	
5	CLM	No	Yes	Normal operation – the device is configured for brick-wall current limit mode. If CLM was previously connected directly to GND when the short to V_{IN} occurs, a short circuit could result, potentially causing damage. If the CLM was pulled-down to GND through a 10 kΩ pull-down to GND, damage is not expected.
6	GND	Yes	No	Improper grounding could cause damage to various internal circuits.
7	PG	Yes	Yes	If PG is asserted and it's directly shorted to V_{IN} an excessive amount of current will flow through this pin causing damage.
8	REF	Yes	No	Current flows into REF which damages the device and stops proper regulation.
9	SS_SET	Yes	No	Current flows into SS_SET which damages the device and stops proper regulation
10	STAB	Yes	No	The pass element turns-off. However, excessive current on STAB may cause damage.
11	OUT	Yes	Yes	Device stops regulation as the control loop senses the output is too high and turns-off the pass element. However, this causes improper internal error amplifier biasing which may cause unexpected voltage stresses which cause damage over time.
12	OUT	Yes	Yes	
13	OUTS	Yes	Yes	Device stops regulation as the control loop senses the output is too high and turns-off the pass element. However, this causes improper internal error amplifier biasing which may cause unexpected voltage stresses which cause damage over time.
14	FB_PG	Yes	No	If V_{IN} > 6 V, this exceeds the recommended operating conditions leading to improper internal biasing which could cause functional failures. If V_{IN} < 6 V, the device is unable to enter soft start mode and PG is always asserted; otherwise operation proceeds as normal. The lack of soft start may result in current limit being reached during startup.

Table 3. Pin Short-Circuited to V_{OUT}

Pin Name	Pin No.	Damage	Functional	Description of Potential Failure Effects
1	BIAS	Yes	No	The device stops regulating or reduces output voltage as there is not enough V_{BIAS} to V_{OUT} headroom. If V_{BIAS} is above 7 V, it will cause improper overvoltage within the error amplifier which causes damage.
2	EN	No	Yes	As long as V_{OUT} is above the $V_{EN(rising)}$ threshold it stays on and continues regulating, otherwise the device turns off.
3	IN	Yes	Yes	The device stops regulation as V_{OUT} rises to V_{IN} and the control loop senses the output is too high and turns-off the pass element. However, this causes improper internal error amplifier biasing which may cause unexpected voltage stresses which cause damage over time.
4	IN	Yes	Yes	
5	CLM	Yes	No	The current limit mode is not well controlled since it changes with output voltage. This can lead to excess V_{IN} current from input buffer shoot-through.
6	GND	Yes	No	Causes current limit on V_{OUT}. The device is not intended to remain in constant current limit for a prolonged period of time. Additionally, if the GND pin is no longer the system ground, the improper grounding could cause damage to various internal circuits.
7	PG	Yes	Yes	If PG is asserted and it's directly shorted to V_{OUT}, an excessive amount of current will flow through this pin.
8	REF	Yes	No	Current flows into or out of REF which damages the device and stops proper regulation
9	SS_SET	Yes	No	Since V_{SS_SET} is nominally equal to V_{OUT} there is no immediate damage as long as SS_SET is able to continue sourcing its current; however, there could be a complicated interaction causing too high of an output voltage or an attempt to sink current through the OUT pin causing damage.
10	STAB	No	No	When enabled, the pass element turns mostly-off. When disabled, forcing STAB to 0 V will cause higher V_{BIAS} current to flow, which could cause damage.
11	OUT	N/A	N/A	N/A
12	OUT	N/A	N/A	
13	OUTS	No	Yes	Nominal operation.
14	FB_PG	No	Yes	When V_{OUT} rises above the $V_{FB\_PG(rising)}$ threshold, PG is asserted and the fast-start current turns off (resulting in a longer startup time).

Table 4. Pin Open Circuited

Pin Name	Pin No.	Damage	Functional	Description of Potential Failure Effects
BIAS	1	No	No	Device stops regulating as there is no V_{BIAS} voltage.
EN	2	No	No	Device may oscillate on and off.
IN	3	Yes	Yes	If only one pin is floating then current will go through the other pin causing the current of the individual pin to be too large, eventually causing damage.
IN	4	Yes	Yes	
CLM	5	Yes	No	The current limit mode is not well controlled. Additionally, an undefined voltage on the CLM input buffer will cause additional V_{IN} shoot-through current to flow, which could damage the device.
GND	6	Yes	No	Improper biasing is expected to cause oscillations with large current spikes.
PG	7	No	No	PG will work when pulled-down but since it's an open drain it cannot go high and will be in an unknown state.
REF	8	No	No	The reference current will not be created and therefore the part will output 0 V when attempting to regulate.
SS_SET	9	Yes	No	A 100 µA will attempt to be forced out of this pin causing it to reach a high voltage. This may result in improper internal error amp biasing, causing overvoltage failures.
STAB	10	No	Yes	The control loop response will be different with potentially worse phase margin, but the part is still operational.
OUT	11	Yes	Yes	If only one pin is floating then current will go through the other pin causing the current of the individual pin to be too large, eventually causing damage.
OUT	12	Yes	Yes	
OUTS	13	Yes	No	The device will not know what voltage to regulate to and will likely oscillate, potentially causing damage.
FB_PG	14	Yes	No	Device fast start current will oscillate, potentially causing damage.

Table 5. Pin Short-Circuited to Adjacent Pin Circuited

Pin Name	Pin No.	Short to Pin No.	Short to Pin Name	Damage	Functional	COMMENTS
BIAS	1	2	EN	Yes	Yes	Depending on the bias supply voltage, the device will be turned on or turned off. If the bias voltage is over 7 V, the EN pin is overstressed.
EN	2	3	IN	No	Yes	Depending on the input supply voltage, the device will be turned-on or turned-off.
IN	3	4	IN	No	Yes	Normal operation
IN	4	5	CLM	No	Yes	Normal operation – the device is configured for brick-wall current limit mode. If CLM was previously connected directly to GND when the short to V_{IN} occurs, a short circuit could result, potentially causing damage. If the CLM was pulled-down to GND through a 10 kΩ pull-down to GND, damage is not expected.
CLM	5	6	GND	No	Yes	Normal operation – device configured for turn-off current limit mode. If CLM was previously connected directly to V_{IN} when the short to ground occurs, a short circuit could result, potentially causing damage. As the schematic shows a 10 kΩ pull-up to V_{IN}, damage is not expected.
GND	6	7	PG	No	Yes	PG remains at 0 V since it's an open drain and doesn't have an internal pull-up voltage.
REF	8	9	SS_SET	Yes	No	The V_{REF} voltage will be unstable since it cannot handle large output capacitance and SS_SET will always be 1.2 V. This control loop instability may cause damage.
SS_SET	9	10	STAB	Yes	No	The STAB voltage will rise as it is charged by the SS_SET pin current source. This causes the pass element to slowly turn-off. However, the SS_SET and OUT voltages will be unstable since STAB components are impacted by the RC of SS_SET. This may cause improper overvoltage within the internal error amplifier, causing damage.
STAB	10	11	OUT	No	No	When enabled, the pass element turns partially-off. When disabled, forcing STAB to 0 V will cause higher V_{BIAS} current to flow, which could cause damage.
OUT	11	12	OUT	No	Yes	Normal operation.
OUT	12	13	OUTS	No	Yes	Normal operation.
OUTS	13	14	FB_PG	No	Yes	Since OUTS is connected to OUT, when V_{OUT} rises above the $V_{FB\_PG(rising)}$ threshold, PG is asserted and the fast-start current turns off (resulting in a longer startup time).

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