User's Guide
SLVU407–October 2010

TPS80010EVM

This user's guide describes the characteristics, operation, and use of the TPS800100's evaluation module (EVM). The EVM demonstrates the Texas Instruments TPS80010 IC. This document includes setup instructions, a schematic diagram, a bill of materials, and printed-circuit board layout drawings for the EVM.

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1 Introduction

The TPS80010's evaluation module (EVM) helps designers evaluate the operation and performance of the TPS80010 IC.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the EVM.

2.1 Input/Output Connector Descriptions and Default Configuration

The default configuration mimics the application mode of the TPS80010, which allows users to evaluate the functionality.

	Default Configuration	Comment
J1	connect	Overall Power Entry
J2	Open	4-wire connector for VIN_BUCK
J3	Open	4-wire connector for VO_BUCK
J8	Open	4-wire connector for VIN_VIO
J9	Open	4-wire connector for VO_VIO
J11	Open	4-wire connector for IN_VM
J12	Open	4-wire connector for OUT_VM
J14	Open	4-wire connector for VIN_BOOST
J15	Open	4-wire connector for VO_BOOST
J19		Monitoring point for battery check
JP1	Open	Socket for insert load resistor for VO_BUCK
JP2	Open	Socket for insert load resistor for VO_VIO
JP3	Open	Socket fot insert load resistor for OUT_VM
JP4	Open	Socket for Battery monitor resistor network
JP5	Open	Socket for Battery monitor resistor network
JP6	Open	Socket for Battery False Load resistor
JP7	Open	Socket for Boost Load Resistor
JPS1	Close	Connects VBAT with VIN_BUCK
JPS3	Close	Connects PG pin with LED indication circuit
JPS4	Close	Connects VIO with IN_VIO1/2
JPS5	Close	Connects VO_BOOST with IN_VM
JPS6	Close	Connects VBAT with VIN_BOOST
JPS7	Close	Connects VBAT with PP_VBAT
JPS8	Close	Connects VBAT with LED indication circuit
JPS9	short pin 1 and 2	EN_SW1 high
JPS10	short pin 1 and 2	EN_BOOST high
JPS11	short pin 1 and 2	EN_LDO high
JPS12	short pin 1 and 2	EN_BAT_CHECK high
JPS13	short pin 1 and 2	BAT_FALSLOAD_EN high
JPS14	short pin 1 and 2	EN_BUCK high
JPS15	short pin 2 and 3	MODE_BUCK low
JPS16	short pin 2 and 3	TEST1 low
JPS17	open	TEST2 HIGH Z

2.2 Other Configurations

Additional configurations are possible for performance evaluation. For example, based on the default configuration, disconnecting JPS5 and JPS6, it is possible to evaluate the standalone performance of the boost regulator by using the 4-wire connectors J14 and J15.

3 Operation

This section provides information about the operation of the TPS80010's EVM.

Connect the positive terminal of a 3 V power supply to J1 terminal 1 and connect the power supply's ground terminal to J1 terminal 2.

Default configuration test point measurements are as follows:

J17 (Boost output) – 3.1 V
J13 (Boost post regulation LDO output) – 3.0 V
J6 (Buck output) – 1.8 V
J10 (Buck load switch output) – 1.8 V

4 Board Layout

This section provides the TPS80010's EVM board layout.

4.1 Layout

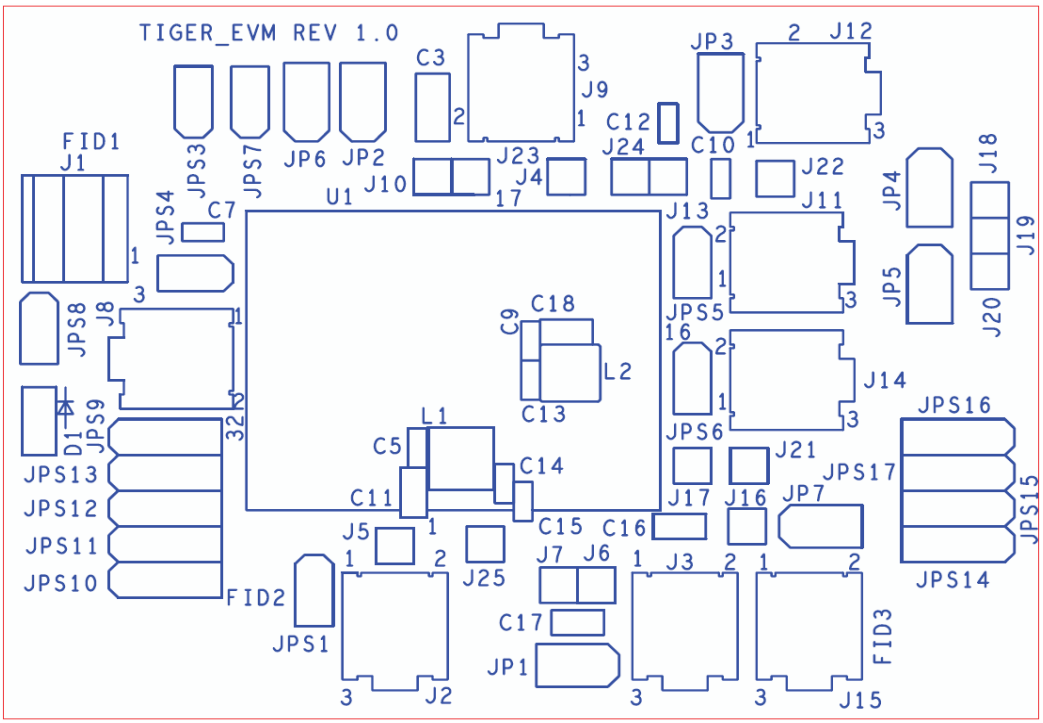

Figure 1. Top Layer Silkscreen

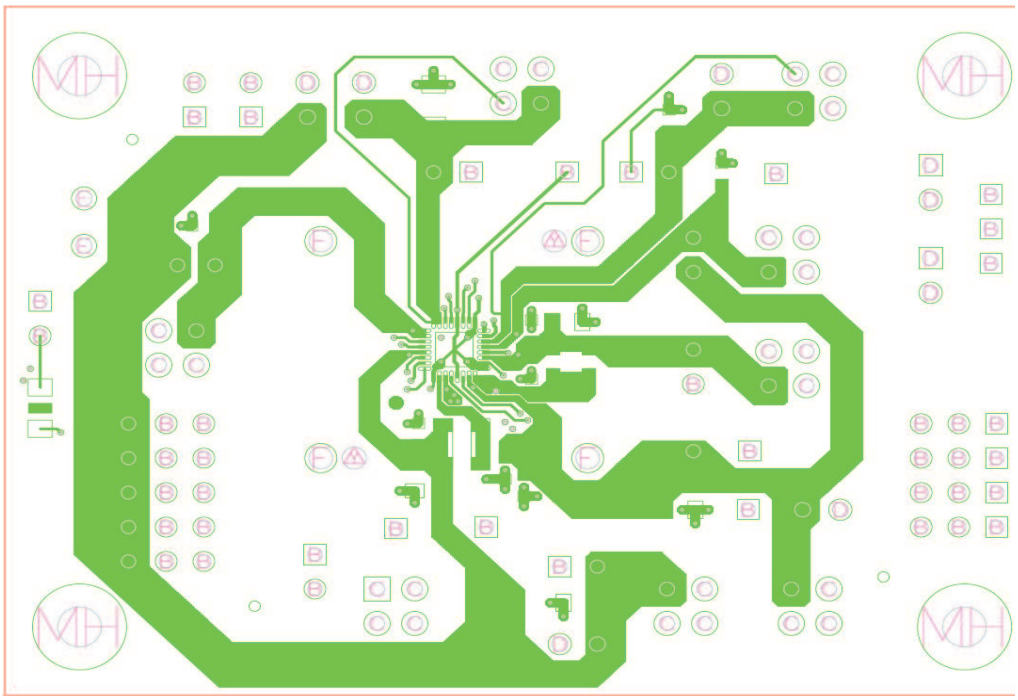

Figure 2. Top Layer

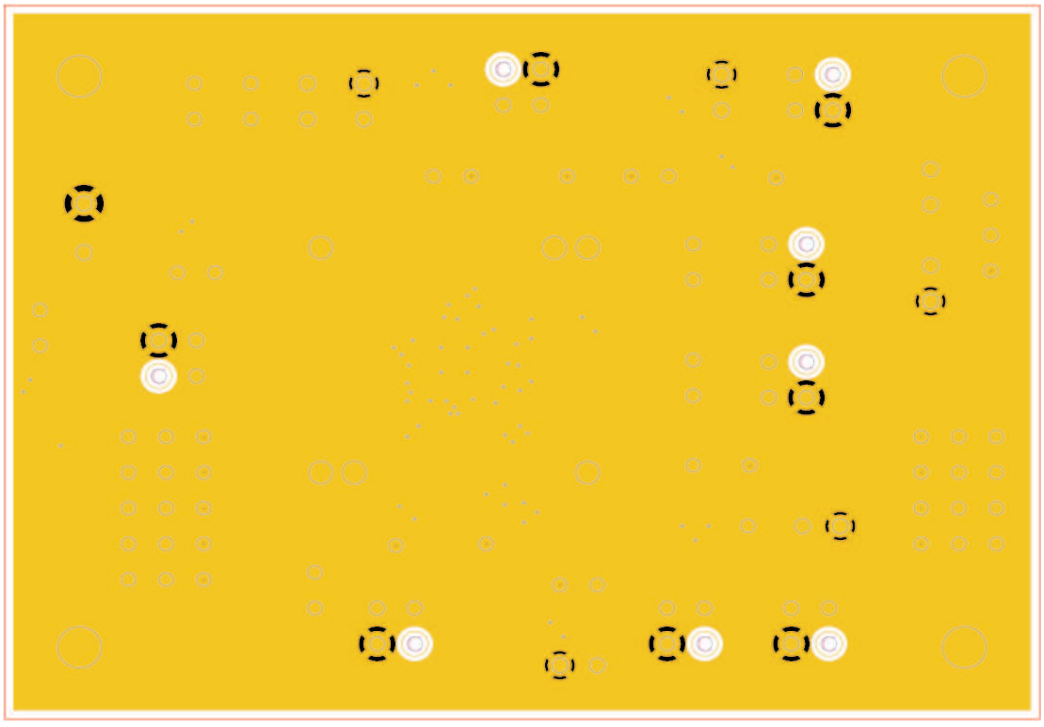

Figure 3. 2nd Layer

Figure 4. 3rd Layer

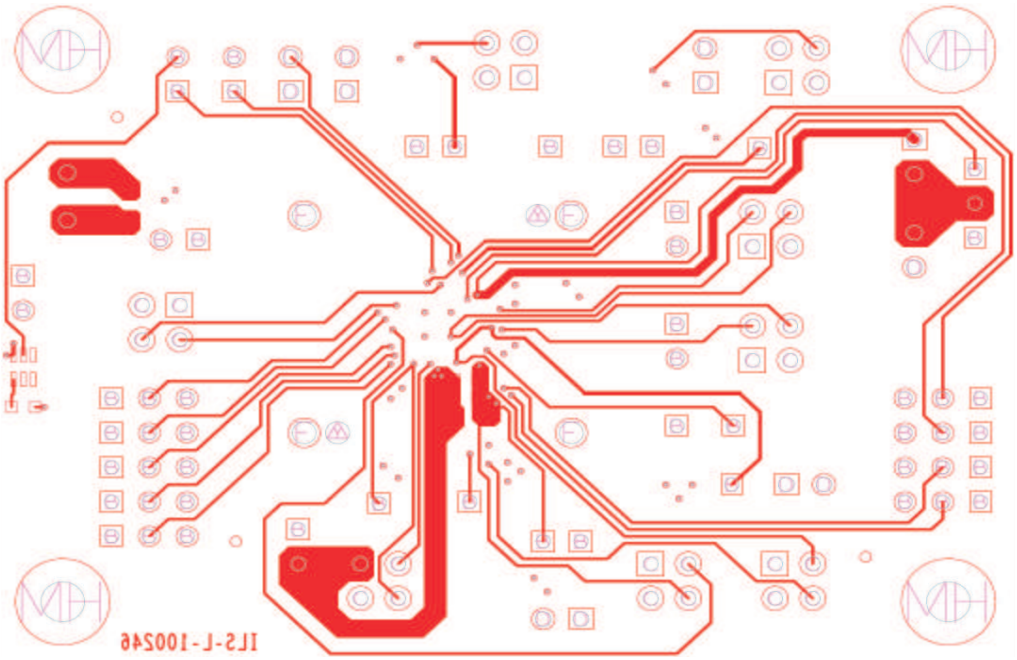

Figure 5. Bottom Layer

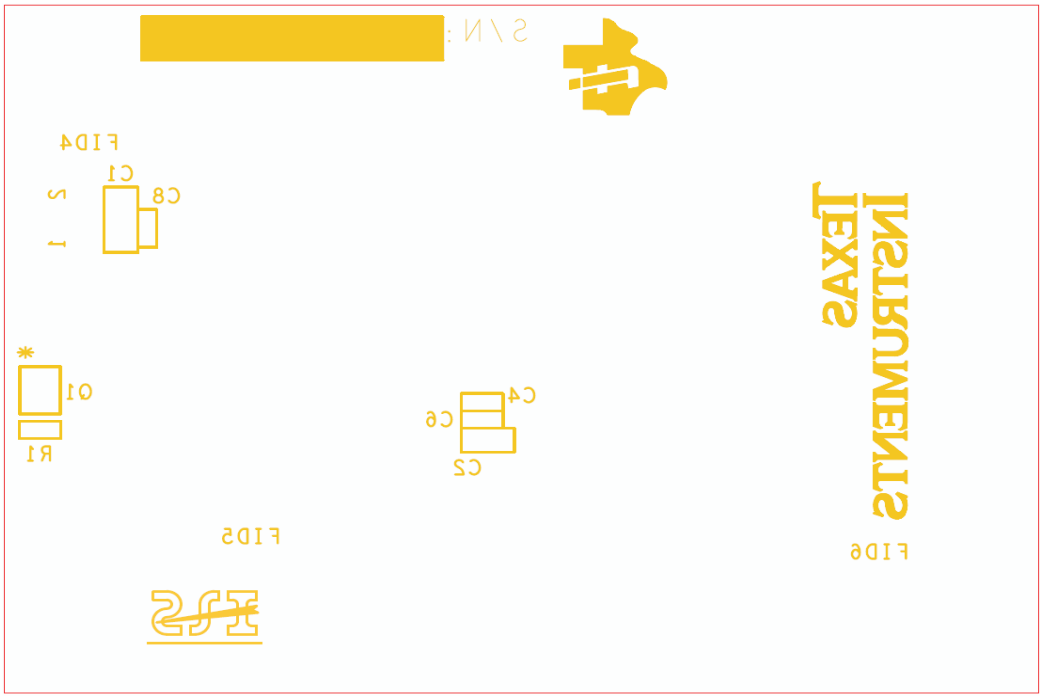

Figure 6. Bottom Layer Silkscreen

5 Schematic and List of Materials

This section provides the TPS80010's EVM schematic and List of Materials.

5.1 Schematic

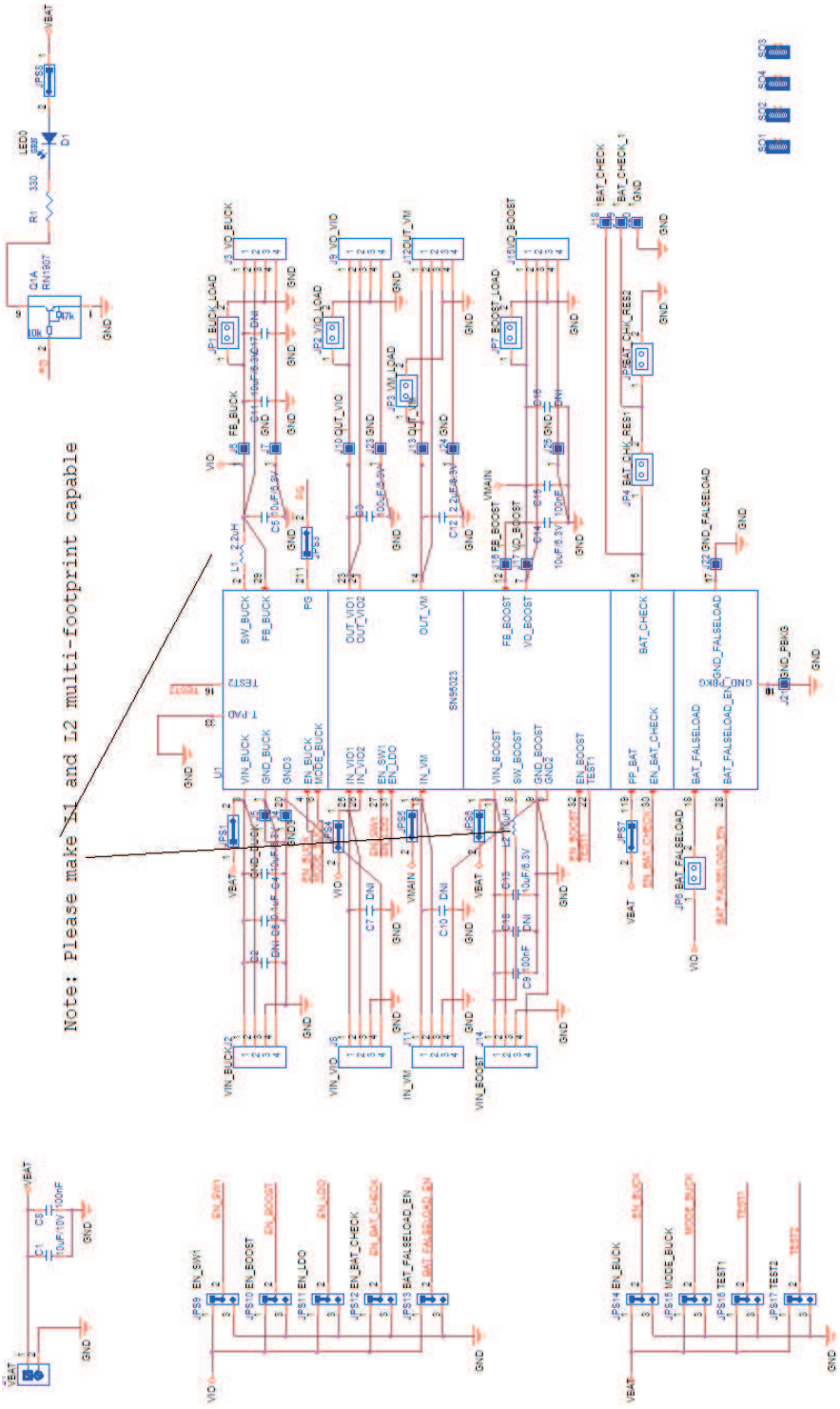

Figure 7. TPS80010 EVM Schematic

5.2 Bill of Materials

Table 1. TPS80010 EVM Bill of Materials

Qty	RefDes	Part	Distributor	Distributor Part #	MFR	MFR Part #	Comment
1	C1	10uF/10V	DigiKey	ED1514-ND			
6	C2, C7, C10, C16, C17, C18	DNI					
1	C3	100µF/6.3V					package 1206
5	C4, C5, C11, C13, C14	10µF/6.3V	DigiKey	490-3896-1-ND	Murata	GRM188R60J106ME47D	
1	C6	0.1µF					package 0603
3	C8, C9, C15	100nF					package 0603
1	C12	2.2µF/6.3V					package 0603
1	D1	LTST-C150CKT	DigiKey	516-1427-2-ND			
7	JPS1, JPS3, JPS4, JPS5, JPS6, JPS7, JPS8	HTSW-102-09-G-S					2 pin header, 0.1" pitch
9	JPS9, JPS10, JPS11, JPS12, JPS13, JPS14, JPS15, JPS16, JPS17	Jumper_1x3_100_430L					3 pin header, 0.1" pitch
7	JP1, JP2, JP3, JP4, JP5, JP6, JP7	1x2_Header_socket_100	DigiKey	50935-ND	AMP_TYCO	50935	
1	J1	ED1514	DigiKey	D1514-ND			
8	J2, J3, J8, J9, J11, J12, J14, J15	IPL1-102-01-S-D-K			Samtec	IPL1-102-01-S-D-K	
16	J4, J5, J6, J7, J10, J13, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25	HEADER_1x1_430L	BISCO	TP-105-01-06	Components Corporation	TP-105-01-06	
1	L1	2.2µH			Murata	LQM2HPN2R2MG0	
1	L2	10µH			Toko	1098AS-H-100M	Avnet is Toko's distributor, or call 408-432-8281
1	Q1	RN1907	DigiKey	FDV301NCT-ND	Fairchild	FDV301N	
			Digi-Key	XP0421400LCT-ND	Panasonic - SSG	XP0421400L	
1	R1	330					package 0603
4	SO1, SO2, SO3, SO4	4-40_.187Dx.5L	Digi-Key	2027K-ND	Keystone	2027	
1	U1	SN95023					DNI

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of xxx V to xxx V and the output voltage range of xxx V to xxx V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than xxx° C. The EVM is designed to operate properly with certain components above xxx° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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