UCC28517 100-W PFC power converter with 12-V, 8-W bias supply, Part 2

By Michael O'Loughlin (Email: michael_oloughlin@ti.com)
Member, Applications Engineering Staff

Introduction

Power factor corrected (PFC) preregulators are generally used in offline ac/dc power converters with a power level higher than 75 W or to meet line harmonic requirements such as EN61000-3-2. PFC is typically done with a boost converter ac/dc topology due to the continuous input current that can be manipulated through average current-mode control to achieve a near-unity power factor (PF). However, due to the high output voltage of a boost converter, a second dc/dc converter is generally needed to step down the output to a usable voltage. In the past this has been accomplished with two pulse-width modulators (PWMs). One PWM controlled and regulated the PFC power stage, while the second was used to control the step-down converter. The UCC28517 controller reduces the need for two PWMs and combines both of these functions into one control-integrated circuit. The UCC28517 operates the second converter at twice the switching frequency of the PFC stage, which reduces the size of the boost magnetics and the ripple current in the boost capacitor. For more information on this device, please see Reference 7. This article reviews the design of the second 12-V, 8-W power stage to be used as an auxiliary bias supply. A review of the PFC preregulator power stage can be found in the 3Q03 issue of the TI *Analog Applications Journal*.

Variable definitions

Δt	Soft-start interval
$\eta 1$	Output A efficiency
$\eta 2$	Output B efficiency
C_{DIODE}	Boost diode capacitance
C_{OSS}	FET drain-to-source capacitance
D_{max}	Duty cycle maximum
ESR	Output capacitance equivalent resistance
f_c	Voltage-loop crossover frequency
f_{opto_pole}	Frequency where optoisolator gain is –3 dB from its dc operating point
f_S	Minimum switching frequency
f_{SA}	Output A switching frequency
f_{SB}	Output B switching frequency
$G_{c(s)}$	Control transfer function
$G_{co(s)}$	Control to output transfer function
$G_{opto(s)}$	Optoisolator gain transfer function
$H_{(s)}$	Voltage divider gain
I_m	Transformer magnetizing current
I_{op_min}	Minimum optocoupler current (1 mA)
I_{PK}	Peak inductor current, peak diode current, peak switch current
I_{RMS}	RMS device current
I_{SS}	UCC28517 soft-start current of 10 µA
L_m	Transformer primary magnetizing inductance
N	Transformer turns ratio
N_p	Primary turns
N_s	Secondary turns
P_{COND}	Device conduction losses
P_{COSS}	Power dissipated by the FET's drain-to-source capacitance
P_{DIODE}	Total loss in the boost diode
P_{DIODE_CAP}	Loss due to boost diode capacitance
P_{FET_TR}	FET transition losses
P_{GATE}	Power dissipated by the FET gate
P_{OUTA}	Output A maximum power
P_{OUTB}	Output B maximum power
Q_{GATE}	FET gate charge
$R_{DS(on)}$	On resistance of the FET
R_{load}	Typical load impedance
R_{SENSE}	Current sense resistor
s	Angular frequency ($j2\pi f$)
t_{blank}	Amount of leading-edge blanking time
t_f	FET fall time
t_r	FET rise time
T_{SB}	$1/f_{SB}$ = 5 µs
$T_{s(f)}$	Voltage loop frequency response
V_{boost}	Same as V_{OUTA}
V_c	Control voltage
V_{ct}	Oscillator peak (5 V)
V_d	Forward diode drop (0.6 V)
$V_{dynamic}$	Current sense voltage range
V_f	Forward voltage of a diode
V_{GATE}	Gate-drive voltage
V_{IN}	RMS input voltage
V_{OUTA}	Boost output voltage (V_{boost})
V_{OUTB}	Auxiliary output voltage
V_{pp}	Output peak-to-peak ripple voltage
V_{REF}	UCC28517 internal reference
V_{ripple}	Output B ripple voltage
V_{slope}	Voltage ramp peak added for slope compensation
V_{VERR}	Feedback error voltage
V_{VREF_TL431}	TL431 (D13) internal reference

Table 1. Design specifications

	MAXIMUM	TYPICAL	MINIMUM
V_{IN}	265 V_{rms}		85 V_{rms}
Output A (V_{OUTA})	410 V	390 V	370 V
Output B (V_{OUTB})	12.6 V	12 V	11.4 V
Output A efficiency (η1)		85%	
Output B efficiency (η2)		50%	
P_{OUTA}	100 W		10 W
P_{OUTB}	8 W		4 W
Output ripple A (V_{pp})	12 V		
Output ripple B (V_{ripple})	750 mV		
Output A THD (% THD)	10%		
PF	1		
Output A switching frequency (f_{SA})		100 kHz	
Output B switching frequency (f_{SB})		200 kHz	

The following design example was generated using typical parameters rather than worst-case values. Please refer to Table 1 and Figures 1–3 for design specifications and component placement. All variables are defined in the sidebar on page 21.

12-V, 8-W auxiliary converter (OUTB)

Due to the high input voltage from the boost converter, this design required a dc/dc converter with a step-down transformer to achieve the desired output voltage of 12 V. The low power requirements permitted use of a discontinuous-mode flyback topology, which uses fewer components than a standard forward converter.

Transformer turns ratio

The following equation can be used to calculate the transformer turns ratio (N) needed for this power stage.

$$N = \frac{D_{max} \times V_{OUTA} \times T_{SB}}{(0.9 - D_{max}) \times (V_{OUTB} + V_d) \times T_{SB}}$$

The UCC28517 PWM/PFC controller has a user-selectable duty-cycle clamp. For this design the duty-cycle clamp was set to a D_{max} of 0.55. The UCC28517 has a forward enable comparator that will not allow the forward converter to operate with a boost voltage less than 50% of the nominal value. This allows the cascaded step-down converter to

Figure 1. PFC power stage schematic

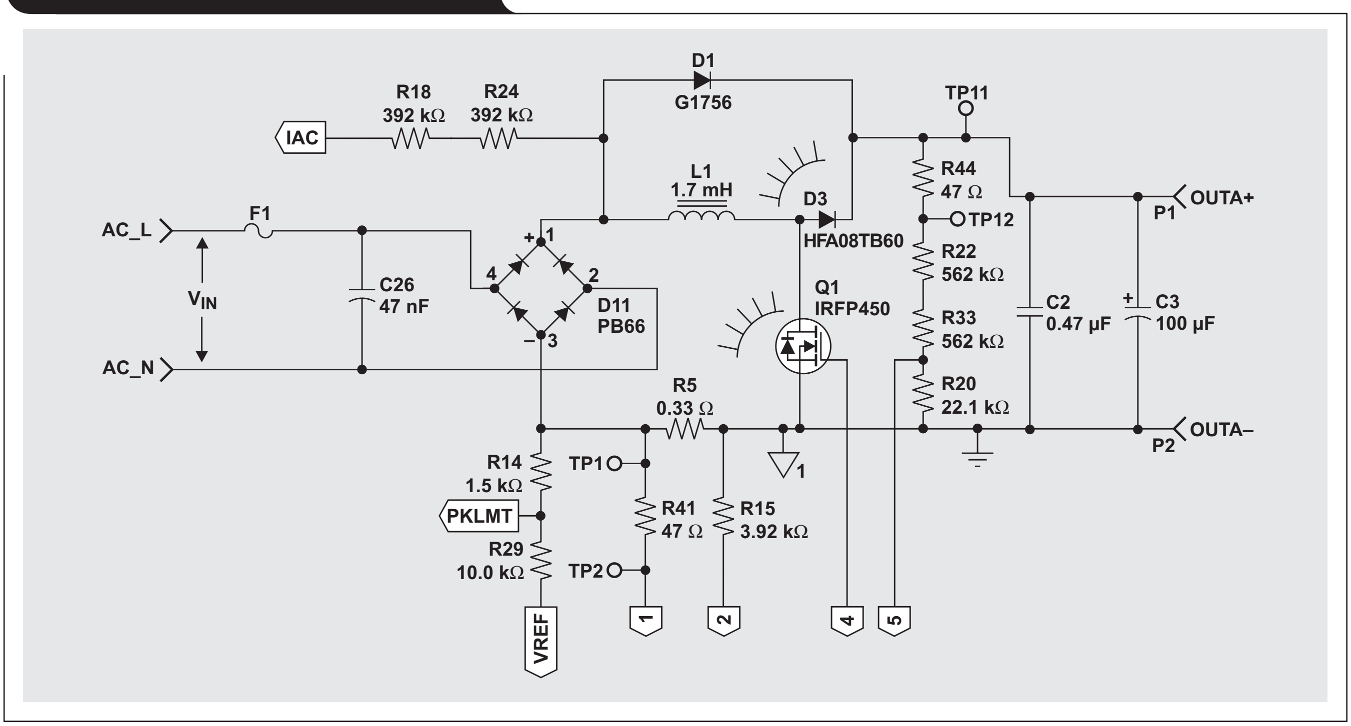


Figure 2. dc/dc power stage schematic

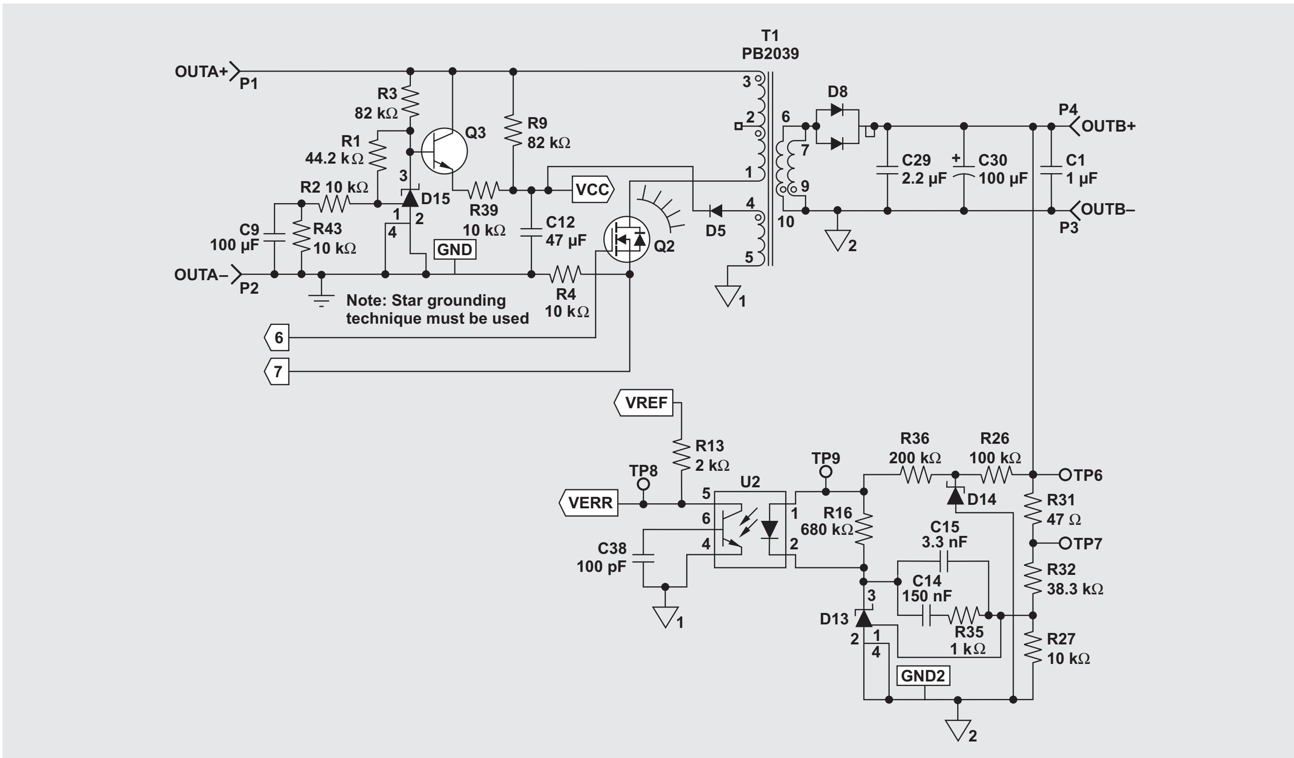
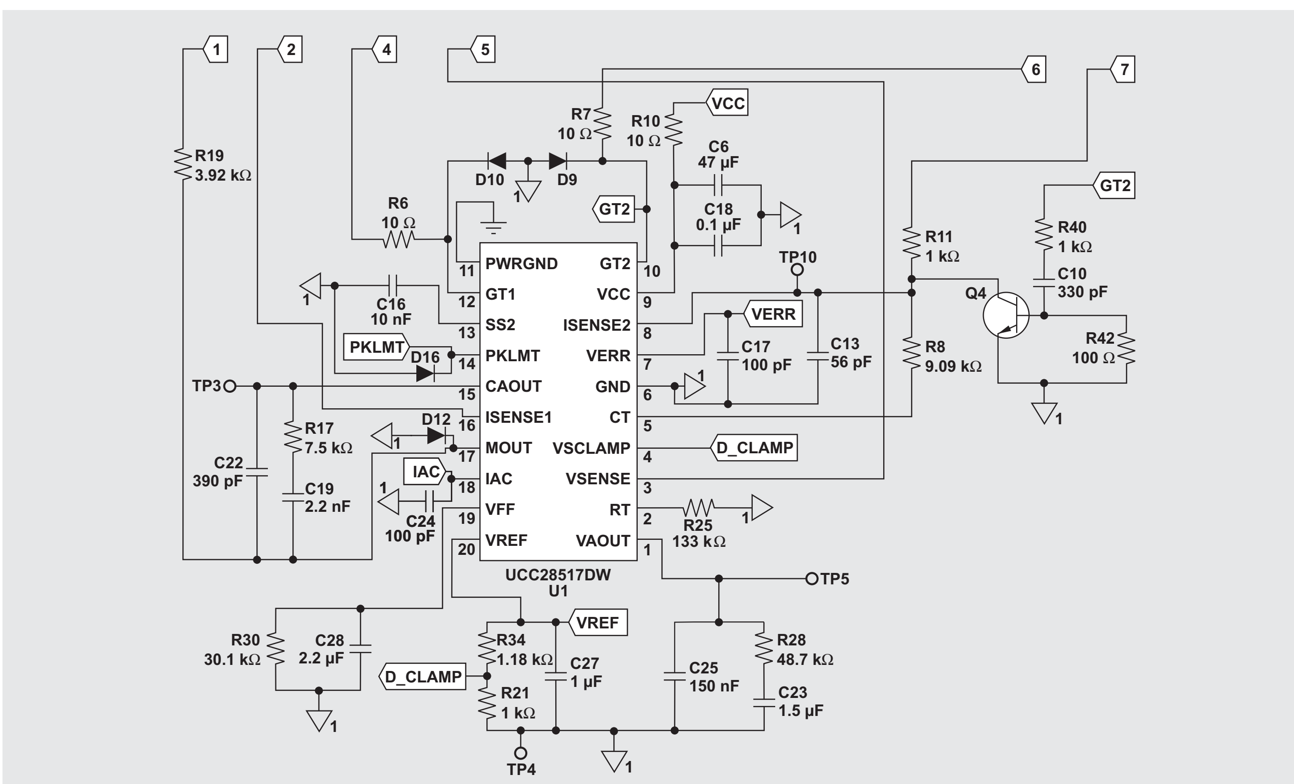


Figure 3. Controller schematic



operate during loss of line voltage. An auxiliary winding of 22 turns was added to power the UCC28517 control IC as well. For this design Pulse Engineering designed a 22-turn transformer (part number PB2039).

Power switch (Q2) and output diode (D8) selection

To select D8 and Q2 properly, a power budget is generally set for these devices to maintain the desired efficiency goal. The following equations were used to estimate power loss in the switching devices. To meet the power budget for this design, an IRFBF20S FET and a 20CJQ045 dual diode from International Rectifier were chosen.

$$I_{PK\_Q2} = \frac{2 \times \frac{P_{OUTB}}{V_{OUTB}}}{\eta 2 \times N}$$

$$I_{RMS\_FET\_Q2} = \frac{P_{OUTB}}{\eta 2 \times N} \times \sqrt{\frac{D_{max}}{3}}$$

$$P_{COND\_FET\_Q2} = R_{DS(on)} \times I^2_{RMS\_FET}$$

$$P_{GATE\_Q2} = Q_{GATE} \times V_{GATE} \times f_S$$

$$P_{COSS\_Q2} = \frac{1}{2} C_{OSS\_Q2} \times V^2_{OUTB} \times f_S$$

$$P_{FET\_TR\_Q2} = \frac{1}{2} V_{OUTB} \times I_{RMS\_Q2} \times (t_r + t_f) \times f_{SB}$$

$$P_{Q2} = P_{GATE\_Q2} + P_{COSS\_Q2} + P_{COND\_FET} + P_{FET\_TR\_Q2}$$

$$I_{PK\_D8} = \frac{2 \times P_{OUTB} \times (1 - D_{max})}{V_{OUTB}}$$

$$P_{DIODE\_CAP\_D8} = \frac{C_{DIODE}}{2} \times V^2_{OUTB} \times f_{SB}$$

$$P_{COND\_D8} = V_f \times I_{RMS\_D8}$$

$$I_{RMS\_D8} = I_{PK\_D8} \times \sqrt{\frac{1 - D_{max}}{3}}$$

$$P_{DIODE} = P_{COND\_D8} + P_{DIODE\_CAP\_D8}$$

Output capacitor

The output capacitor selection for the step-down converter was based on requirements for energy storage, output ripple voltage, RMS current, and peak current.

$$I_{PK\_C30} = 2 \times \frac{\frac{P_{OUTB}}{V_{OUTB}}}{1 - D_{max}}$$

$$ESR_{C30\_max} \le \frac{V_{ripple}}{I_{PK\_C30}}$$

$$C30 \ge \frac{0.5 \times I_{PK} \times (1 - D_{max})}{f_{SB} \times V_{OUTB}}$$

$$I_{RMS\_C30} = I_{PK\_C30} \times \sqrt{(1 - D_{max}) \times \left[\frac{4 - 3 \times (1 - D_{max})}{12}\right]}$$

R_{SENSE2}

The dc/dc power converter is designed for peak-current-mode control. R4 is the current sense resistor, which can be sized through the following two equations.

$$I_m = \frac{V_{OUTA} \times D_{max}}{L_m \times f_{SB}}$$

$$R4 = \frac{V_{dynamic}}{I_m + \frac{I_{PK\_C30}}{N}}$$

Soft start

The UCC28517 has soft-start circuitry to allow for a controlled ramp of the second stage's duty cycle during startup. The following equation was used to calculate the approximate capacitance needed to achieve a soft start of roughly 5 ms (Δt).

$$C16 = \frac{I_{SS} \times \Delta t}{5\ V}$$

Slope compensation

Designing a power converter that uses peak-current-mode control generally requires slope compensation to remove instabilities in the control loop and to make the design less susceptible to noise. Resistors R11 and R8 (Figure 3) sum in a portion of the oscillator signal to the current sense signal for slope compensation. Generally the added slope (V_{slope}) required is equal to half the down slope of the change in output current. By selecting R11 first, you can calculate the required value of R8 to generate the required slope compensation.

$$V_{slope} = \left(I_m + \frac{I_{PK\_C30}}{2N}\right) R4$$

$$R8 \le \frac{R11(V_{ct} - V_{slope})}{V_{slope}}$$

Leading-edge blanking circuit

The typical current sense signal for a converter using peak-current-mode control is shown in Figure 4. As shown, during time T1 there is a leading current spike. This is partly caused by the parasitic gate-to-source capacitance of the power stage switch Q4 and the voltage divider formed off the gate drive by R4 and R7. This leading-edge spike can cause the peak-current-mode signal to terminate the gate drive prematurely. To remove this instability, a leading-edge blanking circuit was constructed.

Electronic components Q4, R40, R42, and C10 form a leading-edge blanking circuit. This circuit is used to clamp leading-edge current spikes. The timing of the leading-edge blanking can be adjusted by modifying the size of timing capacitor C10:

$$C10 = \frac{t_{blank}}{2(R40 + R42)}$$

Figure 4. Typical current sense signal

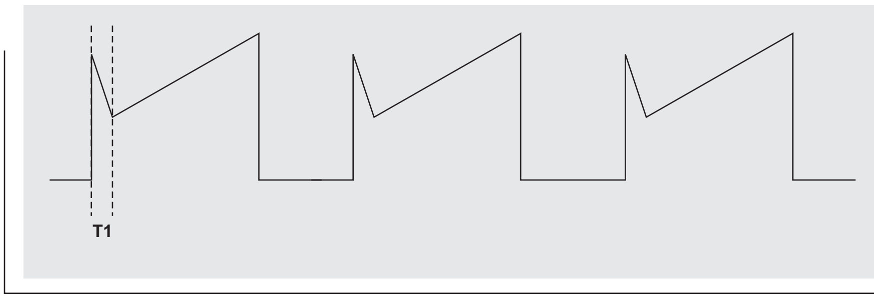
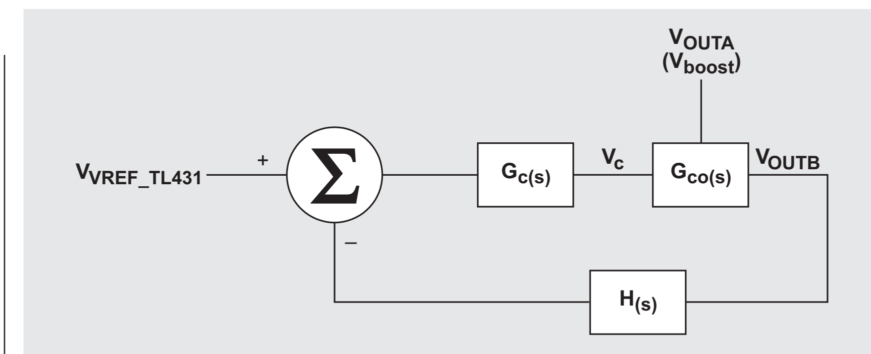


Figure 5. dc/dc converter control loop



Control loop for the dc/dc converter

Figure 5 shows the control block diagram for the control loop of the dc/dc converter. $G_{c(s)}$ is the compensation network's transfer function (TF), $G_{opto(s)}$ is the optoisolator gain TF, $G_{co(s)}$ is the control-to-output gain TF, and $H_{(s)}$ is the divider gain TF. To estimate the frequency response of each gain block, the following equations can be used. f_{opto_pole} is the frequency where the optoisolator gain is –3 dB from its dc operating point; and V_{VREF_TL431} is the internal reference voltage of the TL431 shunt regulator. R_{load} represents the typical load impedance for the design.

$$H_{(s)} = \frac{R27}{R27 + R32} = \frac{V_{VREF\_TL431}}{V_{OUTB}}$$

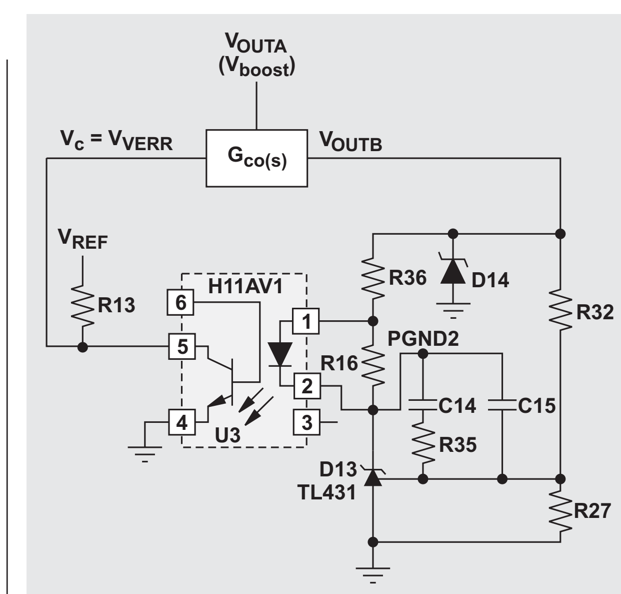
$$G_{opto(s)} = \frac{R13}{R36} \times \frac{1}{1 + \frac{s}{2\pi f_{opto\_pole}}}$$

$$G_{c(s)} = \frac{s \times R35 \times C14 + 1}{s \times C14 \times R31 \times (1 + s \times R35 \times C15)} \times \frac{R13}{R36} \times \frac{1}{1 + \frac{s}{2\pi f_{opto\_pole}}}$$

$$G_{co(s)} = \frac{V_{OUTB}}{V_c} = \frac{R_{load}}{R4} \times \frac{N_p}{N_s} \times \frac{1 + s \times C30 \times ESR}{1 + s \times C30 \times R_{load}}$$

Figure 6 shows the circuitry that was used for the voltage feedback loop. D13 is a TL431 shunt regulator that can function as an operational amplifier to provide feedback control when set up in this configuration.

Figure 6. Voltage feedback loop



Initially the resistor values for the divider gain, $H_{(s)}$, must be selected. The following equation can be used to size these resistors, where V_{OUTB} is the desired output voltage and V_{VREF_TL431} is the internal reference of the TL431.

$$R32 = \frac{R27(V_{OUTB} - V_{VREF\_TL431})}{V_{VREF\_TL431}}$$

It is important to bias the TL431 and the optoisolator correctly for proper operation. Resistors R16 and R13 provide the minimum bias currents for the TL431 and the optoisolator, respectively, and can be selected with the following equations. The optoisolator was configured to have a dc gain of roughly 20 dB, and the optoisolator had a crossover frequency of roughly 80 kHz. Figure 7 shows the small signal frequency response of the optoisolator.

$$R16 = \frac{V_f}{I_{TL431\_min}}$$

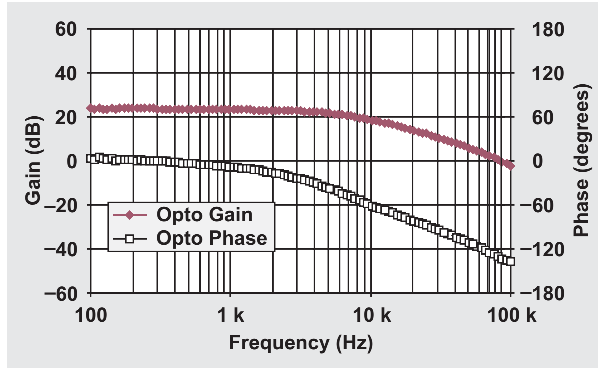
$$R13 = \frac{V_{REF} - V_{VERR(max)}}{I_{op\_min}}$$

Before attempting to compensate the control loop, $T_{s(f)}$, we must define some design goals for the closed-loop frequency response. Typically the loop is designed to cross over at a frequency below one-sixth of the switching frequency (see Reference 3). For this design example to have good transient response, the design goal was to have the loop gain crossover frequency (f_c) at roughly 1 kHz, which is less than one-sixth of the switching frequency (f_{SB}). The following equation describes the frequency response of the system loop gain, $T_{s(f)}$, in decibels.

$$T_{s(f)} = G_{c(s)_{dB}} + G_{co(s)_{dB}} + H_{(s)_{dB}}$$

The compensation network that is used ($G_{c(s)}$) has three poles and one zero. One pole occurs at the origin, and a second pole is caused by the limitations of the optoisolator. The third pole is set at one-half the switching frequency to attenuate the high frequency gain. The zero

Figure 7. Optoisolator frequency response



is set at the desired crossover frequency. The following equations can be used to select R35, C14, and C15 of $G_{c(s)}$ to obtain the desired design goals.

$$H_{(s)_{dB}} = 20\log(H_{(s)})$$

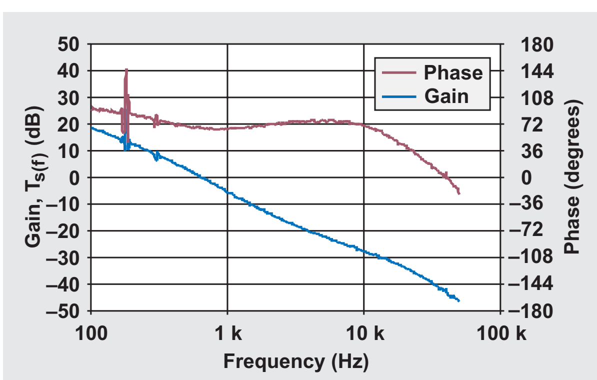
$$R35 = R32 \times 10^{\frac{-(G_{co(s)_{dB}} + G_{opto(s)_{dB}} + H_{(s)_{dB}})}{20}}$$

$$C14 = \frac{1}{2 \times \pi \times R35 \times f_c}$$

$$C15 = \frac{1}{2 \times \pi \times R35 \times \frac{f_S}{2}}$$

Figure 8 shows the measured loop gain frequency response, $T_{s(f)}$. The frequency response characteristics in Figure 8 show that f_c was roughly equal to 800 Hz with a phase margin of roughly 50°. It is important to note that the equations used to compensate the control loop by selecting C14, C15, and R35 are estimates and the values may have to be adjusted to get the appropriate compensation.

Figure 8. Frequency loop response, $T_{s(f)}$



Summary

In this design example we reviewed the design of a 100-W PFC ac/dc preregulator with an auxiliary 12-V, 8-W bias supply. The UCC2851x family of combination PWM controllers is perfect for offline applications that require PFC and auxiliary power supplies to meet different system requirements. The design performance of this two-stage power converter is shown in Figures 9–12.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title **TI Lit. #**

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2. Laszlo Balogh, "Unitrode – UC3854A/B and UC3855A/B Provide Power Limiting With Sinusoidal Input Current for PFC Front Ends," Unitrode Design Note slua196
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7. "Advanced PFC/PWM Combination Controllers," Data Sheet slus517
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Figure 9. Output A THD vs. output power

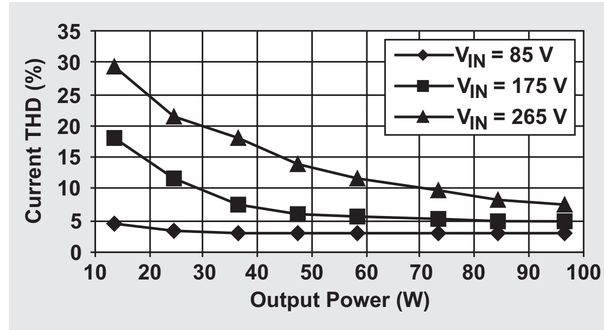


Figure 10. Output A efficiency vs. output power

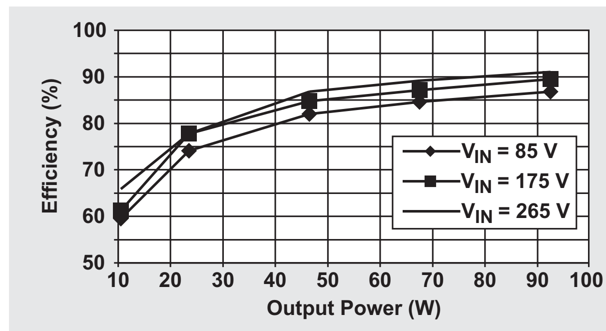


Figure 11. Output A PF vs. output power

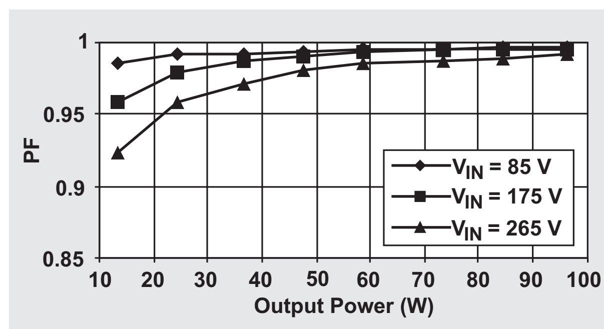
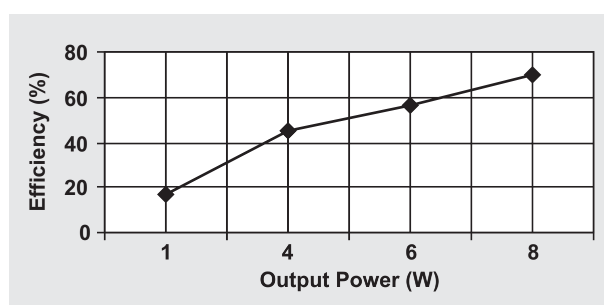


Figure 12. Output B efficiency vs. output power



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