Advantages of the Highly-Programmable DC/DC Controllers in the TPS65086x PMIC

Texas Instruments

Introduction

To extend the battery life in portable applications, designers continue to demand lower cost and higher-efficiency switching regulators. DC/DC buck regulators are widely used as power management modules for powering state-of–the-art industrial systems, FPGAs, point-of-sale terminals and residential gateways. The power supply is a key system component that continues to be optimized to reduce power consumption during various modes of device operation. Higher levels of on-chip integration have increased power dissipation and power density of modules. Maximum power savings is possible when each of the processor cores form separate voltage domains and dynamic voltage scaling (DVS) is applied to them individually. Regulators must also support efficient standby/sleep mode control. This level of fine-grain power control is essential for today's portable electronics. With the integration of power management ICs (PMICs), designers are able to achieve major improvements in power consumption, performance and space.

The TPS65086x is a highly programmable PMIC with wide input-voltage support for its DC/DC controllers. It also supports a large range of I^2C-programmable output voltages that are suitable for the various power domains in any typical processor platform. The switching controllers also support the DVS, decay, and connected standby modes, which are essential to provide a low-power, highly-efficient power solution. Input supply to the regulators range from narrow VDC (NVDC) or non-NVDC power architectures, using 2S or 3S Lithium-Ion battery packs (5.4 to 21 V). Output voltage of the regulators range from 0.5 to 1.67 V with DVS capability and has an option to support the same at higher voltages—up to a maximum of 3.575 V. This wide input and output voltage range of the converter allows a high level of reconfigurability and reusability of the design in many portable applications.

Operating Principles of Adaptive On-Time Control

Figure 1 shows the block diagram of the TPS65086x buck controller. The power stage consists of external N-channel MOSFETs as high-side and low-side switching devices, a filter inductor and an output capacitor. The controller has high-performance internal gate drivers to independently drive low-side and high-side power MOSFETs in a synchronous-buck or half-bridge configuration. The low-side driver output swings between the gate drive voltage (typically 5 V) and ground. The floating high-side gate driver is referenced to the SW pin and is capable of operating with supply voltages up to 28 V. The boot-strap capacitor is designed to charge from the supply for the low-side gate driver during the on time of the low-side MOSFET.

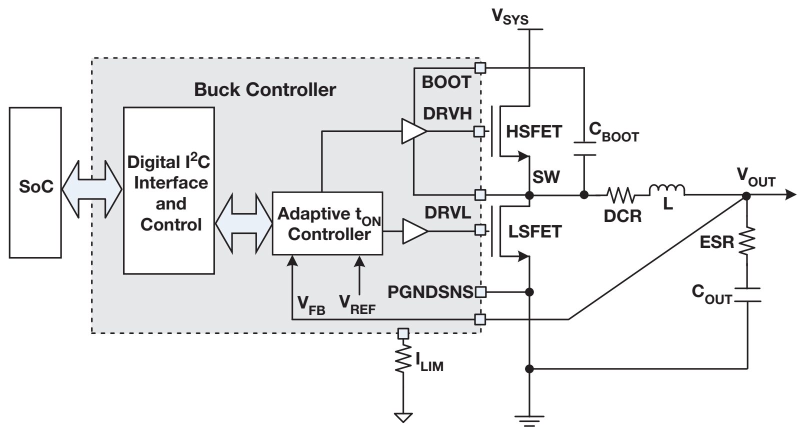

***Figure 1**: Block diagram of a buck controller in the TPS65086x.*

The buck controller in the TPS65086x has adaptive on-time control. Desired on time for the regulator is continuously computed by the control logic and based on the operating points (V_{SYS}, V_{OUT} and load current). It supports low-cost ceramic output capacitors with low ESR and has internal phase compensation to ensure stability. The controller has a programmable switching frequency that ranges from 500 kHz to 1 MHz. A higher switching frequency enables the converter to have smaller output-filter components: Inductor (L) and output capacitor (C_{OUT}). This ensures a low-cost and low-area solution. The controller exhibits a maximum spread of ±10% in switching-frequency variation over a wide range of input and output voltages. This enables the designer to choose lower values for the filter inductor (e.g., 0.33 µH or 0.22 µH) and a lower value of output capacitor.

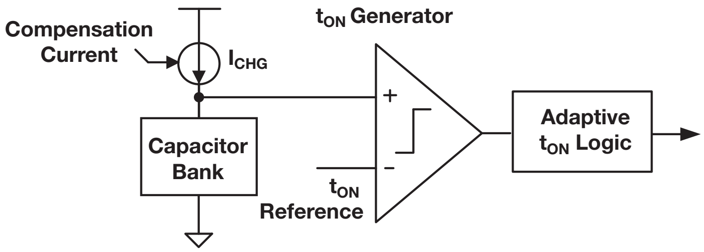

Figure 2: Block diagram of adaptive on-time generation.

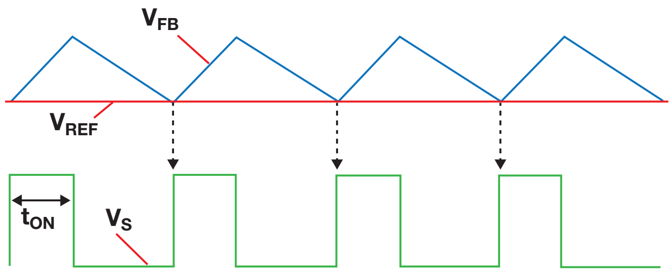

Figure 3: Switching waveforms for adaptive on-time control.

Figure 2 and **Figure 3** depict a block diagram for adaptive on-time generation and its respective switching waveforms. The controller's power efficiency is an asset because it has flexible options for light-load efficiency enhancements. These options enable the controller's ability to optimize its power efficiency at the light- and medium-load current range. **Figure 4** below depicts measured power efficiency of the controller for varied load currents and input voltages. The light-load power efficiency is >80% for V_{IN} ranging from 5.4 to 21 V. Efficiency drops down for the narrow range of load current at the boundary of PFM mode and PWM mode, then once the controller enters full PWM mode, efficiency gradually decreases with the increasing load current.

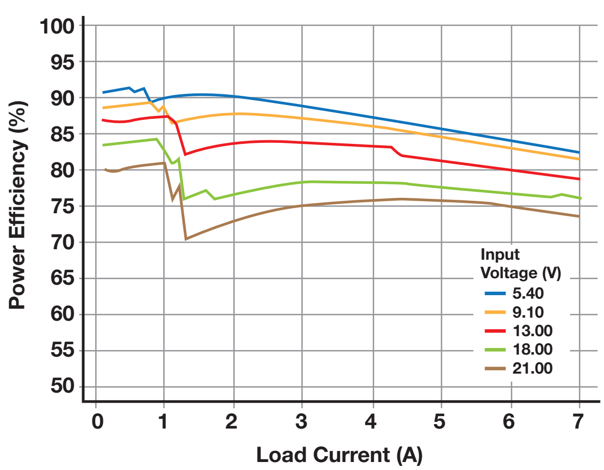

Figure 4: Buck controller power efficiency vs. load current.

Power Saving Modes

DVS Mode

Because of the ever-increasing need for higher efficiency, adaptive-output voltage converters with DVS are needed to provide variable voltage with fast reference tracking. The buck controller in the TPS65086x supports DVS from 0.5 to 1.67 V, and the same controller is reconfigurable to an appropriate DVS range when configured to a maximum output voltage of 3.575 V. The regulator output slews up and down in digital-programmable steps with a minimum DVS slew rate of 2.5 mV/µs. **Figure 5** depicts the DVS behavior. When the regulator is also commanded through digital bits to decay down to zero volts, the output will scale down to 0.5 V and then slowly decays the load current to zero.

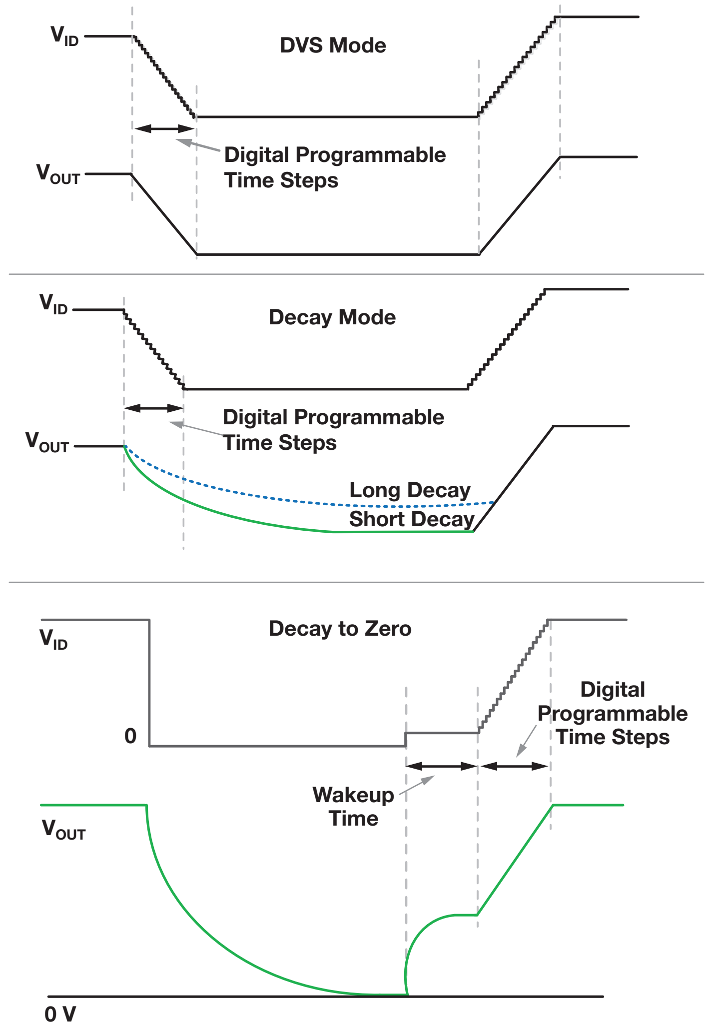

Figure 5: DVS- and decay-mode waveforms.

Decay Mode

The buck controllers in the TPS65086x offer decay mode down to a lower voltage when the feature is enabled through the digital register. The decay mode is only used to transition slowly to a desired lower voltage. This helps the regulator to conserve existing charge on the output capacitor and decay down slowly only with the load current. The conservation of charge in the output capacitor helps improve the energy efficiency of the regulator. **Figure 5** includes decay-mode scenarios, long decay during light-load conditions and short decay during higher load conditions. During decay, if the output voltage is still decaying, and if there is a command for a new higher voltage, the regulator waits and catches up with digital DVS steps. Furthermore, the output can decay all the way to zero volts during decay-to-zero and then wake up on user command. During decay-to-zero, the controller operates in sleep mode and saves standby power. On wake up, it quickly powers up and the DVS function scales the voltage to the new setting. This helps the regulator to quickly wake up for normal operation after exiting decay operation; as opposed to the entire regulator being disabled or powered down.

Ultra-Low-Quiescent (ULQ) Power Mode

The buck controller in the TPS65086x supports the automatic PFM mode in light-load conditions to enhance power efficiency. During idle time in the PFM mode, the internal circuits of the regulator enters the sleep or power-down mode to reduce standby current. The regulator immediately wakes when an energy burst is demanded at the output. This feature offers a seamless dynamic transition between PFM and PWM operation under varying load currents.

Summary

The TPS65086x single-chip PMIC is an elegant, small-footprint and low-cost solution that caters to new processors in systems with NVDC or non-NVDC power architectures that are powered by 2S or 3S Lithium-Ion battery packs. The PMIC has 6 highly-efficient step-down voltage regulators (3 integrated DC/DC converters and 3 DC/DC controllers), a sink/source LDO, 2 LDOs and 3 load switches. PMIC outputs are controlled by power-up sequence logic to provide the proper power rails, sequencing, and protection—including DDR3 and DDR4 memory power. The IC has I^2C interface, which supports simple control through an embedded controller or by a SoC.

Author Information

Sujan K. Manohar and Bhaskar Ramachandran
Integrated Power Group, High Volume Analog
Texas Instruments Inc., Dallas, Texas, USA
(sujan, Bhakar.Ramachandran)@ti.com

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