ADC08D1000,ADC08D1500,ADC10DL065, ADC12DL040,ADC12DL065,ADC12QS065, LMH6550,LMH6551,LMH6703

Understanding High-Speed Signals, Clocks, and Data Capture

Literature Number: SNAA121

SIGNAL PATH designer℠

Tips, tricks, and techniques from the analog signal-path experts

No. 103

Understanding High-Speed Signals, Clocks, and Data Capture

— By Ian King, Applications Engineer

As today's data conversion sample rates for analog-to-digital converters are moving into the Giga Samples Per Second (GSPS) range, systems need to be capable of such high conversion rates and the supporting analog components have to generate and amplify high-frequency signals. In addition to the analog signal path, the circuit areas that the designer should thoroughly understand are the sampling clock and the capturing of digital data at high bit rates. This issue of the *Signal Path Designer* will provide suggested solutions for these two key areas. The following information is particularly relevant for systems that require high-performance ADCs.

Clock Sources

One of the most important sub-circuits within a high-speed data conversion system is the clock source. This is because the timing accuracy of the clock signal can directly affect the dynamic performance of the ADC. To minimize this influence, an ADC clock source must exhibit very low levels of timing jitter or phase noise. If this factor is not considered when choosing a clock circuit, the system could deliver poor dynamic performance irrespective of the quality of the front-end analog input circuitry or ADC. A perfect clock will always deliver edge transitions at precise time intervals. In practice, clock edges will arrive at continuously varying intervals. As a result of this timing uncertainty,

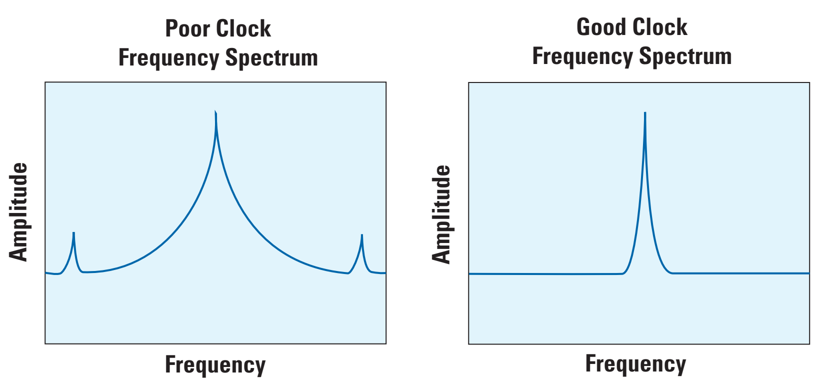

Figure 1. Examples of Clock Signal Spectral Analysis

NEXT ISSUE:

Precision Sensor Interface

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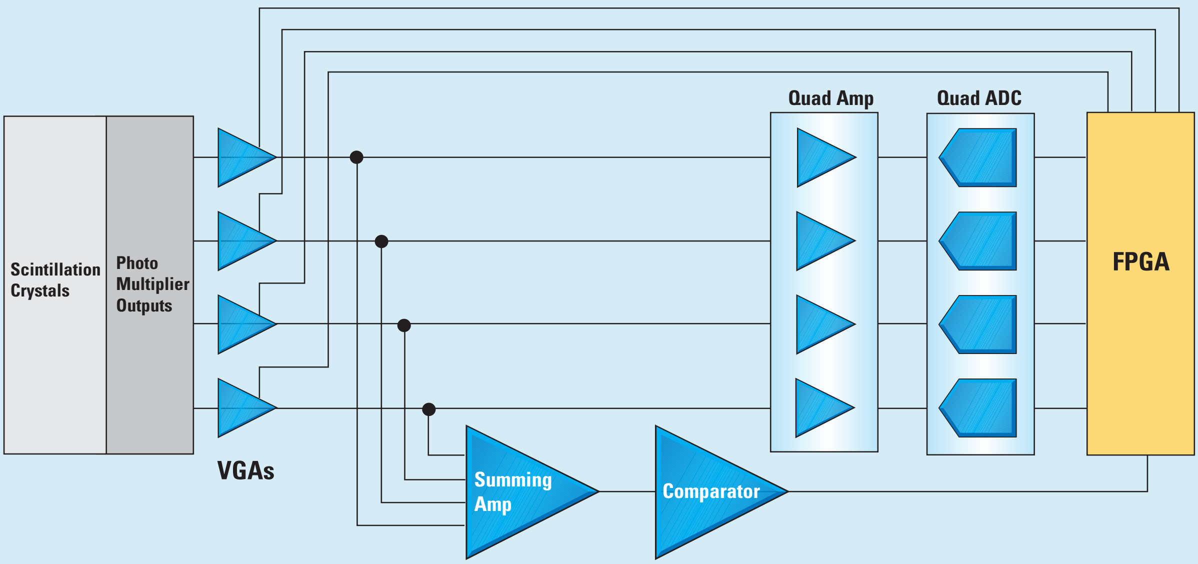
The Sight & Sound of Information

High-Performance Solutions for Medical Imaging

Simplified Positron-Emission Tomography (PET) Scanner Block Diagram



High-Speed ADCs for Medical Imaging

Product ID	Resolution	Speed (MSPS)	Supply Voltage (V)	Power (mW)	Dynamic Performance SFDR (dB)	THD (dB)	ENOB (bit)	SNR (dB)	Package
ADC10065	10 bit	65	3	68.4	80	-72	9.5	59	TSSOP-28
ADC10080	10 bit	80	3	78.6	79	-75	9.5	59	TSSOP-28
ADC10DL065	10-bit dual	65	3.3	360	80	-78	9.8	61	TQFP-64
NEW! **ADC12DL040**	12-bit dual	40	3	210	86	-83	11.1	69	TQFP-64
NEW! **ADC12DL065**	12-bit dual	65	3.3	360	86	-84	11.1	69	TQFP-64
NEW! **ADC12QS065**	12-bit quad	65	3	800	85	-83	11.0	69	TQFP-64, LLP-60
ADC14L020	14 bit	20	3.3	150	92	90	12.0	74	LQFP-32
ADC14L040	14 bit	40	3.3	236	90	87	11.9	73	LQFP-32

High-Speed Amplifiers and Comparators for Medical Imaging

Product ID	Type	SSBW (MHz, $A_V = 1$)	Slew Rate (V/µs, A_V=1)	I_{CC} (mA/ch)	2nd/3rd HD (dBc, $V_{OUT} = 2\ V_{PP}$)	Voltage Noise (nV/$\sqrt{Hz}$)	Package
NEW! **LMH6550**	Fully differential ADC driver w/ disable	400	3000	20.0	-92 / -103 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
NEW! **LMH6551**	Fully differential ADC driver	370	2400	12.5	-94 / -96 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
NEW! **LMH6703**	1.2 GHz low distortion op amp w/shutdown	1.2 GHz[2]	4200[2]	11.0	-69 / -90 at 20 MHz, R_L=100Ω	2.3	SOIC-8, SOT23-6
LMH6502	Linear in dB, variable gain amplifier	130[1]	1800[1]	27.0	-55 / -57 at 20 MHz, R_L=100Ω	7.7	SOIC-14, TSSOP-14
LMH6503	Linear in V/V, variable gain amplifier	135[1]	1800[1]	37.0	-60 / -61 at 20 MHz, R_L=100Ω	6.6	SOIC-14, TSSOP-14
LMH6504	Linear in dB, variable gain amplifier	150[1]	1500[1]	11.0	-47 / -55 at 20 MHz, R_L=100Ω	4.4	SOIC-8, MSOP-8
LMH6722	Quad wideband, low power op amp	400	1800	5.6	-72 / -85 at 5 MHz, R_L=100Ω	3.4	SOIC-14
LMH6725	Quad, ultra low power op amp	370	600[2]	1.0	-65 / -63 at 5MHz, R_L=100Ω	4.3	SOIC-14, TSSOP-14
Product ID	**Type**	**Response Time (ns)**	**Rise/ Fall Times**	**I_{CC} (mA/ch)**	**CMVR**	**Output Config**	**Package**
LMV7219	7 ns, 2.7V to 5V comparator w/ RRO	7	1.3 ns	1.1	-0.2V to 3.8V	Push-pull	SC70-5, SOT23-5

[1] A_V = +10 [2] A_V = +2

the signal-to-noise ratio of a sampled waveform can be compromised by the data conversion process.

The maximum clock jitter that can be tolerated from all jitter sources before the noise due to jitter exceeds the quantization noise (1/2 LSB). This is defined from the following equation:

$$T_{j(rms)} = (V_{IN(p\text{-}p)} / V_{INFSR}) \times (1/(2^{(N+1)} \times \pi \times f_{in}))$$

If the Input Voltage (V_{IN}) is optimized to equal the full scale range of the ADC (V_{INFSR}), then the jitter requirement becomes a factor of the ADC's resolution (N bits) and the input frequency being sampled (f_{in}).

For input frequencies up to the Nyquist rate (500 MHz for a 1 GSPS conversion rate), the total jitter requirement would be:

$$T_{j(rms)} = 1 \times (1/(2^{(8+1)} \times \pi \times 500 \times 10^6))$$

$$T_{j(rms)} = 1.2 \text{ ps}$$

This value represents the total jitter from all sources. A source of jitter that can be accounted for within the ADC device itself is called the aperture jitter. This is a timing uncertainty associated with the input sample and hold circuit of the device and should be considered when determining the maximum allowable clock jitter of the clock source.

$$\text{Clock Circuit Jitter} = \text{SQRT}\left(T_{j(rms)}^2 - (\text{ADC Aperture Jitter})^2\right)$$

Using the ADC08D1000 as an example, the aperture jitter is given in the datasheet as 0.4 ps, this value tightens the jitter specification for the ADC clock to ~1.1 ps.

However, simply matching an oscillator's performance data to the requirements specification may not be enough to obtain the expected result when used in the data conversion system. This is because frequency components that exist alongside the fundamental also play a significant role. It is therefore important to examine the clock signal with a spectrum analyzer and make sure that the energy associated with the fundamental frequency is not spread over too wide a range. Spurs that extend to higher frequencies may be visible and will also have a direct impact on jitter performance. ***Figure 1*** compares an example of a poor performance clock signal alongside the frequency spectrum that would be expected from a good, clean low-jitter clock source.

Figure 2 shows the recommended clock circuit for the ADC08D1000. It consists of a Phase Locked Loop (PLL) device (LMX2312) connected to a Vari-L Voltage Controlled Oscillator (VCO).

The PLL and VCO maintains the required signal to noise ratio (46 dB) for the ADC08D1000 product up to the Nyquist input frequency. The FFT plot in ***Figure 3*** shows the dynamic performance of the ADC when clocked at 1 GSPS

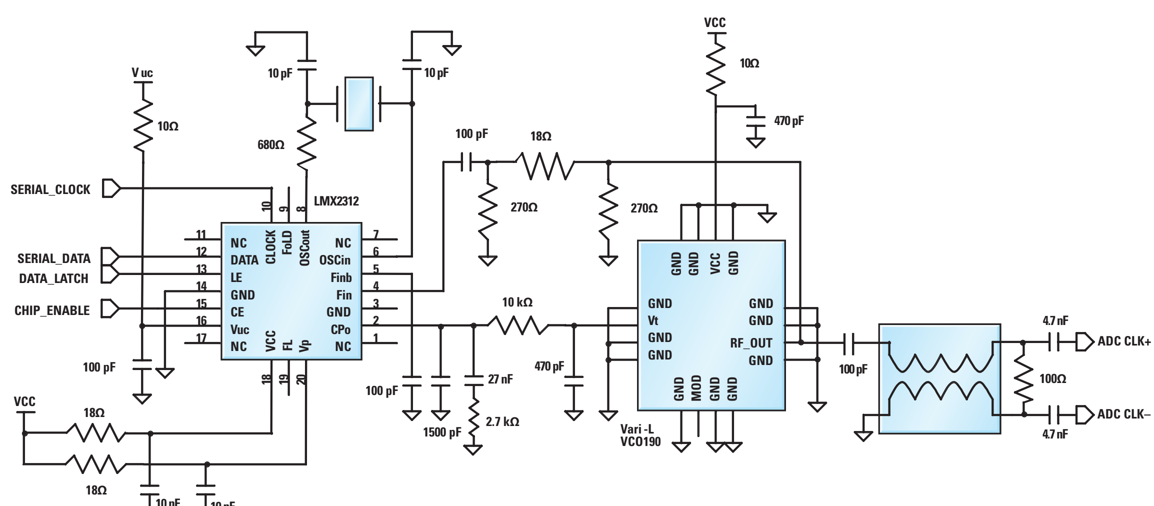
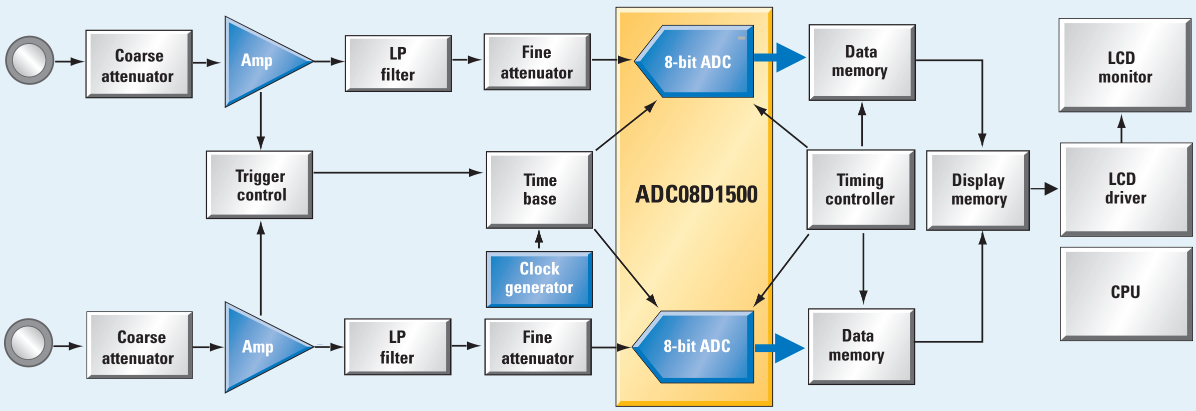


Figure 2. PLL and VCO Clock System

Signal-Path Solutions for Test and Measurement

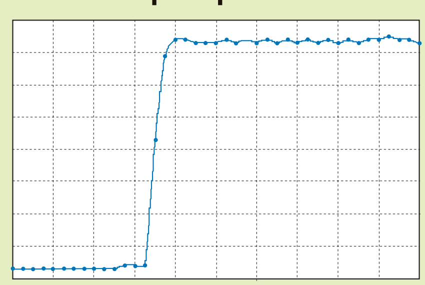
Simplified Oscilloscope



8-bit 1-3 GSPS ADC Family Performance (typical)

- 7.3 to 7.5 Effective Number of Bits (ENOB) at Nyquist
- 1.75 GHz full power bandwidth
- Bit error rate 10^{-18}
- DNL ±0.25 LSB
- Crosstalk -71 dB
- Operating power of only 1W to 1.8W (*no heat sink required*)

Step Response



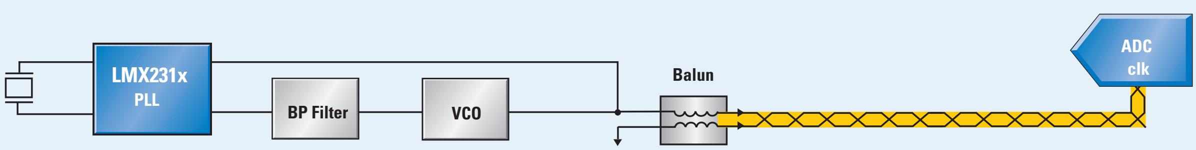
2 nS/div
I Input, 2 GSPS Interleaved Operation

Features

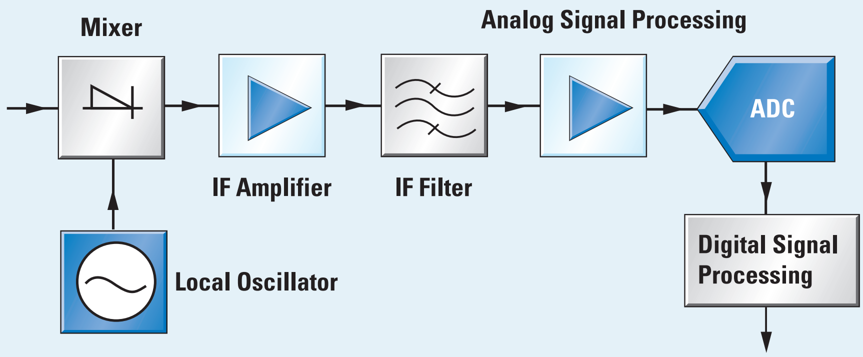
- Interleaved dual-edge sampling (DES) mode enables up to 3.4 GSPS operation
- Choice of single or dual data rate output clocking
- Multiple ADC synchronization capability
- Serial interface for extended control (gain, offset)
- Demultiplexed LVDS outputs simplify data capture

Product ID	Description
ADC081000	8-Bit, 1 GSPS
ADC081500	8-Bit, 1.5 GSPS
ADC08D500	8-Bit, dual, 500 MSPS (1 GSPS in DES mode)
ADC08D1000	8-Bit, dual, 1 GSPS (2 GSPS in DES mode)
ADC08D1500	8-Bit, dual, 1.5 GSPS (3 GSPS in DES mode)

Clock Generator



Simplified Receiver Path



Applications:

- Spectrum analyzer
- Radar system
- Microwave links
- Wireless infrastructure

Local Oscillator PLLatinum™ Frequency Synthesizers

Product ID	Type	Frequency	Normalized Phase Noise	Phase Noise at Offset Frequency	Package
LMX2434	High Frequency Integer-N Dual PLL	1.0 - 5.0 GHz	-219 dBc/Hz	–	UTCSP-20, TSSOP-20
LMX2430	Integer-N Dual PLL	0.2 - 3.0 GHz	-219 dBc/Hz	–	UTCSP-20, TSSOP-20
LMX2470	Delta-Sigma Fractional-N PLL	0.5 - 2.6 GHz	-210 dBc/Hz	–	UTCSP-24
LMX2364	Fractional-N PLL	0.5 - 2.6 GHz	-210 dBc/Hz	–	UTCSP-24, TSSOP-24
LMX2347	Integer-N Single PLL	0.2 - 2.5 GHz	-217 dBc/Hz	–	CSP-16, TSSOP-16
LMX2512	Frequency Synthesizer System with Integrated VCO	~ 1.0 GHz	–	-139 dBc/Hz at 900 kHz	LLP-28

ADCs for Test and Measurement

					Dynamic Performance				
Product ID	**Resolution**	**Speed (MSPS)**	**Supply Voltage (V)**	**Power (mW)**	**SFDR (dB)**	**THD (dB)**	**ENOB (bit)**	**SNR (dB)**	**Package**
ADC08D1000	8-bit dual	1000	1.9	1600	55	-55	7.4	47	LQFP-128 Exp. Pad
NEW! **ADC08D1500**	8-bit dual	1500	1.9	1840	53	-53	7.3	46	LQFP-128 Exp. Pad
NEW! **ADC10DL065**	10-bit dual	65	3.3	360	80	-78	9.8	61	TQFP-64
ADC12L080	12 bit	80	3.3	425	80	-77	10.7	66	LQFP-32
NEW! **ADC12DL040**	12-bit dual	40	3	210	86	-83	11.1	69	TQFP-64
NEW! **ADC12DL065**	12-bit dual	65	3.3	360	86	-84	11.1	69	TQFP-64
NEW! **ADC12QS065**	12-bit quad	65	3	800	85	-83	11.0	69	TQFP-64, LLP-60
NEW! **ADC14L040**	14 bit	40	3.3	236	90	87	11.9	73	LQFP-32

Amplifiers and Comparators for Test and Measurement

Product ID	Type	SSBW (MHz, A_V = 1)	Slew Rate (V/μs, A_V=1)	I_{CC} (mA/ch)	2nd/3rd HD (dBc, V_{OUT} = 2 V_{PP})	Voltage Noise (nV /√Hz)	Package
NEW! **LMH6550**	Fully differential ADC driver with disable	400	3000	20.0	-92 / -103 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
NEW! **LMH6551**	Fully differential ADC driver	370	2400	12.5	-94 / -96 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
LMH6702	Ultra-low distortion CFB op amp	1.7 GHz[1]	3100[1]	12.5	-100 / -96 at 5 MHz, R_L=100Ω	1.8	SOIC-8, SOT23-5
NEW! **LMH6703**	1.2 GHz low distortion op amp w/shutdown	1.2 GHz[1]	4200[1]	11.0	-87/ -100 at 5 MHz, R_L=100Ω	2.3	SOIC-8, SOT23-6
LMH6609	900 MHz, unity gain stable, VFB op amp	900	1400	7.0	-87 / -82 at 5 MHz, R_L=100Ω	3.1	SOIC-8, SOT23-5
LMH6574	4:1 Mux, -70 dB crosstalk	500[1]	2200	13.0	-65 / -86 at 5 MHz, R_L=100Ω	5.0	SOIC-14
Product ID	**Type**	**Response Time (ns)**	**Rise/ Fall Times**	**I_{CC} (mA/ch)**	**CMVR**	**Output Config**	**Package**
LMV7219	7 ns, 2.7V to 5V comparator w/ RRO	7	1.3 ns	1.1	-0.2V to 3.8V	Push-pull	SC70-5, SOT23-5

[1] A_V = +2

Understanding High-Speed Signals...

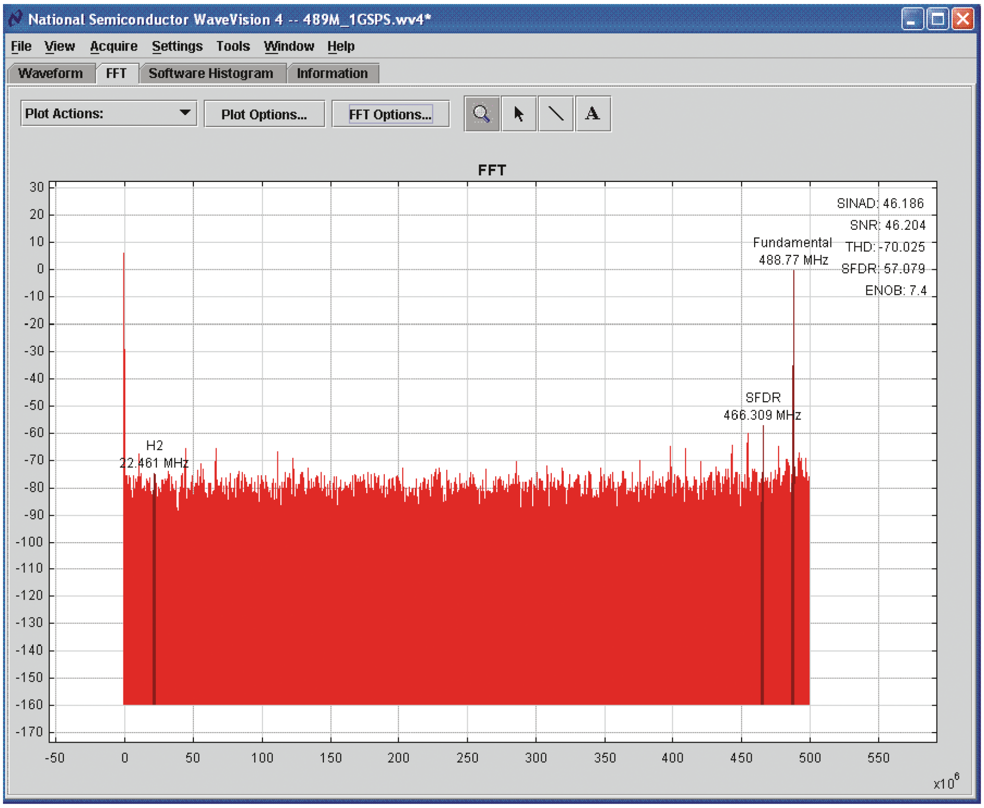


Figure 3. FFT Plot of a 489 MHz Sine Wave Sampled at 1 GSPS

using the circuit in ***Figure 2*** to sample an input frequency of 489 MHz.

Data Capture

Sampling signals at high frequencies (1 GSPS and above) means that the digital output data produced by the conversion has to be stored or at least transferred at very fast speeds. The two key issues when handling a billion conversions a second is that of signal integrity between the digital components in the system and also the rate of data transfer for each clock cycle.

To maximize the signal integrity of the digital outputs, high-speed ADCs use Low Voltage Differential Signaling or LVDS (see ***Figure 4***).

The main advantage of the LVDS signaling method is that high data rates can be reached for a very low power budget. This is achieved through the use of 2 wires for each discrete signal that is to be carried across a circuit board or cable. The voltages on each of these conductors swing in opposite directions and also have a very small amplitude (typically 350 mV) when compared to single-ended signaling such as CMOS or TTL. It is because of the inherent noise immunity of the differential circuit that low voltage swings can be used. This in turn means that the signal frequency can be faster as the rise time is shorter.

The signal lines that carry the differential waveform on a circuit board should be designed to have a characteristic impedance of 100 Ohms (defined by the LVDS standard). These lines are then differentially terminated at the receiver with a 100 Ohm resistor to match the line. A signal voltage is generated across this 100 Ohm resistor by a 3.5 mA current source within the transmitter circuit which provides the 350 mV signal swing for the receiving circuit to detect.

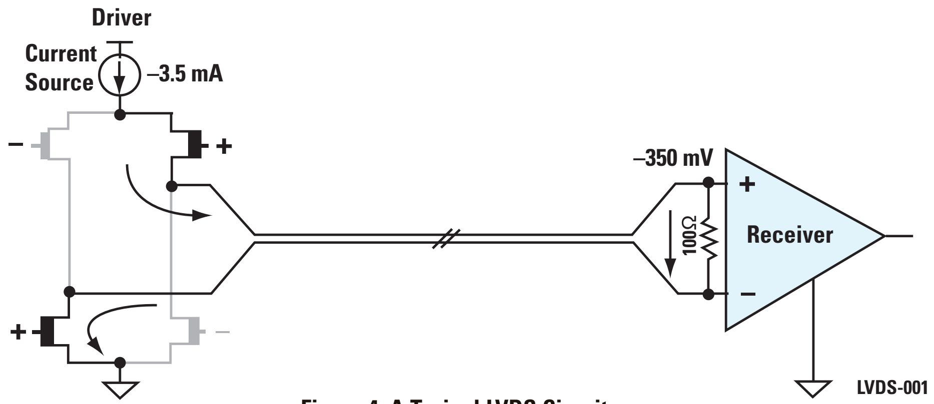


Figure 4. A Typical LVDS Circuit

Transmitting the data at high speeds is only half of the problem. Storing the data into a memory array for post processing is also to be considered. The ADC provides a de-multiplexed data output for each of its two channels. Instead of providing a single 8-bit bus running at a data rate equal to the sample rate, the device outputs two consecutive samples simultaneously on two 8-bit data buses. This method reduces the data rate by a half but increases the number of bits. For a 1 GSPS sample rate, the conversion data output from the ADC is 500 MHz. Even at this reduced speed, most discrete or internal FPGA memories would have problems capturing this data reliably. It is therefore beneficial to use a Dual Data Rate (DDR) method where data is presented to the outputs on both the rising and falling edges of the clock. While the data rate remains the same for DDR signaling, the clock frequency is halved again to a more manageable 250 MHz. This frequency is now in the realm of CMOS memory circuits. Before the data can be stored to memory, it requires an intermediate pair of data latches at the input to the FPGA device. The first latch of the pair is clocked using an in-phase data clock, while the second latch is clocked using a signal that is 180 degrees out of phase or an inverted data clock (see ***Figure 5***).

To simplify this clocking requirement, FPGAs come equipped with digital clock managers in the form of PLLs (Phase Locked Loop) or DLLs (Delay Locked Loop). These devices allow clock signals to be generated internally that are phase locked to an input clock, and offer phase delay taps of 0, 90, 180, and 270 degrees. This clock management feature allows a DDR clocking scheme to work effectively by providing a precise 180 degree phase-shifted clock. This in turn allows the incoming data synchronous to the falling edge to be captured reliably into a data latch.

After being latched, the incoming data can be transferred to a FIFO memory or Block RAM. From there the data can be easily retrieved by the system microcontroller at a much slower speed for post-capture processing.

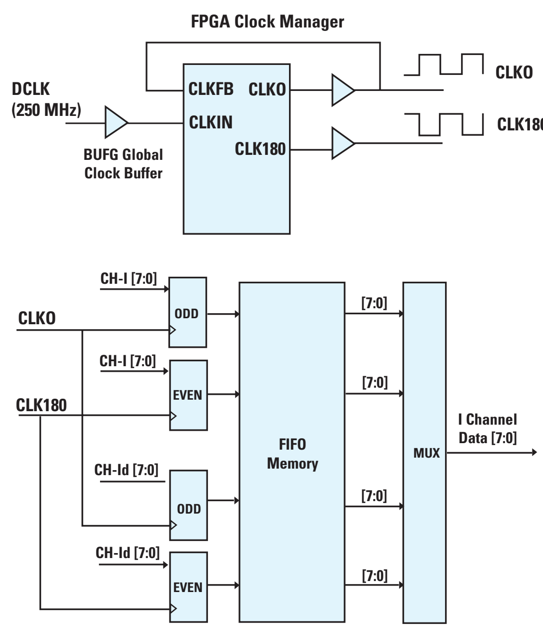


Figure 5. FPGA Data Capture Architecture

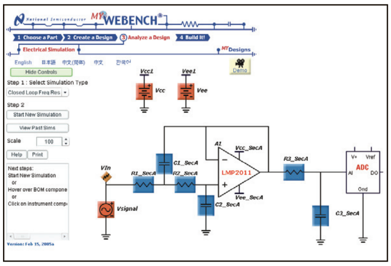
Summary

Ultra high-speed data conversion offers many challenges to the system designer. This is truly a mixed-signal environment in which all the sub circuits have to be considered carefully to allow the ADC to deliver the optimum dynamic performance. Clock systems that meet the low jitter requirements can be realized economically using off-the-shelf components. Similarly, FPGAs are available today with many supporting features for systems that include full LVDS support and clock management circuits. ■

Design Tools

INTRODUCING...

Signal-Path Design Tool



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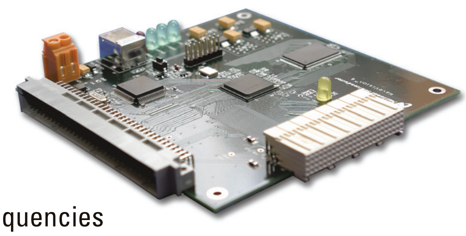

Features and benefits:

- Plug-n-play ADC evaluation board
- USB interface to PC
- PC-based data capture
- Easy data capture and evaluation
- Highlighted harmonic and SFDR frequencies
- Easy waveform examination
- Produces and displays FFT plots
- Dynamic performance parameter readout with FFT
- Produces and displays histograms

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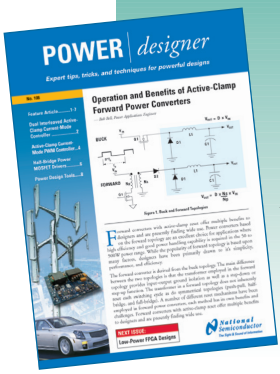

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