Application Report

ITU-T G.8262 Compliance Test Results for the LMK5C33216

ABSTRACT

The LMK5C33216 is an ultra-low jitter clock synchronizer with integrated EEPROM targeted for communication and industrial applications. This document details the compliance of the LMK5C33216 to the ITU-T G.8262 (timing characteristics of a synchronous Ethernet equipment slave clock) standard.

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Trademarks

1 Introduction

The LMK5C33216 device is a high-performance network clock generator, synchronizer, and jitter attenuator with advanced reference clock selection and hitless switching capabilities designed to meet the stringent requirements of communications infrastructure applications.

This document contains the summary of the test setups and measured results highlighting compliance to ITU-T G.8262 (Timing characteristics of a synchronous Ethernet equipment slave clock) standard. The device-under-test (LMK5C33216) was configured using Texas Instruments' TICS Pro Silicon EVM Programming Tool. Unless specified otherwise, the LMK5C33216 Digital PLL loop bandwidth for EEC-Option 1 was set to 10 Hz and for EEC-Option 2 to 0.1 Hz.

All measurement results included in this document are for DPLL1. The measurement results for DPLL1 are an accurate representation of compliance characteristics for all three DPLLs. All three DPLLs passed standard compliance test requirements.

Throughout this document, the acronym MTIE stands for maximum time interval error and the acronym TDEV stands for time deviation.

Testing was performed using the Calnex Rb/GPS frequency reference and Calnex Paragon-T hardware. Other test hardware was used as required for the measurements.

Notable features of this high-performance device includes:

- Hitless Switching with minimal phase transients (< 100 ps)
- Ultra High-Performance VCO allows use of a low-cost holdover reference without sacrificing performance
- High-Performance DPLL Channel with Programmable loop bandwidth for jitter and wander filtering suitable for EEC Option 1 and EEC Option 2
- Reference Priority Selection, Gapped Clock and Runt Pulse Detectors, Automatic/Manual Switchover, Holdover, and Tuning Word History

Table 1-1. DPLL1 ITU-T G.8262 Compliance Summary

SECTION	DESCRIPTION	EEC OPT 1 (SECTION IN G.8262)	EEC OPT 2 (SECTION IN G.8262)	COMPLIANT
WANDER GENERATION				
Section 2.1	MTIE EEC Option 1; Must not exceed MTIE mask	8.1.1		Yes
Section 2.2	TDEV EEC Option 1; Must not exceed TDEV mask	8.1.1		Yes
Section 2.3	MTIE EEC Option 2; Must not exceed MTIE mask		8.1.2	Yes
Section 2.3	TDEV EEC Option 2; Must not exceed TDEV mask		8.1.2	Yes
WANDER TRANSFER				
Section 3.1	Transfer function of the PLL for EEC Option 1 and EEC Option 2; Must meet bandwidth requirements	10.1	10.2	Yes
Section 3.2	Wander Transfer TDEV G.8262 for EEC Option 2; Must not exceed TDEV mask		10.2	Yes
WANDER TOLERANCE				
Section 4.1	Wander Tolerance EEC Option 1; Must tolerate at least input wander defined by MTIE/TDEV mask	9.1.1		Yes
Section 4.2	Wander Tolerance EEC Option 2; Must tolerate at least input wander defined by TDEV mask		9.1.2	Yes
JITTER TOLERANCE				
Section 5.1	Jitter Tolerance for EEC Option 1 and EEC Option 2; Must tolerate jitter defined by UI mask	9.2.1	9.2.1	Yes
PHASE TRANSIENT GENERATION				
Section 6.1	Short Term Phase Transient EEC Option 1; Must not exceed limits set by standard	11.1.1		Yes
Section 6.2	Short Term Phase Transient EEC Option 2; Must not exceed MTIE mask set by standard		11.1.2 11.4.2	Yes
Section 6.3	Phase Transient Generation with Signal Interruptions EEC Option 1; Must not exceed phase variation limit	11.3.1		Yes

Table 1-1. DPLL1 ITU-T G.8262 Compliance Summary (continued)

SECTION	DESCRIPTION	EEC OPT 1 (SECTION IN G.8262)	EEC OPT 2 (SECTION IN G.8262)	COMPLIANT
Section 6.4	Phase Discontinuity EEC Option 1; Must not exceed phase variation limits	11.4.1		Yes
Section 6.5	Phase Discontinuity EEC Option 2; Must not exceed MTIE mask set by standard		11.4.2	Yes
HOLDOVER PERFORMANCE				
Section 7.1	Holdover EEC Option 1; Must not exceed TIE mask set by standard	11.2.1		Yes
Section 7.2	Holdover EEC Option 2; Must meet TIE mask set by standard		11.2.2	Yes
FREE-RUN ACCURACY				
Section 8.1	Free-run Accuracy EEC Option 1 and Option 2; Must not exceed ±4.6 ppm	6.1	6.2	Yes
PULL-IN AND HOLD-IN				
Section 9	Pull-in and Hold-in EEC Option 1 and Option 2; Minimum pull-in range and hold-in range must be ±4.6 ppm	7.1.1	7.1.2 7.2.2	Yes

2 Wander Generation

The following MTIE and TDEV ECC option 1 and 2 tests measure the amount of wander generated by the LMK5C33216. Figure 2-1 shows the setup used for these tests.

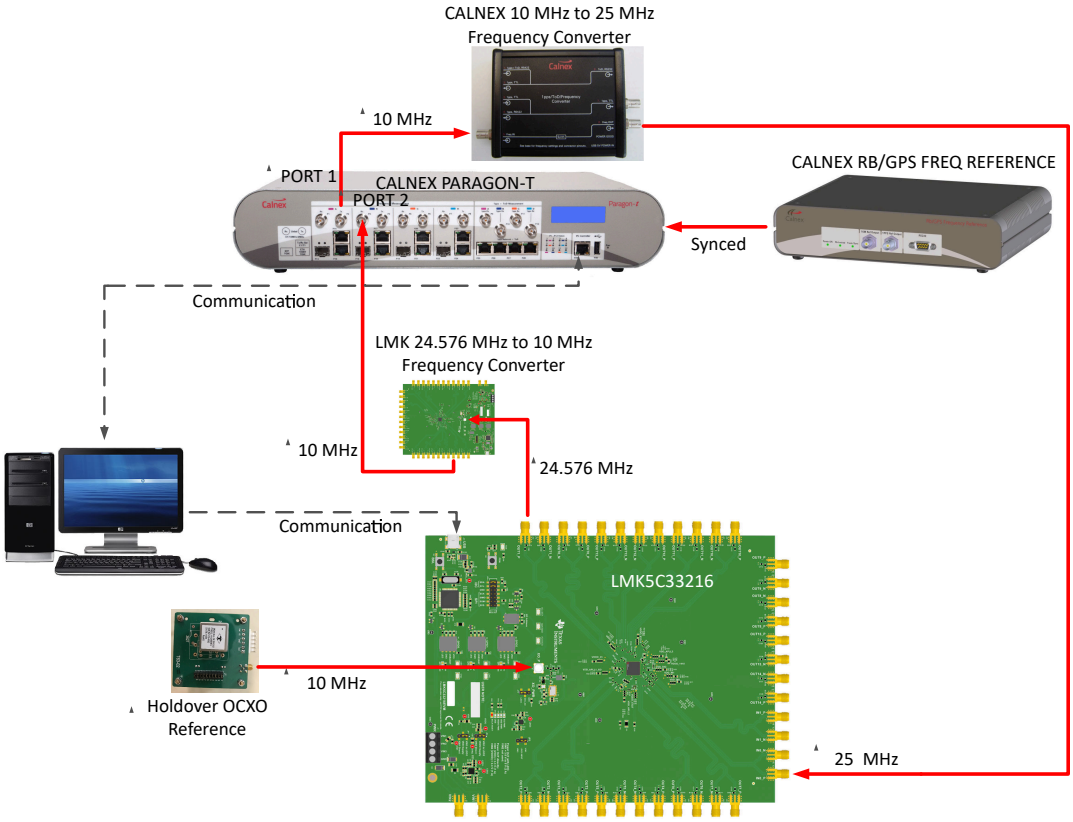

Figure 2-1. Test Setup for Wander Generation

2.1 Wander Generation MTIE Option 1, G.8262 EEC Option 1

While the DPLL is locked to an input clock that is wander-free, it will not generate wander that exceeds the green MTIE masks shown in Figure 2-2 and Figure 2-3. These masks can be seen in Figure 1 in the G.8262 specification. There is no noise modulation applied to the input for this test. The LMK5C33216 passed the Wander Generation MTIE Option 1, G.8262 EEC Option 1 requirement as shown in Figure 2-2 and Figure 2-3.

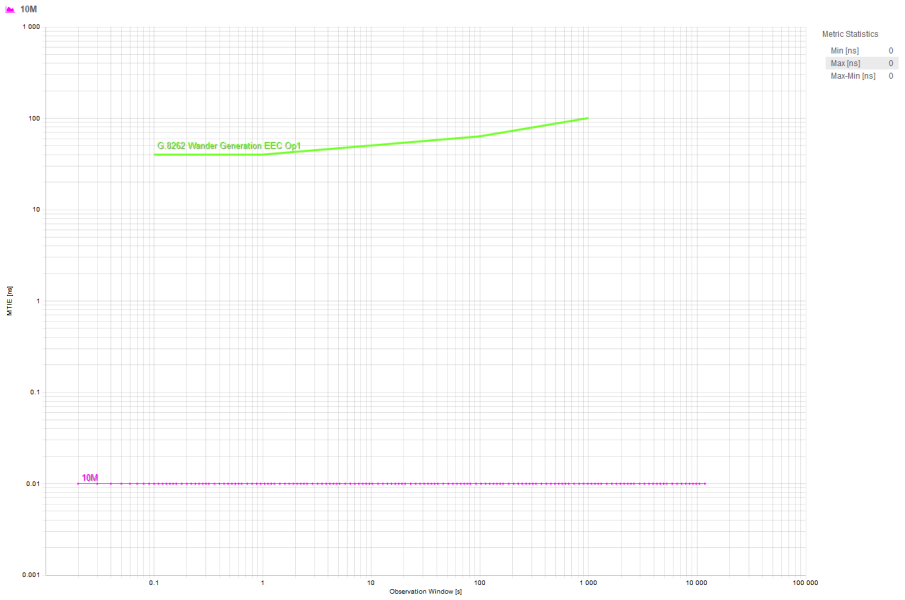

Figure 2-2. Wander Generation MTIE Option 1, G.8262 EEC Option 1 Results, Tested at Constant Room Temperature With DPLL Bandwidth of 10 Hz

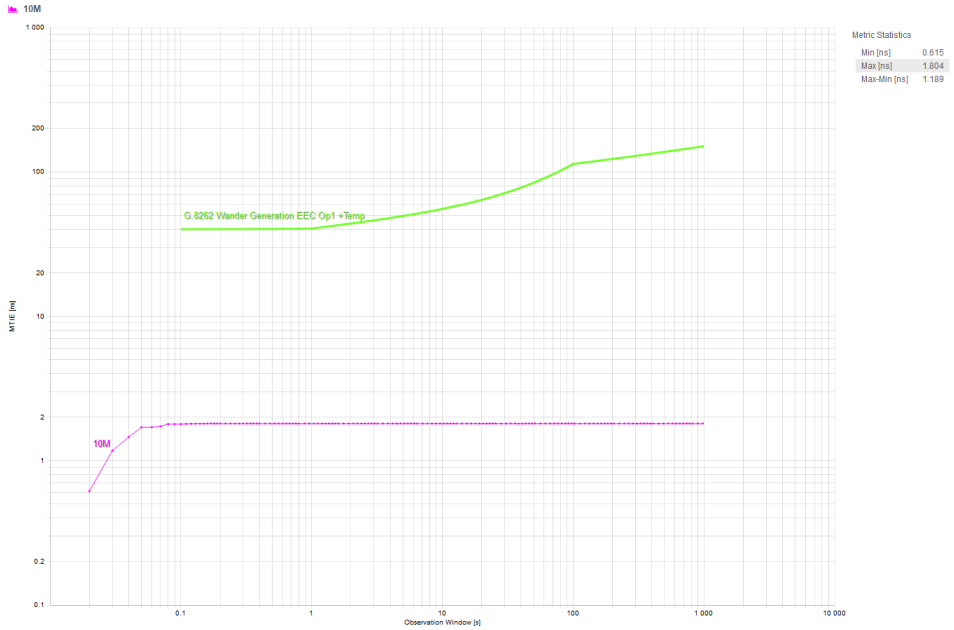

Figure 2-3. Wander Generation MTIE Option 1, G.8262 EEC Option 1 Results, Tested at Temperature of 85°C With DPLL Bandwidth of 10 Hz

2.2 Wander Generation TDEV G.8262 EEC Option 1

While the DPLL is locked to an input clock signal that is wander-free, it will not generate wander that exceeds the green TDEV mask shown in Figure 2-4 (Figure 2 in the G.8262 specification). The LMK5C33216 passed the Wander Generation TDEV G.8262 EEC Option 1 requirement as shown in Figure 2-4.

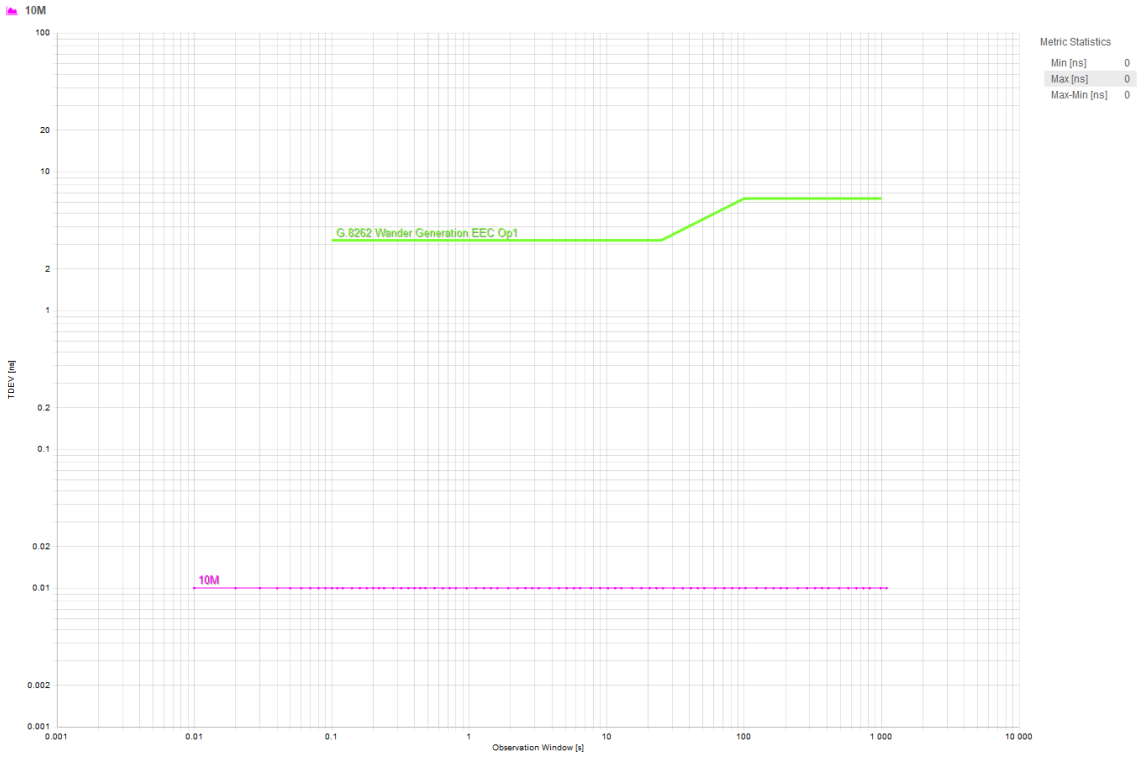

Figure 2-4. Wander Generation TDEV G.8262 EEC Option 1 Results, Tested at Constant Room Temperature With DPLL Bandwidth of 10 Hz

2.3 Wander Generation MTIE Stratum ITU-T G.8262 EEC Option 2

While the DPLL is locked to an input clock signal that is wander-free, it will not generate wander that exceeds the green MTIE mask shown in Figure 2-5 (Figure 3 in the G.8262 specification). The LMK5C33216 passed the Wander Generation MTIE Stratum ITU-T G.8262 EEC Option 2 requirement as shown in Figure 2-5.

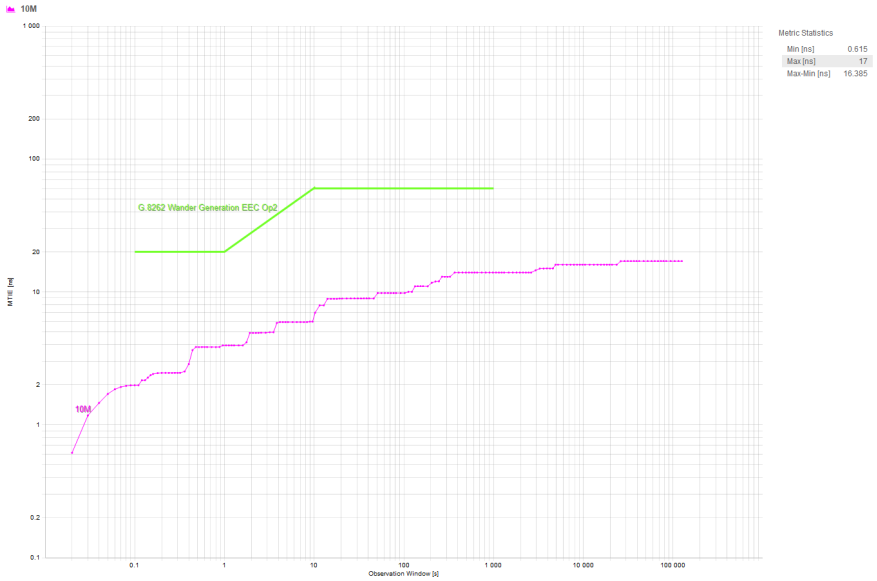

Figure 2-5. Wander Generation MTIE ITU-T G.8262 EEC Option 2 Results, Tested at Constant Room Temperature With DPLL Bandwidth of 0.1 Hz

2.4 Wander Generation TDEV G.8262 EEC Option 2

While the DPLL is locked to an input clock signal that is wander-free, it will not generate wander that exceeds the green TDEV mask shown in Figure 2-6 (Figure 4 in the G.8262 specification). The LMK5C33216 passed the Wander Generation TDEV G.8262 EEC Option 2 requirement as shown in Figure 2-6.

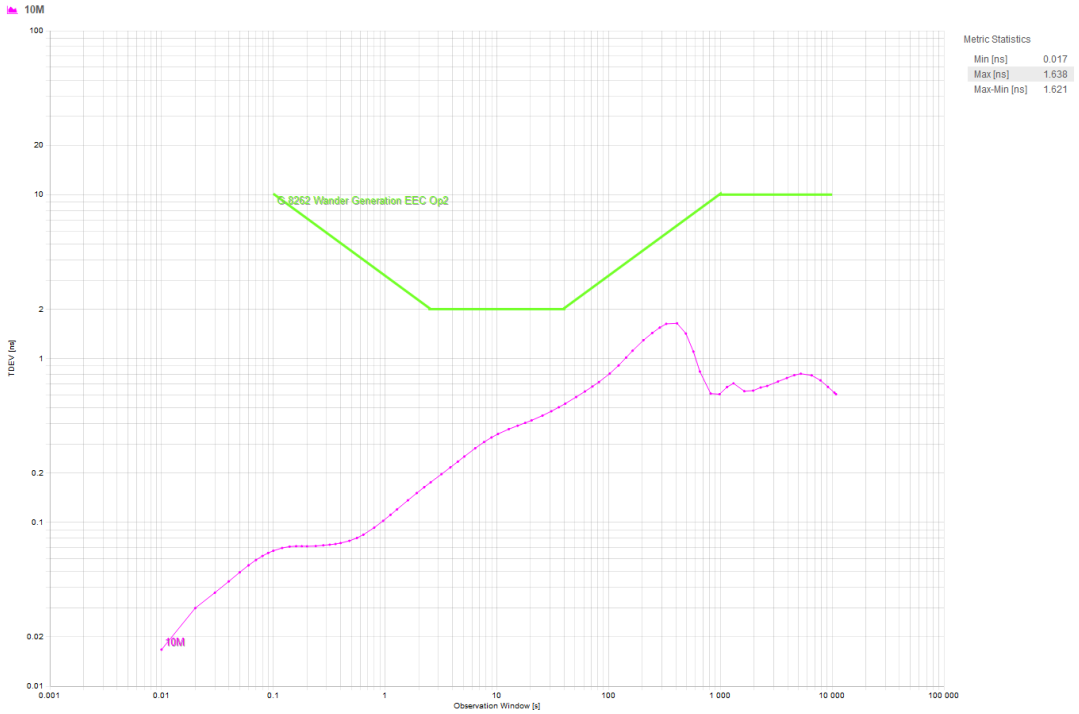

Figure 2-6. Wander Generation TDEV G.8262 EEC Option 2 Results, Tested at Constant Room Temperature With DPLL Bandwidth of 0.1 Hz

3 Wander Transfer

The following ECC option 1 and 2 tests measure the wander transfer of the LMK5C33216. Figure 3-1 shows the setup used for these tests.

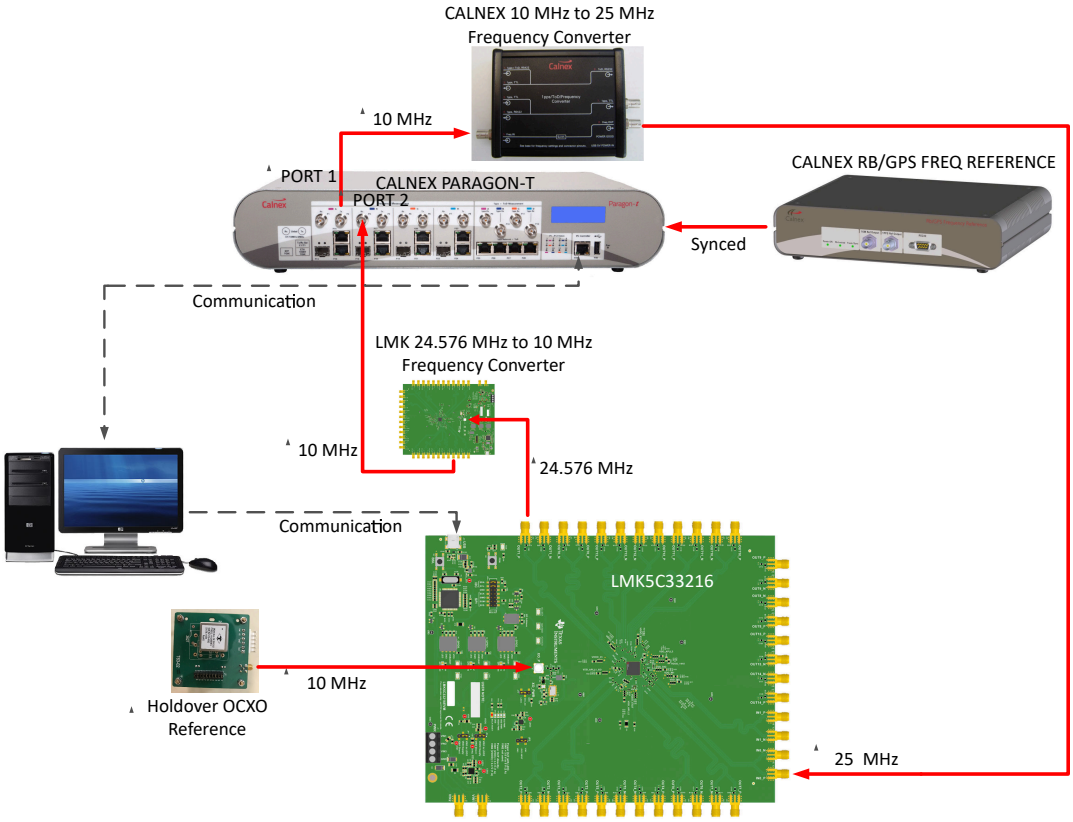

Figure 3-1. Test Setup for Wander Transfer

3.1 Transfer Function of the PLL for Option 1 and Option 2

Wander transfer is determined by the DPLL loop BW and peaking. For Option 1, the DPLL loop bandwidth was set to 10 Hz and for Option 2, the DPLL loop bandwidth was set to 0.1 Hz. Both Option 1 and Option 2 require < 0.2 dB of peaking. The LMK5C33216 meets the requirements for the transfer function of the PLL for EEC Option 1 and Option 2 as shown in Figure 3-2 and Figure 3-3. The results show a close match between expected bandwidth and measured bandwidth on LMK5C33216. For Option 1, the expected bandwidth is 10 Hz and the measured bandwidth is around 10 Hz. For Option 2, the expected bandwidth is 0.1 Hz and the measured bandwidth is around 0.1 Hz.

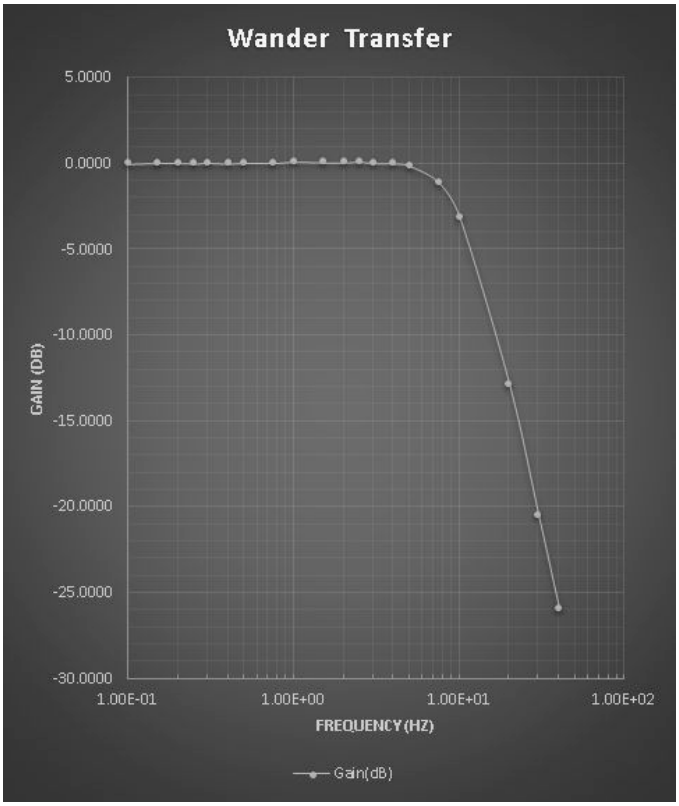

Figure 3-2. Wander Transfer EEC Option 1 With Max DPLL Bandwidth of 10 Hz

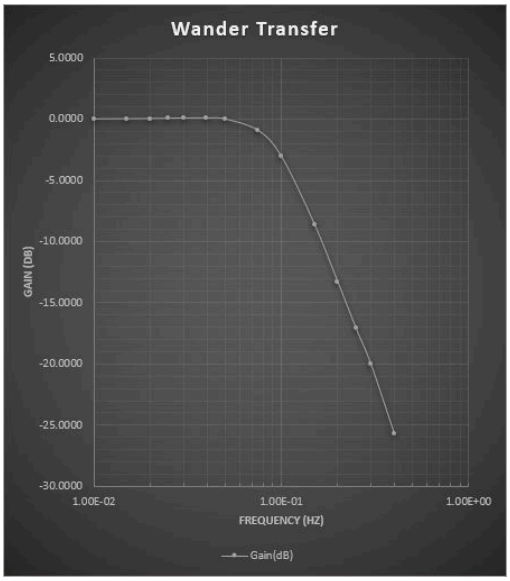

Figure 3-3. Wander Transfer EEC Option 2 With Max DPLL Bandwidth of 0.1 Hz

3.2 Wander Transfer TDEV G.8262 Option 2

The process for this specification is to measure the output wander (TDEV) when the device is locked to a clock that has wander as defined by the TDEV mask shown in figure 8 in the G.8262 specification and Table 3-1 (Table 10 in the G.8262 specification) and to ensure that the TDEV output is below the mask shown in figure 11 in the G.8262 specification. Results from Section 3.1 offer sufficient information regarding the bandwidth of the DPLL to state that the LMK5C33216 meets the requirements for wander transfer TDEV G.8262 Option 2.

Table 3-1. Input Wander Tolerance (TDEV) for EEC-Option 2

TDEV LIMIT (ns)	OBSERVATION INTERVAL τ (s)
17	$0.1 < \tau \leq 3$
$5.77 \times \tau$	$3 < \tau \leq 30$
$31.6325 \times \tau^{0.5}$	$30 < \tau \leq 1000$

4 Wander Tolerance

The following ECC option 1 and 2 tests measure the wander tolerance of the LMK5C33216. Figure 4-1 shows the same general setup used for these tests.

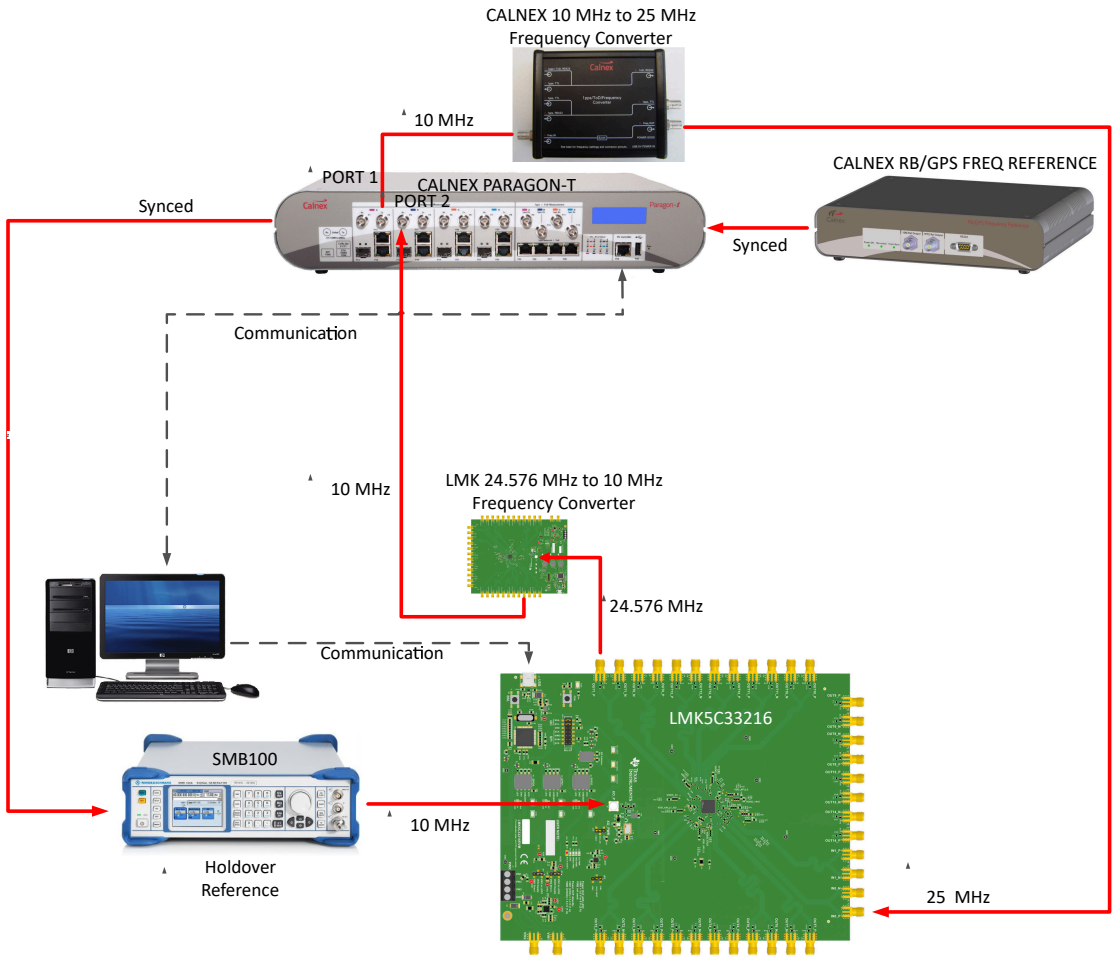

Figure 4-1. Test Setup for Wander Tolerance

4.1 Wander Tolerance G.8262 Option 1

A PLL that is locked to an input clock must be able to tolerate the wander defined in figure 5 in the G.8262 specification. The definition of tolerance is such that the device will not trigger any alarms while locked to such an input clock and it will be able to pull-in to such as an input clock. Test signals with a sinusoidal phase variation

can be used, according to the levels in Table 4-1 (Table 9 in the G.8262 specification), to check conformance to the mask in figure 5 in the G.8262 specification.

Test signals with sinusoidal phase variation according to levels shown in Table 4-1 were introduced using the Calnex Paragon-T box. There were no amplitude, frequency, or missing clock cycle alarms flagged by the LMK5C33216 DUT (10-Hz loop bandwidth). The device stayed locked and was able to pull-in to the input clock throughout the duration of this test. The LMK5C33216 showed a passing result for the wander tolerance G.8262 Option 1 specification.

Table 4-1. Lower Limit of Maximum Tolerable Sinusoidal Input Wander for EEC-Option 1 (1)

PEAK-TO-PEAK WANDER AMPLITUDE			WANDER FREQUENCY				
A_1 (µs)	A_2 (µs)	A_3 (µs)	f_4 (mHz)	f_3 (mHz)	f_2 (mHz)	f_1 (Hz)	f_0 (Hz)
0.25	2	5	0.32	0.8	16	0.13	10

(1) Table 4-1 shows the resultant requirements

4.2 Wander Tolerance G.8262 Option 2

A PLL that is locked to an input clock must be able to tolerate the wander defined in figure 8 in the G.8262 specification. The definition of tolerance is such that the device will not trigger any alarms while locked to such an input clock and it will be able to pull-in to such as an input clock. Test signals with sinusoidal phase variation according to levels shown in Table 4-1 (Table 9 in the G.8262 specification) were introduced using the Calnex Paragon-T box for this test, too. There were no amplitude, frequency, or missing clock cycle alarms flagged by the LMK5C33216 DUT (0.1-Hz loop bandwidth), and the device stayed locked and was able to pull-in to the input clock throughout the duration of this test. The LMK5C33216 showed a passing result for the wander tolerance G.8262 Option 2 specification.

5 Jitter Tolerance

The following ECC option 1 and 2 tests measure the jitter tolerance of the LMK5C33216. Figure 5-1 shows the setup used for these tests.

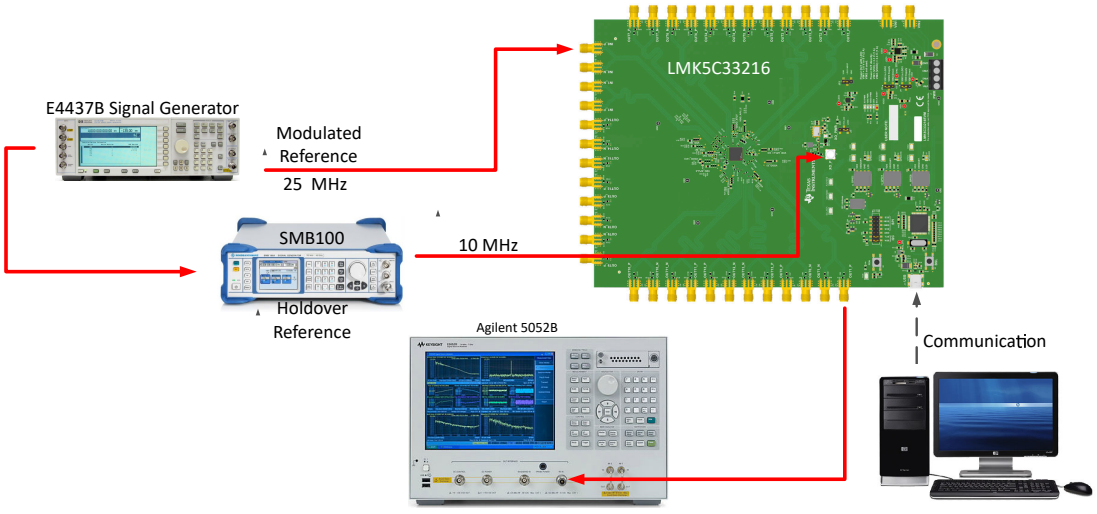

Figure 5-1. Test Setup for Jitter Tolerance

5.1 Jitter Tolerance G.8262 Option 1 and Option 2

A PLL that is locked to an input clock must be able to tolerate the jitter defined in figure 9 in the G.8262 specification and figure 10 in the G.8262 specification. The definition of tolerance is that the device will not trigger any alarms while locked to such an input clock and that it will be able to pull-in to such an input clock. For Option 1, LMK5C33216 DPLL loop bandwidth was set to 10 Hz. For Option 2, the DPLL loop bandwidth was set to 0.1 Hz. For this test, the modulation frequency and frequency deviation was applied on the E4437B.

In compliance with the jitter tolerance specification requirement, the reference clock to LMK5C33216 (generated using E4437B) was modulated. The LMK5C33216 met the jitter tolerance requirements per the standard. The

LMK5C33216 did not trigger any alarms, stayed locked to the reference and there was no observed degradation to the integrated RMS (12 kHz to 20 MHz) phase jitter of the output clock (156.25 MHz). The integrated RMS phase jitter was < 250 fs (max) for the duration for this test.

Table 5-1. 1G Synchronous Ethernet Wideband Jitter Tolerance for EEC-Option 1 & EEC-Option 2 (1)

PEAK-TO-PEAK JITTER AMPLITUDE (UI)	FREQUENCY f (Hz)
312.5	10 < f ≤ 12.1
3750 f^{-1}	12.1 < f ≤ 2.5k
1.5	2.5k < f ≤ 50k

(1) 1G includes 1000BASE-KX, -SX, -LX; multi-lane interfaces are for further study.

Table 5-2. 10G Synchronous Ethernet Wideband Jitter Tolerance for EEC-Option 1 and EEC-Option 2 (1)

PEAK-TO-PEAK JITTER AMPLITUDE (UI)	FREQUENCY f (Hz)
2488	10 < f ≤ 12.1
3000 f^{-1}	12.1 < f ≤ 20k
1.5	20k < f ≤ 40k

(1) 10G includes 10GBASE-SR/LR/ER, 10GBASE-LRM, 10GBASE-SW/LW/EW and multi-lane interfaces consisting of 10G lanes including 40GBASE-KR4/CR4/SR4/LR4 and 100GBASE-CR10/SR10.

Table 5-3. 25G Synchronous Ethernet Wideband Jitter Tolerance for EEC-Option 1 and EEC-Option 2 (1)

PEAK-TO-PEAK JITTER AMPLITUDE (UI)	FREQUENCY f (Hz)
6445	10 < f ≤ 11.17
72000 f^{-1}	11.17 < f ≤ 20k
3.6	20k < f ≤ 100k

(1) 25G includes multi-lane interfaces consisting of 25G lanes including 100GBASE-LR4/ER4.

Table 5-4. 1G Test Conditions

MOD FREQUENCY (Hz)	PEAK-TO-PEAK PHASE AMPLITUDE (UI)	FREQ DEVIATION (kHz)
10	312.5	0.245
12.1	312.5	0.297
100	40	0.314
1000	4	0.314
2500	1.5	0.295
10000	1.5	1.178
50000	1.5	5.890

Table 5-5. 10G Test Conditions

MOD FREQUENCY (Hz)	PEAK-TO-PEAK PHASE AMPLITUDE (UI)	FREQ DEVIATION (kHz)
10	2488	0.195
12.1	2488	0.236
100	300	0.236
1000	30	0.236
2500	12	0.236
20000	1.5	0.236

Table 5-5. 10G Test Conditions (continued)

MOD FREQUENCY (Hz)	PEAK-TO-PEAK PHASE AMPLITUDE (UI)	FREQ DEVIATION (kHz)
40000	1.5	0.471

Table 5-6. 25G Test Conditions

MOD FREQUENCY (Hz)	PEAK-TO-PEAK PHASE AMPLITUDE (UI)	FREQ DEVIATION (kHz)
10	6455	0.203
11.17	6455	0.227
100	720	0.226
1000	72	0.226
2500	28.8	0.226
20000	3.6	0.226
100000	3.6	1.131

6 Phase Transient Generation

The following EEC option 1 and 2 tests measure the short-term phase transient of the LMK5C33216. Figure 6-1 shows the setup used for these tests.

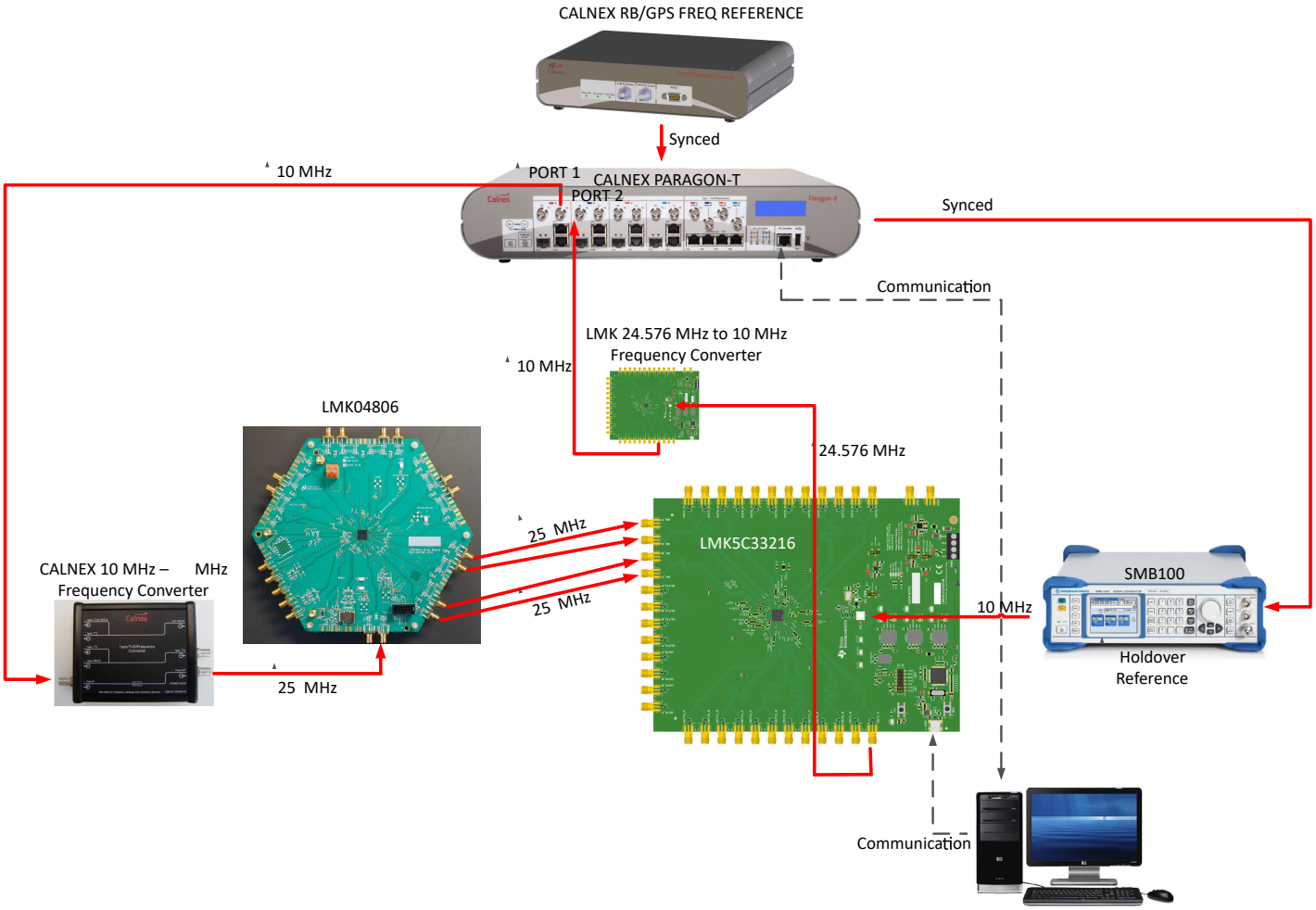

Figure 6-1. Test Setup for Phase Transient Generation

6.1 Short-Term Phase Transient Response G.8262 Option 1

For this test, the device is forced into holdover for 15 seconds by performing a manual switch from a valid active clock input (IN0) to another input with no valid signal (IN1), then the holdover state is exited by manually switching back to the valid active clock input. The test is completed after an entry into holdover and exit from holdover has taken place within 15 seconds. The output phase variation, relative to the input reference before it was lost, is bounded by the following requirements.

The phase error must not exceed $\Delta t + 5 \times 10^{-8} \times S$ seconds over any period S up to 15 seconds. Δt represents two phase jumps that may occur during the transition into and out of holdover state which both must not exceed 120 ns with a temporary frequency offset of no more than 7.5 ppm. The resultant overall requirements is summarized in green in Figure 6-2 (Figure 12 in the G.8262 specification). This figure is intended to depict the worst-case phase movement attributable to an EEC reference clock switch.

The LMK5C33216 passed the requirements for short-term phase transient response. No significant *phase hits* were observed during holdover entry and exit using LMK5C33216.

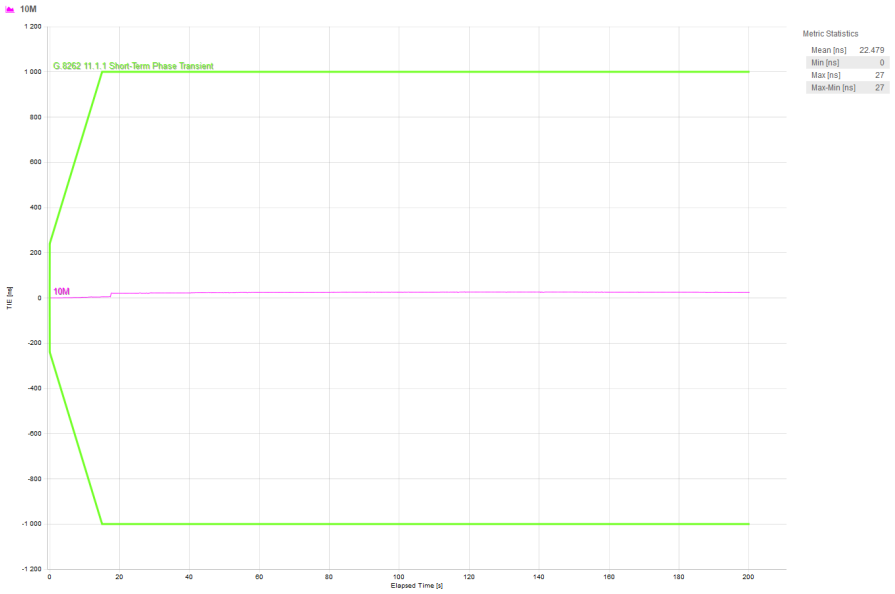

Figure 6-2. Short-Term Phase Transient Result

6.2 Short-Term Phase Transient Response G.8262 Option 2

For this test, the device is forced into holdover for 15 seconds by performing a manual switch from a valid active clock input (IN0) to another input with no valid signal (IN1), then the holdover state is exited by manually switching back to the valid active clock input. The test is completed after an entry into holdover and exit from holdover has taken place within 15 seconds. The output will not exceed the green MTIE requirement shown in Figure 6-3 (Figure 14 in the G.8262 specification).

The below MTIE data captures the phase transient at the output of LMK5C33216 during multiple reference clock switchover events, displaying a passing result. The resolution of Calnex equipment is limited to 1 ns for MTIE. The unique phase cancellation scheme implemented in LMK5C33216 allows for a phase transient < 100 ps which cannot be measured accurately using this setup.

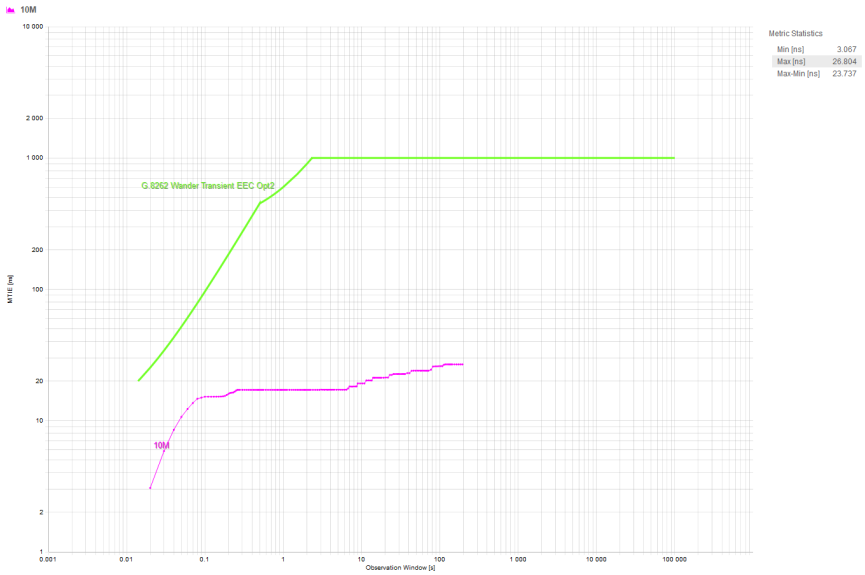

Figure 6-3. Short-Term Phase Transient Option 2

6.3 Phase Transient Generation With Signal Interruptions G.8262 EEC Option 1

The passing condition for this specification is that an input interruption that does not force a switchover does not cause an output phase transient greater than 120 ns with a maximum frequency offset of 7.5 ppm in a period of 16 ms. For this setup, a pulse generator was inserted into the general setup as in Figure 6-4. An 8110A pulse generator is used to generate a gapped clock and was set to generate 25 MHz with 1 pulse missing every 2048 clock cycles. This gapped clock was used as reference to LMK5C33216 and the LMK5C33216 output was monitored for phase transients.

The LMK5C33216 passed the requirements for the phase transient generation with signal interruptions G.8262 EEC Option 1. There were no significant phase hits (meets compliance requirements) during operation of the device while receiving a gapped clock as reference.

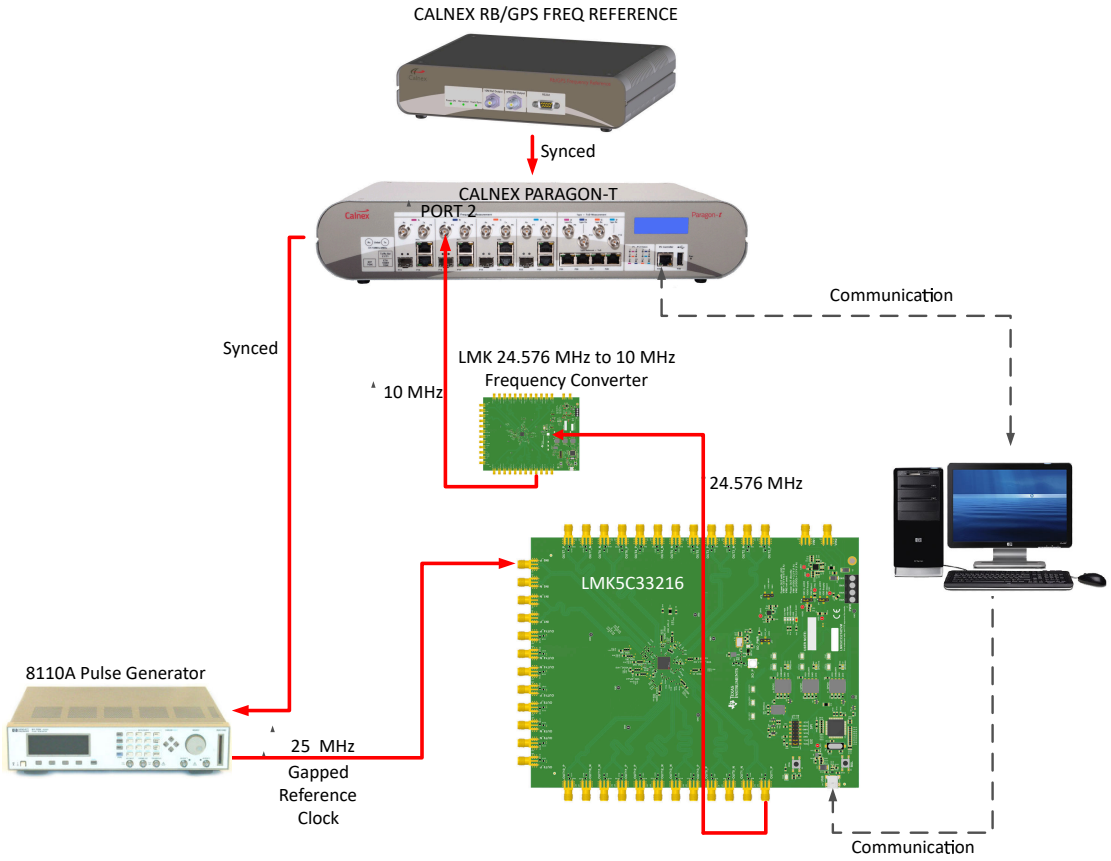

Figure 6-4. Test Setup for Phase Transient Generation With Signal Interruption

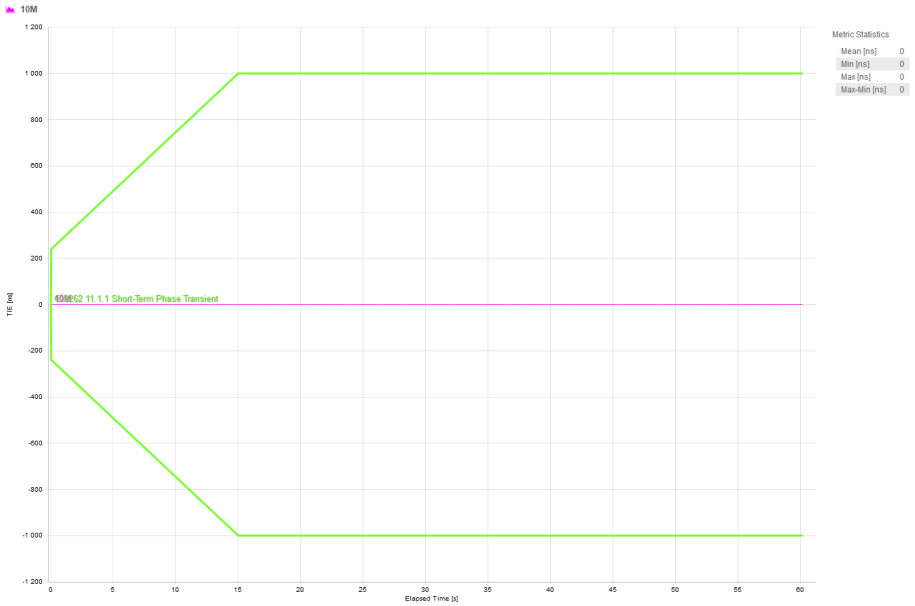

Figure 6-5. Phase Transient With Signal Interruptions Results

6.4 Phase Discontinuity G.8262 Option 1

Passing this test requires that switching between two input clocks of the same frequency but with different phases does not cause an output phase transient greater than what is outlined in Section 11.4.1 of the G.8262 specification. The setup for this test (shown in Figure 6-6) is as follows:

- There are two inputs that are 180 degrees out of phase going into the DUT
- The output is measured to ensure that the objective is met

The TIE data for phase discontinuity during reference switchover G.8262 EEC Option 1 (shown in Figure 6-7) indicates compliance to the standard.

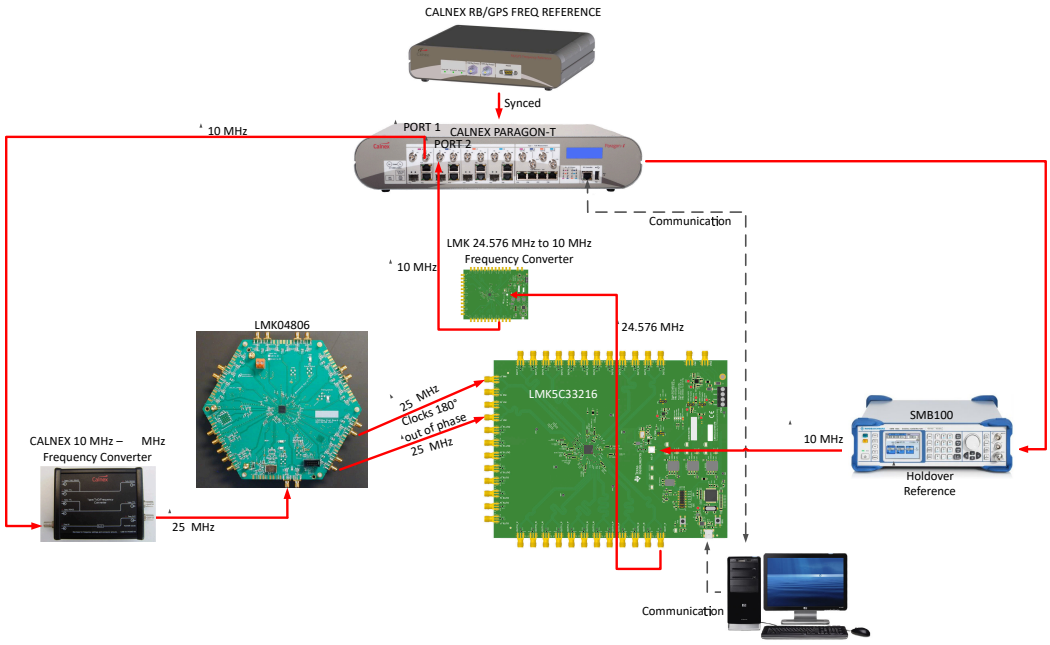

Figure 6-6. Test Setup for Phase Discontinuity

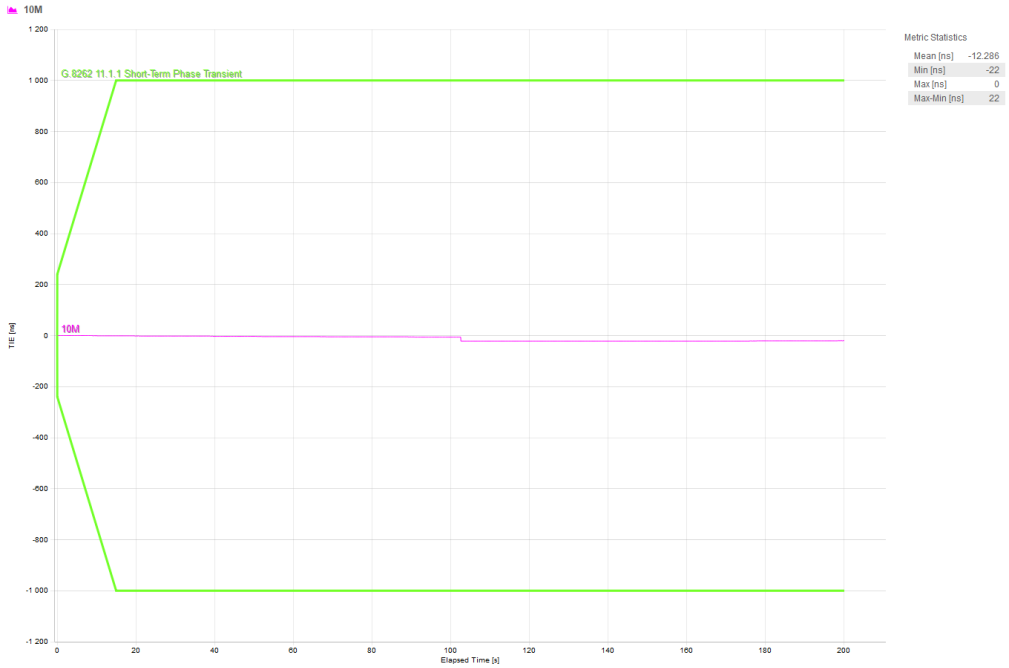

Figure 6-7. Phase Discontinuity Results

6.5 Phase Discontinuity G.8262 Option 2

For this test, the requirement is that switching between two input clocks of the same frequency but with different phase will not exceed the green MTIE mask shown in Figure 6-8 (Figure 14 and Table 15 in the G.8262 spec).

The LMK5C33216 met this requirement, as shown in Figure 6-8.

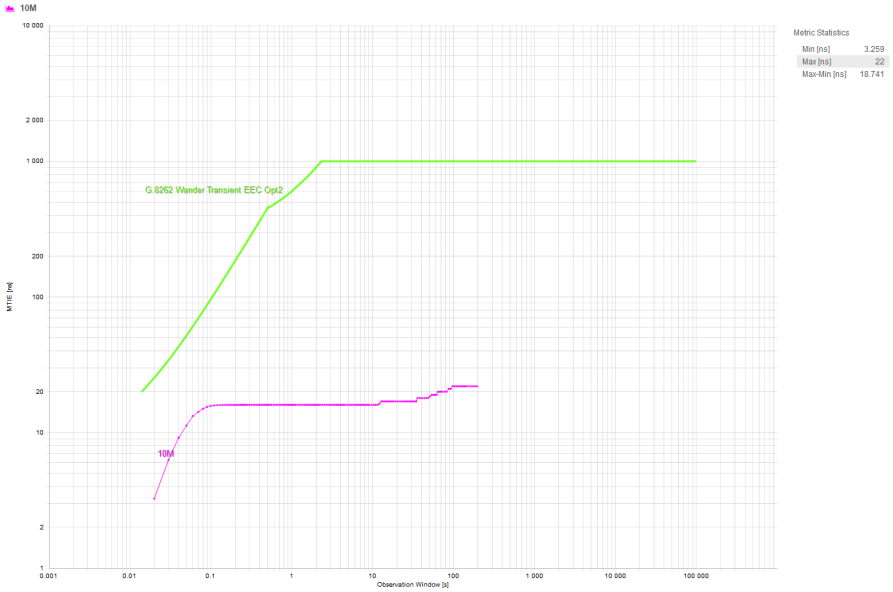

Figure 6-8. Phase Discontinuity Option 2 Results

7 Holdover

7.1 Holdover G.8262 Option 1

To meet this specification, a PLL in holdover must meet the requirements shown in figure 13 in the G.8262 specification. The procedure for this test is that the LMK5C33216 DUT will lock to IN0, which contains a valid input clock. Then the input is switched to IN1, which contains no valid input, thereby causing the device to enter holdover and remain in holdover for the remainder of the test. The LMK5C33216 device was set up in with a 10-Hz loop bandwidth and forced into holdover. The LMK5C33216 met this specification. The TIE plot shown in Figure 7-1 demonstrates compliance to the standard in green.

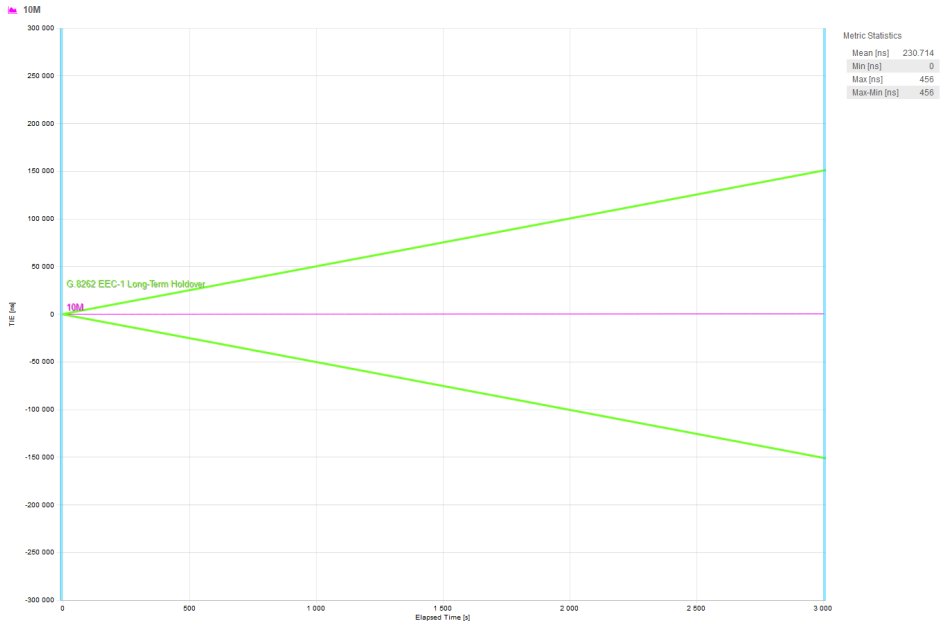

Figure 7-1. Holdover Option 1 Result

7.2 Holdover G.8262 Option 2

To meet this specification, a PLL in holdover must meet the requirements in Table 7-1 (Table 15 in the G.8262 specification). The procedure for this test is that the DUT obtains lock from IN0, which contains a valid input clock. Then the input is switched to IN1, which contains no valid input, thus entering holdover and remains in holdover for the remainder of the test. The LMK5C33216 met this specification. The TIE plot shown in Figure 7-2 demonstrates compliance to the standard in green.

Table 7-1. Transient Response Specifications During Holdover

	EEC Option 2
Applies For	S > **TBD** (6)
a_1 (ns/s)(1)	50
a_2 (ns/s)(2)	300
b (ns/s^2)(3)	4.63×10^{-4}
c (ns)(4)	1000
d (ns/s^2)(5)	4.63×10^{-4}

(1) a_1 represents an initial frequency offset under constant temperature conditions (±1 K)

(2) a_2 accounts for temperature variations after the clock went into holdover. If there are no temperature variations, the term $a_2 S$ should not contribute to the phase error.

(3) b represents the average frequency drift caused by aging. This value is derived from typical aging characteristics after 60 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

(4) The phase offset c takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.

(5) d represents the maximum temporary frequency drift rate at constant temperature allowed during holdover. However, it is not required that d and b be equal.

(6) TBD: To be defined.

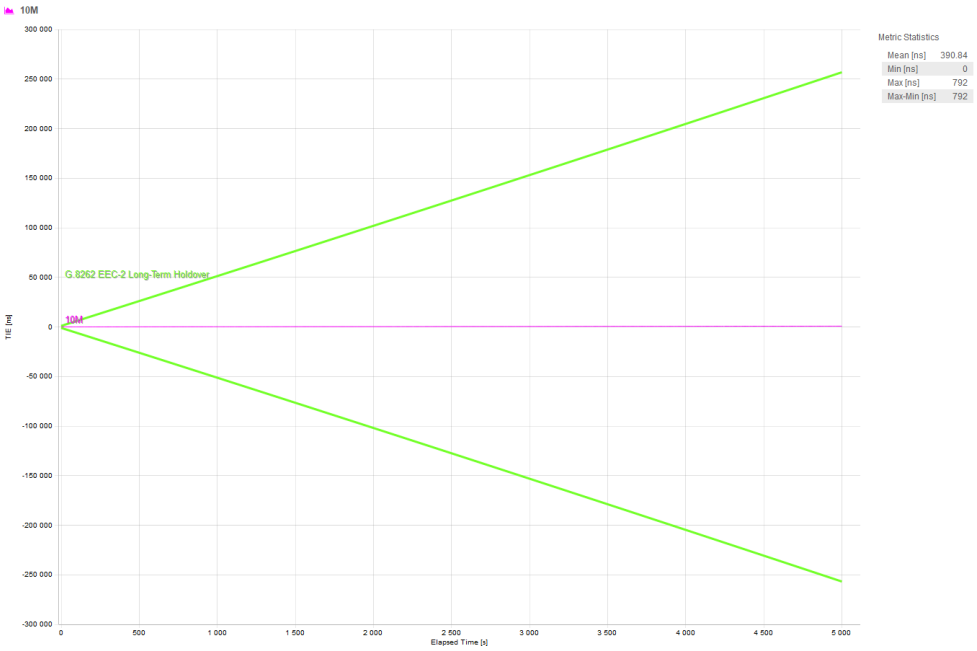

Figure 7-2. Holdover Option 2 Result

8 Free-Run Accuracy

8.1 Free-Run Accuracy G.8262 Option 1 and Option 2

To meet this requirement, the free-run frequency will never exceed ±4.6 ppm with reference to a traceable Stratum-1 reference. This includes initial power-up or wherever there is not sufficient holdover history accumulated.

With the LMK5C33216 reference removed, the device was locked to the holdover reference upon power on reset until holdover history was available. The holdover reference selected was within ±4.6 ppm. The output clock from LMK5C33216 followed the holdover reference.

9 Pull-In and Hold-In

9.1 Pull-In Range G.8262 Option 1 and Option 2

To meet this requirement, a PLL which is in free-run or holdover within its ±4.6 ppm frequency range (based on its TCXO/OCXO) must be able to pull-in to a reference that is within ±4.6 ppm frequency (traceable to Stratum-1). In other words, the PLL should be able to pull-in a minimum of ±9.2 ppm and no alarms should be asserted during this process. Hold-in range is defined as the largest offset between the reference frequency of a slave clock and a specified nominal frequency, within which the slave clock maintains lock as the frequency varies over the frequency range. The hold-in range for EEC-Option 2 should be ±4.6 ppm, whatever the internal oscillator frequency offset may be. The minimum pull-in range for Option 1 and Option 2 should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

The LMK5C33216 meets the specification for pull-in and hold-in range as shown in Table 9-1 and Table 9-2.

Table 9-1. Pull-In Results

REFERENCE TO DPLL	TCXO	OUTPUT	NOTES
25 MHz - 4.6 ppm	10 MHz + 4.6 ppm	10 MHz - 4.6 ppm	Lock from POR with FASTLOCK Enabled
25 MHz - 4.6 ppm	10 MHz - 4.6 ppm	10 MHz - 4.6 ppm	
25 MHz + 4.6 ppm	10 MHz + 4.6 ppm	10 MHz + 4.6 ppm	
25 MHz + 4.6 ppm	10 MHz - 4.6 ppm	10 MHz + 4.6 ppm	

Table 9-2. Hold-In Results

REFERENCE TO DPLL	TCXO	OUTPUT	NOTES
25 MHz - 4.6 ppm	10 MHz ± 4.6 ppm	10 MHz - 4.6 ppm	'±' here refers to reference frequency (TCXO or Reference to DPLL) being swept from '-' to '+' and vice-versa
25 MHz + 4.6 ppm	10 MHz ± 4.6 ppm	10 MHz + 4.6 ppm	
25 MHz ± 4.6 ppm	10 MHz - 4.6 ppm	10 MHz ± 4.6 ppm	
25 MHz ± 4.6 ppm	10 MHz + 4.6 ppm	10 MHz ± 4.6 ppm	

10 Conclusion

The LMK5C33216 Network Synchronizer device, along with a compliant TCXO or OCXO, meets or exceeds the requirement set in ITU-T G.8262/Y.1362 (07/2010) and Amendment 2 (10/2012).

Notable features of this high performance device includes:

- Hitless Switching with minimal phase transients (< 100 ps)
- Ultra High-Performance VCO allows use of a low-cost holdover reference without sacrificing performance
- High-Performance DPLL Channel with Programmable loop bandwidth for jitter and wander filtering suitable for EEC Option 1 and EEC Option 2
- Reference Priority Selection, Gapped Clock and Runt Pulse Detectors, Automatic/Manual Switchover, Holdover, and Tuning Word History

11 References

For reference, see the following:

- ITU-T G.8262 Standard

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