

Jitter and Phase Noise Measurement Techniques for BAW Oscillators



Connor Lewis

Clocks and Timing Solutions

ABSTRACT

Jitter and phase noise are some of the key performance parameters of oscillators and other clocking products. With some TI oscillators offering RMS jitter near 100 fs, advanced measurement techniques and equipment can be required to accurately measure device performance. Understanding the correct test equipment and hardware setup for different clocking formats is needed to have a clear idea of the true system performance of clocking components.

Table of Contents

1 Introduction	2
1.1 Why use a Phase Noise Analyzer?.....	2
2 Understanding Phase Noise Plots	2
3 Phase Noise Analyzer Measurement Settings	3
3.1 Start or Stop Frequency.....	3
3.2 Averaging and Correlation.....	3
3.3 Persistence.....	3
3.4 Spurious View Modes.....	3
3.5 Other Settings.....	3
4 Hardware Setup for Different Clocking Formats	4
4.1 LVCMOS.....	4
4.2 LVDS.....	4
4.3 LVPECL/HCSL.....	4
4.4 Balun Recommendations.....	5
5 Typical Measurements with Different Termination Schemes	6
5.1 LVCMOS.....	6
5.2 LVDS.....	7
5.3 LVPECL.....	7
5.4 HCSL.....	8
6 Summary	8
7 References	8

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

1.1 Why use a Phase Noise Analyzer?

Measuring time-domain jitter characteristics, such as total jitter (TJ) and cycle-to-cycle jitter, can be done using a high speed oscilloscope as described in the [How to Measure Total Jitter \(TJ\)](#) application note. However, for many applications time-domain jitter measurements are not as relevant compared to their frequency-domain counterparts such as integrated jitter or phase noise. For example, in wired networking applications the RMS jitter integrated from 12kHz to 20MHz is commonly used to make sure that the bit-error rate (BER) of an Ethernet PHY meets system-level requirements. As another example, medical imaging equipment can have strict phase noise requirements at a specific offset close to the carrier frequency (such as a 1kHz offset). For these types of applications, use a phase noise analyzer (PNA) due to the low noise floor and advanced jitter calculation tools. Oscilloscopes, spectrum analyzers, and other equipment are not recommended to measure phase noise for high performance clocks due to their high noise floor. Some PNAs that TI uses for device characterization include the Agilent E5052, R&S FSWP, and Microchip 53100A.

2 Understanding Phase Noise Plots

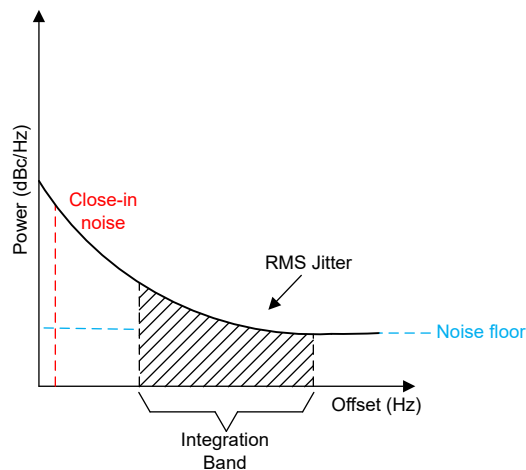


Figure 2-1. Phase Noise Curve

A phase noise plot shows the noise of a clock source in the frequency-domain.

The Y-axis shows the power of noise in units of dBc/Hz - Decibels relative to the carrier signal with a bandwidth of 1Hz.

The X-axis is the offset from the carrier frequency in Hz.

Integrating a region of the phase noise curve can give the RMS jitter in units of seconds according to the following equation:

$$\text{RMS Jitter} = \frac{2 \times \sqrt{10 \frac{N}{10}}}{2 \times \pi \times f} \quad (1)$$

where N is the integral of the phase noise curve over a specified integration band (usually 12kHz - 20MHz) and f is the carrier frequency in Hz.

3 Phase Noise Analyzer Measurement Settings

3.1 Start or Stop Frequency

The start and stop frequency changes the range of frequency offsets from the carrier where measurements are collected. Increasing the start or stop range (for example, reducing the start frequency from 1kHz to 1Hz) provides more information about the phase noise of the measured signal at the expense of longer measurement times. For applications where close-in phase noise measurements are not needed, the start offset can be increased to greatly improve measurement speed.

Note that the maximum stop frequency the equipment can measure can be limited by the carrier frequency. For example, the Agilent E5052B supports a stop frequency up to 40MHz for carrier signals in the 99MHz - 1.5GHz band, but the Agilent E5052B limits the maximum stop frequency to 20MHz for carriers in the 39MHz - 101MHz band.

3.2 Averaging and Correlation

To reduce uncertainty from a single measurement point, averaging can be used. Averaging over several measurements smooths out the phase noise trace to give a more realistic phase noise measurement at any given frequency offset. When averaging is enabled, cross correlation can also be adjusted. Correlation measures the input signal against different reference sources. Since the noise profiles of the different reference sources are correlated, the reference noise is subtracted out and the resulting measurement is a better representation of the signal rather than noise from the measurement equipment. Increasing the correlation is especially important when measuring the noise floor of a very clean clock source.

3.3 Persistence

Persistence memory mode can be useful to track inconsistent, spurious behavior. For example, when stress-testing a clock source over extreme temperature, voltage, radiation, vibration and shock testing, and so on. It can be useful to take plots with persistence mode enabled to observe any transient behavior.

3.4 Spurious View Modes

Some PNAs can change how spurs are represented in phase noise plots. *Power* or *Spurs Enabled* mode can show the full power of spurs without any filtering. *Normalized* mode will divide down the spur power by the frequency offset, meaning higher frequency spurs will appear proportionally smaller compared to spurs that are close to the carrier frequency. *Omit* or *Spurs Off* mode will remove spurs entirely from the phase noise plot. The following images show a comparison between spurious view modes for a LMK6P 156.25MHz variant.

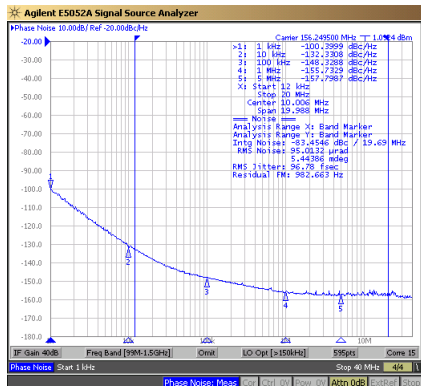


Figure 3-1. Omit Spur View

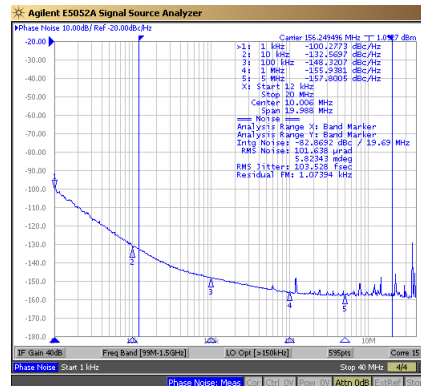


Figure 3-2. Normalized Spur view

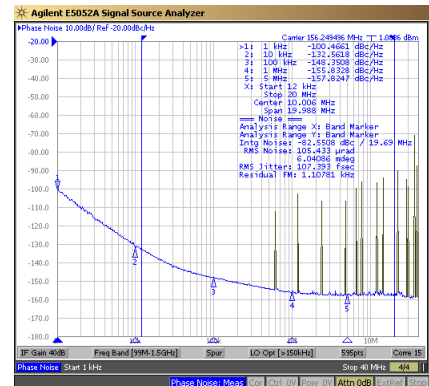


Figure 3-3. Power Spur View

3.5 Other Settings

Other PNA settings can impact phase noise measurements such as IF gain, input attenuation, and so on. The ideal choices for these settings can depend on the carrier frequency and amplitude. See the PNA's operating manual for more details on how to adjust these settings to get the most accurate phase noise and jitter measurements.

4 Hardware Setup for Different Clocking Formats

Always AC-couple the inputs of the PNA to prevent damaging the measurement equipment. If AC-coupling capacitors are not placed on the output of the clock source, a DC block can be used directly at the input of the PNA. Note that PNAs usually have an internal 50Ω termination to match the impedance of most coaxial cables. These are both important considerations when deciding how to terminate the clock source to maximize power and reduce signal reflections.

The following sections detail different measurement setups for TI's [LMK6x](#) family of oscillators.

4.1 LVCMOS

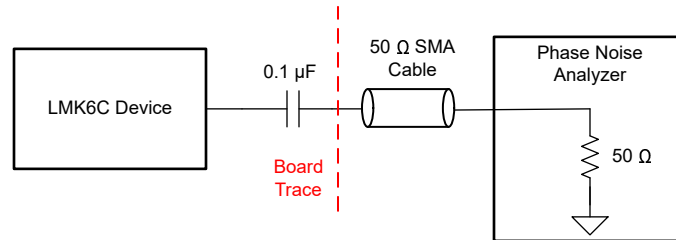


Figure 4-1. Recommended LVCMOS Termination Scheme for Phase Noise Measurements

4.2 LVDS

AC-couple LVDS clocks before the balun to avoid significant attenuation of the clock signal. If a balun is unavailable, the measurements can be taken single-ended. Note that for single-ended measurements, it is important to correctly terminate the unused end of the output as shown in [Figure 4-3](#) to make sure proper loading on the output driver. When taking single-ended measurements without a balun, there can also be some degradation in phase noise performance due to a decrease in signal power and lack of common-mode noise rejection.

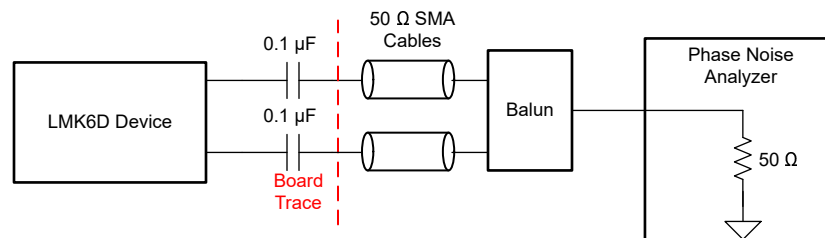


Figure 4-2. Recommended LVDS Termination Scheme for Phase Noise Measurements

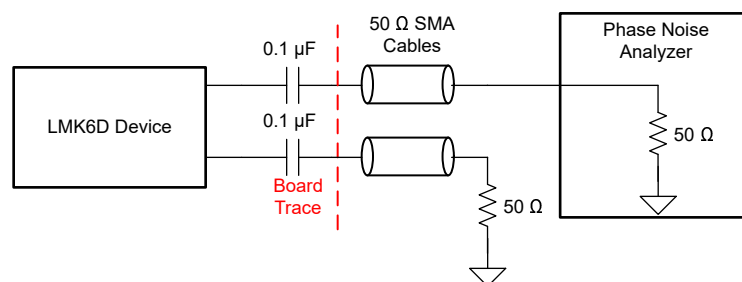


Figure 4-3. Alternative LVDS Termination Scheme for Phase Noise Measurements (Single-Ended)

4.3 LVPECL/HCSL

If a balun is unavailable, the measurements can be taken single-ended. Note that for single-ended measurements, it is important to correctly terminate the unused end of the output as shown in [Figure 4-5](#) to make sure proper loading on the output driver. When taking single-ended measurements without a balun, there

can also be some degradation in phase noise performance due to a decrease in signal power and lack of common-mode noise rejection.

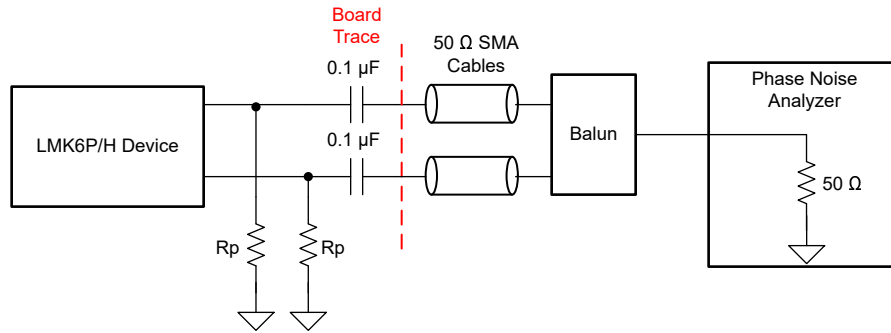


Figure 4-4. Recommended LVPECL/HCSL Termination Scheme for Phase Noise Measurements

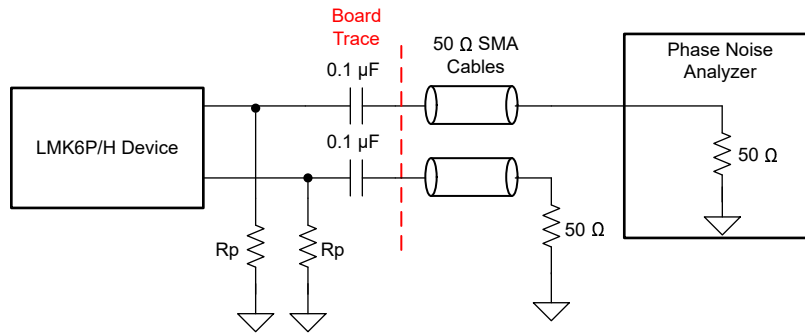


Figure 4-5. Alternative LVPECL/HCSL Termination Scheme for Phase Noise Measurements (Single-Ended)

Table 4-1. Source Termination Resistor Values for LMK6P

Supply Voltage (V)	Rp (Ω)
3.3	207.5
2.5	112.5
1.8	83.3

Table 4-2. Source Termination Resistor Values for LMK6H

Supply Voltage (V)	Rp (Ω)
3.3	50
2.5	50
1.8	50

4.4 Balun Recommendations

To maintain signal integrity, it is recommended to use a balun with a Voltage Standing Wave Ratio (VSWR) less than 2 and a phase imbalance of less than 8°.

A hybrid coupler can also be used to convert differential signals to single-ended and is commonly used for measurements of TI clocking devices. Hybrid couplers typically have less insertion loss compared to baluns which results in better noise floor performance. Some hybrid couplers that TI uses include the MACOM H-183-4, Mini-Circuits ZFSCJ-2-1+, and Mini-Circuits ZFSCJ-2-4+.

5 Typical Measurements with Different Termination Schemes

This section includes typical measurements for LMK6x devices using the different termination schemes as described in Section 4. In these measurements the PNA had a correlation setting of 15, averaging count of 4, and a normalized spur view. Note that the recommended termination schemes for each output format result in better jitter measurements compared to the alternative setups.

5.1 LVCMOS

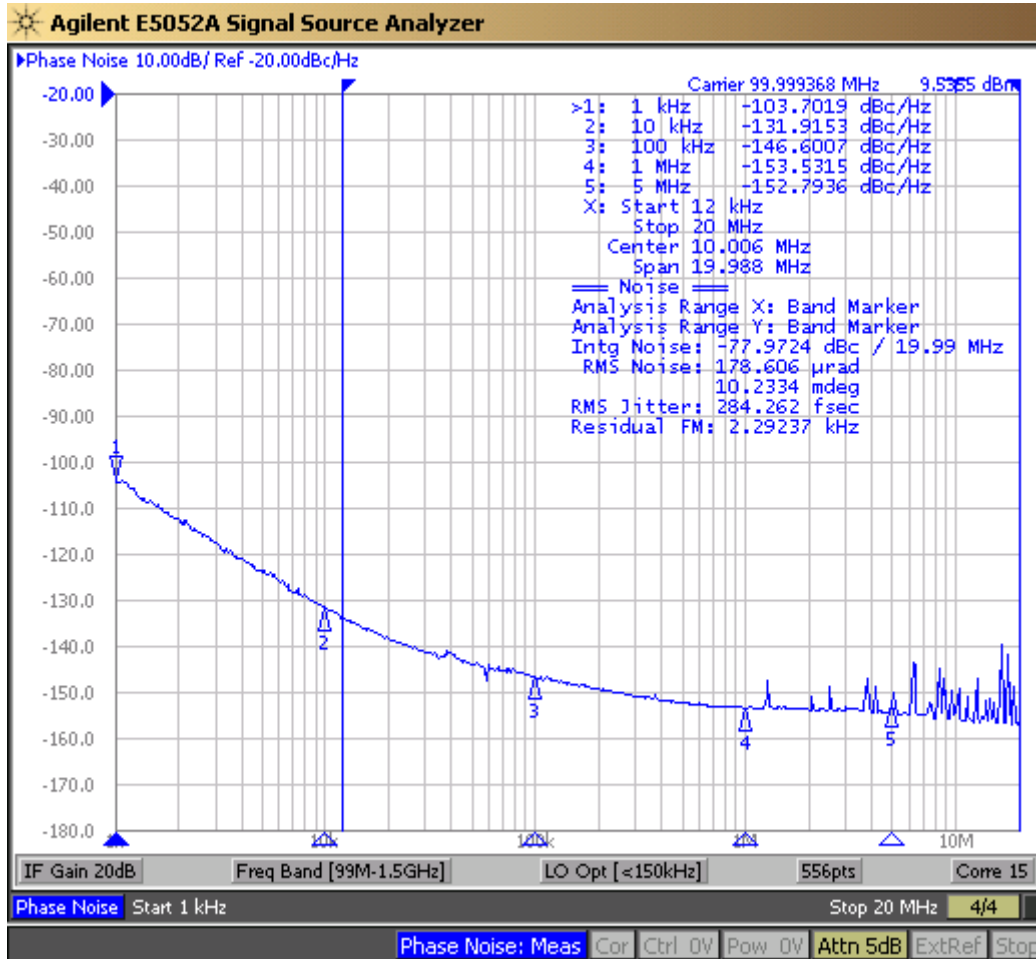


Figure 5-1. Phase Noise Plot of LMK6C 100MHz Variant With Recommended Termination

5.2 LVDS

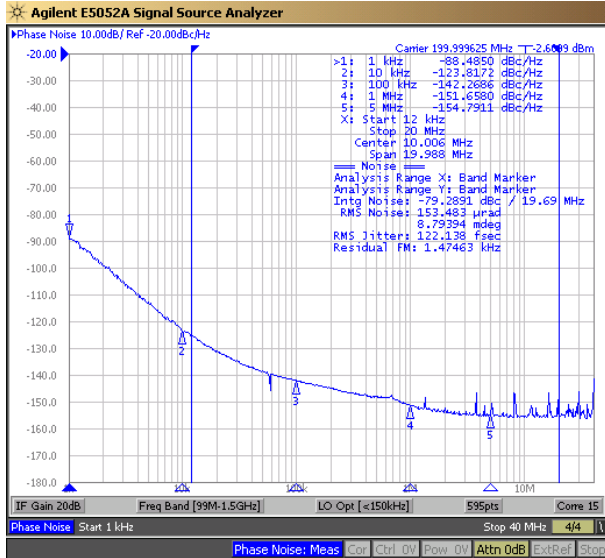


Figure 5-2. Phase Noise Plot of LMK6D 200MHz Variant With Recommended Termination

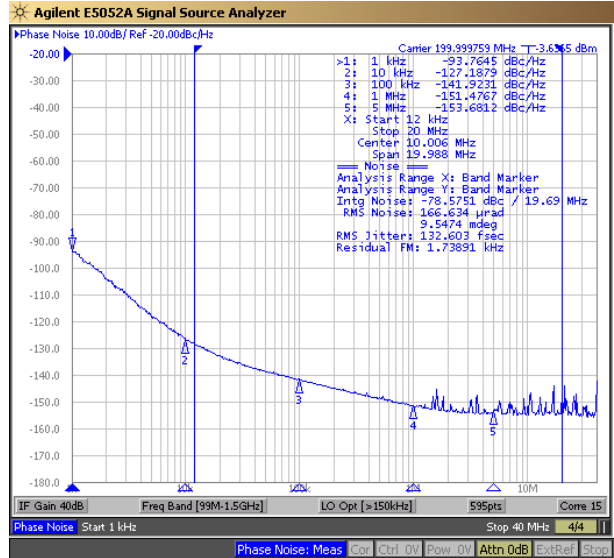


Figure 5-3. Phase Noise Plot of LMK6D 200MHz Variant With Single-Ended Termination

5.3 LVPECL

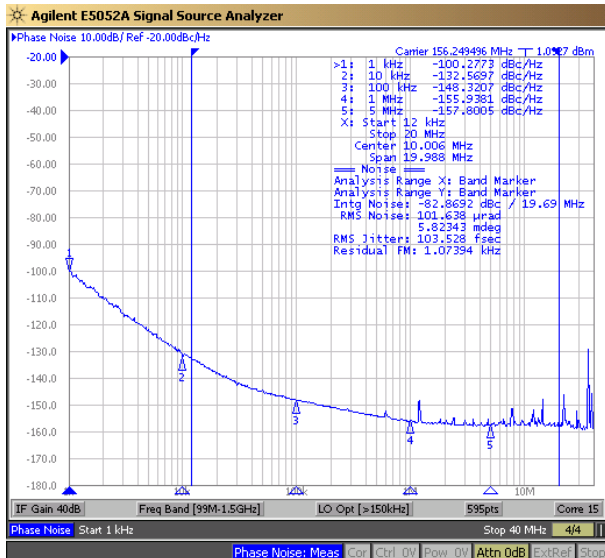


Figure 5-4. Phase Noise Plot of LMK6P 156.25MHz Variant With Recommended Termination

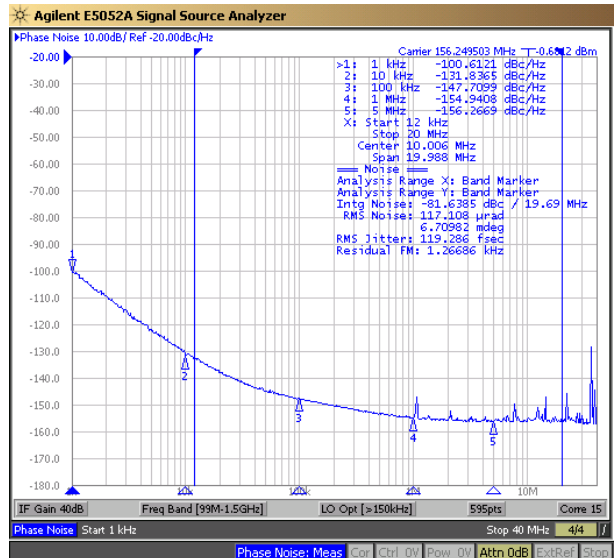


Figure 5-5. Phase Noise Plot of LMK6P 156.25MHz Variant With Single-Ended Termination

5.4 HCSSL

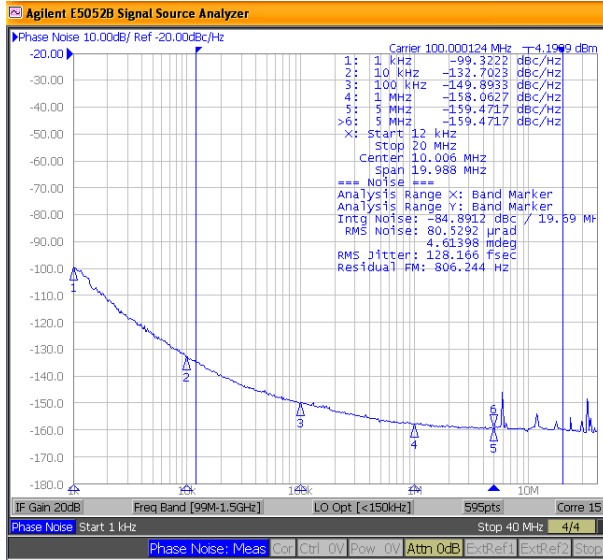


Figure 5-6. Phase Noise Plot of LMK6H 100MHz Variant With Recommended Termination

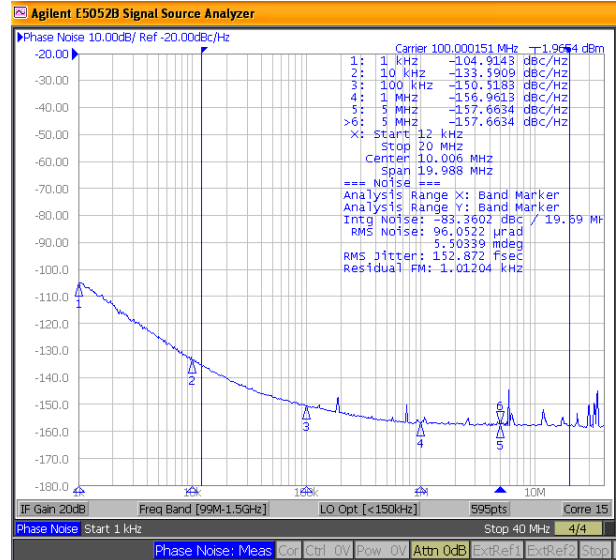


Figure 5-7. Phase Noise Plot of LMK6H 100MHz Variant With Single-Ended Termination

6 Summary

In summary, it is important to consider the signal terminations for each type of output format to obtain accurate measurements of high-performance clock sources such as the *LMK6x Low Jitter, High-Performance BAW Oscillator*. To measure the true phase noise performance of such devices, use a properly configured PNA with a low noise floor. The techniques described in this application note maximize signal power and reduce system-level noise and phase noise errors from measurement equipment.

7 References

- Texas Instruments, *LMK6x Low Jitter, High-Performance BAW Oscillator*, data sheet.
- Texas Instruments, *How to Measure Total Jitter (TJ)*, application note.
- Texas Instruments, *Time-Domain Jitter Measurement Considerations for Low-Noise Oscillators*, application note.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated