Application Note

DP83TC811, DP83TC812, DP83TC814, DP83TG720 Hardware Rollover Document

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ABSTRACT

Texas Instruments 100BASE-T1 and 1000BASE-T1 Automotive Ethernet PHYs have been designed to be implemented on a single PCB design (DP83TC811, DP83TC812, and DP83TC814 are 100BASE-T1 PHYs; DP83TG720 is a 1000BASE-T1 PHY.) This application note is a reference guide to help design a single system that can support all four devices with minor component changes.

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1 Introduction

Texas Instruments Automotive Ethernet PHY portfolio consists of 100BASE-T1 (DP83TC811, DP83TC812, DP83TC814) and 1000BASE-T1 (DP83TG720) devices.

Automotive system qualification cycles are time-consuming and any notable change can lead to significant increases in development costs. Therefore, to reduce the complexity of automotive Ethernet system design, Texas Instruments designed their Ethernet PHYs to be implemented on a single system. This avoids a complete system redesign when changing devices, based on the application requirement.

To achieve this, all four devices (DP83TC811, DP83TC812, DP83TC814, and DP83TC720) have the same package:

- 36-QFN, 6mm x 6mm (wettable flanks)

Furthermore, MAC interface selection can also affect PCB design:

- DP83TC811, DP83TC812, DP83TC814 support MII, RMII, RGMII, and SGMII MAC interfaces.
  - This application report assumes that DP83TC811/812/814 will be operated in RGMII or SGMII mode.
- DP83TG720 supports RGMII and SGMII MAC interfaces.
  - MII and RMII standards were defined only for 10 and 100Mbps only, so DP83TG720 does not support these options.

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2 Device Comparison

2.1 Pin Map Comparison

2.1.1 DP83TC811S

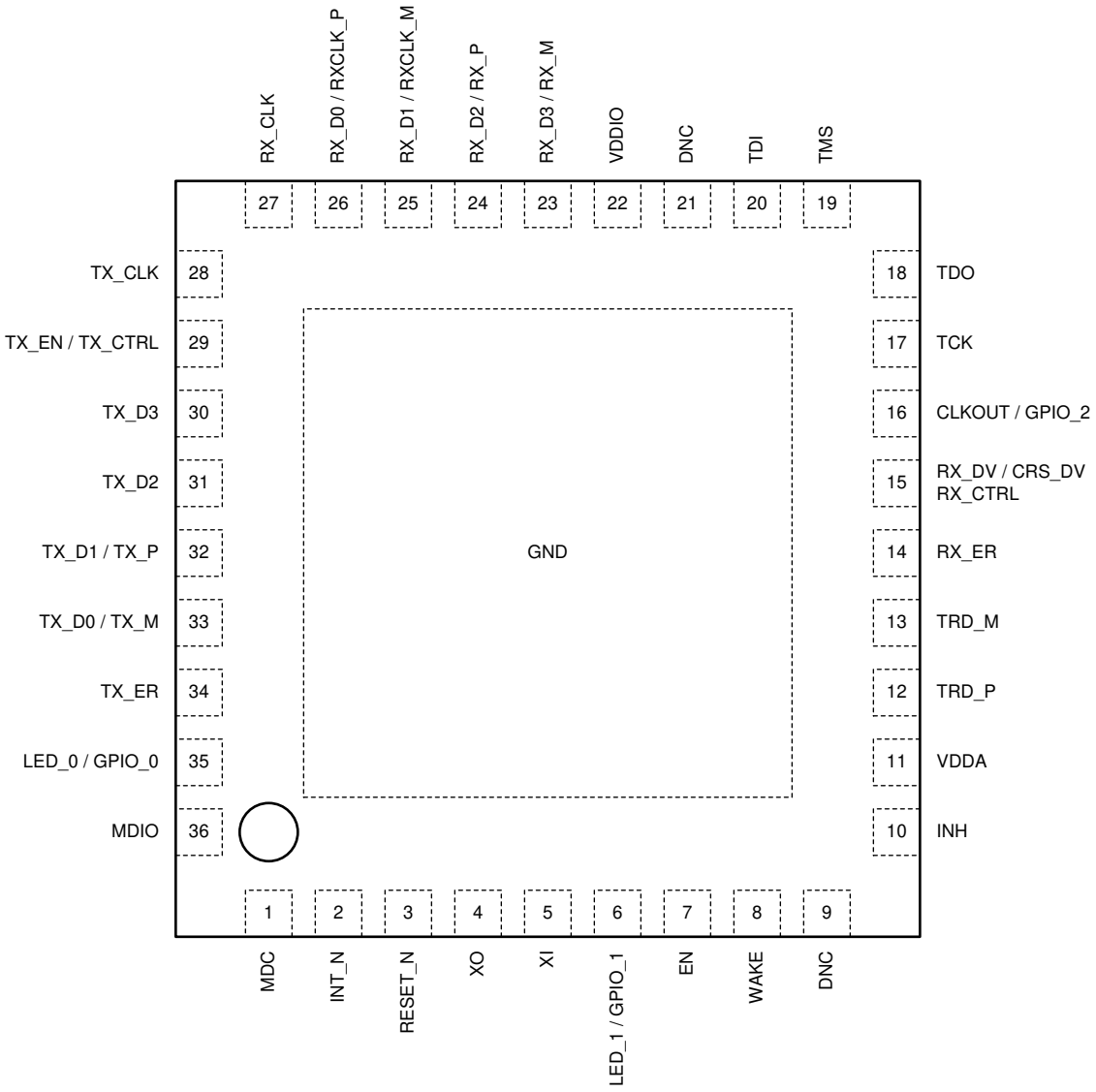

Figure 2-1. DP83TC811S RND Package 36-QFN Pin Map

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2.1.2 DP83TC811R

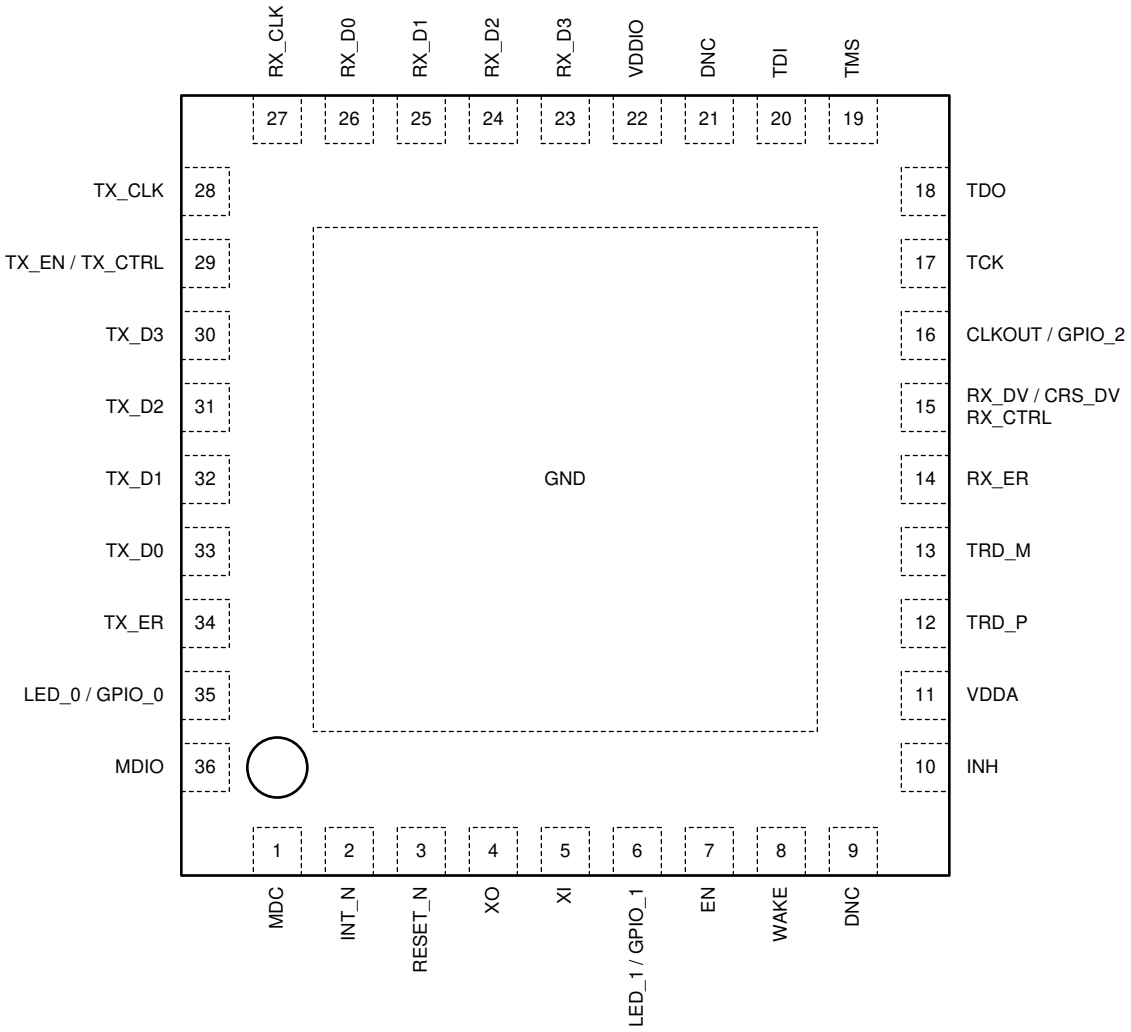

Figure 2-2. DP83TC811R RND Package 36-QFN Pin Map

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2.1.3 DP83TC812S

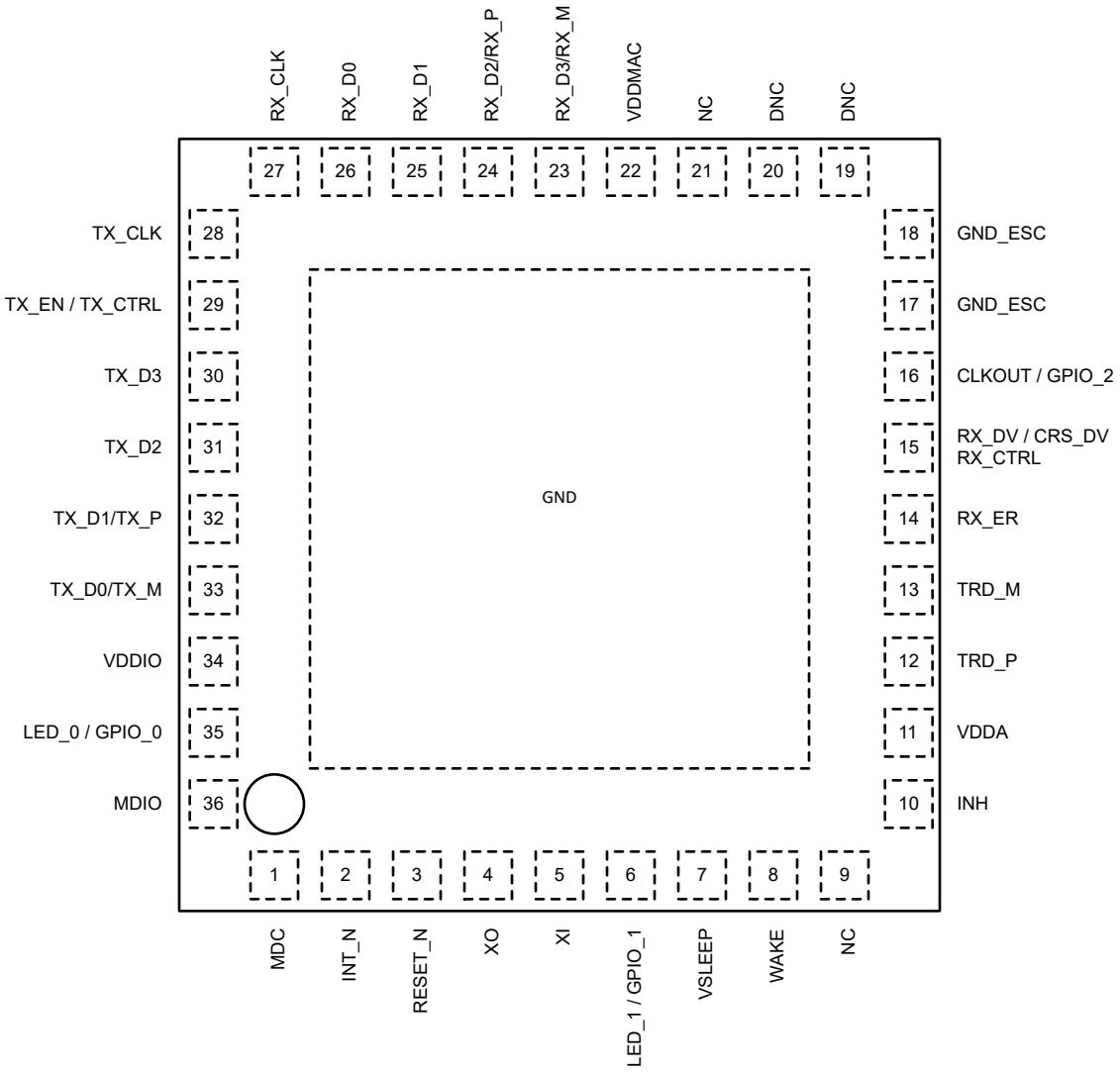

Figure 2-3. DP83TC812S RHA Package 36-QFN Pin Map

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2.1.4 DP83TC812R

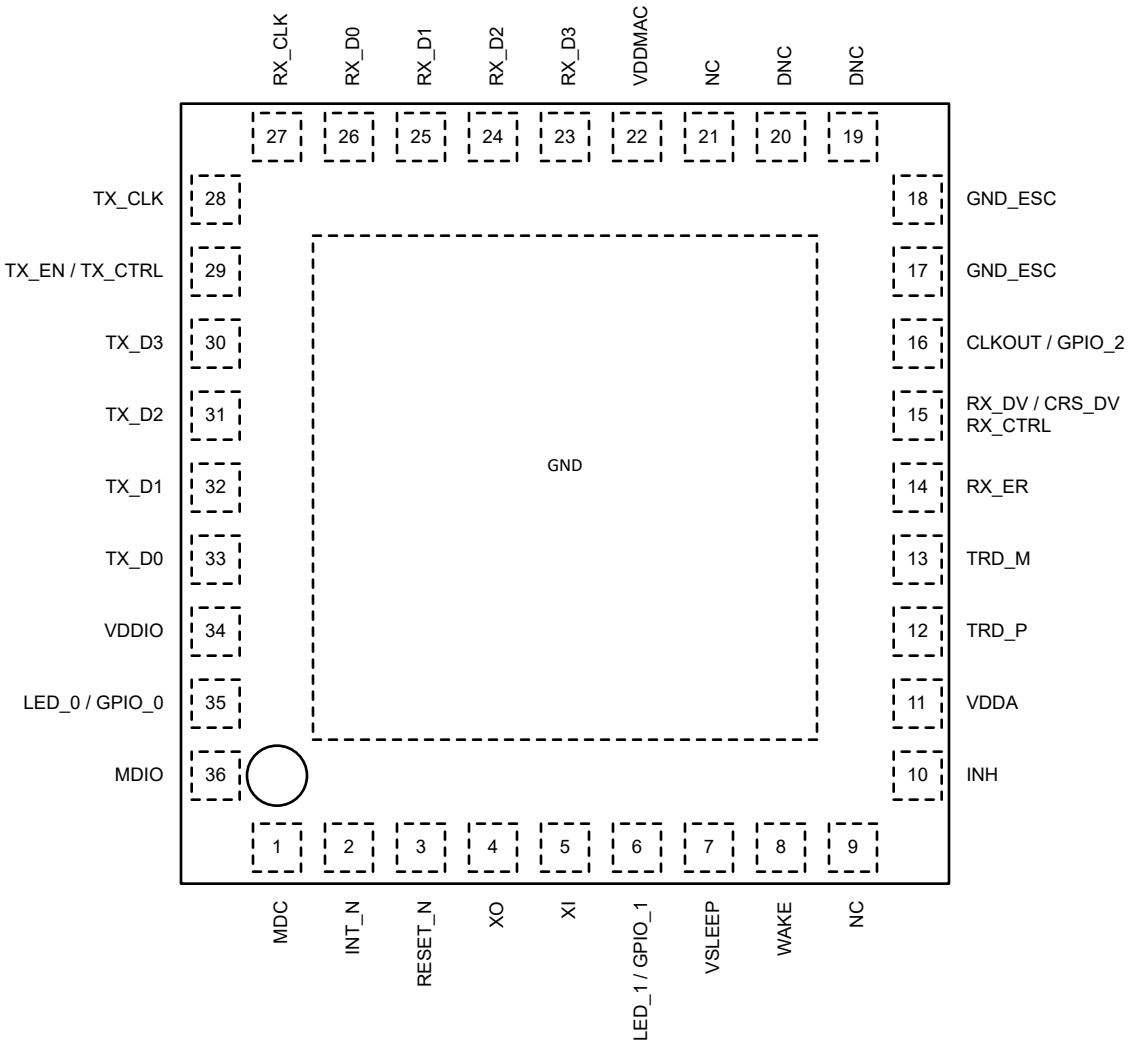

Figure 2-4. DP83TC812R RHA Package 36-QFN Pin Map

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2.1.5 DP83TC814S

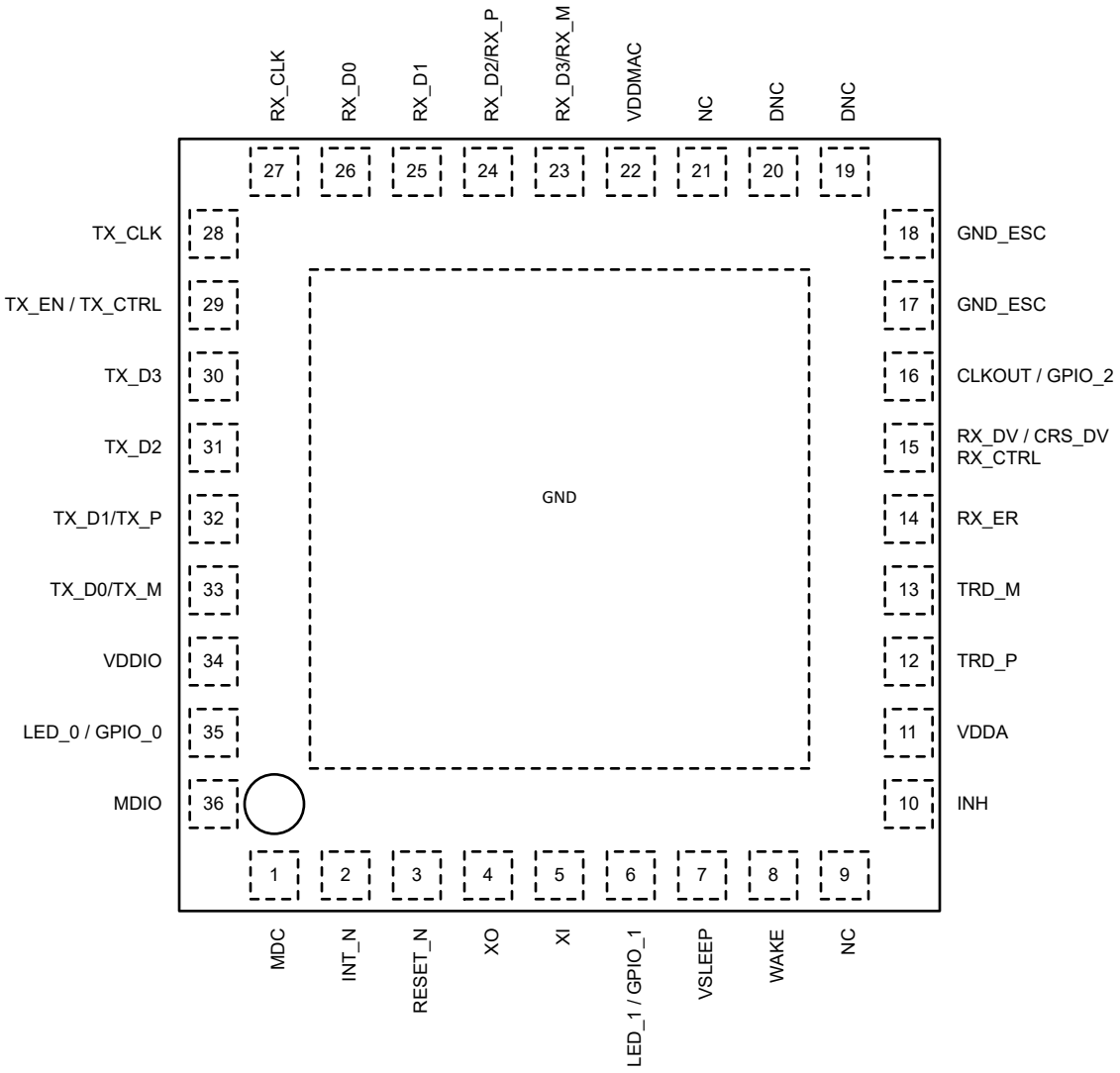

Figure 2-5. DP83TC814S RHA Package 36-QFN Pin Map

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2.1.6 DP83TC814R

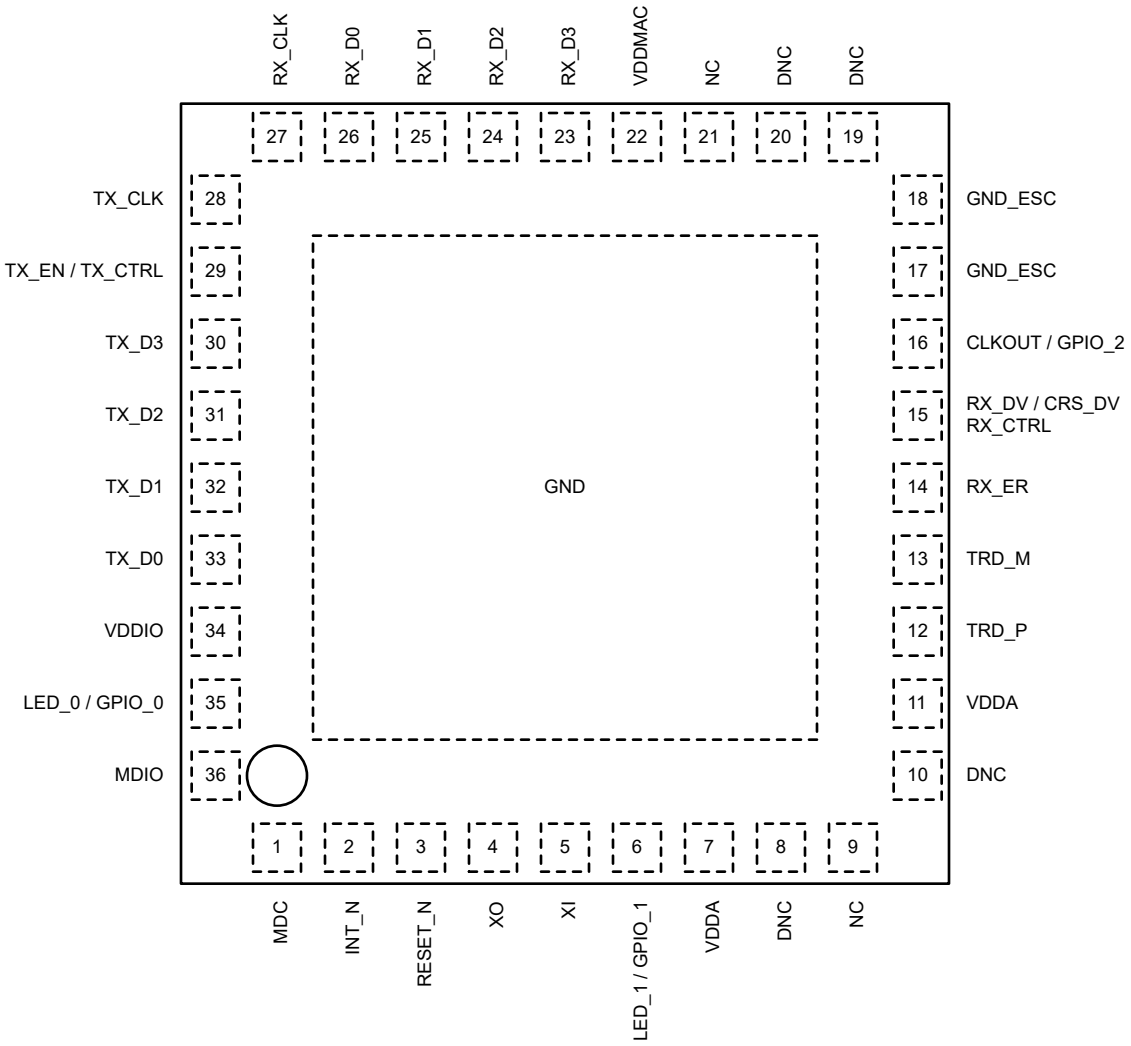

Figure 2-6. DP83TC814R RHA Package 36-QFN Pin Map

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2.1.7 DP83TG720S

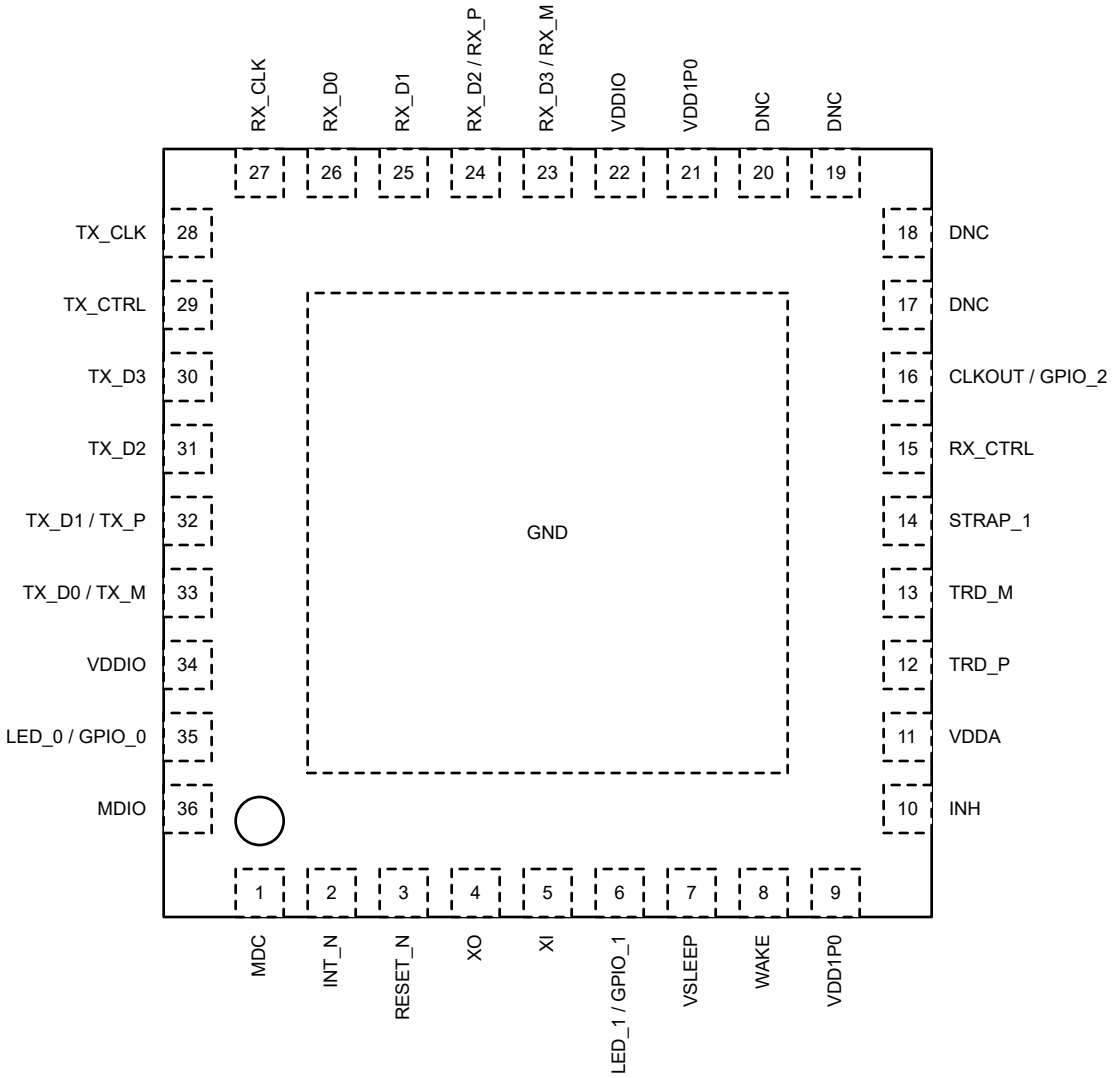

Figure 2-7. DP83TG720S RHA Package 36-QFN Pin Map

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2.1.8 DP83TG720R

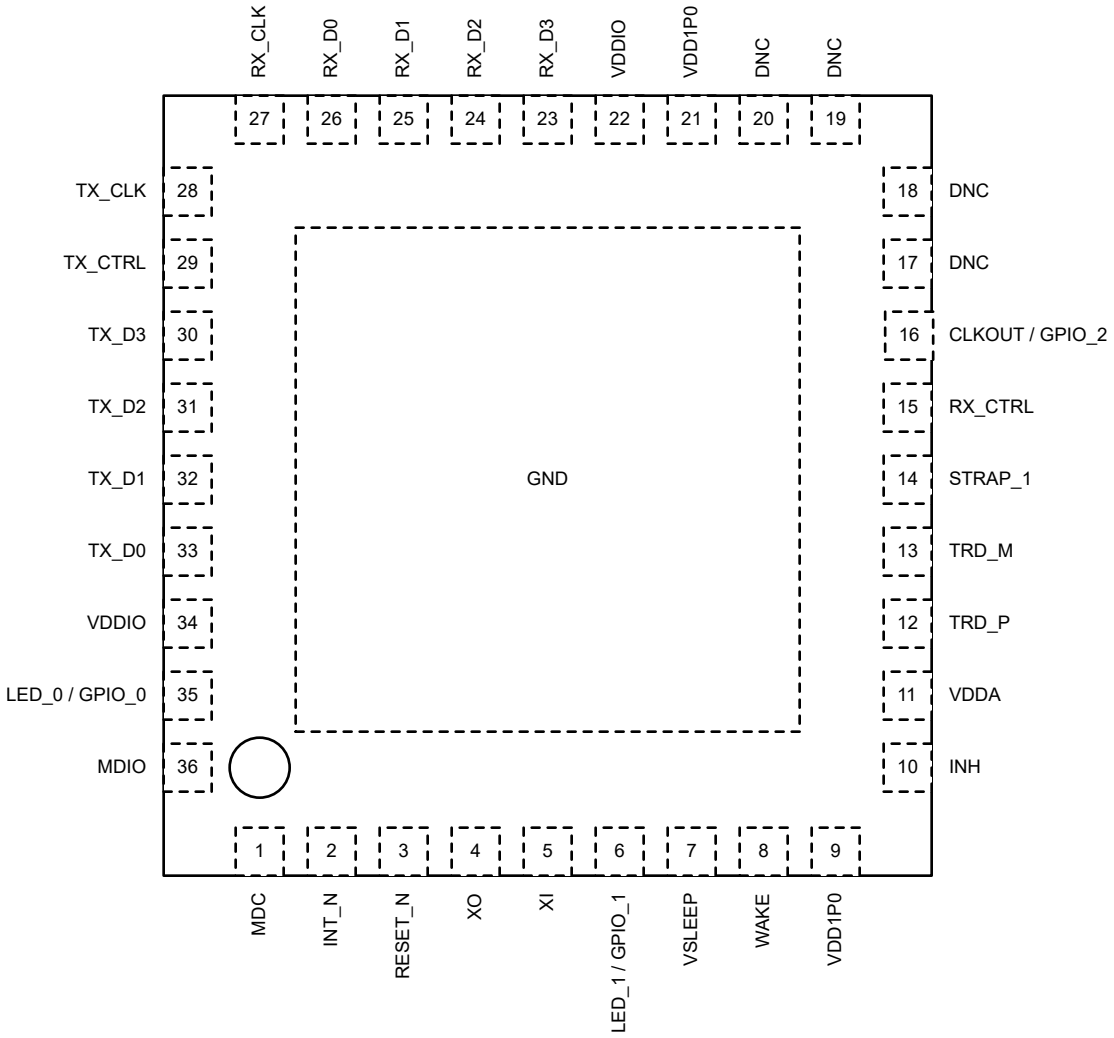

Figure 2-8. DP83TG720R RHA Package 36-QFN Pin Map

2.2 Feature Comparison

Table 2-1 shows feature comparison between DP83TC811, DP83TC812, DP83TC814, and DP83TG720.

Table 2-1. Device Comparison Table

DEVICE	SPEED	MAC INTERFACE	TC-10
DP83TC811	100BASE-T1	MII, RMII, RGMII, SGMII	No
DP83TC812	100BASE-T1	MII, RMII, RGMII, SGMII	Yes
DP83TC814	100BASE-T1	MII, RMII, RGMII, SGMII	No
DP83TG720	1000BASE-T1	RGMII, SGMII	Yes(1)

(1) DP83TG720 supports a proprietary sleep mode with wake-up on energy detect.

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2.3 Pin Comparison Table

Table 2-2 shows pin comparison between DP83TC811, DP83TC812, DP83TC814, and DP83TG720. All four PHYs have majority of the pins in the same location with a few minor differences.

Table 2-2. Pin Comparison Table

PIN NO.	DP83TC811	DP83TC812	DP83TC814	DP83TG720	NOTES
1	MDC	MDC	MDC	MDC	
2	INT_N	INT_N	INT_N	INT_N	
3	RESET_N	RESET_N	RESET_N	RESET_N	
4	XO	XO	XO	XO	
5	XI	XI	XI	XI	
6	LED_1	LED_1	LED_1	LED_1	
7	**EN**	**VSLEEP**	**VDDA**	**VSLEEP**	**Pin 7 changes from input pin on DP83TC811 to supply pin on DP83TC812, DP83TC814, and DP83TG720**
8	**WAKE**	**WAKE**	**DNC**	**WAKE**	**DP83TC814 does not have low power sleep mode. Wake functionality has been removed.**
9	**DNC**	**NC**	**NC**	**VDD1P0**	**DP83TG720 has an external 1.0 V supply**
10	**INH**	**INH**	**DNC**	**INH**	**DP83TC814 does not have Low Power Sleep Mode. Wake functionality has been removed.**
11	VDDA	VDDA	VDDA	VDDA	
12	TRD_P	TRD_P	TRD_P	TRD_P	
13	TRD_M	TRD_M	TRD_M	TRD_M	
14	RX_ER	RX_ER	RX_ER	STRP1	
15	RX_DV/CRS_DV/ RX_CTRL	RX_DV/CRS_DV/ RX_CTRL	RX_DV/CRS_DV/ RX_CTRL	RX_CTRL	
16	CLKOUT	CLKOUT	CLKOUT	CLKOUT	
17	**TCK**	**GND_ESC**	**GND_ESC**	**DNC**	**All devices other than DP83TC811 do not support JTAG functionality and hence corresponding pins have been removed**
18	**TDO**	**GND_ESC**	**GND_ESC**	**DNC**	
19	**TMS**	**DNC**	**DNC**	**DNC**	
20	**TCK**	**DNC**	**DNC**	**DNC**	
21	**DNC**	**NC**	**NC**	**VDD1P0**	**Pin 21 is a supply pin for DP83TG720**

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Table 2-2. Pin Comparison Table (continued)

PIN NO.	DP83TC811	DP83TC812	DP83TC814	DP83TG720	NOTES
22	VDDIO	VDDMAC	VDDMAC	VDDIO	
23	RX_D3/RX_M	RX_D3/RX_M	RX_D3/RX_M	RX_D3/RX_M	
24	RX_D2/RX_P	RX_D2/RX_P	RX_D2/RX_P	RX_D2/RX_P	
25	RX_D1	RX_D1	RX_D1	RX_D1	
26	RX_D0	RX_D0	RX_D0	RX_D0	
27	RX_CLK	RX_CLK	RX_CLK	RX_CLK	
28	TXCLK	TXCLK	TXCLK	TXCLK	
29	TX_EN	TX_EN	TX_EN	TX_CTRL	
30	TX_D3	TX_D3	TX_D3	TX_D3	
31	TX_D2	TX_D2	TX_D2	TX_D2	
32	TX_D1/TX_P	TX_D1/TX_P	TX_D1/TX_P	TX_D1/TX_P	
33	TX_D0/TX_M	TX_D0/TX_M	TX_D0/TX_M	TX_D0/TX_M	
34	**TX_ER**	**VDDIO**	**VDDIO**	**VDDIO**	**Pin 34 is a supply pin for all devices other than DP83TC811**
35	LED_0	LED_0	LED_0	LED_0	
36	MDIO	MDIO	MDIO	MDIO	

Table Legend:

- DNC (Do Not Connect): This pin should be left unconnected on the PCB.
- NC (No Connect): This pin does not have any internal connection to the device. Any component connected to this pin will not affect device performance.
- GND_ESC (Ground Escape): Optional ground escape pins for simplifying layout. The can be connected directly to ground or left unconnected.

2.3.1 Strap Comparison

In order to maintain pin compatibility, the features associated with each strap pins are same for all four devices. There are differences in their implementation and strap resistor selection. DP83TC811 uses 4 level strap on all pins. DP83TC812/814, and DP83TG720 use 3 level straps for PHY Address and 2 level straps for all other functions.

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2.3.1.1 PHY Address Straps

Table 2-3 shows the PHY address strap comparison between DP83TC811, DP83TC812, DP83TC814, and DP83TG720.

DP83TC811 can support 16 PHY addresses from 0x00 to 0x0F. DP83TC812, DP83TC814, and DP83TG720 can support 9 PHY addresses: 0x00, 0x04, 0x05, 0x08, 0x0A, 0x0C, 0x0D, 0x0E, 0x0F. By provisioning for a pull up and pull down resistor on pin 14 and 15 of the PHY, all four devices can be supported by simply changing the resistor combination.

Table 2-3. PHY Address Strap Comparison Table

PIN NO.	PIN NAME	DP83TC811			DP83TC812, DP83TC814, DP83TG720		
		STRAP MODE Table 2-4	STRAP		STRAP MODE Table 2-5	STRAP	
15	RX_DV/ CRS_DV/ RX_CTRL (DP83TC81x) RX_CTRL (DP83TG720)		PHYADD[0]	PHYADD[2]		PHYADD[0]	PHYADD[2]
		Mode 1	0	0	Mode 1	0	0
		Mode 2	0	1	Mode 2	0	1
		Mode 3	1	0	NA	NA	NA
		Mode 4	1	1	Mode 3	1	1
14	RX_ER (DP83TC81x) STRAP_1 (DP83TG720)		PHYADD[1]	PHYADD[3]		PHYADD[1]	PHYADD[3]
		Mode 1	0	0	Mode 1	0	0
		Mode 2	0	1	Mode 2	0	1
		Mode 3	1	0	NA	NA	NA
		Mode 4	1	1	Mode 3	1	1

Table 2-4 shows strap resistor values for DP83TC811 and Table 2-5 show the recommended strap resistor values for DP83TC812, DP83TC814, and DP83TG720. RH are pull-up resistors and RL are pull down resistors.

Table 2-4. Recommended 4-level Strap Resistor Ratios For DP83TC811

MODE	IDEAL RH (kΩ)	IDEAL RL (kΩ)
1	OPEN	OPEN
2	10	2.49
3	5.76	2.49
4	2.49	OPEN

Table 2-5. Recommended 3-level Strap Resistor Ratios for DP83TC812/814, DP83TG720

MODE	IDEAL RH (kΩ) for VDDIO = 3.3 V	IDEAL RH (kΩ) for VDDIO = 2.5 V	IDEAL RH (kΩ) for VDDIO = 1.8V
1	OPEN	OPEN	OPEN
2	13	12	4
3	4.5	2	0.8

2.3.1.2 MAC Interface, Master/Slave, Autonomous Strap

Strap features on RX_D0, RX_D1, RX_D2, LED_0, and LED_1 are same for all four devices. They can be used by keeping the strap resistors open or by using a pull up resistor. Test Mode straps are not supported on DP83TC812, DP83TC814, and DP83TG720. This allows those strap pins to be used as two level straps. The PHYs can be configured in Test Modes via register access.

When strap resistors are not used, the PHY's internal pull down resistors will configure the PHY in Mode 1 by default. However, for LED pins it is recommended to use pull down resistor in parallel with the an LED when using Mode 1.

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Table 2-6. MAC Interface, Master/Slave, Autonomous Strap Comparison Table

PIN NO.	PIN NAME	DP83TC811			DP83TC812, DP83TC814, DP83TG720		
		STRAP MODE Table 2-7	STRAP		STRAP MODE Table 2-8	STRAP	
26	RX_D0		MAC[0]	TEST[0]		MAC[0]	NA
		Mode 1	0	0	Mode 1	0	
		Mode 2	0	1	NA	NA	
		Mode 3	1	0	NA	NA	
		Mode 4	1	1	Mode 2	1	
25	RX_D1		MAC[1]	TEST[1]		MAC[1]	NA
		Mode 1	0	0	Mode 1	0	
		Mode 2	0	1	NA	NA	
		Mode 3	1	0	NA	NA	
		Mode 4	1	1	Mode 2	1	
24	RX_D2		MAC[2]	TEST[2]		MAC[2]	NA
		Mode 1	0	0	Mode 1	0	
		Mode 2	0	1	NA	NA	
		Mode 3	1	0	NA	NA	
		Mode 4	1	1	Mode 2	1	
35	LED_0		MS	RESERVED		MS	NA
		Mode 1	0		Mode 1	0	
		Mode 2	RESERVED	RESERVED	NA	NA	
		Mode 3	RESERVED	RESERVED	NA	NA	
		Mode 4	1		Mode 2	1	
6	LED_1		$\overline{\text{AUTO}}$	RESERVED		$\overline{\text{AUTO}}$	RESERVED
		Mode 1	0		Mode 1	0	
		Mode 2	RESERVED	RESERVED	NA	NA	
		Mode 3	RESERVED	RESERVED	NA	NA	
		Mode 4	1		Mode 2	1	

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Table 2-7 shows strap resistor values for DP83TC811 and Table 2-8 shows strap resistor values for DP83TC812, DP83TC814, and DP83TG720.

Table 2-7. Recommended 4-level Strap Resistor Ratios For DP83TC811

MODE	IDEAL RH (kΩ)	IDEAL RL (kΩ)
1	OPEN	OPEN
2	10	2.49
3	5.76	2.49
4	2.49	OPEN

Table 2-8. Recommended 2-level Strap Resistor for DP83TC812/814, DP83TG720

MODE	IDEAL RH (kΩ)
1	OPEN
2	2.49

Table 2-9. 100BASE-T1 Master and 100BASE-T1 Slave Selection Bootstrap

MS	DESCRIPTION
0	100BASE-T1 Slave Configuration
1	100BASE-T1 Master Configuration

Table 2-10. MAC Interface Selection Bootstraps

MAC[2]	MAC[1]	MAC[0]	DESCRIPTION
0	0	0	SGMII (4-wire)
0	0	1	MII (DP83TC81x only)
0	1	0	RMII Slave (DP83TC81x only)
0	1	1	RMII Master (DP83TC81x only)
1	0	0	RGMII (Align Mode)
1	0	1	RGMII (TX Internal Delay Mode)
1	1	0	RGMII (TX and RX Internal Delay Mode)
1	1	1	RGMII (RX Internal Delay Mode)

Table 2-11. Test Mode Bootstraps

TEST[2]	TEST[1]	TEST[0]	DESCRIPTION
0	0	0	Normal Operation
0	0	1	Test Mode 1
0	1	0	Test Mode 2
0	1	1	RESERVED
1	0	0	Test Mode 4
1	0	1	Test Mode 5
1	1	0	RESERVED
1	1	1	RESERVED

Table 2-12. Autonomous Mode Bootstrap

AUTO	DESCRIPTION
0	Autonomous Mode, PHY able to establish link after power-up
1	Managed Mode, PHY must be allowed to establish link after power-up based on register write

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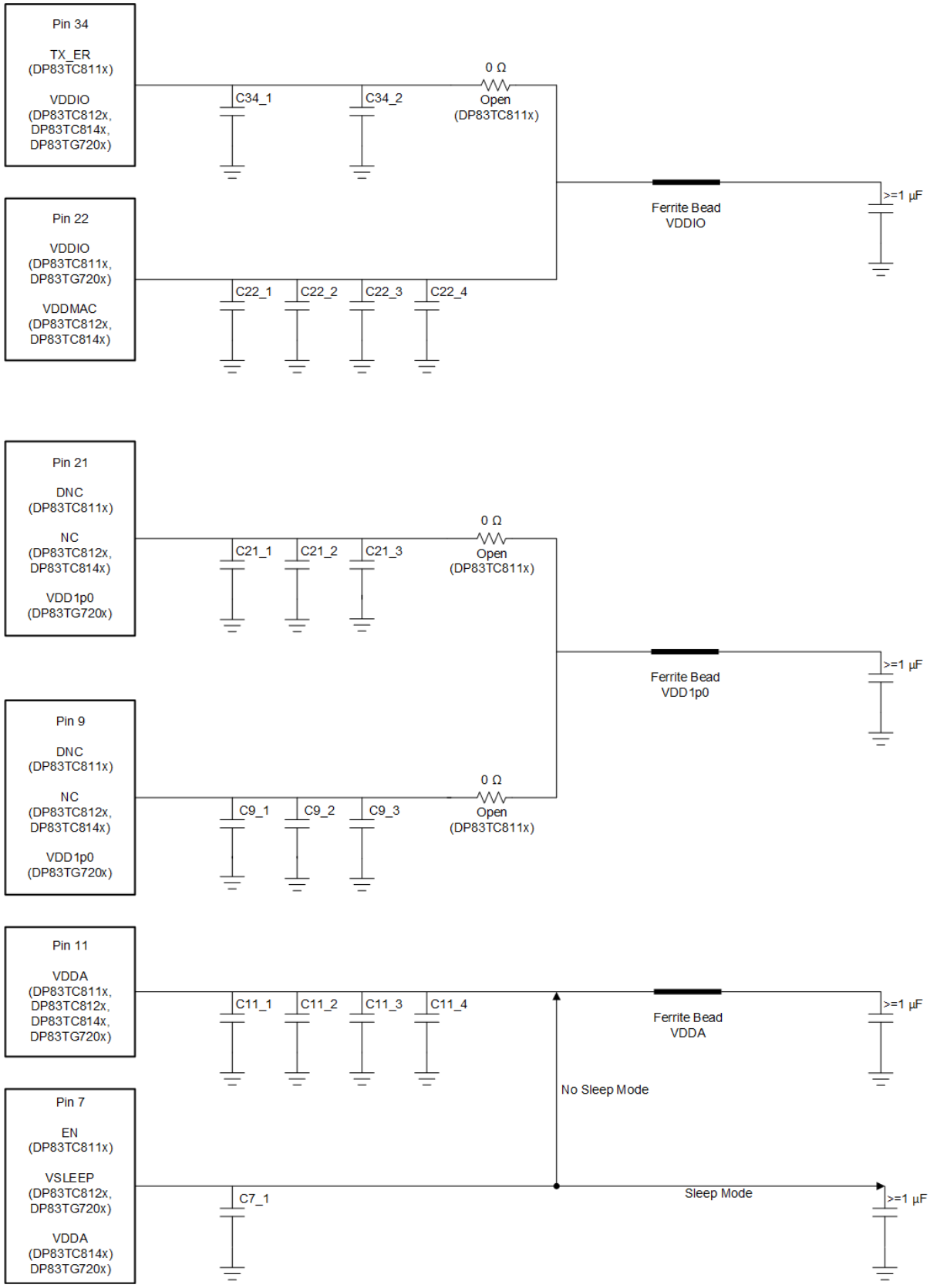
2.4 Power Supply Comparison

Figure 2-9. DP83TC811, DP83TC812, DP83TC814, DP83TG720 Power Supply Comparison



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2.5 Design Parameters

Design Parameter	DP83TC811 [1]	DP83TC812 [2] [3]	DP83TC814 [4] [5]	DP83TG720
V_{DDIO}	**1.8 V, 2.5 V, 3.3 V**	**1.8 V, 2.5 V, 3.3 V**	**1.8 V, 2.5 V, 3.3 V**	**1.8 V, 2.5 V, 3.3 V**
V_{DDMAC}	**N/A**	**1.8 V, 2.5 V, or 3.3 V**	**1.8 V, 2.5 V, or 3.3 V**	**N/A**
Ferrite Bead for V_{DDIO}	1 kΩ at 100 MHz (BLM18AG102SH) (Optional)	1 kΩ at 100 MHz (BLM18KG601SH1D)	1 kΩ at 100 MHz (BLM18KG601SH1D)	(BLM18HE102SN1)
C34_1	DNP	0.01 µF	0.01 µF	10 nF
C34_2	DNP	DNP	DNP	100 nF
C22_1	10 nF	0.01 µF	0.01 µF	10 nF
C22_2	100 nF	0.47 µF	0.47 µF	100 nF
C22_3	1 µF	DNP	DNP	2.2 µF
C22_4	10 µF	DNP	DNP	DNP
V_{DDA}	**3.3 V**	**3.3 V**	**3.3 V**	**3.3 V**
Ferrite Bead for V_{DDA}	1 kΩ at 100 MHz (BLM18AG102SH)	1 kΩ at 100 MHz (BLM18KG601SH1D)	1 kΩ at 100 MHz (BLM18KG601SH1D)	(BLM18KG601SH1)
C11_1	10 nF	0.01 µF	0.01 µF	10 nF
C11_2	100 nF	0.47 µF	0.47 µF	100 nF
C11_3	1 µF	DNP	DNP	2.2 µF
C11_4	10 µF	DNP	DNP	DNP
C7_1 (V_{DDA})	DNP	DNP	0.1 µF	DNP
V_{SLEEP}	**N/A**	**3.3 V**	**N/A**	**3.3 V**
C7_1 (V_{SLEEP})	DNP	0.1 µF	DNP	DNP
V_{DD1p0}	**N/A**	**N/A**	**N/A**	**1V**
Ferrite Bead for V_{DD1P0}	DNP	DNP	DNP	(BLM18KG601SH1)
C21_1	DNP	DNP	DNP	10 nF
C21_2	DNP	DNP	DNP	100 nF
C21_3	DNP	DNP	DNP	2.2 µF
C9_1	DNP	DNP	DNP	10 nF
C9_2	DNP	DNP	DNP	100 nF
C9_3	DNP	DNP	DNP	2.2 µF

Table Legend:

- DNP (Do Not Populate)

[1] DP83TC811 - 10% tolerance components are recommended.
[2] DP83TC812 - 10% tolerance components are recommended.
[3] DP83TC812 - If VDDIO is separate from VDDMAC then additional ferrite bead and 0.47 µF capacitor will be required on VDDIO.
[4] DP83TC814 - 10% tolerance components are recommended.
[5] DP83TC814 - If VDDIO is separate from VDDMAC then additional ferrite bead and 0.47 µF capacitor will be required on VDDIO.

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2.6 MDI Comparison

DP83TC811 data sheet recommends the optional LPF to pass certain EMC tests. DP83TC812, DP83TC814, DP83TG720 all have integrated LPF to improve EMC performance. The LPF components should be removed when using these three devices.

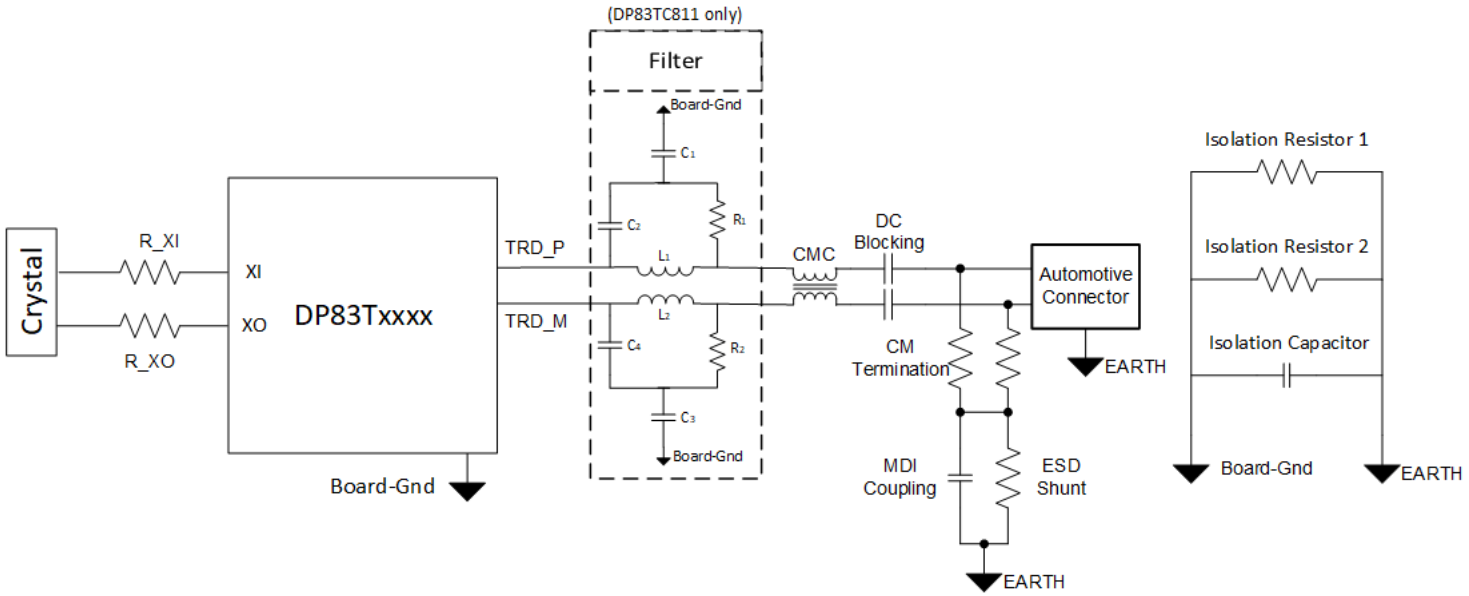

Figure 2-10. DP83Txxxx MDI and Crystal Schematic with Optional LPF

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2.7 CMC Comparison

CMC for 100BASE-T1 devices and 1000BASE-T1 devices are different. When changing between 100BASE-T1 and 1000BASE-T1, CMC needs to be changed accordingly.

The following CMCs are recommended for use with the DP83TC811:

- Pulse Electronics (AE2002)
- Murata (DLW43MH201XK2L; DLW32MH201XK2)
- TDK (ACT45L-201; ACT1210L-201)

The following CMCs are recommended for use with the DP83TC812 and DP83TC814:

- Pulse Electronics (AE2002)
- Murata (DLW43MH201XK2L; DLW32MH201XK2)
- TDK (ACT1210L-201)

The following CMCs are recommended for use with the DP83TG720:

- Murata (DLW32MH101XT2)

The layout should be optimized for 1000BASE-T1 PHY when creating a PCB to support both 1000Mbps and 100Mbps PHYs.

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2.8 SGMII Reference Schematics

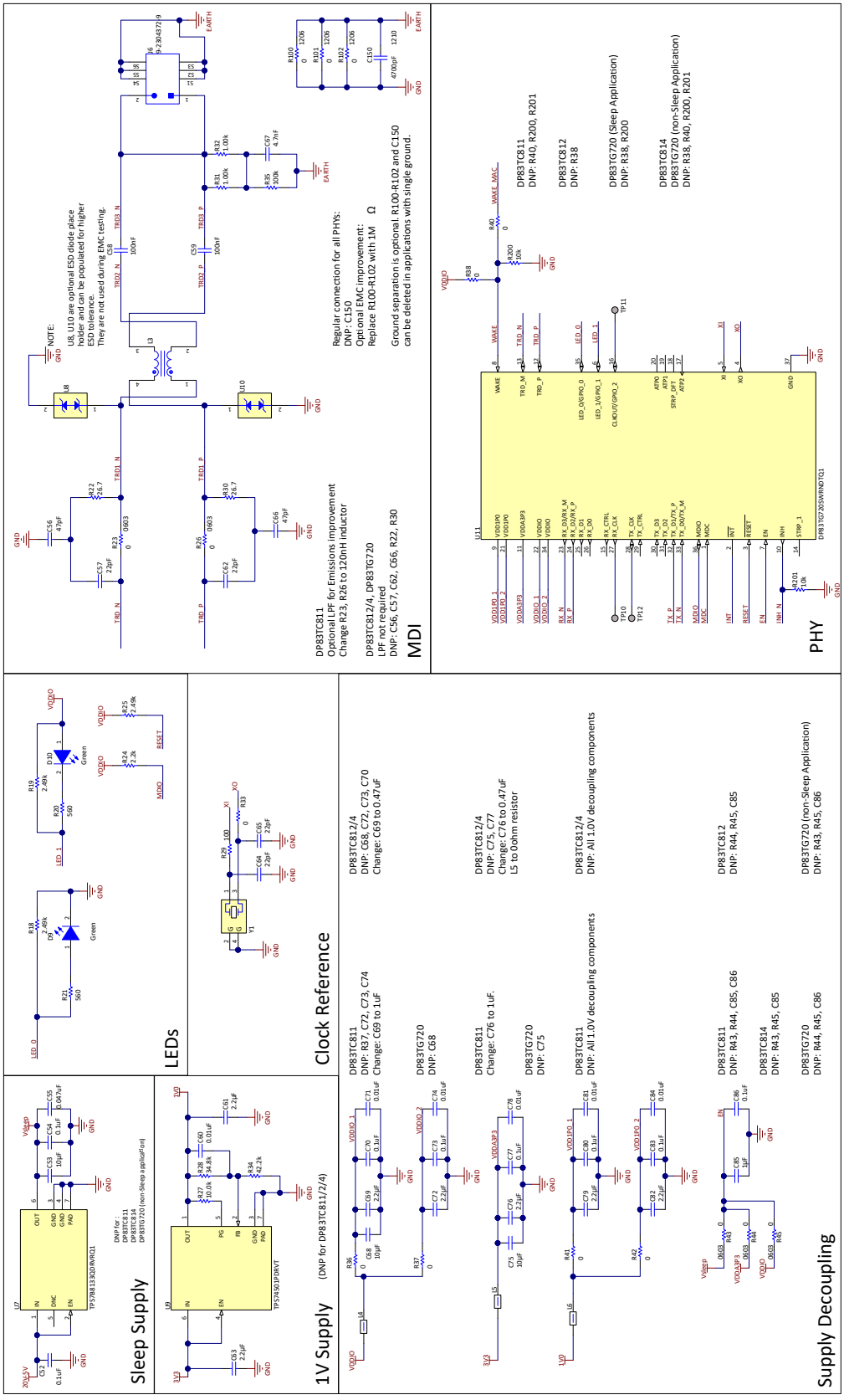

Figure 2-11. SGMII Reference Schematics

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2.9 RGMII Reference Schematics

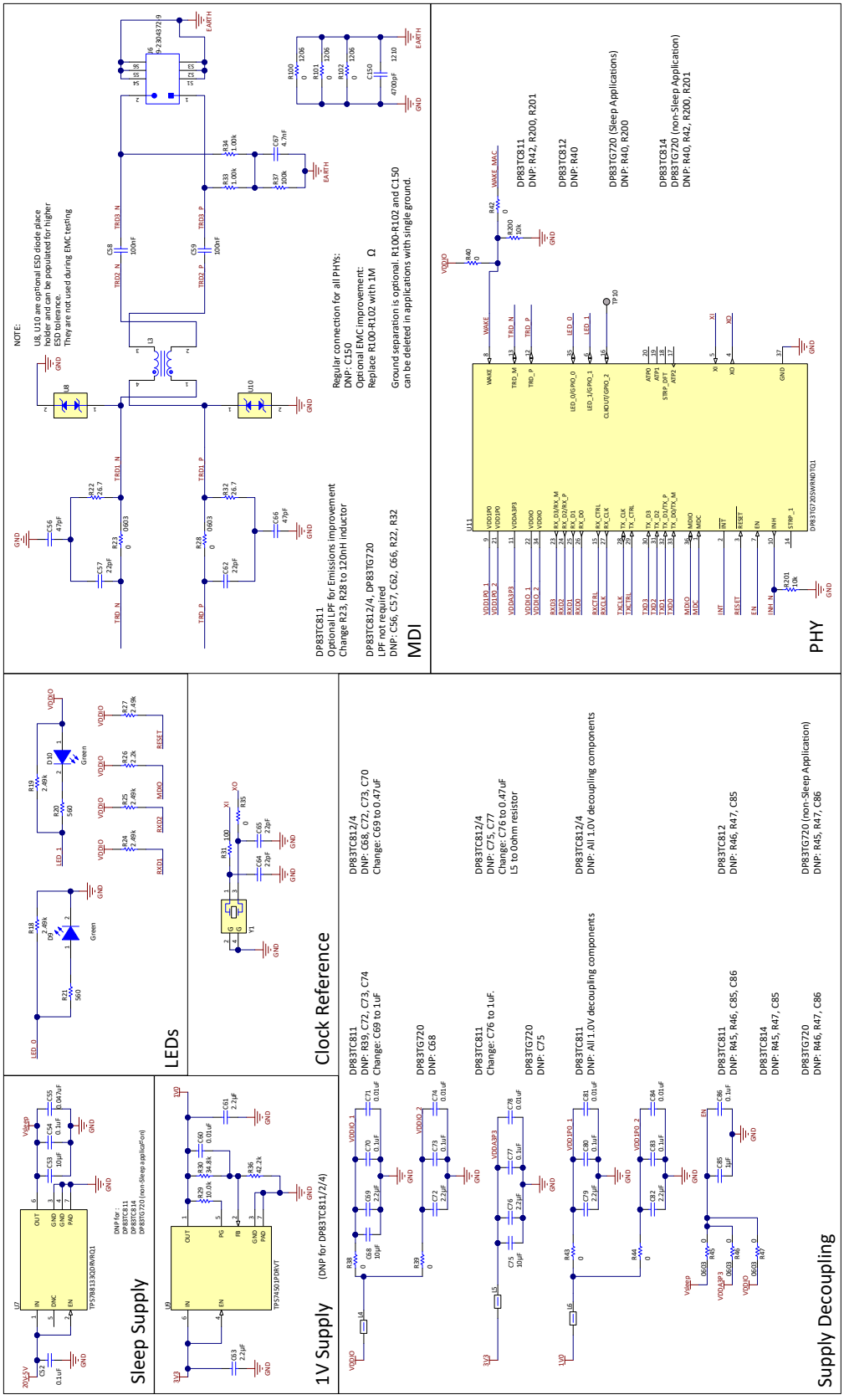

Figure 2-12. RGMII Reference Schematics

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3 Summary

This application note discusses the differences between Texas Instruments four 36-QFN Ethernet PHYs and details how they all can be accommodated on a single design. With proper component selection, DP83TC811, DP83TC812, DP83TC814, and DP83TG720 can all be used on the same PCB.

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