Application Brief

Space-Grade, 100-krad, Linear Thermoelectric Cooler (TEC) Driver Circuit

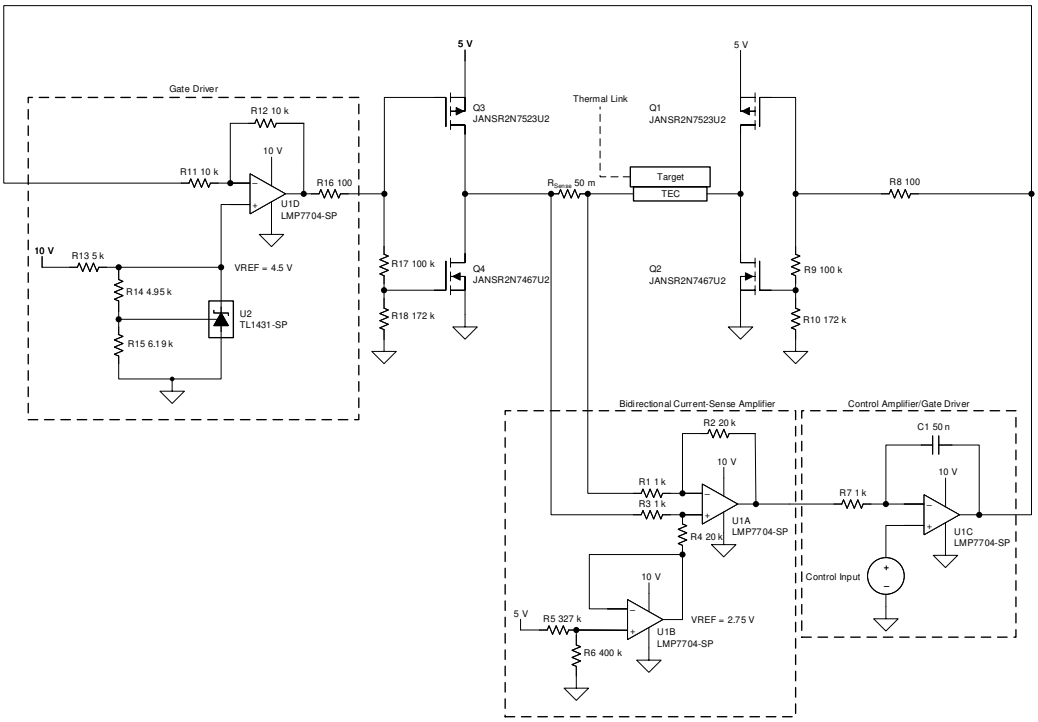
Fadi Matloob

Design Goals

Parameter	Output
TEC Driver Control Signal	0.25V to 5.25V
TEC Current Range ($-I_{max}$ to I_{max})	–2.5A to 2.5A
TEC Voltage Range ($-V_{max}$ to V_{max})	–4.5V to 4.5V
Total Ionizing Dose (TID)	100-krad(Si)
Single Event Latch-up (SEL) Immunity	85 MeV·cm^2/mg

Design Description

Thermoelectric coolers (TECs) are solid-state heat pumps that utilize electrical energy to heat or cool. They are often used in laser communication systems to regulate laser temperatures or in low-noise imaging systems such as star trackers or wide field planetary cameras. The TEC has two sides where it transfers heat from one side to the other side depending on the direction of electrical current flow through it. The amount of heat being transferred depends on the magnitude of the electrical current. This results in a temperature difference between the two sides. The two sides of the TEC are known as the *cold side* and *hot side*. The ability to swap the two sides by reversing the direction of current flow allows for heating and cooling without changing any physical configurations. The following figure shows a rad-hard linear TEC driver that can accurately control the magnitude and direction of the current through the TEC without injecting any switching noise into the system.



Design Notes

- Typically, when designing a TEC system, the first steps are to identify the heat load (usually power rating) of the system and the desired ΔT between the hot side and cold side. Once these specifications are determined, then the TEC can be selected. Once a TEC is selected, it is important to identify the rated I_{max} and V_{max}. Note that I_{max} and V_{max} are not the maximum ratings before the TEC is damaged; rather, they are the maximum ratings before the heat generated by the TEC starts to degrade the heating or cooling performance.
- To operate the H-bridge correctly and control the current going through the TEC, one channel of the LMP7704-SP (U1A) is used as a bidirectional current-sense amplifier, which measures the current through the TEC. There is also a DC reference generated by another channel of the LMP7704-SP (U1B) to account for the negative current since it is assumed that the amplifier is operated from a single positive supply. A control amplifier (U1C) utilizes the output of the bidirectional current-sense amplifier (U1A) as feedback in conjunction with a control input signal (DAC, PID, and so forth) to determine the drive level of the H-bridge. The control input signal sets the desired current level through the TEC. The control amplifier is also responsible for driving the half-bridge on the right side. The gate driver (U1D) is responsible for driving the half-bridge on the left side. There are two things to note:
  1. U1D is DC biased by a TL1431-SP (U2) voltage reference which defaults the output of U1D to a high voltage. As the output of U1C increases, the output of U1D will decrease (larger inverting signal).
  2. When the N-channel FET (low-side) on one half-bridge is ON (Q2 or Q4), the P-channel FET (high-side) of the opposite half-bridge will be ON as well (Q3 or Q1). This allows for current to flow in both directions based on which diagonal pair of FETs is turned ON.
- The LMP7704-SP supply voltage of 10V was selected according to the derating specifications provided by the National Aeronautics and Space Administration (NASA) in document EEE-INST-002 (April 2008) and the European Cooperation for Space Standardization (ECSS) in document ECSS-Q-ST-30-11C Rev.1 (4 October 2011). The documents specify an 80% and 90% derating of the absolute maximum supply voltage for linear ICs, respectively.
- For proper operation, the power supplies must be decoupled. For supply decoupling, TI recommends placing 10-nF to 1-µF capacitors as close as possible to the operational-amplifier power supply pins. For the single supply configuration shown, place a capacitor between the V+ and V– supply pins. Bypass capacitors must have a low ESR of less than 0.1Ω.

Design Steps

1. **Identify the TEC specifications:**
   - Specifications for the circuit shown:
     - TEC maximum current (I_{max}): 2.5A
     - TEC maximum voltage (V_{max}): 4.5V
2. **H-bridge voltage supply selection:**
   - Important Considerations:
     - Voltage drops across the FETs (V_{FETs})
     - Voltage drop across R_{Sense} (V_{Rsense})
     - Voltage drop across the TEC (V_{TEC})
       - The H-bridge voltage supply ($V_{H\text{-}Bridge}$) should be at least:

$$V_{\mathrm{H-Bridge}} = V_{\mathrm{FETs}} + V_{R_{\mathrm{Sense}}} + V_{\mathrm{TEC}}$$

   - In the previous circuit shown, a 5-V supply is used for the H-bridge to give 0.5V of headroom and accommodate for all of the voltage drops.
   - The H-bridge supply may need to be increased if:
     - A higher voltage is needed for the TEC.
     - FETs cannot be turned ON fully and produce significant voltages drops.
3. **Bidirectional current-sense amplifier (U1A):**
   - The current-sense amplifier senses the current through the TEC using a sense resistor (R_{Sense}). The output is used as feedback to the control amplifier (U1C) which determines the gate drive strength (TEC current).
   - **R_{Sense} selection:**
     - Smaller values of R_{Sense} give better power dissipation performance and produce a lower voltage drop. Depending on the desired system accuracy, small values require a precision amplifier with great DC performance to accurately read the sense resistor voltage.
     - R_{Sense} for this circuit was chosen to be 50mΩ. A 50-mΩ resister produces a voltage drop of 125mV at 2.5A. The LMP7704-SP has a typical offset voltage of ±37µV which produces an error of about 0.75mA at peak current.
   - **U1A Gain Selection:**
     - The current-sense amplifier gain is determined by the resistors R1, R2, R3, and R4
     - In the previous circuit shown, it is desirable to measure the current as a voltage level by adjusting U1A gain. The chosen gain for the current-sense amplifier is G = 20.
       - A TEC current of 2.5A equates to a 125mV across R_{Sense}. 125mV across R_{Sense} translates to 2.5V (125mV × 20) at the output of U1A. The gain selection produces a 1-to-1 relationship between the current through the TEC and the output voltage of the current-sense amplifier.
     - Gain selection equations:

$$G_{\mathrm{U1A}} = \frac{1}{R_{\mathrm{Sense}}} = \frac{1}{50\mathrm{m\Omega}} = 20 = \frac{\mathrm{R2}}{\mathrm{R1}} = \frac{20\mathrm{k\Omega}}{1\mathrm{k\Omega}}$$

$$\mathrm{R2} = \mathrm{R4} \text{ and } \mathrm{R1} = \mathrm{R3}$$

     - Following the previous equations always results in a 1-to-1 relationship between the TEC current and the output voltage of the current-sense amplifier.

- **Voltage Reference Selection (U1B):**
  - A single-supply op amp is not able to measure current bidirectionally unless it has a DC offset. If no offset is used, the output of the amplifier saturates when the current has the opposite sign of the voltage supply of the op amp. This is why a voltage reference is used to generate a DC offset and prevent saturation.
  - Reference voltage value selection:
    - The voltage reference needs to be at least equivalent to the expected maximum current through the TEC. If 2.5A is the rated I_{max} of the TEC, then at least a 2.5-V reference must be used to account for the current range of –2.5A to 2.5A. It is also paramount to account for the output swing limitation (V_O) of the amplifier.

$$V_{\mathrm{REF}} = R_{\mathrm{Sense}} \times I_{\mathrm{Max}} \times G_{\mathrm{U1A}} + V_{\mathrm{O}}$$

    - A reference voltage of 2.75V was chosen due to the amplifier negative output rail limitation of (V–) + 0.2V.

$$V_{\mathrm{REF}} = 2.75\mathrm{V} \geq 50\mathrm{m\Omega} \times 2.5\mathrm{A} \times 20 + 0.2\mathrm{V}$$

      a. The voltage divider formed by R5 and R6 is fed to one of the LMP7704-SP channels (U1B) as a buffer. The voltage divider generates the reference voltage of 2.75V.
        - To adjust the output of the reference, use the following equation:

$$V_{\mathrm{REF}} = \left(\frac{\mathrm{R6}}{\mathrm{R5} + \mathrm{R6}}\right) \times 5\mathrm{V}$$

        - The accuracy of the voltage reference depends on the tolerance of the resistors in the divider.
      b. With a voltage reference, **calculate the output voltage of the current-sense amplifier as follows:**

$$V_{\mathrm{out(U1A)}} = R_{\mathrm{Sense}} \times I_{\mathrm{TEC}} \times G_{\mathrm{U1A}} + V_{\mathrm{REF}}$$

        - As the current through the TEC goes from –2.5A to 2.5A, the output voltage of the current-sense amplifier goes from 0.25V to 5.25V (2.75V is equivalent to 0A).
      c. If the negative rail output swing limitation of the chosen amplifier is not accounted for, the current-sense amplifier could saturate and cause the rest of the system to saturate to the maximum possible negative current. The value of the saturated current through the TEC could be more than 2.5A and it would depend on the H-bridge supply voltage and gate drive capability.
        - Fortunately, the LMP7704-SP is a rail-to-rail output amplifier so 0.25V is satisfactory to mitigate the output swing limitation. A different amplifier with less swing requires more headroom from the voltage reference.
- **Voltage Supply Selection:**
  - The voltage supply of the current-sense amplifier must be above the maximum expected output V_{max} and the maximum output swing limitation V_O.

$$V_{\mathrm{Supply}} \geq V_{\mathrm{Max}} + V_{\mathrm{O}}$$

$$10\mathrm{V} \geq 5.25\mathrm{V} + 0.2\mathrm{V}$$

  - The chosen amplifier supply is 10V which meets these requirements.
  - Failing to consider the positive output swing limitation can result in the system saturating to the maximum positive TEC current. The maximum positive TEC current could be more than 2.5A (similar to the case of saturating to the negative supply mentioned in the *Voltage Reference Selection* section).

4. **Control Amplifier (U1C)**:
   - The control amplifier U1C *controls* the gate drive strength (discussed in *Gate Drivers (U1C and U1D)*). To determine the gate drive strength and direction, it compares the output from the current-sense amplifier to a ***control input***. The control input (V_{IN}) can come from a PID or an averaged PWM (usually as an output of a temperature control loop). Since an op amp drives its output until both its input terminals are at the same voltage level, V_{IN} is what determines the desired current level through the TEC.
   - To control the current through the TEC, set the control input, V_{IN}, to a voltage from 0.25V to 5.25V. The control amplifier output goes as high or as low as needed to reach the point where the feedback (U1A output) and V_{IN} are at the same level. Calculate the set TEC current level according to the control input voltage (V_{IN}) and the voltage reference of the current-sense amplifier (V_{REF}):

$$I_{\mathrm{TEC}} = V_{\mathrm{IN}} - V_{\mathrm{REF}}$$

$$I_{\mathrm{TEC}} = V_{\mathrm{IN}} - 2.75\mathrm{V}$$

   - A V_{IN} of 0.25V means the control amplifier changes its output until –2.5A is sensed through the TEC. Similarly, a 5.25-V input signal means the control amplifier changes its output until 2.5A is sensed through the TEC.
     - This behavior can be susceptible to oscillations; therefore, components R1 and C1 are added to not allow for the output of the control amplifier to change instantaneously. The values were chosen to induce at least 60° of phase margin as shown in the *AC Simulation Results* section.
5. **Gate Drivers (U1C and U1D):**
   - The gate drivers are responsible for providing gate signals to each half-bridge.
   - **Gate driver functionality:**
     - Taking a look at either gate driver and its corresponding half-bridge:
       - When the output of the gate driver is a high voltage this only turns ON the N-channel FET (Q2 or Q4). When the output is a low voltage, the P-channel FET is ON (Q1 or Q3).
         - It is important to consider if there is any point where three FETs can be ON simultaneously. This is discussed in the *MOSFET Selection* section.
       - An isolation resistor (R_{iso}) is added to prevent instability when driving the FETs capacitive load. The value of R8 and R16 is calculated with the following equation:

$$R_{\mathrm{iso}} \geq \frac{1}{2 \times \pi \times f_{\mathrm{20DB}} \times C_{\mathrm{load}}}$$

$$R_{\mathrm{iso}} = 100\Omega \geq 80\Omega \approx \frac{1}{2 \times \pi \times 248\mathrm{kHz} \times 8000\mathrm{pF}}$$

         - For more details, see *TI Precision Labs - Op Amps: Stability - Capacitive loads*.
   - **Setting the gate drive maximum output:**
     - To set the maximum output voltage of the gate drivers ($V_{maxDriver}$), change the reference voltage TL1431-SP (U2) applied to U1D. **Ensure that $V_{maxDriver}$ is within the output swing capability of the chosen amplifier.** In this case the LMP7704-SP output swing is 0.2V from the positive rail; therefore, the maximum $V_{maxDriver}$ is 9.8V.
       - Setting the TL1431-SP (U2) reference:

$$V_{\mathrm{REF(U2)}} = \left(1 + \frac{\mathrm{R14}}{\mathrm{R15}}\right) \times 2.5\mathrm{V}$$

$$V_{\mathrm{REF(U2)}} = 4.5\mathrm{V} = \left(1 + \frac{4.95\mathrm{k}\Omega}{6.19\mathrm{k}\Omega}\right) \times 2.5\mathrm{V}$$

  - R13 is used to limit supply current when biasing the cathode. Ensure that R13 provides more than 1mA to U2:

$$I_{U2} = \frac{V_{Supply} - V_{REF(U2)}}{R13} \geq 1mA$$

$$I_{U2} = 1.1mA = \frac{10V - 4.5V}{5k\Omega} \geq 1mA$$

- Setting $V_{maxDriver}$ Voltage:

$$V_{maxDriver} = \left(1 + \frac{R12}{R11}\right) \times V_{REF(U2)}$$

$$V_{maxDriver} = 9V = \left(1 + \frac{10k\Omega}{10k\Omega}\right) \times 4.5V$$

- In the previous design shown, the maximum driver output voltage is equivalent to double the reference voltage due to the non-inverting gain being G = 2.
- Note that $V_{maxDriver}$ is the maximum voltage the gate driver U1D could ever produce. **However, $V_{maxDriver}$ is not the maximum voltage applied to the H-bridges by the gate drivers to generate 2.5A through the TEC ($V_{maxGate}$).** $V_{maxGate}$ depends on the MOSFETs selected and $V_{H\text{-}Bridge}$. Determine $V_{maxGate}$ through simulation or by looking at the MOSFET data sheets and identifying the V_{GS} required to attain I_{max}. Simulation showed that a maximum $V_{maxGate}$ of 8V (worst-case FET threshold voltages) is needed to achieve 2.5A through the TEC.
  - Ensure that $V_{maxDriver}$ is above the maximum $V_{maxGate}$ by the amount of output swing limitation of the control amplifier ($V_{O(U1C)}$):

$$V_{maxDriver} \geq V_{maxGate} + V_{O(U1C)}$$

$$V_{maxDriver} = 9V \geq 8V + 0.2V$$

  - $V_{maxDriver}$ needs to be above $V_{maxGate}$ to ensure that the control amplifier (U1C) does not saturate into the negative rail.

- **Inverting gate driver signals:**
  - It is important to note that if both gate drivers (U1C and U1D) tracked each other, then all 4 FETs will turn ON at the same time. This is undesirable as it causes shoot-through current. The ideal behavior is that only one of the two diagonal pairs of FETs is turned ON. The diagonal pairs being (Q1 and Q4) OR (Q3 and Q2).
    - To achieve this behavior, the output of U1C is connected to the inverting input of U1D. Looking at how this works: U1D defaults its output to $V_{maxDriver}$. However, as the minimum 0.25V V_{IN} is applied, the output of U1C will slightly increase and settle until –2.5A is sensed. This causes the output of U1D to be at $V_{maxGate}$. As V_{IN} changes, the relationship between both gate driver outputs is defined as follows:

$$U1D_{OUT} = V_{maxDriver} - U1C_{OUT}$$

- This causes the outputs to linearly track each other and in opposite directions, that is, when U1D is at 9V then U1C is at 0V.
  a. This is why $V_{maxDriver}$ needs to be above $V_{maxGate}$ by $V_{O(U1C)}$: to avoid a situation where the output of the U1C is at 0V since it can only swing down to 0.2V of the negative rail (GND).
  b. Assuming that the MOSFET threshold voltages are accounted for, this gate driver design ensures that only one of the two aforementioned diagonal pairs is ON during operation.

- **Amplifier selection:**
  - Ensure that the op amp chosen has enough output swing to support the desired maximum voltage. The LMP7704-SP can swing to 0.2V of the positive supply (9.8V).

6. **MOSFET Selection:**
   - The FET threshold voltage is critical to obtaining a working design. During operation, only one pair of the diagonal FETs must be turned ON at a time. The pairs being: (Q1 and Q4) or (Q3 and Q2). If three FETs were to be ON simultaneously, for example – Q1, Q2, and Q4 then the H-bridge supply rail could connect to GND with a very small resistance through Q2 and cause a spike in current known as shoot-through current. This could damage the FET and lead to system failure. To avoid this, it is absolutely crucial to have only one of the diagonal FET pairs turned ON at a time.
     - For the circuit shown, the FETs selected all have a minimum threshold voltage (V_{th}) of 2V (N-channel) or –2V (P-channel).
       - This means a 2.5-V gate signal, without the resistor divider on the N-channel FETs, can turn ON both the high-side and low-side FET of the same half-bridge and cause shoot-through current.
         - To ensure this does not happen, a voltage divider is added for the N-channel FETs. Choose the voltage divider such that when the P-channel FET is about to turn ON, the N-channel FET, driven by the same gate signal, should be off. For the chosen FETs that have a V_{th} of 2V, it was chosen that the N-channel FET gate ($V_{N\text{-}Gate}$) should be at 1.9V when 3V is an output of a gate driver. Calculate the voltage divider as follows (assume R_{TOP} = 100kΩ and ensure that $V_{N\text{-}Gate}$ is lower than the minimum N-channel V_{th}):

$$R_{BOTTOM} = \frac{\frac{V_{N-Gate}}{\left(V_{H-Bridge} + V_{th(min)PFET}\right)}}{1-\frac{V_{N-Gate}}{\left(V_{H-Bridge} + V_{th(min)PFET}\right)}} \times R_{TOP}; \quad V_{N-Gate} < V_{th(min)NFET}$$

$$R_{BOTTOM} = 172k\Omega \approx \frac{\frac{1.9V}{(5V + (-2V))}}{1-\frac{1.9V}{(5V + (-2V))}} \times 100k\Omega$$

     - With the previously-calculated resistor divider, if a 2.5-V gate signal is applied to turn ON the P-channel FET then the N-channel gate only sees 1.6V and therefore it is off. This ensures only one of the diagonal pairs of FETs is ON during operation.
       - Ensure that the gate can be driven high enough such that the maximum V_{th} of the FETs (from the data sheet) can still be used with the resistor divider. According to the data sheet, the maximum V_{th} is 4V. When an absolute maximum $V_{maxGate}$ (8.8V) signal is applied, the maximum $V_{N\text{-}Gate}$ with the divider is 5.56V. Ensuring turn ON at V_{th} variation.
         - The absolute maximum $V_{maxGate}$ without saturating U1C is 8.8V and is derived based on the following equation:

$$V_{maxGate} \leq V_{maxDriver} - V_{O(U1C)}$$

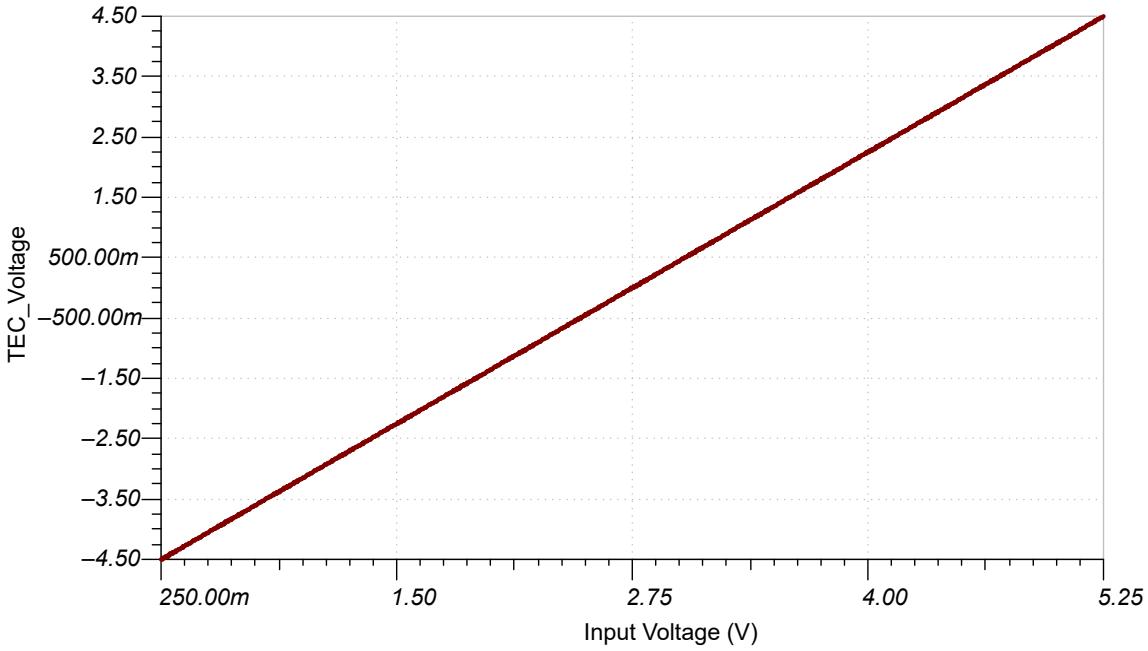
$$V_{maxGate} = 8.8V \leq 9V - 0.2V$$

Design Simulations

DC Simulation Results

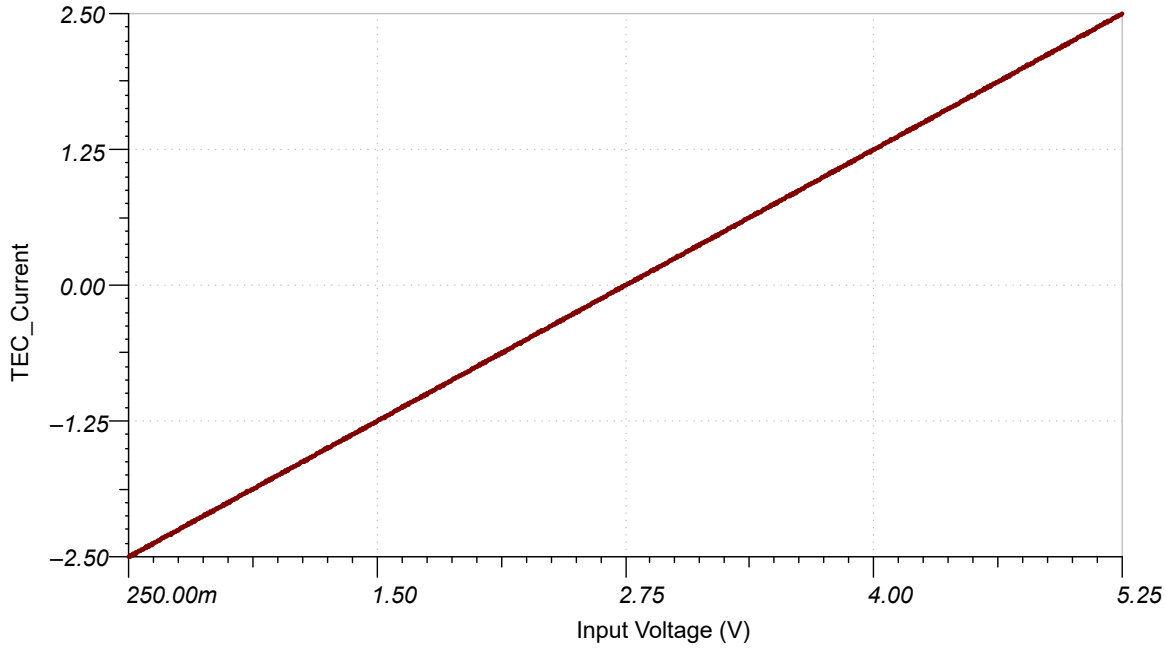
TEC Voltage

The following plot shows the output voltage across the TEC as a function of the control input voltage. As the control input voltage varies from 0.25V to 5.25V, the TEC voltage varies from –4.5V to 4.5V, which meets the design criteria.



TEC Current

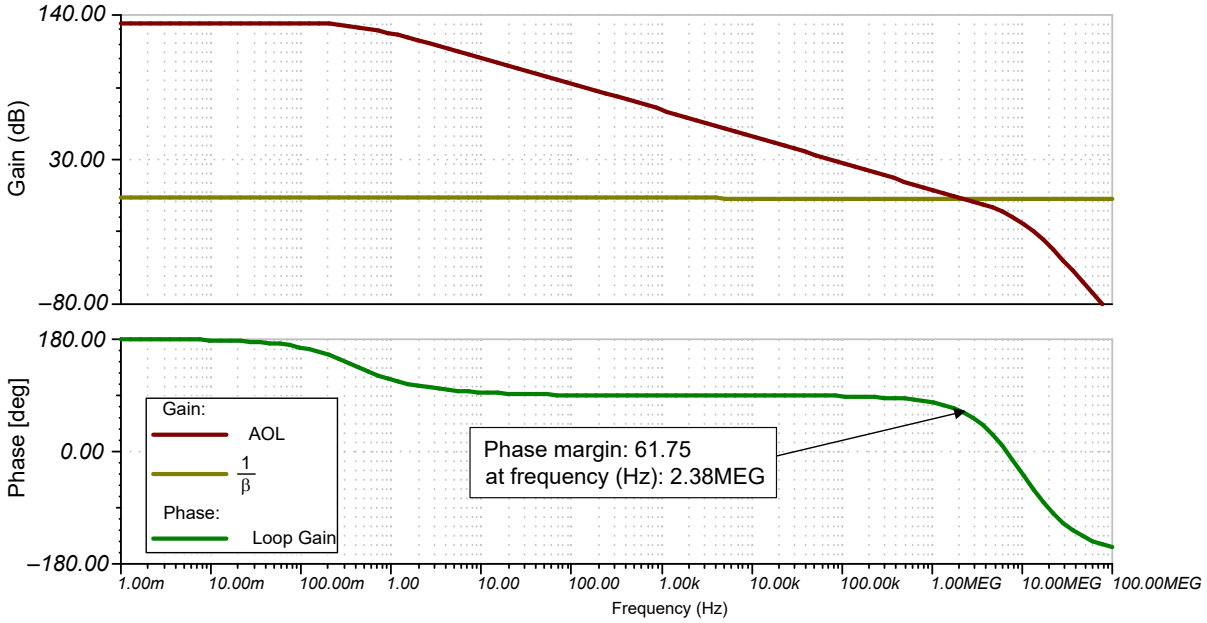
The following plot shows the current through the TEC as a function of the control input voltage. As the control input voltage varies from 0.25V to 5.25V, the TEC current varies from –2.5A to 2.5A, which meets the design criteria.

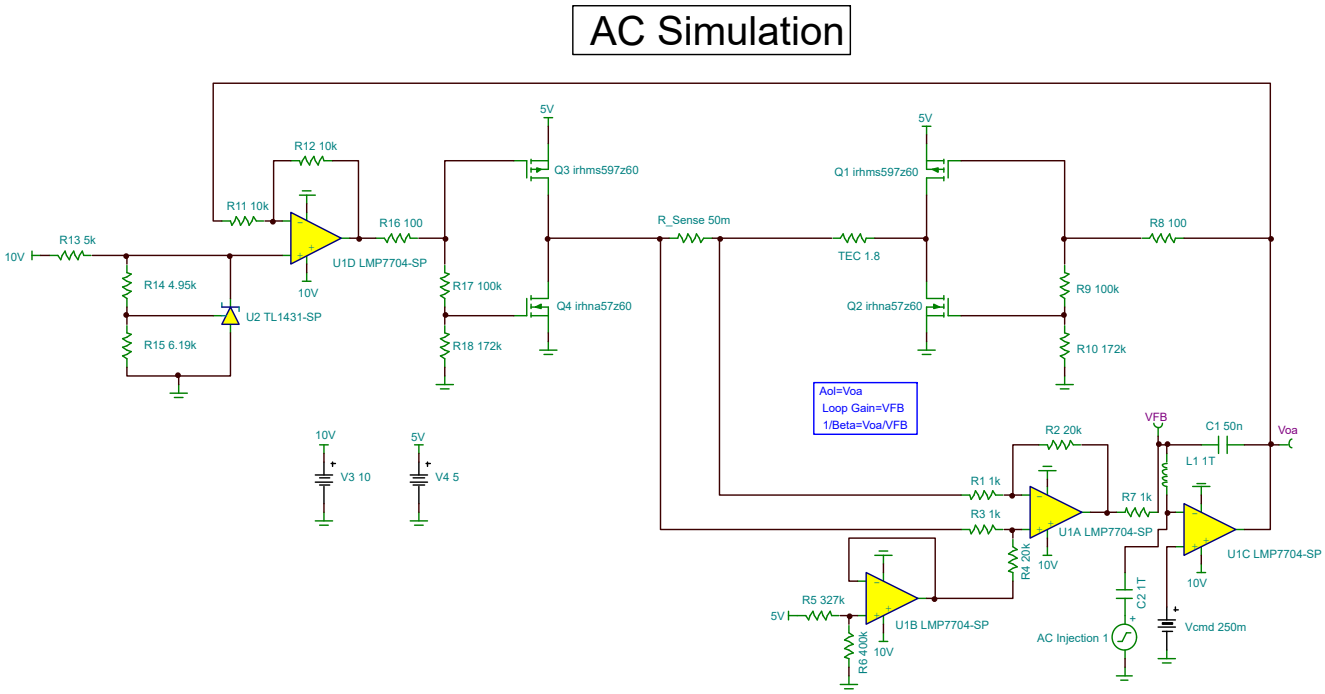


AC Simulation Results

Stability

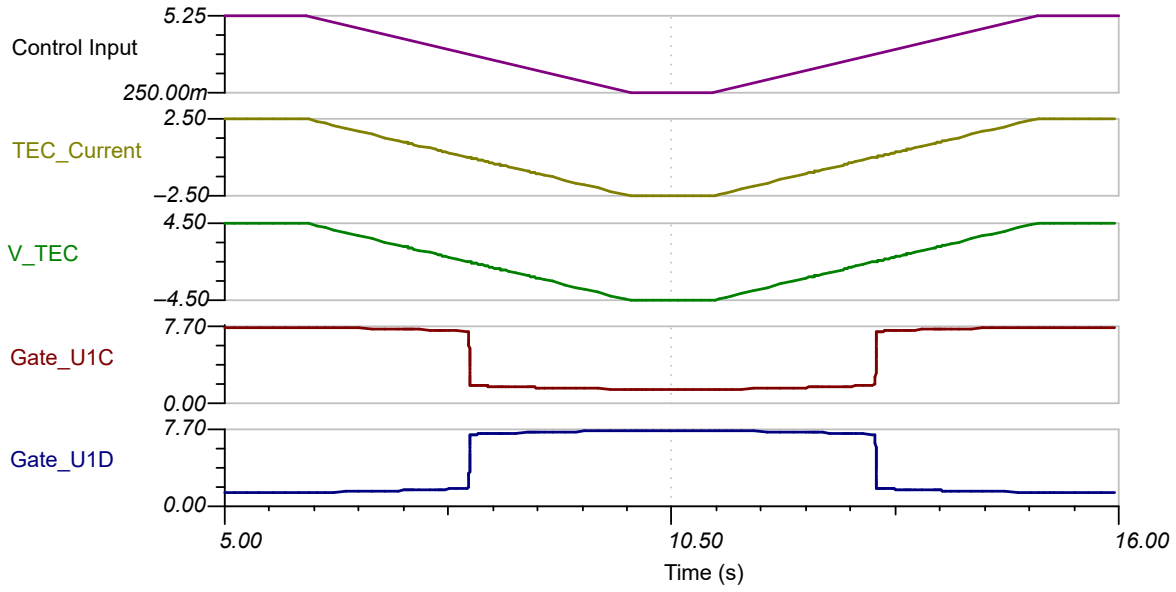
The following image illustrates the gain and phase plot of the system. The phase margin is found to be ≈ 62°. The criterion for stability is: the rate-of-closure at fcl = (Aol slope – 1/β slope) is 20dB/decade. The following gain plot shows both Voa (Aol) and 1/β. Without capacitor C1, 1/β experiences a zero and provides a rate-of-closure of 40dB/decade. Adding capacitor C1 creates a pole in 1/β and ensures the rate-of-closure is at 20dB/decade and therefore the circuit is stabilized. For more details, see *TI Precision Labs - Op Amps: Stability - Introduction*.

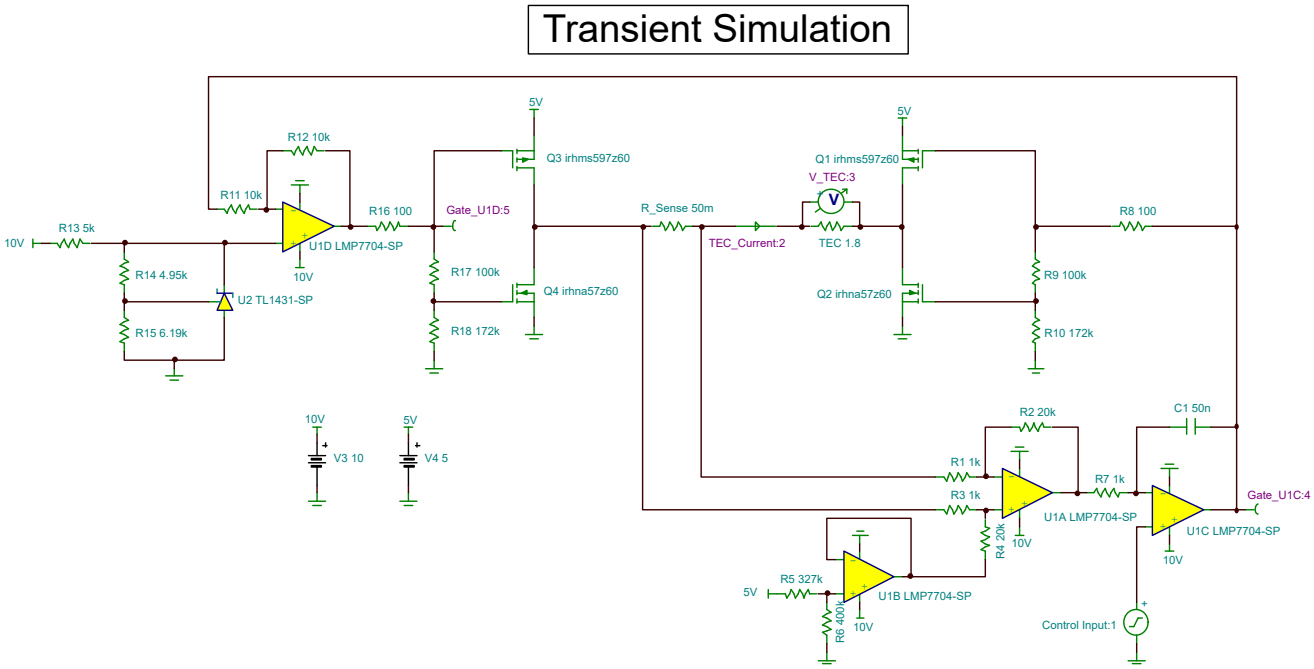




Transient Simulation Results

The following simulation shows the system response as a function of time. The control input voltage varies from 5.25V to 0.25V and back to 5.25V. The TEC voltage and current vary from –4.5V to 4.5V and –2.5A to 2.5A, respectively. This meets the TEC design specifications. The gate signals can be seen as inversions of one another (as designed) and ranging from 1.36V to 7.63V to achieve –2.5A to 2.5A through the TEC. This implies that $V_{maxGate}$ based on the MOSFETs selected is 7.63V.





Design References

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2. European Cooperation for Space Standardization. (October 2011). *ECSS-Q-ST-30-11C Rev.1 – Derating – EEE components*. Retrieved from https://ecss.nl/standard/ecss-q-st-30-11c-rev-1-derating-eee-components-4-october-2011

Design Featured Op Amp

LMP7704-SP	
V_{ss}	2.7V to 12V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	±32µV
I_q	2.9mA
I_b	±0.2pA
UGBW	2.5MHz
SR	1V / µs
#Channels	4
Total Ionizing Dose (TID)	100-krad(Si)
Single Event Latch-up (SEL) Immunity	85 MeV·cm^2/mg
LMP7704-SP	

Design Alternate Op Amp

LM124AQML-SP	
V_{ss}	3V to 32V
V_{os}	2mV
I_b	45nA
UGBW	1MHz
SR	0.1V / µs
#Channels	4
Total Ionizing Dose (TID)	100-krad(Si)
SEL Immunity	SEL Immune (Bipolar process)
LM124AQML-SP	

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