User's Guide

LM2745 and LM2748 Buck Controller Evaluation Module User's Guide

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1 Introduction

This evaluation board describes the LM2745/LM2748 printed circuit board (PCB) design and provides an example typical application circuit. The demo board allows component design flexibility in order to demonstrate the versatility of the LM2745/LM2748 IC.

The demo board contains a voltage-mode, high-speed synchronous buck regulator controller. Though the control sections of the IC are rated for 3 V to 6 V (V_{CC}), the driver sections are designed to accept input supply rails (V_{IN}) as high as 14 V.

The demo board design regulates to an output voltage of 1.2 V at 3.5A with a switching frequency of 1 MHz from a 1-MHz clock source that has an amplitude from 0 V to V_{CC}. Note, the demo board is optimized for a 1-MHz, 14-V input voltage compensation design with V_{CC} = 3.3 V. If a slower switching frequency and input voltage is desired, consult the device-specific data sheet for control loop compensation procedures. For additional design modifications, see the *Design Consideration* section of the *LM2745/8 Synchronous Buck Controller with Pre-bias Startup, and Optional Clock Synchronization Data Sheet*.

The demo board accommodates the use of banana clips to clip onto pads on the board. If preferred, the pads inner diameters are 100 mils, for which a solder terminal can be placed (Newark 40F6004). The PCB is designed on two layers with 1-oz. copper on a 62-mil FR4 laminate.

2 Additional Footprints

An additional footprint D1 is available for a Schottky diode to be placed in parallel with the low-side MOSFET. This component can improve efficiency, due to the lower forward drop than the low-side MOSFET body diode conducting during the anti-shoot–through period. Select a Schottky diode that maintains a forward drop around 0.4 V to 0.6 V at the maximum load current (consult the I-V curve). In addition, select the reverse breakdown voltage to have sufficient margin above the maximum input voltage.

Footprint C13 is available for a multilayer ceramic capacitor (MLCC) connected flush to the source of the low-side MOSFET and drain of the high-side MOSFET, in order to provide low supply impedance. For example, component C13 is used in combination with aluminum electrolytic input filter capacitors, placed in designators C12 and C14. If MLCCs are used in designators C12 and C14, component C13 is not necessary.

3 Typical Application Circuit

The typical application circuit in Figure 3-1 provides the component designators used on the demo board.

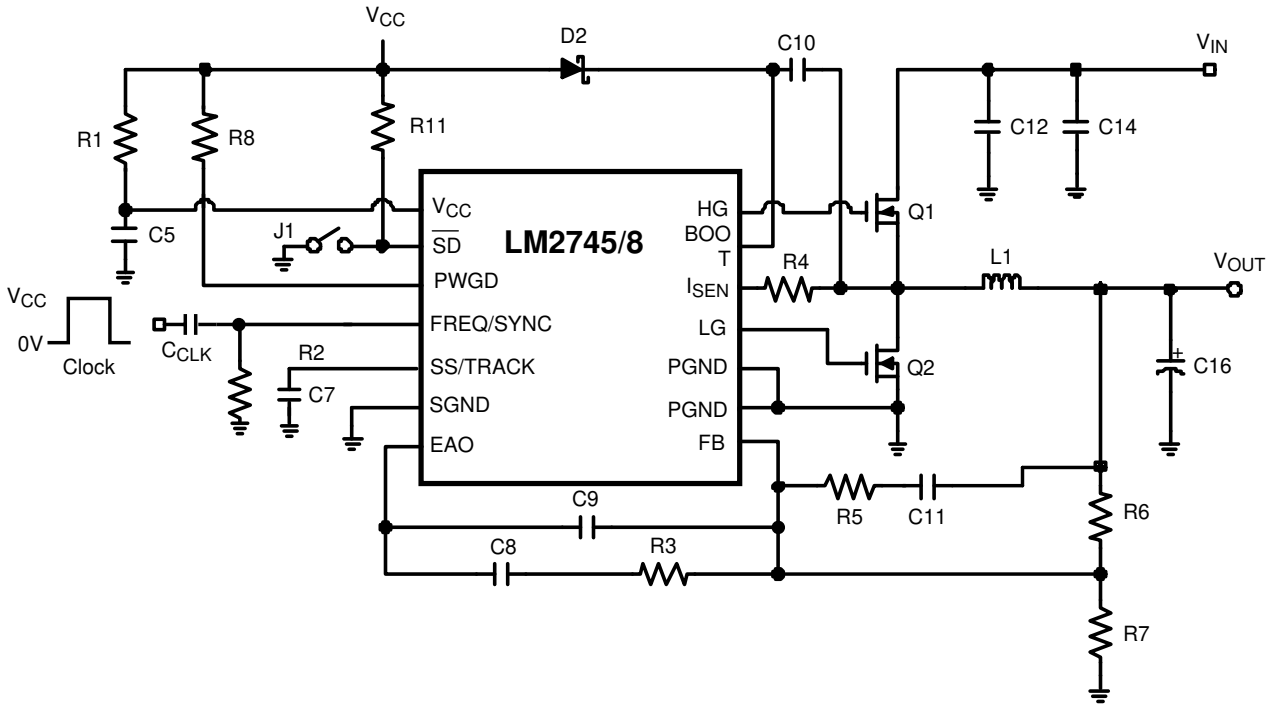

Figure 3-1. Typical Application

4 Performance Characteristics (Output Ripple Voltage and Switch Node Voltage)

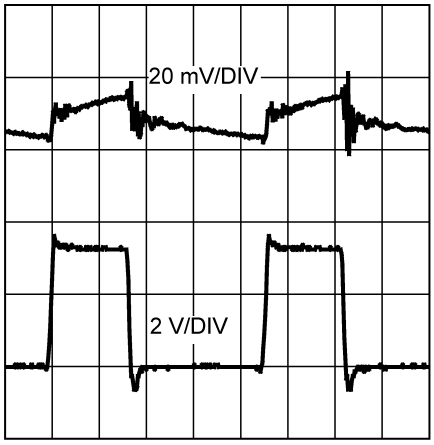

Figure 4-1. V_{IN} = V_{CC} = 3.3 V, V_{OUT} = 1.2 V, I_{LOAD} = 0 A, f_{SW} = 1 MHz, 20-MHz Bandwidth Limit

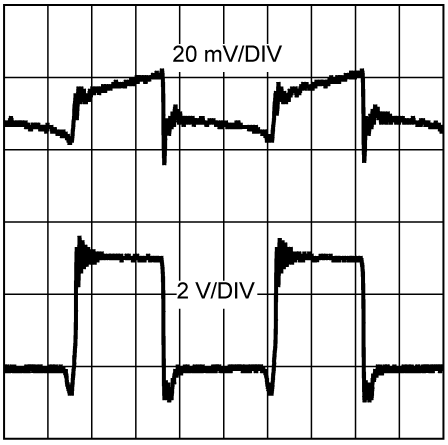

Figure 4-2. V_{IN} = V_{CC} = 3.3 V, V_{OUT} = 1.2 V, I_{LOAD} = 3.5 A, f_{SW} = 1 MHz, 20-MHz Bandwidth Limit

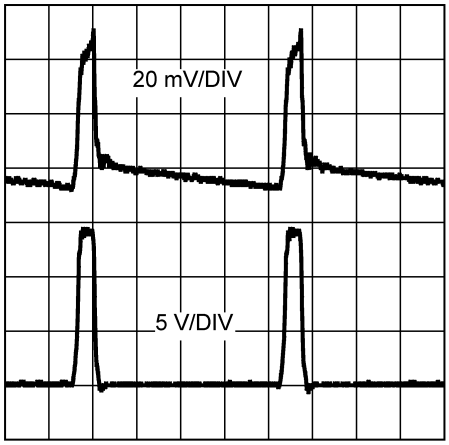

Figure 4-3. V_{IN} = 14 V, V_{CC} = 5 V, V_{OUT} = 1.2 V, I_{LOAD} = 0 A, f_{SW} = 1 MHz, 20-MHz Bandwidth Limit

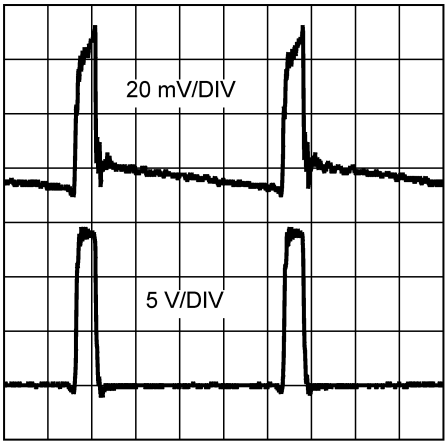

Figure 4-4. V_{IN} = 14 V, V_{CC} = 5 V, V_{OUT} = 1.2 V, I_{LOAD} = 3.5 A, f_{SW} = 1 MHz, 20-MHz Bandwidth Limit

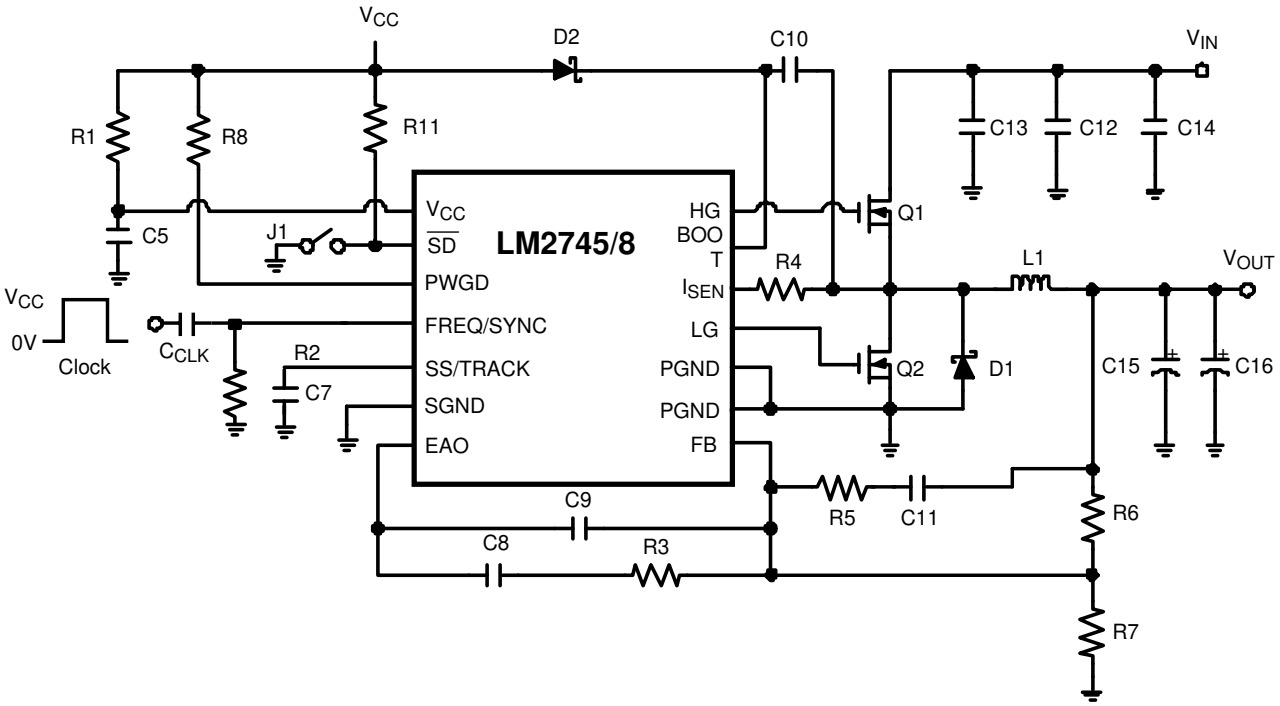

Figure 4-5. Complete Demo Board Schematic

Table 4-1. Bill of Materials (BOM)

Designator	Function	Part Description	Part Number
U1	Controller	LM2745/LM2748 TSSOP14	Texas Instruments
C5	VCC Decoupling	Cer Cap 1 µF 25 V 10% 0805	Murata GRM216R61E105KA12B
C7	Soft Start Cap	Cer Cap 12 nF 25 V 10% 0805	Vishay VJ0805Y123KXX
C8	Comp Cap	Cer Cap 1.5 nF 25 V 10% 0805	Vishay VJ0805Y152KXX
C9	Comp Cap	Cer Cap 18 pF 25 V 10% 0805	Vishay VJ0805A180KAA
C10	Cboot	Cer Cap 0.1 µF 25 V 10% 0805	Vishay VJ0805Y104KXX
C11	Comp Cap	Cer Cap 1.8 nF 25 V 10% 0805	Vishay VJ0805Y182KXX
C12	Input Filter Cap	Cer Cap 10 µF 25 V 10% 1210	AVX 12103D106MAT
C14	Input Filter Cap	Cer Cap 10 µF 25 V 10% 1210	AVX 12103D106MAT
C15	Output Filter Cap	470µF, 6.3 V, 10 mΩ ESR POScap	Sanyo 6TPD470
R1	Filter Resistor	Res 10 Ω .25W 0805	Vishay CRCW08051000F
R2	Frequency Adjust Res	Res18.7 kΩ .25W 0805	Vishay CRCW08052187F
R3	Comp Res	Res 17.4 kΩ .25W 0805	Vishay CRCW08051742F
R4	Current Limit Res	Res 3.16 kΩ .25W 0805	Vishay CRCW08053161F
R5	Comp Res	Res 2.94 kΩ .25W 0805	Vishay CRCW08052941F
R6	Res Divider, upper	Res 10.0 kΩ .25W 0805	Vishay CRCW08051002F
R7	Res Divider, lower	Res 10.0 kΩ .25W 0805	Vishay CRCW08051002F
R8	PWGD Pullup	Res 100 kΩ .25W 0805	Vishay CRCW08051003F
R11	Shutdown Pullup	Res 100 kΩ .25W 0805	Vishay CRCW080561003F
D2	Bootstrap Diode	Schottky Diode, SOD-123	MBR0530LTI
L1	Output Filter Inductor	Inductor 1 µH, 5.3Arms, 10.2 mΩ	Cooper DR73-1R0
Q1-Q2	Top and Bottom FETs	Dual N-MOSFET, V_{DS} = 20 V, 24 mΩ @ 2.5 V	Vishay 9926BDY
C_{CLK}	Sync AC Coupling Cap	Cer Cap 56 pF 25 V 10% 0805	Vishay VJ0805A560KXAA

5 PCB Layout Diagrams

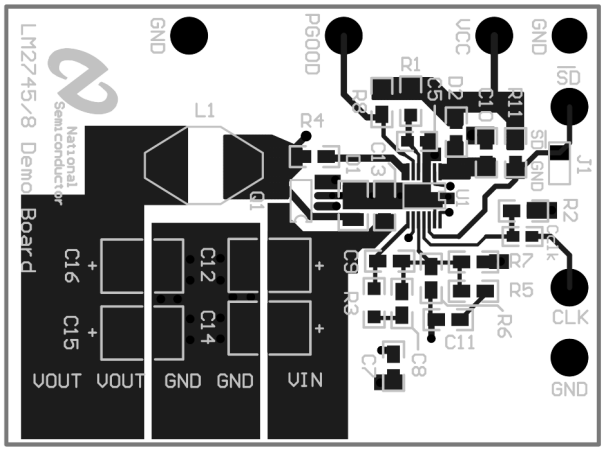

Figure 5-1. Top Layer and Top Overlay

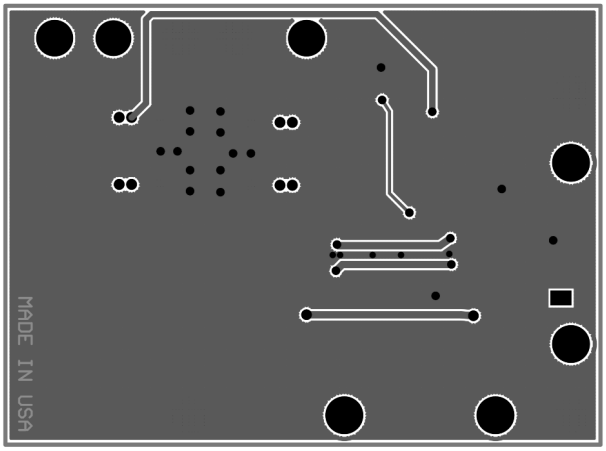

Figure 5-2. Bottom Layer

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2013) to Revision B (February 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title	2

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