

# LM20242 Demonstration Board

National Semiconductor  
LM20242  
CADC Design Group  
November 2007



## 1.0 Design Specifications

Inputs	Output #1
VinMin=8V	Vout1=3.3V
VinMax=18V	Iout1=2A

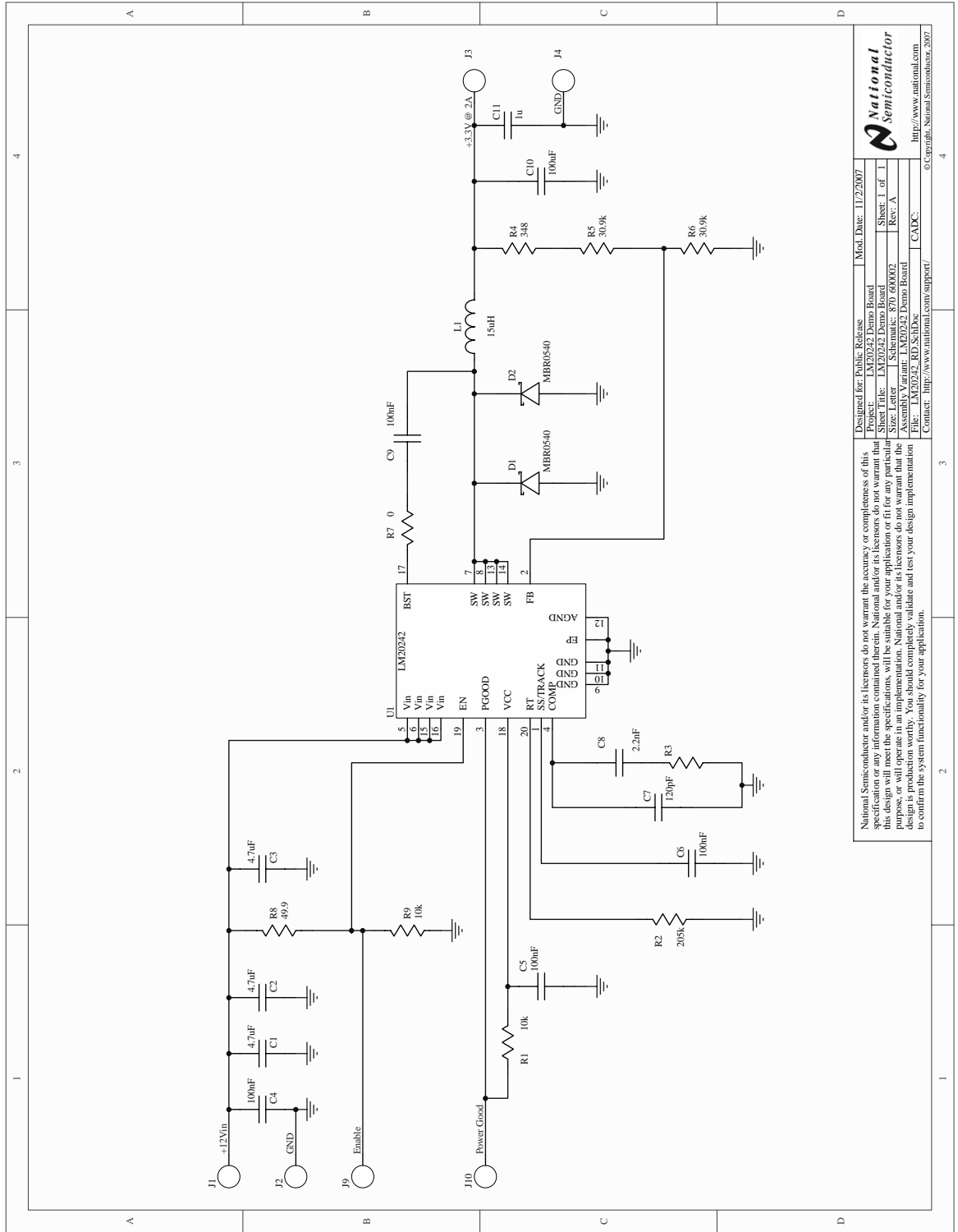
## 2.0 Design Description

The LM20242 demonstration board is designed to provide the design engineer with a small, fully functional buck converter based on Current Mode Control to evaluate the LM20242 switching regulator IC. The demonstration board provides a 3.3V output with 2A current capability. The input voltage ranges from 8V to 18V, and is optimized for 12V. The design operates at 300KHz, a good compromise between conversion efficiency and solution size, and employs a soft-start sequence. The printed circuit board consists of 2 layers of 2 ounce copper on FR4 material with a thickness of 0.062 inches. Refer to the LM20242 datasheet for complete circuit design information.

## 3.0 Features

- Optimized for 12V to 3.3V conversion
- 2A output current, 89% efficiency
- 1.5% output voltage accuracy
- 300 kHz switching frequency
- Current Mode Control
- Starts up into pre-biased loads
- Soft-start set by external capacitor
- Precision enable pin with hysteresis
- OVP, UVLO inputs and PGOOD output
- Internally protected with peak current limit, shutdown and restart
- Accurate current limit with frequency foldback
- Input voltage range 8V to 18V

# 4.0 Schematic



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File: LM20242_RD_SchDoc		Sheet Title: LM20242 Demo Board	
CADC:		Sheet 1 of 1	
Contact: <a href="http://www.national.com/support/">http://www.national.com/support/</a>		Rev: A	
© Copyright, National Semiconductor, 2007		Assembly Variant: LM20242 Demo Board	
		Schematic: 870-000002	

FIGURE 1. Schematic

## 5.0 Bill of Materials

Designator	Comp Type	Value	Footprint	Parameters	Vendor	PartNumber
C1, C2, C3	Capacitor	4.7uF	1210	Ceramic, X7R, 50V, 10%	MuRata	GRM32ER71H475K
C4	Capacitor	100nF	0805	Ceramic, X7R, 100V, 10%	TDK	C2012X7R2A104K
C5, C6, C9	Capacitor	100nF	0603	Ceramic, X7R, 16V, 10%	MuRata	GRM188R71C104KA01D
C7	Capacitor	120pF	0603	Ceramic, C0G, 50V, 5%	AVX	06035A121JAT2A
C8	Capacitor	2.2nF	0603	Ceramic, X7R, 50V, 10%	MuRata	GRM188R71H222KA01D
C10	Capacitor	100uF	1210	Ceramic, X7R, 6.3V, 20%	TDK	C3225X5R0J107M
C11	Capacitor	1uF	0805	Ceramic, X7R, 50V, 10%	MuRata	GRM21BR71H105KA12L
D1, D2	Diode		SOD-123	Vr = 40V, Io = 0.5A, Vf = 0.51V	Fairchild	MBR0540
J1, J2, J3, J4	Terminal		TURRET		Keystone	1503-2
J9, J10	Test Point		TESTPOINT		Keystone	5002
L1	Inductor	15uH	MSS1278	Shielded Drum Core, 6.5A, 0.038Ohm	Coilcraft Inc.	MSS1278-153
R1, R9	Resistor	10kΩ	0603	1%, 0.1W	Vishay	CRCW06031002F
R2	Resistor	205kΩ	0603	1%, 0.1W	Vishay	CRCW06032053F
R3	Resistor	12.1kΩ	0603	1%, 0.1W	Vishay	CRCW06031212F
R4	Resistor	348Ω	0603	1%, 0.1W	Vishay	CRCW0603348RF
R5, R6	Resistor	30.9kΩ	0603	1%, 0.1W	Vishay	CRCW06033092F
R7	Resistor	0Ω	0603	0%, 0.1W	Vishay	CRCW0603000Z0EA
R8	Resistor	49.9Ω	0603	1%, 0.1W	Vishay	CRCW06034992F
U1	Switcher		MXA20A		National Semiconductor	LM20242

## 6.0 Other Operating Values

Operating Values

Description	Parameter	Value	Unit
Steady State Efficiency	Efficiency	89	%
Input Voltage	V <sub>in</sub>	12	V
Load Current	I <sub>out</sub>	2	A
Load Regulation		0.1	%
Line Regulation		0.1	%

## 7.0 Board Photos



boardphoto1

FIGURE 3. LM20242 Demo Board Photo

## 8.0 Quick Start

### Powering and Loading Considerations

Read this entire section prior to attempting to power the demonstration board.

#### QUICK SETUP PROCEDURE

##### Step 1:

Set the input voltage source current limit to 2A. Turn off the input source. Connect the positive output of the input voltage source to J1 and the negative output to J2.

##### Step 2:

Connect the load, with 2A capability, to J3 for the positive output voltage connection and J4.

##### Step 3:

The ENABLE pin, J9, should be left open for normal operation.

##### Step 4:

Set the input voltage source to 12V and the load to 0.1A. The load voltage should be in regulation with a nominal 3.3V output.

##### Step 5:

Slowly increase the load while monitoring the load voltage at J3 and J4. It should remain in regulation with a nominal 3.3V output as the load is increased up to 2A.

##### Step 6:

Slowly sweep the input source voltage from 12V to 18V. The load voltage should remain in regulation with a nominal 3.3V output.

##### Step 7:

Temporarily short the ENABLE pin (J9) to GND (J2 or J4) to check the shutdown function.

##### Step 8:

Increase the load beyond the normal range to check current limiting while the input source is set to 12V. The output current should limit at approximately 3.9A. The input source current limit should be increased for this step. Fan cooling is critical during this step.

#### AIR FLOW

Prolonged operation at full power and high ambient temperature will cause the thermal shutdown circuit within the regulator IC to activate. A fan with a minimum of 200 LFM should always be provided.

#### POWERING UP

Using the ENABLE pin (J9) provided will allow powering up the input source with the current level set low. It is suggested that the load power be kept low during the first power up. Set the current limit of the input source to provide about 1.5 times the anticipated wattage of the load. As you remove the connection from the ENABLE pin to GND (J2), immediately check for 3.3V at the output. A quick efficiency check is the best way to confirm that everything is operating properly. If something

is amiss you can be reasonably sure that it will affect the efficiency adversely. Few parameters can be incorrect in a switching power supply without creating losses and potentially damaging heat.

#### OVER CURRENT PROTECTION

The demonstration board is configured with peak over-current protection. This function is completely contained in the LM20242.

#### POWER GOOD

A POWER GOOD pin (J10) has been provided on the demonstration board. This pin can be used to monitor the output voltage status. Refer to the LM20242 datasheet for complete information.

#### BUCK TOPOLOGY

An excellent introduction to the buck converter is available on the National Semiconductor website. The Application Notes AN-1197 and AN-1253 discuss both output inductor selection and considerations for wide input voltage range designs when using buck converters.

## 9.0 Layouts

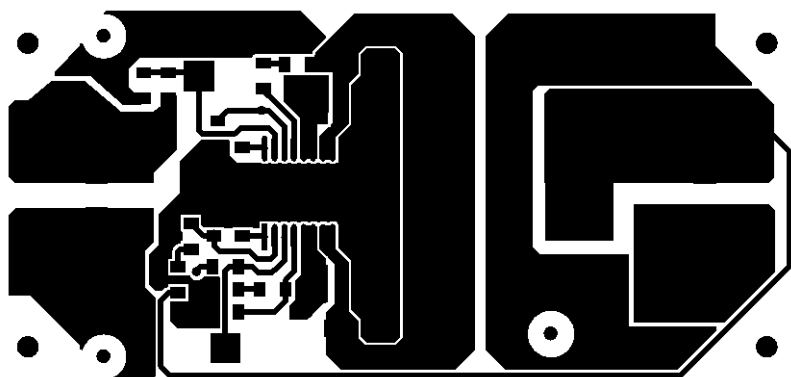


FIGURE 4. Top Layer

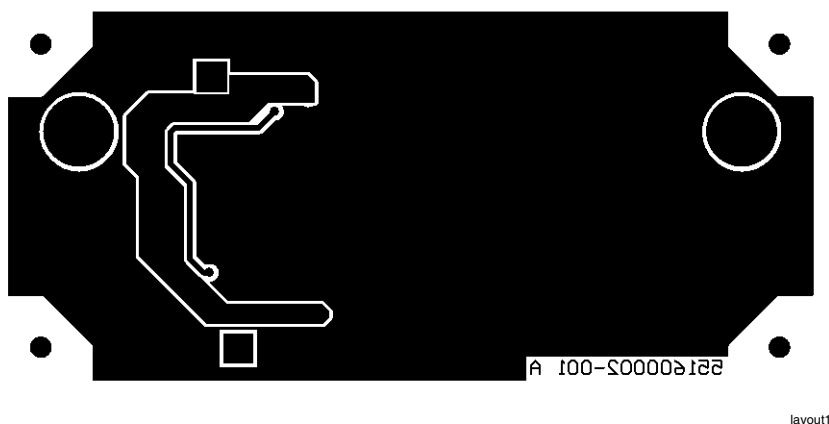
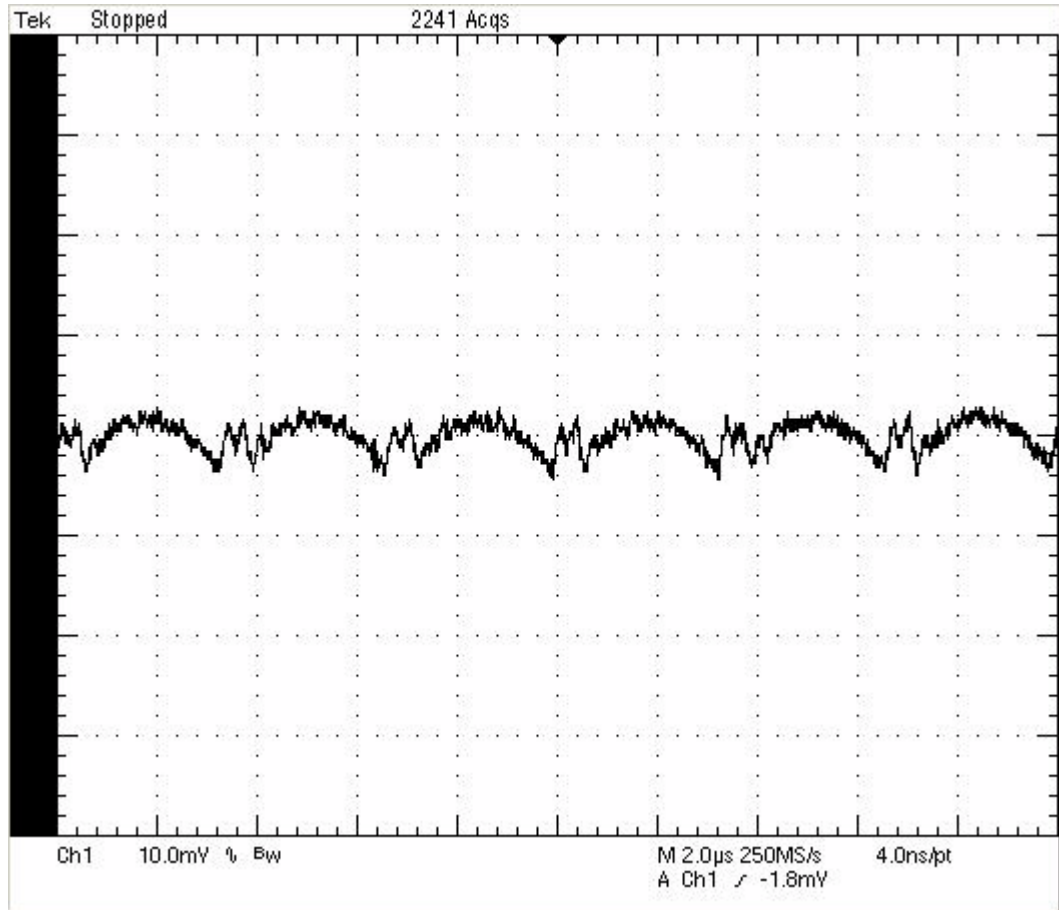


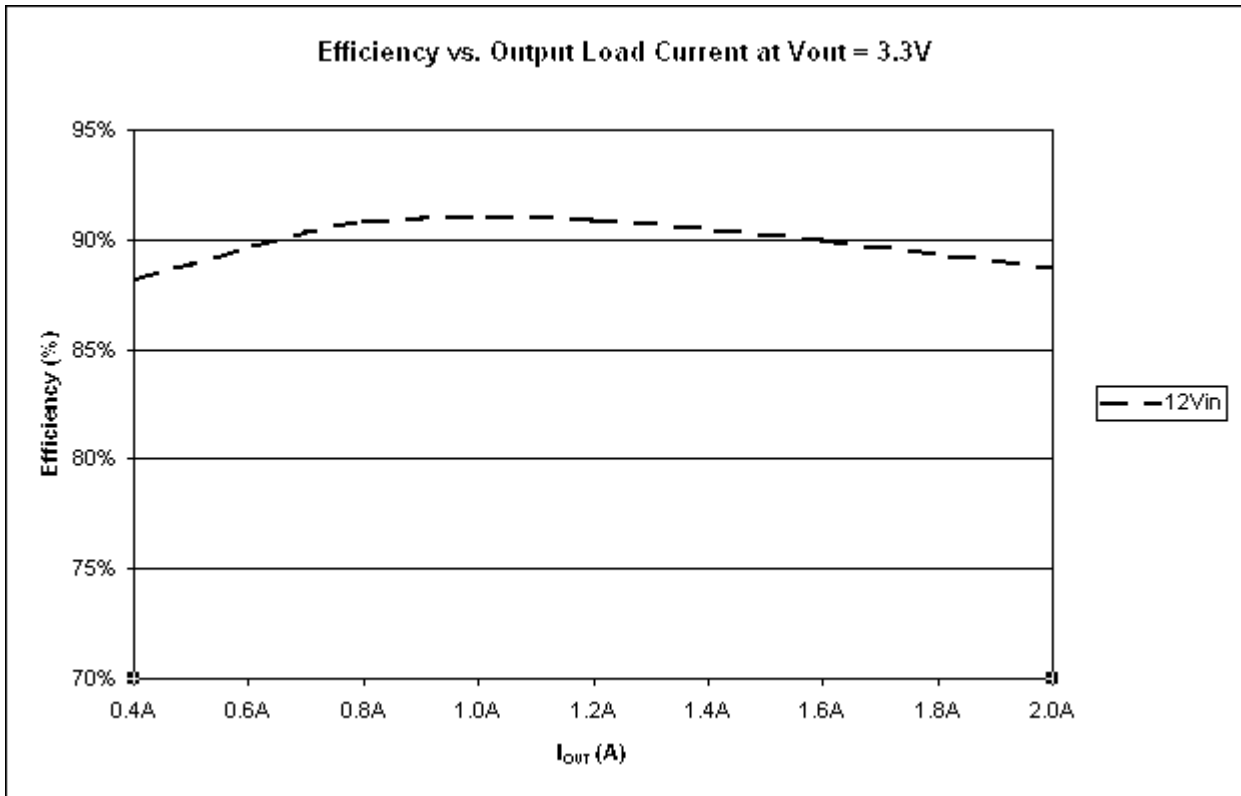
FIGURE 5. Bottom Layer

## 10.0 Waveforms



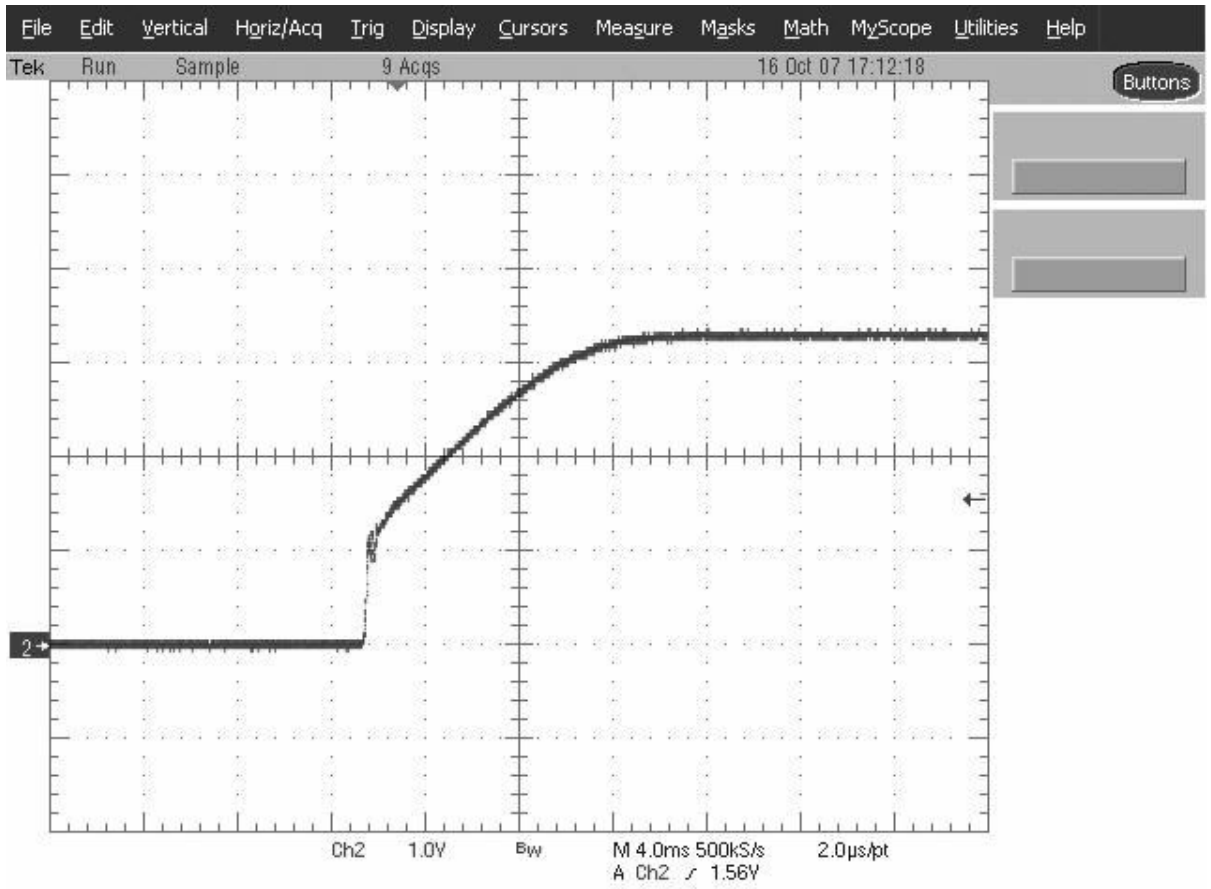
waveform17

**FIGURE 6.** shows the output voltage ripple. Input Voltage = 12VDC, Output Current = 2A. This measurement was taken with the scope probe tip placed on the J3 load terminal and the scope probe ground barrel pushed against the J4 load terminal. The scope bandwidth is set to 20MHz



waveform6

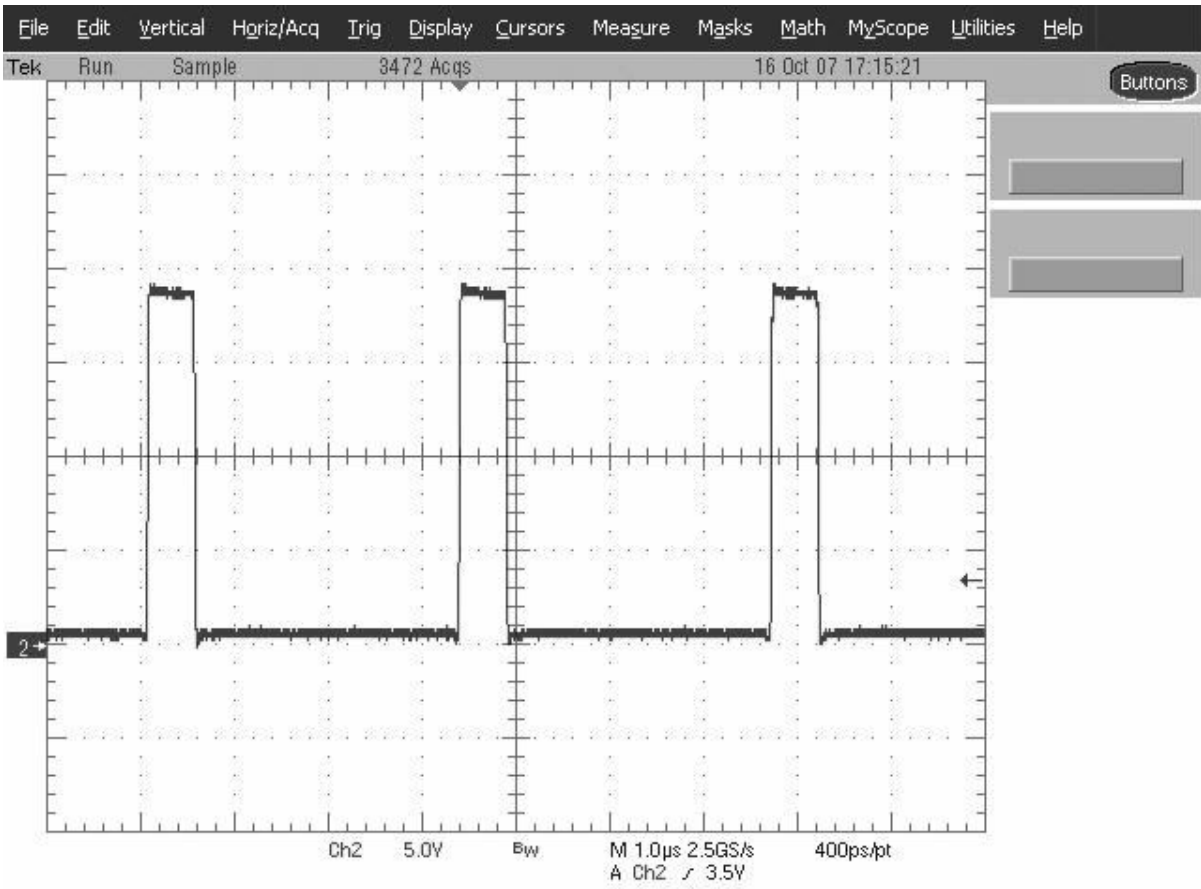
FIGURE 7. shows the conversion efficiency versus output at Vin = 12V



waveform20

**FIGURE 8. Output voltage during a typical start-up sequence.**

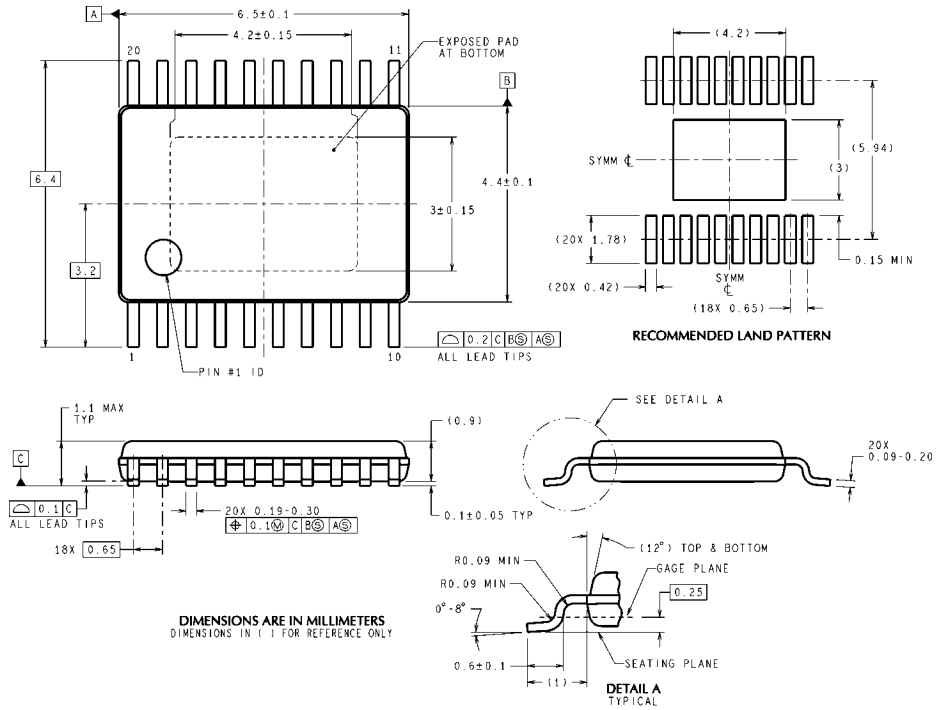




waveform21

**FIGURE 9.** shows the typical primary voltage during continuous conduction mode (CCM).

# 11.0 Physical Dimensions inches (millimeters) unless otherwise noted



MXA20A (Rev C)

# Notes

LM20242

## Notes

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