User's Guide

LM63460-Q1 and LM64460-Q1 EVM User's Guide

ABSTRACT

The LM63460EVM-2MHZ and LM64460EVM-2MHZ evaluation modules (EVMs) are specifically designed to conveniently evaluate the performance of the LM63460-Q1 and LM64460-Q1 synchronous buck converters, respectively. As shown in Table 1-1, both converters are available in a 22-pin Enhanced HotRod™ QFN package.

Table 1-1. Device and Package Configuration

REF DES	CONVERTER IC	OUTPUT CURRENT	PACKAGE
U1	LM63460-Q1	6 A	22-pin wettable-flank Enhanced HotRod QFN package, 3.5 mm × 4 mm × 1 mm
	LM64460-Q1	6 A	

Both EVMs provide a 5-V output voltage at up to 6-A load current with exceptional efficiency and output accuracy in a very small solution size. The EVMs showcase a recommended PCB layout that is optimized specifically for EMI and thermal performance. Input and output voltage sense terminals and a test point header facilitate measurement of key parameters such as efficiency and power dissipation, line and load regulation, enable ON/OFF, and bode plot performance. The header also provides connections for synchronization (SYNC) and power-good (PGOOD) device features. The EVMs share a common schematic and layout – the main differences being the converter IC and the connections for setting the switching freqeuncy (either with an RT resistor or by external clock synchronization).

> Refer to the LM63460-Q1 and LM64460-Q1 data sheets, LM6k Quickstart Calculator, and WEBENCH® Power Designer for additional guidance pertaining to converter modes of operation, component selection, and expected performance.

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1 High-Density EVM Description

The LM63460EVM-2MHZ and LM64460EVM-2MHZ feature the LM63460-Q1 and LM64460-Q1 synchronous buck converters, respectively. The EVMs provide the full 6-A output current rating of these converters, and a wide-V_{IN} range of 3 V to 36 V offers outsized voltage rating and operating margin to withstand automotive supply-rail voltage transients.

The selected input capacitors accommodate the entire range of input voltage and are available from multiple component vendors. Input and output voltage sense terminals and a test point header facilitate measurement of the following:

- Efficiency and power dissipation
- Line and load regulation
- Load transient response
- Enable ON/OFF
- Bode plot (crossover frequency and phase margin)

The 8-pin header also provides connections for enable (EN), external clock synchronization (SYNC), and power-good (PGOOD) features. The recommended PCB layout maximizes thermal performance and minimizes output ripple and noise. The EVMs share a common PCB layout, whereas the BOMs have minor differences in installed components. The main differences between the ICs relate to pins 7 and 8, which are EN/SYNC and RT for the LM63460-Q1 and EN and MODE/SYNC for the LM64460-Q1, respectively.

1.1 Typical Applications

- Automotive infotainment and cluster: head unit, media hub, USB charge, display
- Automotive ADAS and body electronics
- Inverting buck-boost (IBB) circuits requiring negative output voltage

1.2 Features and Electrical Performance

- Complete 6-A buck power stage with integrated power MOSFETs and PWM controller
- Wide input voltage operating range of 3 V to 36 V (absolute maximum rating of 42 V)
  - Input voltage UVLO turn-on and turn-off thresholds set at 4.5 V and 3.2 V, respectively
- Default output voltage and switching frequency of 5 V and 2.1 MHz, respectively. The LM63460-Q1 has a resistor-programmable switching frequency from 200 kHz to 2.2 MHz using its RT pin, whereas the LM64460-Q1 has a default frequency of 2.1 MHz but is synchronizable over the same range.
- High efficiency across a wide load-current range
  - Half-load and full-load efficiencies of 94.4% and 92.5% at V_{IN} = 13.5 V
  - External bias option reduces no-load supply current and enhances thermal performance
- Improved EMI performance for noise-sensitive automotive applications
  - Meets CISPR 25 Class 5 EMI standard for both conducted and radiated emissions
  - Input π-stage EMI filter with electrolytic capacitor for parallel damping
  - Parallel input and output paths with symmetrical capacitor layouts minimize radiated field coupling
  - Clock synchronization and optional FPWM mode provide constant switching frequency across the full load range
  - Integrated input, VCC, and bootstrap capacitors enable low-noise switching performance
  - Pseudo-random spread spectrum modulation (PRSS) for lower peak emissions
    - Included by default in the LM63460-Q1
    - Configurable in the LM64460-Q1 – connect the MODE/SYNC pin of the IC to VCC or GND to enable spread spectrum in FPWM and auto modes, respectively.
- Peak current-mode control architecture enables fast line and load transient response
  - Integrated loop compensation components and frequency-proportional slope compensation
- Inherent protection features for robust and reliable design
  - Overcurrent protection (OCP) with peak and valley current limits
  - Thermal shutdown protection with hysteresis
  - PGOOD indicator with 100-kΩ pullup resistor to VOUT
  - Resistor-programmable input voltage UVLO
- Fully assembled, tested and proven, 4-layer PCB layout with 76-mm × 38-mm total footprint

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2 EVM Performance Specifications

Unless otherwise indicated, V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 6 A and F_{SW} = 2.1 MHz

Table 2-1. Electrical Performance Specifications

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage range, V_{IN}	Operating		5.5		36	V
Input voltage turn-on, $V_{IN(on)}$	Adjusted using EN divider resistors			4.5		
Input voltage turn-off, $V_{IN(off)}$				3.2		
Input voltage hysteresis, $V_{IN(hys)}$				1.3		
Input current, disabled, $I_{IN(off)}$	V_{EN} = 0 V (with 255-kΩ and 100-kΩ EN divider)			39		µA
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT} (1)	Adjustable from 1 V to 95% VIN		4.95	5.0	5.05	V
Output current, I_{OUT}	V_{IN} = 6 V to 36 V (2)		0		6	A
Output voltage regulation, ΔV_{OUT}	Load regulation	I_{OUT} = 0 A to 6 A		0.1%		
	Line regulation	V_{IN} = 6 V to 36 V		0.1%		
Output voltage ripple, $V_{OUT(AC)}$				25		mVrms
Output overcurrent protection, $I_{OUT(OCP)}$				8.5		A
SYSTEM CHARACTERISTICS						
Default switching frequency, $F_{SW(nom)}$	Adjustable from 200 kHz to 2.2 MHz (with suitable choice of buck inductance and input/ouptut capacitance at lower F_{SW})			2.1		MHz
Efficiency, η(1)	V_{IN} = 8 V	I_{OUT} = 3 A		95%		
		I_{OUT} = 6 A		92%		
	V_{IN} = 13.5 V	I_{OUT} = 3 A		94.5%		
		I_{OUT} = 6 A		92.5%		
	V_{IN} = 18 V	I_{OUT} = 3 A		93%		
		I_{OUT} = 6 A		91.7%		
	V_{IN} = 24 V	I_{OUT} = 3 A		91.4%		
		I_{OUT} = 6 A		90.6%		
Thermal impedance, $R_{\theta JA}$				23		°C/W
Junction temperature, T_J			–40		150	°C

(1) The default output voltage and switching frequency of this EVM are 5 V and 2.1 MHz, respectively. The BIAS pin connects to the output for output voltages of 3.3 V and above. Efficiency and other performance metrics can change based on operating input voltage, load current, switching frequency, external bias voltage, ambient temperature, externally connected output capacitance, and other parameters.

(2) The recommended airflow is 200 LFM when operating at output currents greater than 4 A.

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3 EVM Photo

Figure 3-1 highlights the buck converter power stage and the various connection interfaces associated with the EVM. Use terminal blocks J1 and J2 to connect the input supply and load, respectively. These terminal blocks accept up to 16-AWG wire thickness.

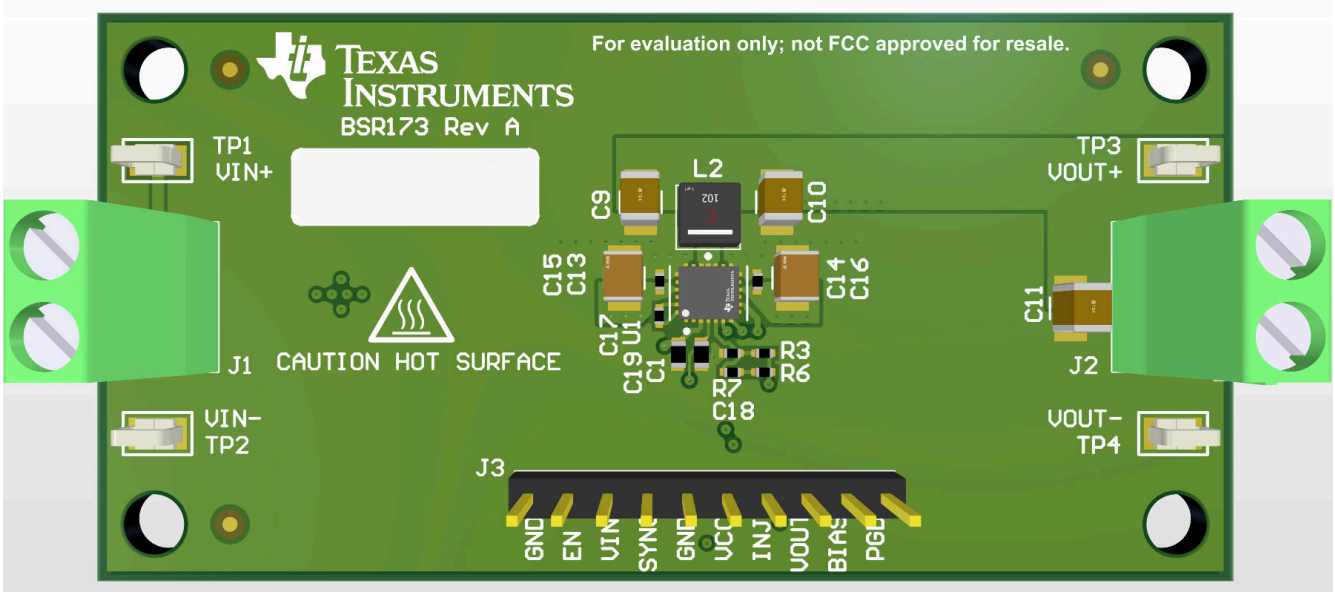

Figure 3-1. BSR173 EVM Photo

CAUTION

Caution Hot surface.
Contact may cause burns.
Do not touch.

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4 Test Setup and Procedure

4.1 EVM Connections

Referencing the EVM connections described in Table 4-1, use the recommended test setup in Figure 4-1 to evaluate the LM63460-Q1 and LM64460-Q1 converter. Working at an ESD-protected workstation, make sure that any wrist straps, bootstraps, or mats are connected and referencing the user to earth ground before power is applied to the EVM.

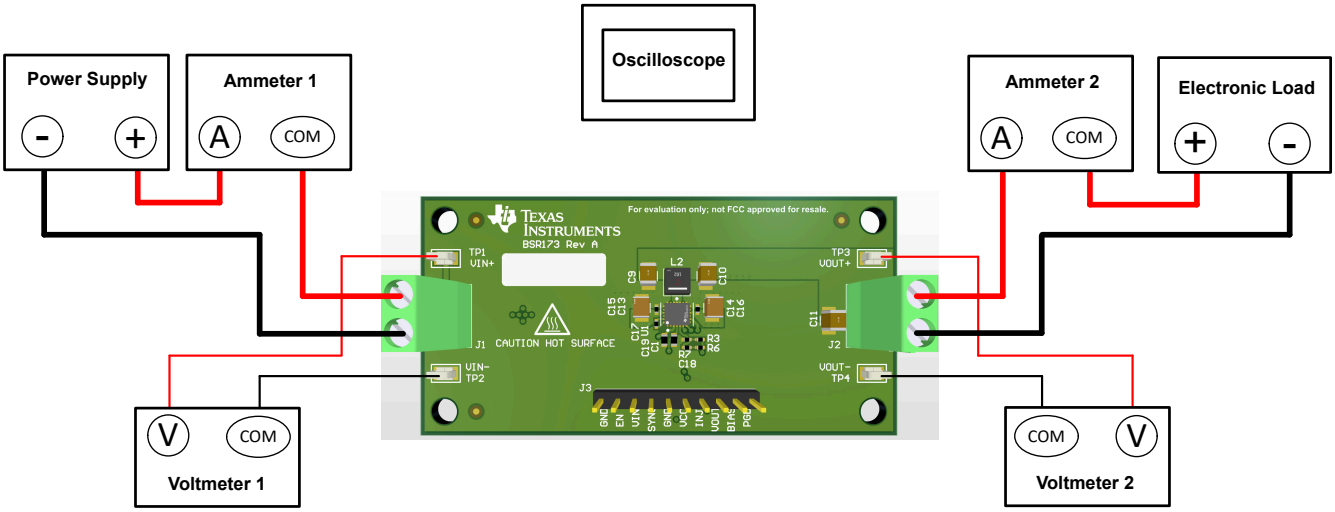

Figure 4-1. EVM Test Setup

Table 4-1. EVM Power Connections

LABEL	DESCRIPTION
VIN+	Positive input power connection
VIN–	Negative input power connection
VOUT+	Positive output power connection
VOUT–	Negative output power connection

Table 4-2. EVM Signal Connections

LABEL(1)	DESCRIPTION
VIN+ (TP1)	Positive input sense terminal. Connect the multimeter positive lead for measuring efficiency.
VIN– (TP2)	Negative input sense terminal. Connect a multimeter negative lead for measuring efficiency.
VOUT+ (TP3)	Positive output sense terminal. Connect a multimeter positive lead for measuring efficiency and line/load regulation.
VOUT– (TP4)	Negative output sense terminal. Connect the multimeter negative lead for measuring efficiency and line/load regulation.
GND	Ground reference point at J3
EN	Precision enable input. Tie EN to GND to disable the regulator. Use a logic signal to control EN for remote ON/OFF functionality. Leave EN open for UVLO turn-on threshold set at 4.5 V.
SYNC	Synchronization input (connects to the EN/SYNC or MODE/SYNC pins of the LM63460-Q1 and LM64460-Q1, respectively). Connect a valid clock signal to synchronize the switching frequency from 200 kHz to 2.2 MHz.
VCC	VCC output
PGD	Power-good monitor output. This is an open-drain flag with a 100-kΩ pullup resistor to VOUT.
INJ, VOUT	Bode plot measurement and signal injection using a 50-Ω resistor from INJ to VOUT
BIAS	External bias supply connection. A 1-Ω resistor from VOUT to BIAS simplifies bias current measurement.

(1) Refer to the LM63460-Q1 or LM64460-Q1 data sheets for absolute maximum ratings associated with the features in this table.

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4.2 EVM Setup

- Use the VIN+ and VIN– test points along with the VOUT+ and VOUT– test points located near the power terminal blocks as voltage monitoring points where voltmeters are connected to measure the input and output voltages, respectively. *Do not use these sense terminals as the input supply or output load connection points.* The PCB traces connected to these sense terminals are not designed to support high currents.
- Header J3 provides access to the following test points:
  - VIN
  - EN
  - SYNC
  - VCC
  - PGD
  - BIAS
  - VOUT
  - INJ

  The SYNC test point provides a convenient location to connect an external clock signal. The power-good (PGD) test point is available to monitor when a valid output voltage is present on the EVM. Refer to Section 4.1 for specific information related to the various test points.

Note

The default switching frequency of the EVM is 2.1 MHz. Adjust the switching frequency by applying a clock signal at the SYNC test point. Note that lower frequency can necessitate a change in buck inductance to maintain a recommended 30% to 50% inductor peak-to-peak ripple current and optimal internal slope compensation contribution. Refer to the LM63460-Q1 or LM64460-Q1 data sheets, LM63k-LM64k Quickstart Calculator, and WEBENCH® Power Designer for additional guidance related to converter operation and component selection..

4.3 Test Equipment

Voltage Source: The input voltage source V_{IN} should be a 36-V variable DC source capable of supplying 6 A.

Multimeters:

- **Voltmeter 1:** Measure the input voltage at VIN+ to VIN–.
- **Voltmeter 2:** Measure the output voltage at VOUT+ to VOUT–.
- **Ammeter 1:** Measure the input current. Set the ammeter to 1-second aperture time.
- **Ammeter 2:** Measure the output current. Set the ammeter to 1-second aperture time.

Electronic Load: Use an electronic load set to constant-resistance (CR) or constant-current (CC) mode and capable of 0 ADC to 6 ADC. For a no-load input current measurement, disconnect the electronic load as it can draw a small residual current.

Oscilloscope: With the scope set to 20-MHz bandwidth and AC coupling, measure the output voltage ripple directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the ground barrel of the probe through the ground lead to the negative terminal of the capacitor. TI does not recommend using a long-leaded ground connection because this can induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

Safety: Always use caution when touching any circuits that can be live or energized.

4.4 Recommended Test Setup

4.4.1 Input Connections

- Prior to connecting the DC input source, set the current limit of the input supply to 0.1-A maximum. Ensure the input source is initially set to 0 V and connected to the VIN+ and VIN– connection points as shown in Figure 4-1.
- Connect voltmeter 1 at VIN+ and VIN– sense terminals (adjacent to J1) to measure the input voltage.
- Connect ammeter 1 to measure the input current and set it to at least a 0.1-second aperture time.

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4.4.2 Output Connections

- Connect an electronic load to the VOUT+ and VOUT– connections as shown in Figure 4-1. Set the load to constant-resistance mode or constant-current mode at 0 A before applying input voltage.
- Connect voltmeter 2 at VOUT+ and VOUT– sense terminals (adjacent to J2) to measure the output voltage.
- Connect ammeter 2 to measure the output current.

4.5 Test Procedure

4.5.1 Line/Load Regulation and Efficiency

- Set up the EVM as described in Section 4.
- Set load to constant resistance or constant current mode to sink 0 A.
- Increase the input source voltage from 0 V to 13.5 V; use voltmeter 1 to measure the input voltage.
- Increase the current limit of the input supply to 6 A.
- Use voltmeter 2 to measure the output voltage, V_{OUT}, and vary the load current from 0 A to 6 A DC; V_{OUT} should remain within the load regulation specification. For optimal accuracy, measure the output voltage at the output capacitors close to the converter.
- Set the load current to 3 A (50% rated load) and vary the input source voltage from 6 V to 24 V; V_{OUT} should remain within the line regulation specification.
- Set the load current to 6 A (100% rated load) and measure the efficiency at typical input voltages (8 V, 12 V, 13.5 V, and 18 V cover the automotive battery voltage range).
- Decrease the load to 0 A. Decrease the input source voltage to 0 V.

CAUTION

Extended operation at high output current can raise component temperatures above 55°C. To avoid risk of a burn injury, do not touch the components until they have cooled sufficiently after disconnecting power.

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5 Test Data and Performance Curves

Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements. Unless otherwise indicated, V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 6 A, and F_{SW} = 2.1 MHz.

5.1 Conversion Efficiency

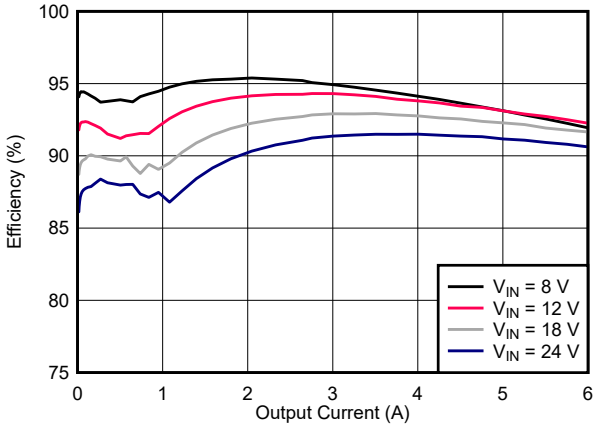

Figure 5-1. Auto Mode, Linear Scale

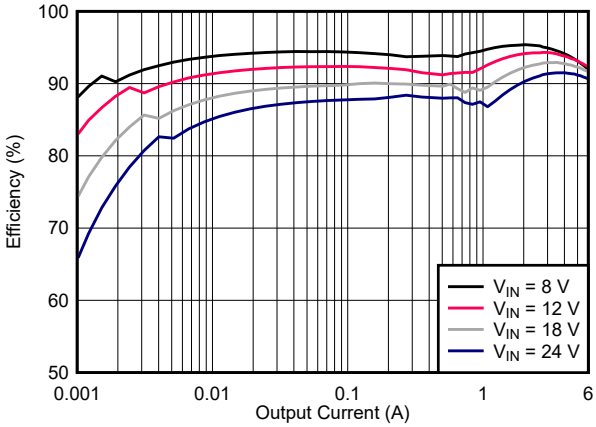

Figure 5-2. Auto Mode, Log Scale

5.2 Output Voltage Regulation

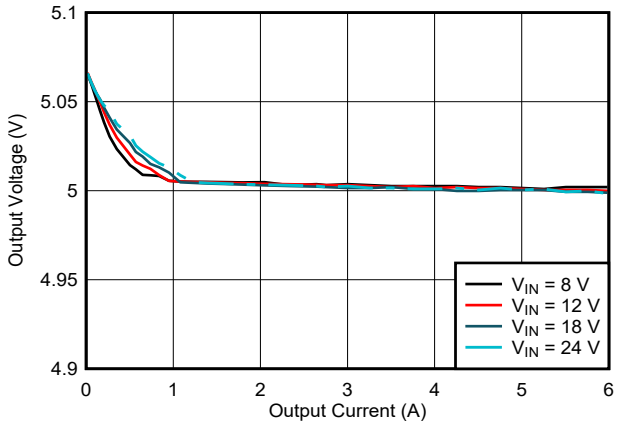

Figure 5-3. Load and Line Regulation

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5.3 Operating Waveforms

5.3.1 Start-Up and Enable ON/OFF

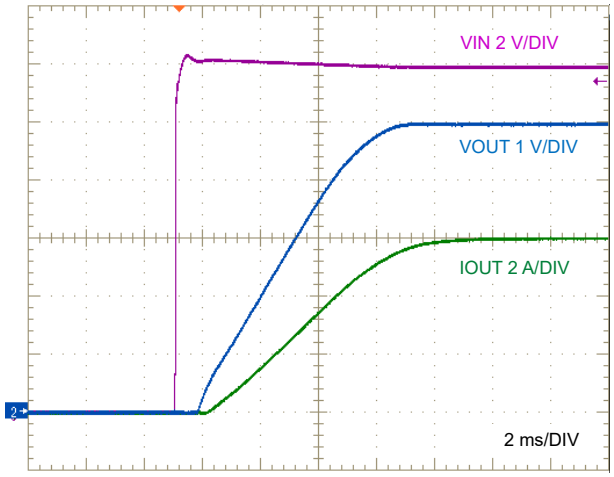

Figure 5-4. Start-Up, 6-A Resistive Load

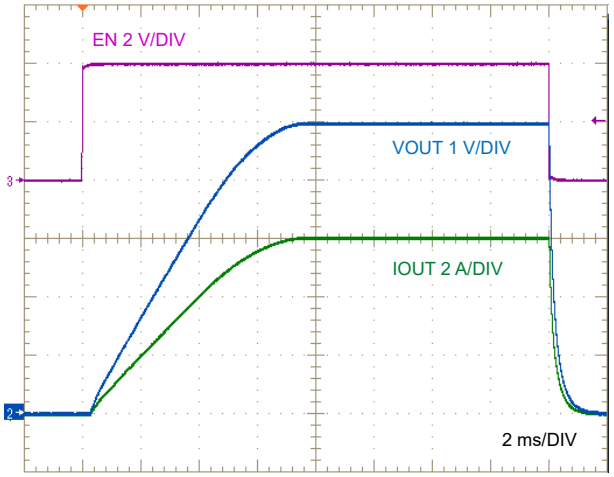

Figure 5-5. Enable ON/OFF, 6-A Resistive Load

5.3.2 Line and Load Transients

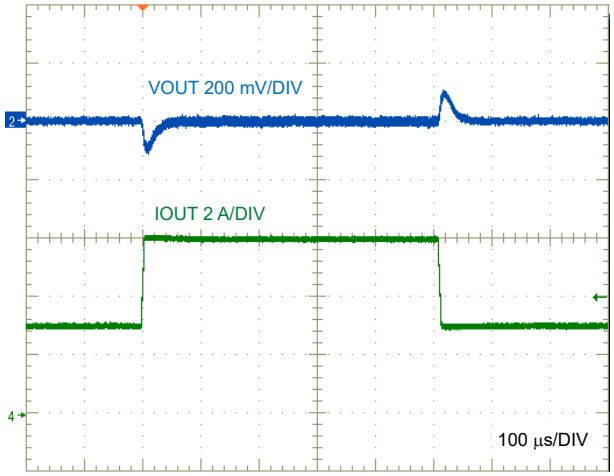

Figure 5-6. Load Transient, 3 A to 6 A

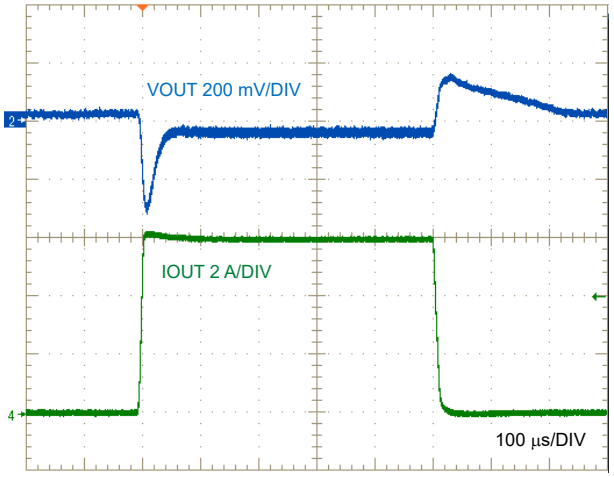

Figure 5-7. Load Transient, 0 A to 6 A

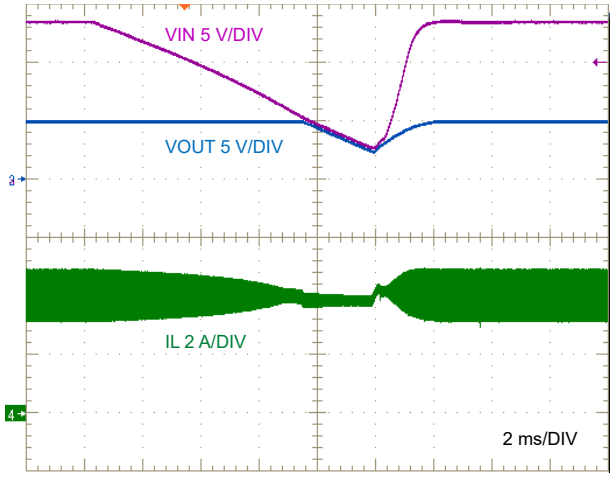

Figure 5-8. Line Transient and Dropout Recovery

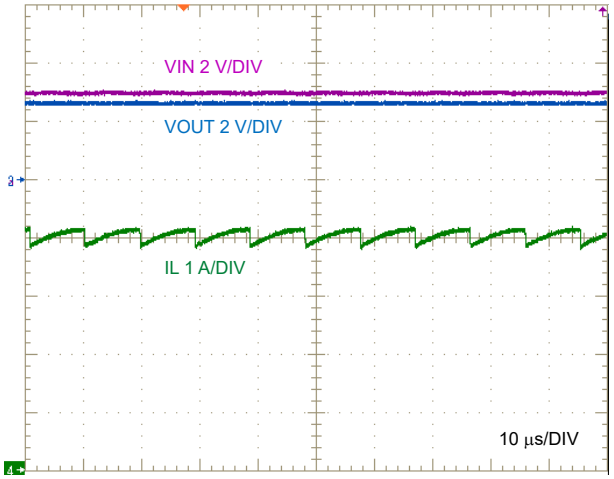

Figure 5-9. Frequency Foldback at V_{IN} = 3 V

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5.3.3 Short Circuit and Recovery

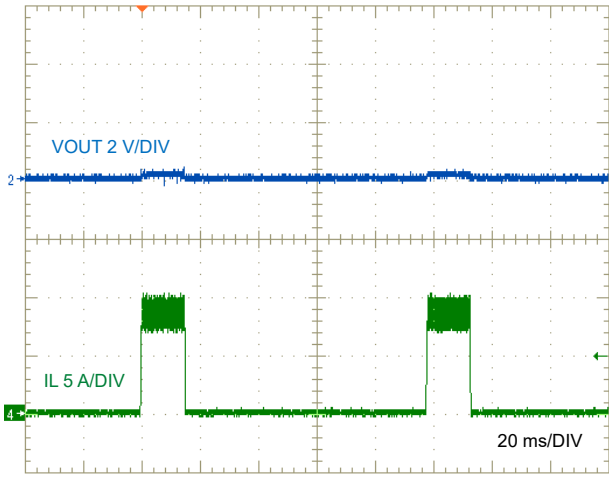

Figure 5-10. Short Circuit Hiccup

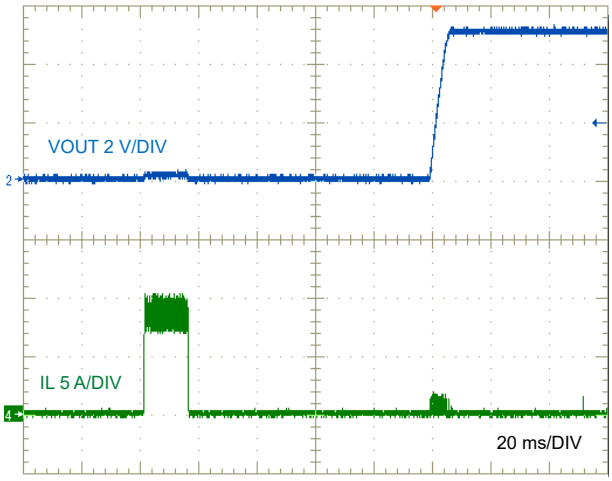

Figure 5-11. Short Circuit Recovery to No Load

5.4 Thermal Performance

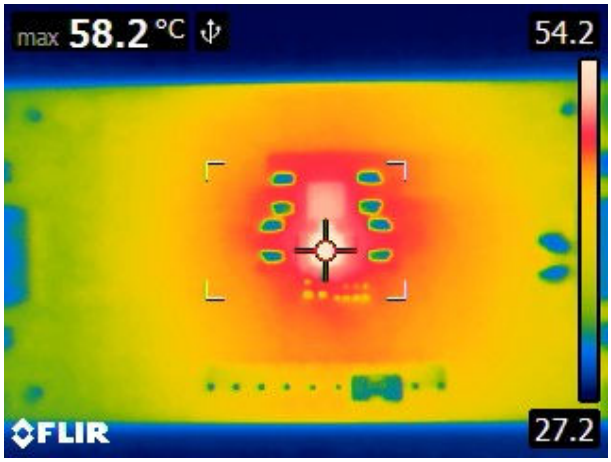

Figure 5-12. IR Thermal Image, 4-A Load

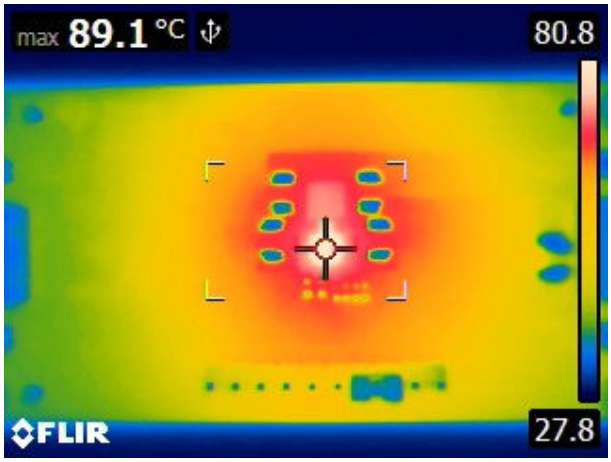

Figure 5-13. IR Thermal Image, 6-A Load

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5.5 EMI Results – CISPR 25 Class 5

5.5.1 Conducted EMI

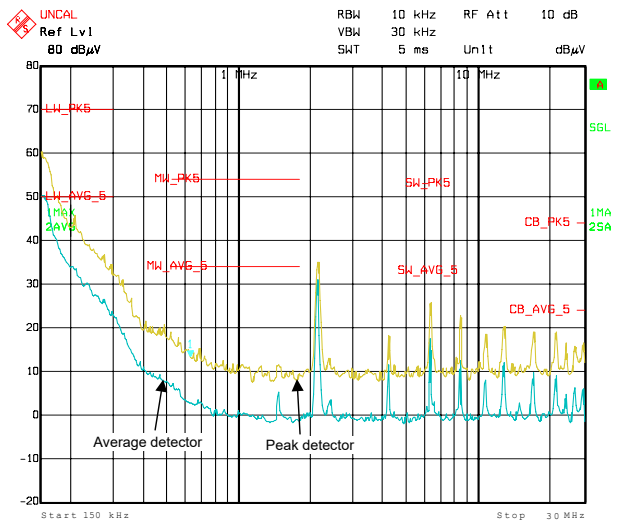

Figure 5-14. Conducted EMI, 150 kHz to 30 MHz

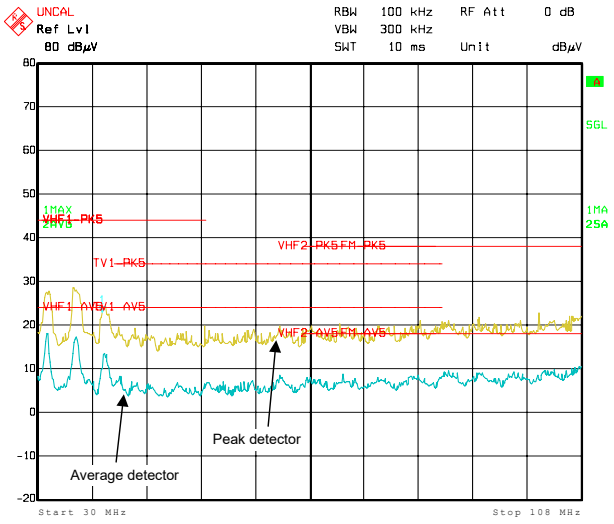

Figure 5-15. Conducted EMI, 30 MHz to 108 MHz

5.5.2 Radiated EMI

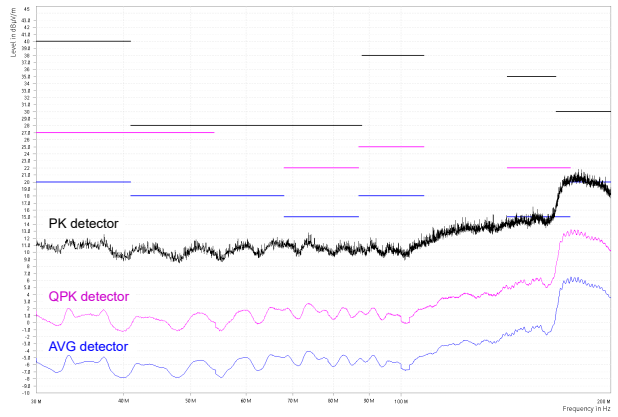

Figure 5-16. CISPR 25 Class 5 Radiated EMI, Bicon Antenna, Horizon. Polarization, 30 MHz to 200 MHz

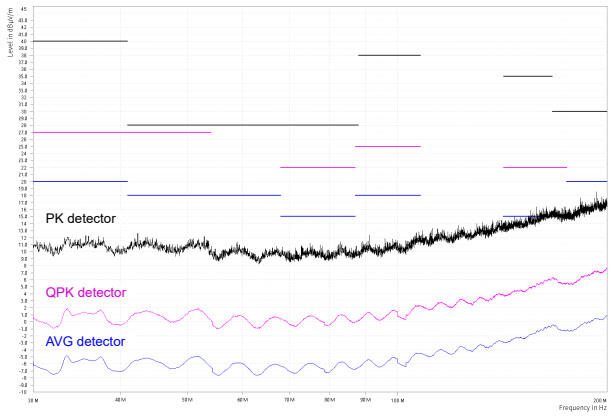

Figure 5-17. CISPR 25 Class 5 Radiated EMI, Bicon Antenna, Vertical Polarization, 30 MHz to 200 MHz

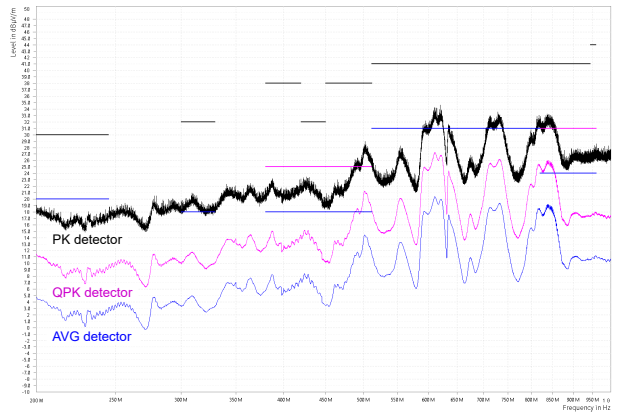

Figure 5-18. CISPR 25 Class 5 Radiated EMI, Log Antenna, Horizon. Polarization, 200 MHz to 1 GHz

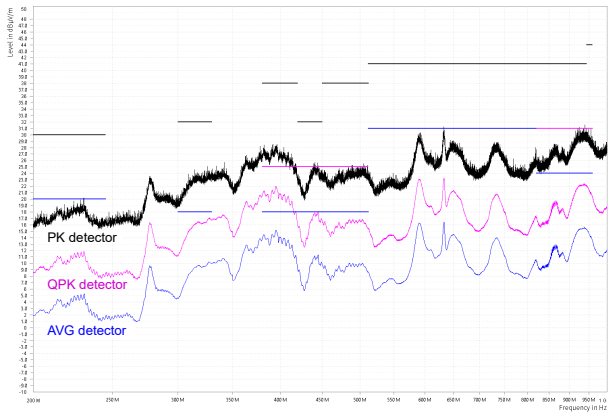

Figure 5-19. CISPR 25 Class 5 Radiated EMI, Log Antenna, Vertical Polarization, 200 MHz to 1 GHz

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6 EVM Documentation

6.1 Schematics

6.1.1 LM63460EVM-2MHZ Schematic

Figure 6-1 shows the schematic for the LM63460EVM-2MHZ. Suitable component placements configure the EVM to accommodate the EN/SYNC and RT pin features of the LM63460-Q1. More specifically, C20 (1 nF) connects SYNC from header J3 to the EN/SYNC pin of the LM63460-Q1, and R11 (6.04 kΩ) sets the switching freqeunecy at 2.1 MHz.

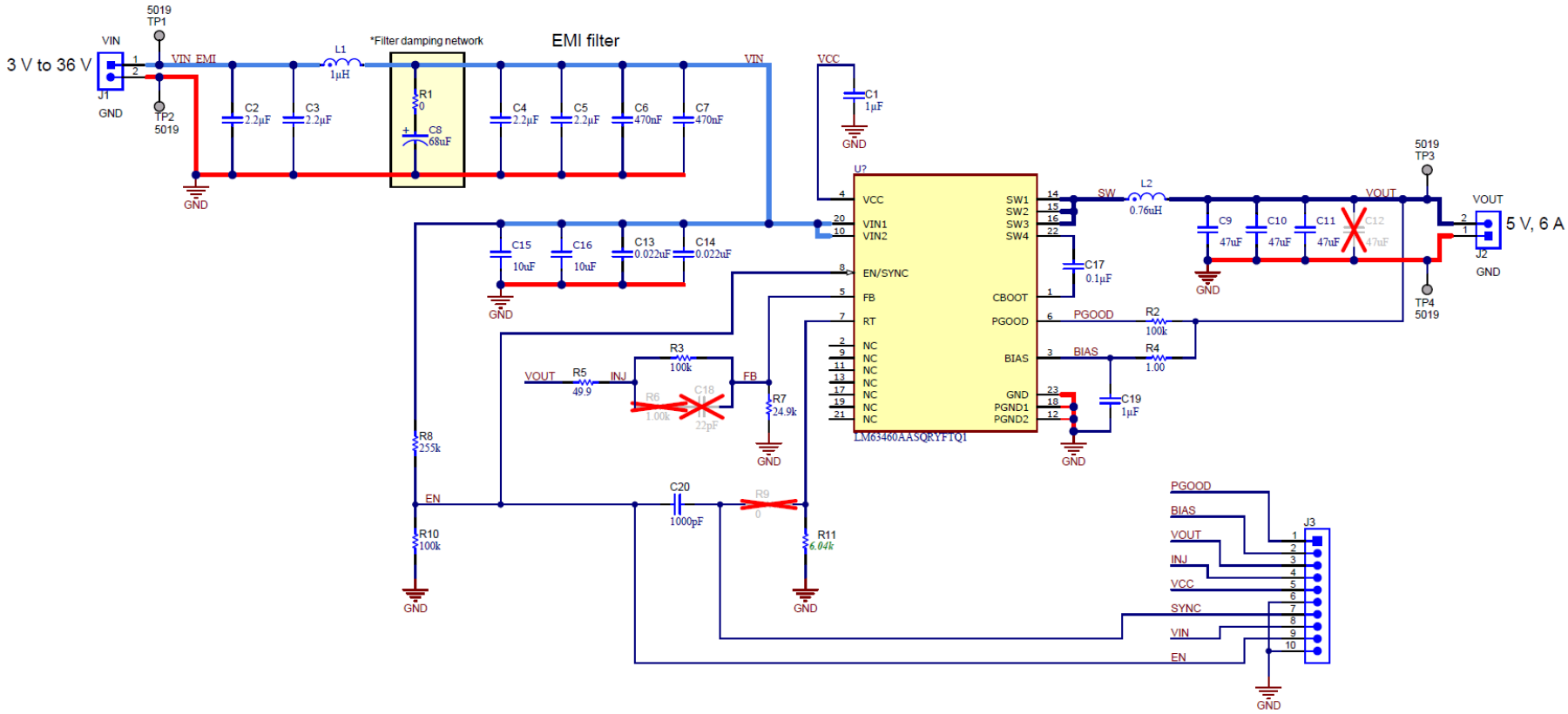

Figure 6-1. LM63460-Q1 EVM Schematic

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6.1.2 LM64460EVM-2MHZ Schematic

Figure 6-2 shows the schematic for the LM64460EVM-2MHZ. Suitable component placements configure the EVM to accommodate the EN and MODE/SYNC pin features of the LM64460-Q1. More specifically, R9 (0 Ω) connects SYNC from header J3 to the MODE/SYNC pin of the LM64460-Q1, and R11 (100 kΩ) configures the LM64460-Q1 for AUTO mode with spread spectrum disabled. Tie SYNC to VIN or GND to enable spread spectrum in FPWM and AUTO modes, respectively.

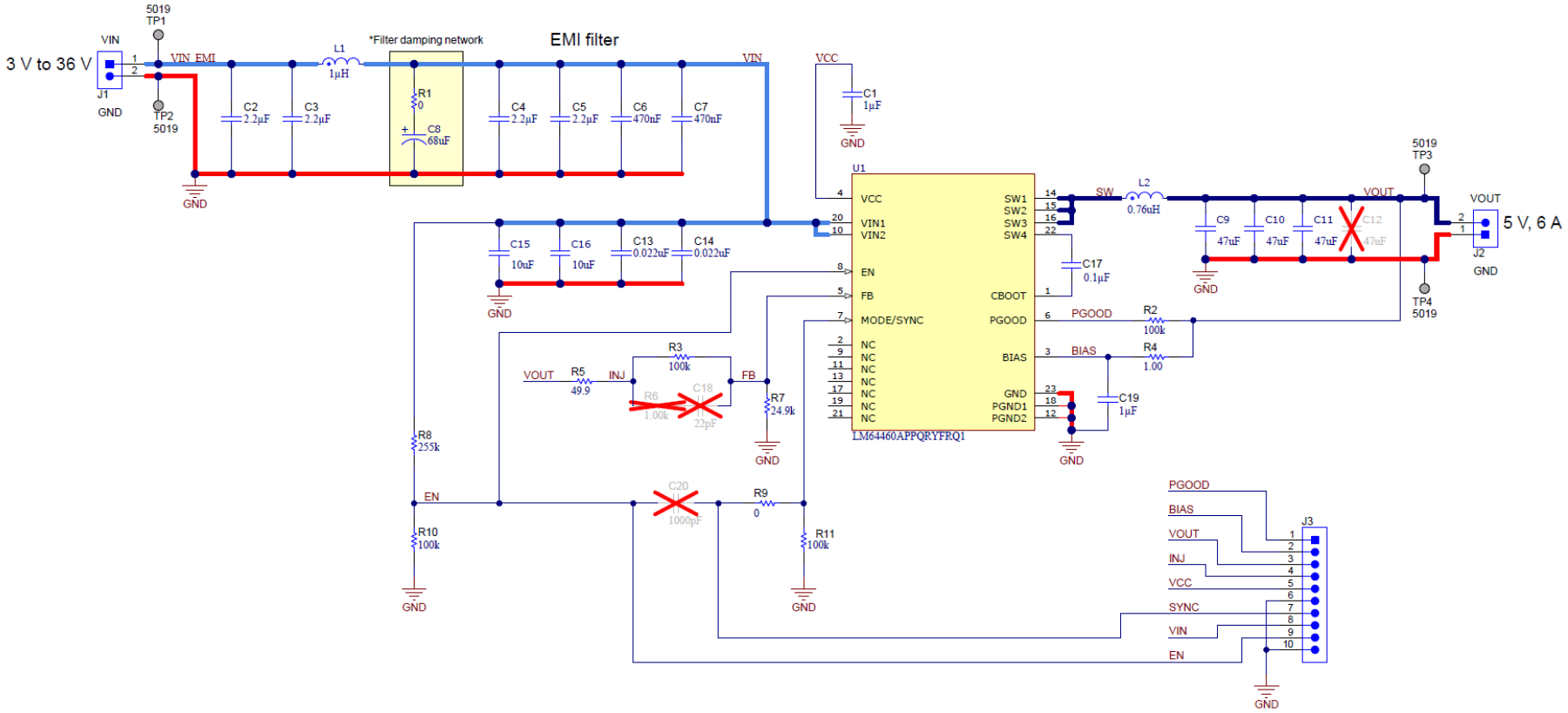

Figure 6-2. LM64460-Q1 EVM Schematic

Note

The input damping network based on electrolytic capacitor C8 mitigates the effect of long input power lines with series parasitic inductance. For more information regarding this topic, please refer to the *EMI Filter Components and Their Nonidealities for Automotive DC/DC Regulators* technical brief.

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6.2 Bill of Materials

Table 6-1 shows the bill of materials for the LM63460EVM-2MHZ and LM64460EVM-2MHZ EVMs. Note that the main BOM difference between the two EVM variants is the IC (U1). The LM63460-Q1 has an RT pin for resistor-adjustable switching frequency and allows external clock synchronization by AC coupling to its EN/SYNC pin. Conversely, the LM64460-Q1 has a default switching frequency of 2.1 MHz and has a MODE/SYNC pin for synchronization and operating mode configuration. Placement of either C20 or R9 accommodates this difference in functionality on a shared PCB design.

Table 6-1. LM63460EVM-2MHZ (BSR173-001) and LM64460EVM-2MHZ (BSR173-002) Bill of Materials

REF DES		QTY	VALUE	DESCRIPTION	PACKAGE	PART NUMBER	MANUFACTURER
C1, C9		2	1 µF	CAP, CERM, 1 µF, 16 V, 10%, X7R, 0603	0603	C0603C105K4RACAUTO	Kemet
C2, C3, C4, C5		4	2.2 µF	CAP, CERM, 2.2 µF, 50 V, 10%, X7R 0805	0805	CGA4J3X7R1H225K125AB	TDK
C6, C7		2	0.47 µF	CAP, CERM, 0.47 µF, 50 V, 10%, X7R, 0603	0603	CGA3E3X7R1H474K080AE	TDK
C8		1	68 µF	68 µF, 50 V, aluminum electrolytic cap	1210	EEE-FN1H680XL	Panasonic
C9, C10, C11		3	47 µF	CAP, CERM, 47 µF, 10 V, 20%, X7S, 1210	1210	CGA6P1X7S1A476M250AC	TDK
C13, C14		2	22 nF	CAP, CERM, 22 nF, 50 V, 10%, X7R, 0402	0402	Std	Std
C15, C16		2	10 µF	CAP, CERM, 10 µF, 50 V, X7R, 1210	1210	CNA6P1X7R1H106K250AE	TDK
C17		1	0.1 µF	CAP, CERM, 0.1 µF, 10 V, 10%, X7R, 0402	0402	Std	Std
C20	BSR173-001	1	1 nF	CAP, CERM, 1 nF, 25 V, 10%, X7R, 0402	0402	Std	Std
H1, H2, H3, H4		4	–	Standoff, Hex, 0.5"L, #4-40, Nylon	–	1902C	Keystone
H5, H6, H7, H8		4	–	Screw, Pan Head, 4-40, 3/8", Nylon	–	NY PMS 440 0038 PH	B&F Fastener Supply
J1, J2		2	–	Terminal block 2 POS 5 mm, TH	–	TSW-110-07-G-S	Phoenix Contact
J3		1	–	Header, 100 mil, 10 × 1, Gold, TH	–	TSW-110-07-G-S	Samtec
L1		1	1 µH	Shielded power inductor	–	XGL4020-102MEC	Coilcraft
L2		1	0.76 µH	Shielded power inductor	–	XGL4030-761MEC	Coilcraft
R1		1	0 Ω	RES, 0 Ω, 5%, 0.1 W, 0603	0603	Std	Std
R2, R3, R10		3	100 kΩ	RES, 100 kΩ, 1%, 0.063 W, 0402	0402	Std	Std
R4		1	1 Ω	RES, 1 Ω, 1%, 0.063 W, 0402	0402	Std	Std
R5		1	10 Ω	RES, 10 Ω, 1%, 0.063 W, 0402	0402	Std	Std
R7		1	24.9 kΩ	RES, 24.9 kΩ, 1%, 0.0.063 W, 0402	0402	Std	Std
R8		1	255 kΩ	RES, 255 kΩ, 1%, 0.0.063 W, 0402	0402	Std	Std
R9	BSR173-002	1	0 Ω	RES, 0 Ω, 5%, 0.1 W, 0402	0402	Std	Std
R11	BSR173-001	1	6.04 kΩ	RES, 6.04 Ω, 1%, 0.063 W, 0402	0402	Std	Std
	BSR173-002	1	100 kΩ	RES, 100 kΩ, 1%, 0.063 W, 0402	0402	Std	Std
SH-J3		1	–	Shunt, 100 mil, gold plated, black	Shunt 2 pos. 0.1"	881545-2	TE Connectivity
TP1, TP2, TP3, TP4		4	–	Test point, miniature, SMT	–	5019	Keystone
U1	BSR173-001	1	–	36-V, 6-A buck converter with EN/SYNC and RT	VQFN-FCRLF (22)	LM63460AASQRYFRQ1	Texas Instruments
	BSR173-002			36-V, 6-A buck converter with EN and MODE/SYNC		LM64460APPQRYFRQ1	

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6.3 PCB Layout

Figure 6-3 through Figure 6-8 show the board layout. The design offers appropriate test points to configure the following:

- PGOOD monitor
- Precision enable and input voltage UVLO
- Bode plot measurement
- External clock synchronization

The 22-pin Enhanced HotRod package enables a very small solution size and a low-EMI design. The PCB consists of a 4-layer design with 2-oz copper on all layers and an array of thermal vias to connect to all four layers. Input and output connectors with adjacent sense points for the supply and load enable a convenient setup to power the EVM, measure efficiency, and so forth.

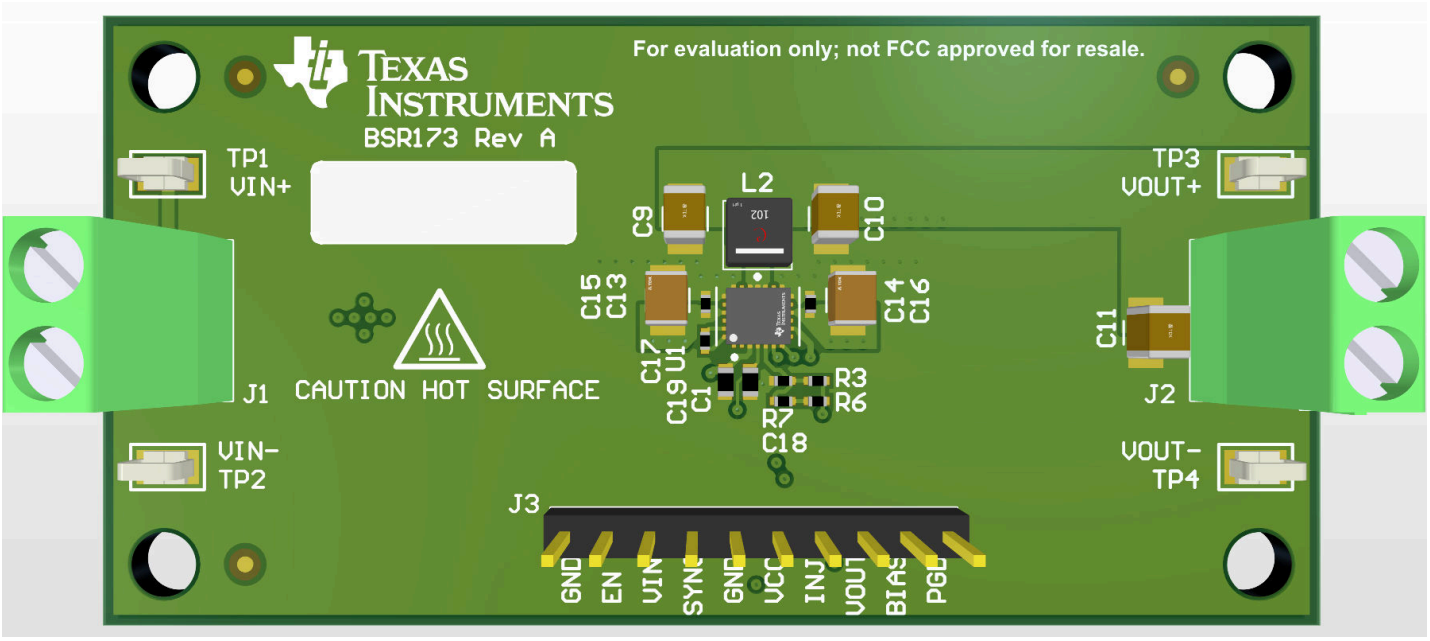

Figure 6-3. Top 3D View

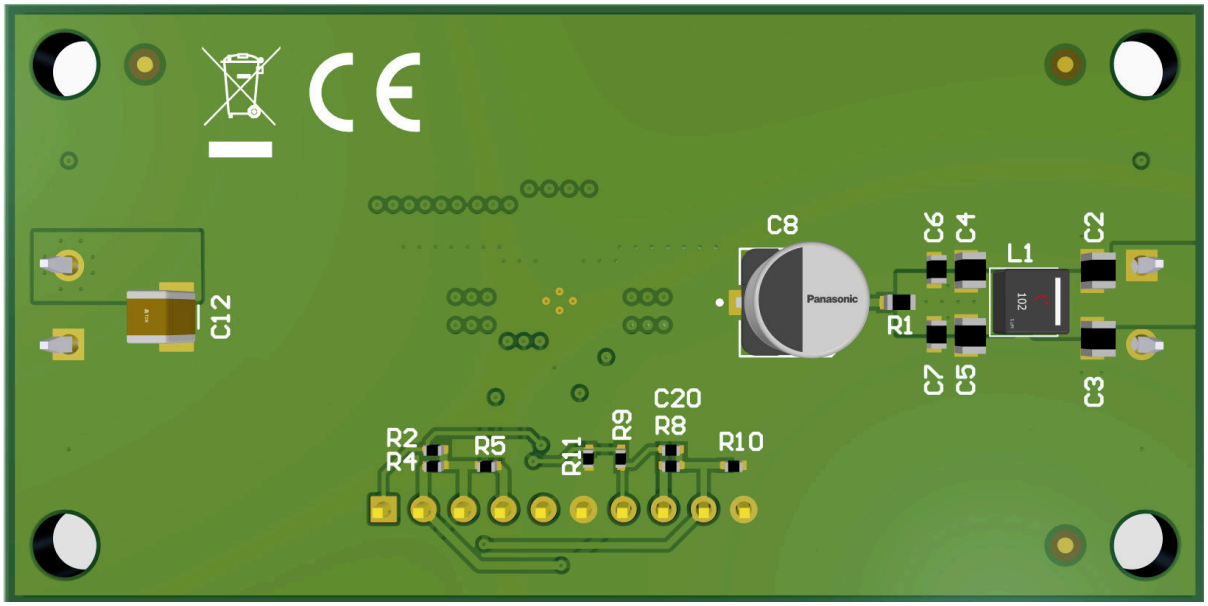

Figure 6-4. Bottom 3D View (viewed from Bottom)

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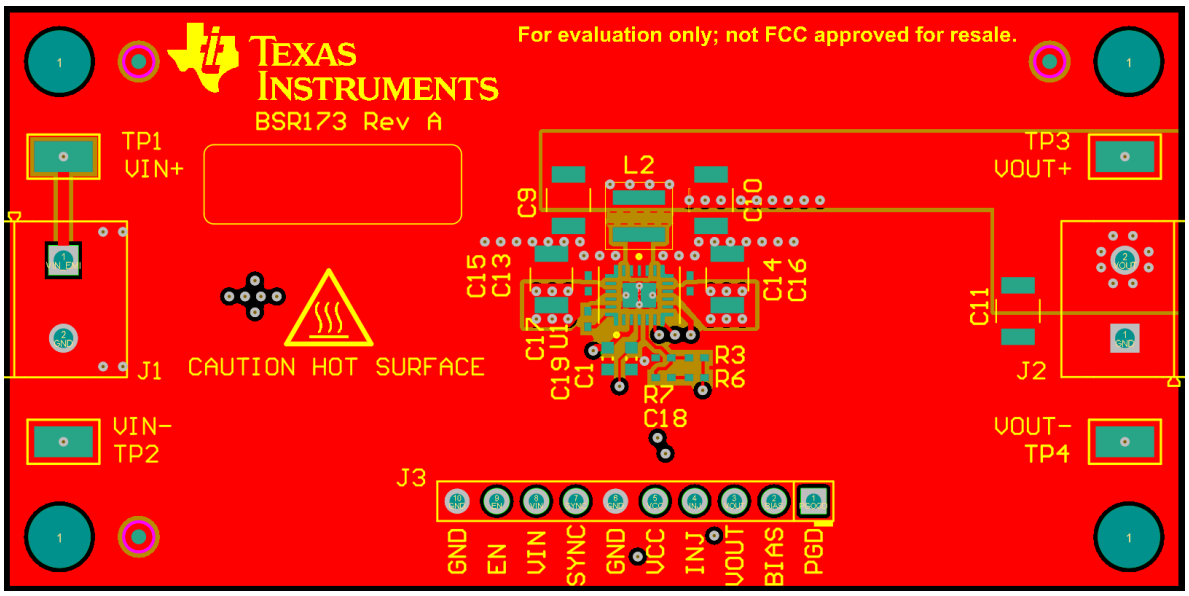

Figure 6-5. Top Layer

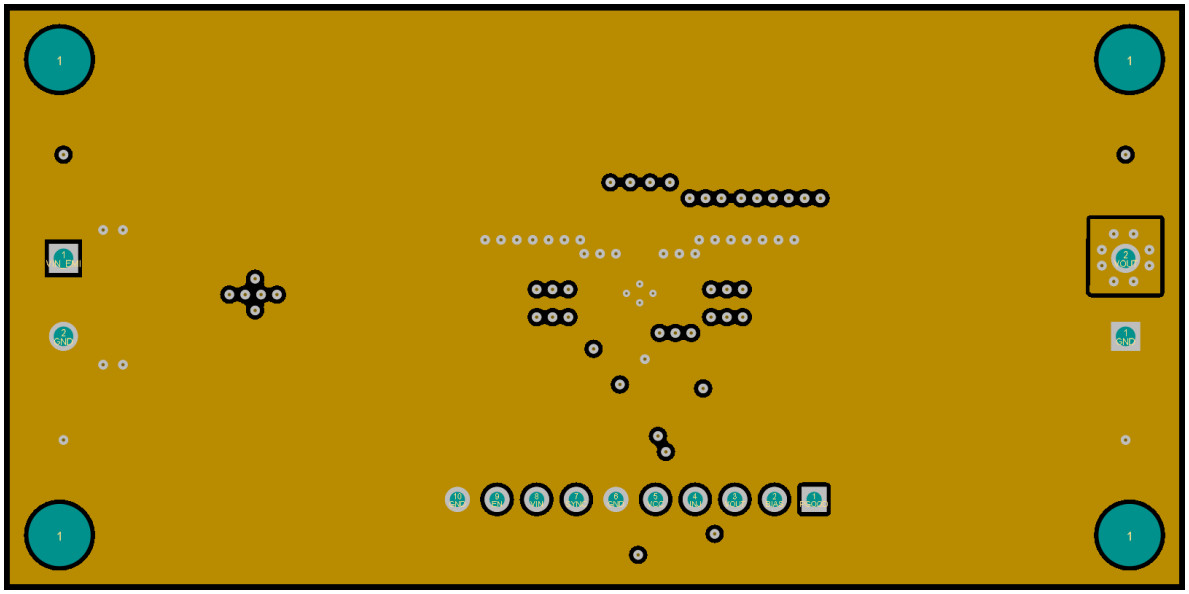

Figure 6-6. Layer 2

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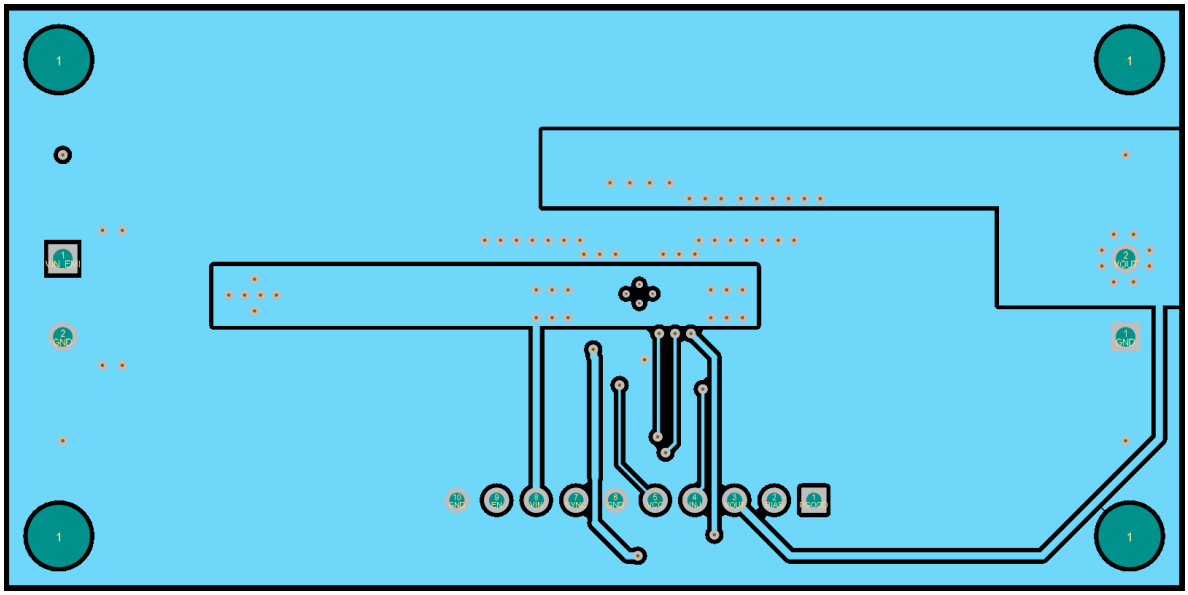

Figure 6-7. Layer 3

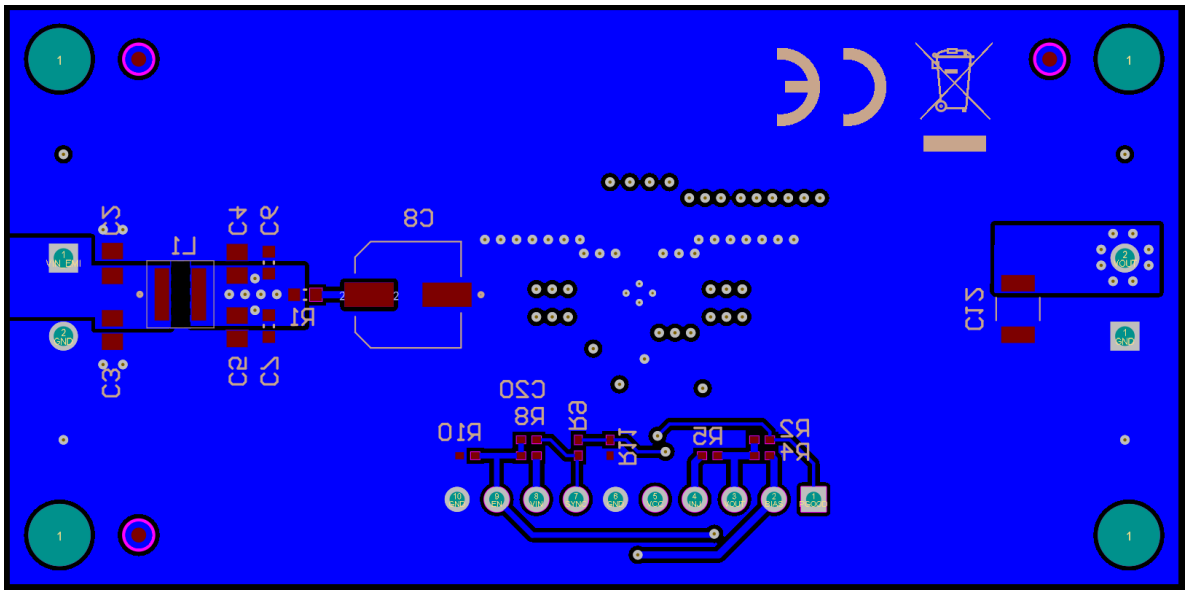

Figure 6-8. Bottom Layer

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6.4 Assembly Drawings

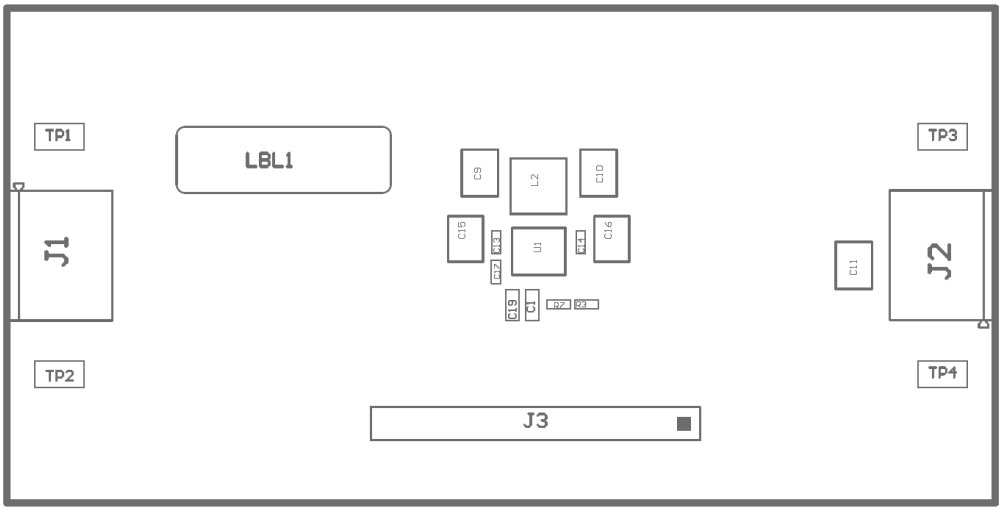

Figure 6-9. Top Assembly (Top View), LM63460EVM-2MHZ and LM64460EVM-2MHZ

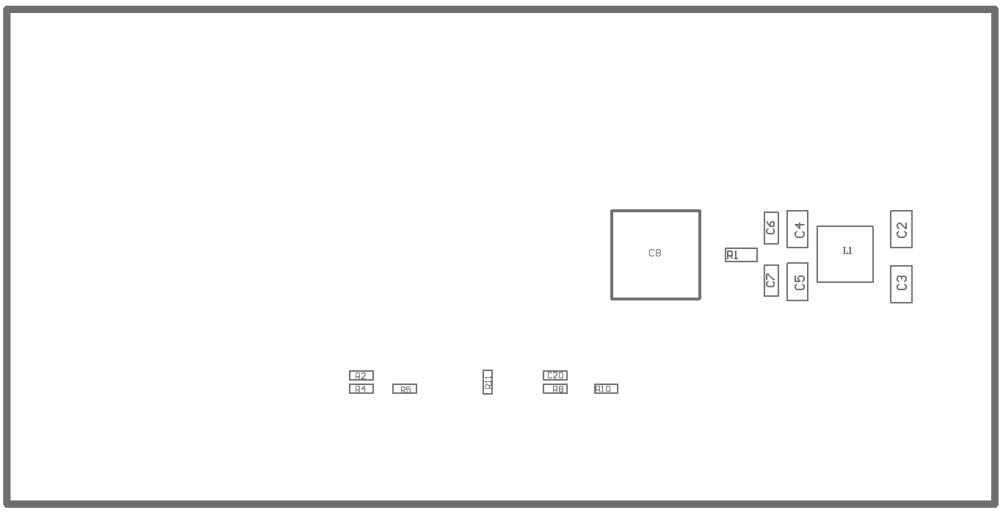

Figure 6-10. Bottom Assembly (Bottom View), LM63460EVM-2MHZ

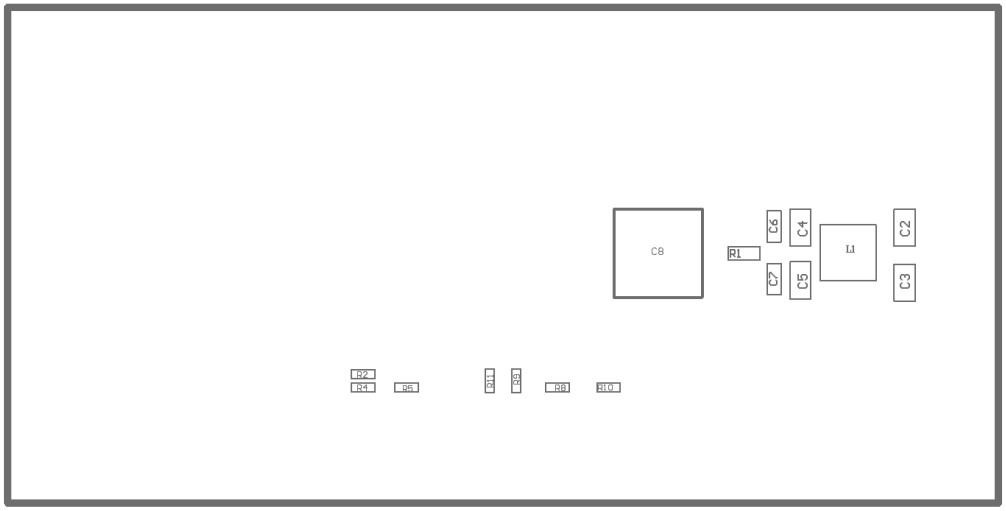

Figure 6-11. Bottom Assembly (Bottom View), LM64460EVM-2MHZ

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7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

With an input operating voltage as low as 3 V and up to 36 V as specified in Table 7-1, the LM6k family of automotive synchronous buck converters from TI provides flexibility, scalability and optimized solution size for a range of applications. These converters enable DC/DC solutions with high density, low EMI and increased flexibility. Available EMI mitigation features include pseudo-random spread spectrum (PRSS), integrated input bypass capacitors, RBOOT-configured switch-node slew rate control, and optimized package design with symmetrical VIN and PGND pins that shield a small switch-node copper area. All converters are rated for a maximum operating junction temperature of 150°C, have AEC-Q100 grade 1 qualification, and are functional safety capable.

Table 7-1. Automotive Synchronous Buck DC/DC Converter Family

DC/DC CONVERTER	RATED I_{OUT}	PACKAGE	FEATURES	EMI MITIGATION
LM60430-Q1, LM60440-Q1	3 A, 4 A	WQFN (13)	400 kHz fixed f_{SW}, 3 × 2-mm package	Shielded switch node
LM63610-Q1, LM63615-Q1, LM63625-Q1, LM63635-Q1	1 A, 1.5 A, 2.5 A, 3.25 A	WSON (12), HTSSOP (16)	RT adjustable f_{SW}, MODE/SYNC	PRSS
LM61430-Q1, LM61435-Q1, LM61440-Q1, LM61460-Q1	3 A, 3.5 A, 4 A, 6 A	VQFN-HR (14)	RT adjustable f_{SW}, EN/SYNC	PRSS, RBOOT
LM62435-Q1, LM62440-Q1	3.5 A, 4 A		2.1 MHz default f_{SW}, MODE/SYNC	
LMQ61460-Q1	6 A		RT adjustable f_{SW}, EN/SYNC	PRSS, RBOOT, integrated capacitors
LMQ62440-Q1	4 A		2.1 MHz default f_{SW}, MODE/SYNC	
LM62460-Q1, LM61480-Q1, LM61495-Q1	6 A, 8 A, 10 A	VQFN-HR (16)	RT adjustable f_{SW}, MODE/SYNC	DRSS, RBOOT
LM63460-Q1	6 A	VQFN-FCRLF (22)	RT adjustable f_{SW}, EN/SYNC, pin FMEA	PRSS
LM64460-Q1			2.1 MHz default f_{SW}, MODE/SYNC, pin FMEA	

For development support see the following:

- LM63460-Q1 and LM64460-Q1 *Quickstart Calculator*
- LM63460-Q1 *Simulation Models*
- LM64460-Q1 *Simulation Models*
- LM63460-Q1 and LM64460-Q1 *EVM Altium Layout Files*
- For TI's reference design library, visit TI Designs.
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center.
- To design a low-EMI power supply, review TI's comprehensive EMI Training Series.
- TI Reference Designs:
  - *30-W Power For Automotive Dual USB Type-C™ Charge Port Reference Design*
  - *High Efficiency, Low Noise, 5-V/3.3-V/1.8-V/1.1-V Automotive Display Reference Design*
- Technical Articles:
  - *How Device-level Features And Package Options Can Help Minimize EMI In Automotive Designs*
  - *Optimizing Flip-chip IC Thermal Performance In Automotive Designs*
  - *Powering Levels Of Autonomy: A Quick Guide To DC/DC Solutions For SAE Autonomy Levels*
  - *Powering Infotainment Systems Of The Future*

7.1.1.1 Custom Design With WEBENCH® Tools

Click here (LM63460-Q1) or here (LM64460-Q1) to create a custom design using the converter with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

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In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2 Documentation Support

7.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *EMI Filter Components And Their Nonidealities For Automotive DC/DC Regulators* technical brief
- Texas Instruments, *Designing High Performance, Low-EMI, Automotive Power Supplies* application report
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC/DC Converters Application Report* application report
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application report

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