Application Report
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TMS320C6748/46/42 and OMAP-L1x8 Universal Serial Bus Upstream Device Compliance Testing

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ABSTRACT

This application report describes the TMS320C6748/46/42 and OMAP-L1x8 electrical compliance of a high-speed (HS) universal serial bus (USB) operation conforming to the USB 2.0 specification. The on-the-go (OTG) controller supports the USB 2.0 device and host mode at high-speed (HS), full-speed (FS) and low-speed (LS).

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1 Introduction

The device high-speed electrical test procedure is comprised of a series of tests and related procedures developed by the USB 2.0 compliance committee to verify electrical requirements of high-speed USB operations designed to meet USB 2.0 specification. This document outlines the test setup and captures the results of the series tests performed on the C6748/46/42 and OMAP-L1x8 device.

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The C6748/46/42 and OMAP-L1x8 device high-speed electrical test of the USB is performed on a VDB, a board that is used to validate the device feature and is not optimized for USB characterization. Better results are expected when using test boards that are optimized for characterization purposes.

Figure 1 shows the USB functional block diagram.

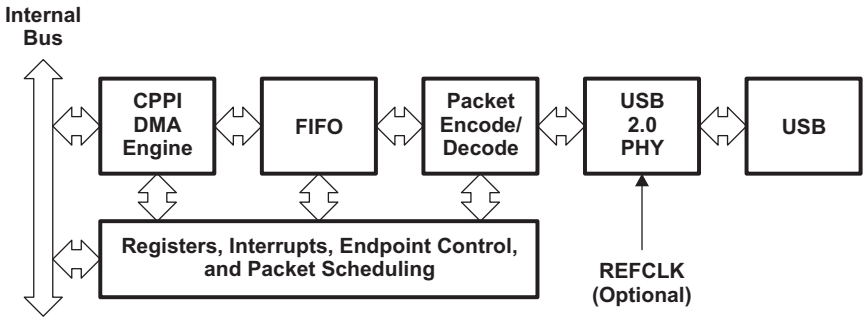

Figure 1. USB Functional Block Diagram

2 Test Items

Table 1 captures the series of compliance tests and the summary of results for each test. Details on the tests and specific results are discussed in the following sections.

Table 1. Device Electrical Tests Result Summary

Test#	Test Items	Result
USB_EL_2	HS Transmitter data rate 480 Mb/s ± 0.05%	PASS
USB_EL_4	Signal quality test measured at the near end	PASS
USB_EL_6	10% to 90% differential rise and fall time > 500ps	PASS
USB_EL_7	Monotonic data transitions over the vertical openings in the appropriate EYE pattern template	PASS
USB_EL_21	Synchronization (SYNC) field (packet originating from C6748/46/42 and OMAP-L1x8)	PASS
USB_EL_22	Inter-packet gap (delay between Host and device packet)	PASS
USB_EL_25	End of packet (EOP) field (packet originating from C6748/46/42 and OMAP-L1x8)	PASS
USB_EL_28	Chirp reset time	PASS
USB_EL_29	Chirp-K duration	PASS
USB_EL_31	Delay between last Host chirp and device disconnect 1.5 K pull-up resistor and enable termination	PASS
USB_EL_27	Chirp handshake generation while Host performing reset in the middle of idle (non-suspend HS mode)	PASS
USB_EL_28	Chirp-K duration when reset is invoked from a suspended state	PASS
USB_EL_38	Chirp reset time when reset is applied from a suspend state	PASS
USB_EL_39	Device support for suspend state	PASS
USB_EL_40	Device transitioning from suspend state to HS operation due to reaching the EOF	PASS
USB_EL_8	Test J/K (controller transmits continuous J)	PASS
USB_EL_8	Test K (controller transmits continuous K)	PASS
USB_EL_9	Test_SE0_NAK (controller responds to any valid IN token with a NAK)	PASS
USB_EL_16	Device receiver level	PASS
USB_EL_17	Device squelch level	PASS
USB_EL_18	Device capability for locking PLL with 12-bit SYNC field	PASS

Table 2 lists the categorized series of tests outlined in the electrical test procedure in the USB2.0 compliance test.

Table 2. Test Categories

Test Items	Categories
HS transmitter data rate 480 Mb/s ± 0.05%	HS Upstream Signal Quality Test
Signal quality test measured at the near end	
10% to 90% differential rise and fall time > 500 ps	
Monotonic data transitions over the vertical openings in the appropriate EYE pattern template	
SYNC field (packet originating from C6748/46/42 and OMAP-L1x8)	Device Packet Parameters
Inter-packet gap (delay between Host and device packet)	
EOP field (packet originating from C6748/46/42 and OMAP-L1x8)	
Chirp reset time	Device Chirp Timing
Chirp-K duration	
Delay between the last Host chirp and the device disconnect 1.5 K pull-up resistor and enable termination	
Chirp handshake generation while Host is performing reset in the middle of idle (non-suspend HS mode)	Device Suspend/Resume/Reset Timing
Chirp-K duration when reset is invoked from a suspended state	
Chirp reset time when reset is applied from a suspended state	
Device support for suspend state	
Device transitioning from suspend state to high-speed operation when resume signaling is issued by the Host (from a suspend state)	
Test J (controller transmits continuous J)	Device Test_J/K and Test_SE0_NAK
Test K (controller transmits continuous K)	
Test_SE0_NAK (controller responds to any valid IN token with a NAK)	
Device receiver level	Device Receiver Sensitivity
Device squelch level	
Device capability for locking PLL with 12-bit SYNC Field	

3 Required Instruments

Table 3 lists the test instruments used to perform the outlined series of tests. These instruments are not all identical to the ones outlined in the test document and are mentioned here since test setup, equipment, and cables have a large influence on the test outcome.

Table 3. Required Instruments

Type	Manufacturer	Product	Use
USB high-speed electrical test tool to be loaded on a test bed computer	USB-IF	USBHSET	To enumerate and send command
Oscilloscope	Tektronix	DSA71604	To measure USB signals
Differential probe (1)	Tektronix	P7313	Signal quality/receiver sensitivity tests
Single-ended FET probe (2)	Tektronix	P6243	Packet parameters/CHIRP timings
Measurement application (USB test software that is part of the scope application)	Tektronix	TDSUSB	USB compliance test software specifically used for USB
Test fixture	Tektronix	TDSUSBF	For USB test
Power supply	Agilent	E3633A	5 V power supply for TDSUSBF
Arbitrary waveform generator	Tektronix	AWG5002	To generate serial test data for receiver sensitivity test

Table 3. Required Instruments (continued)

Type	Manufacturer	Product	Use
Digital multimeter	Fluke	Fluke 45 Series	Measure voltage and current DP and DM lines
Test board (VDB)	TI	EVM Like Board	Non-optimized test board used for C6748/46/42 and OMAP-L1x8 Device validation

4 Test Condition

4.1 Power Supply Voltage/Temperature

Table 4 shows power supply voltage and temperature conditions.

Table 4. Power Supply Voltage and Temperature Conditions

Parameter	MIN	TYP	MAX	Unit
USB_$V_{DDA1P2LDO}$	1.14	1.2	1.26	V
USB_V_{DDA3P3}	3.1	3.3	3.5	V
Operating Temperature	-10	25	95	°C

4.2 HS Upstream Signal Quality Test

The HS upstream signal quality test uses the *TEST_PACKET* command to place the C6748/46/42 and OMAP-L1x8 device in test mode where the controller continuously transmits a fixed format test packet, which is defined in the USB 2.0 specification, Section 7.1.20. The test bed computer uses the electrical test tools to issue the *TEST_PACKET* command to the C6748/46/42 and OMAP-L1x8. Upon receiving this command, the C6748/46/42 and OMAP-L1x8 device enters the test packet test mode and begins continually sending a test packet. Using the test packet, this test measures the signal quality sent from the C6748/46/42 and OMAP-L1x8 device.

The oscilloscope, along the embedded software, automatically analyzes the test packet signal quality as observed on the USB bus. For detailed procedures, see the *Device High Speed Electrical Test Procedure* document issued by the USB Implementers Forum (http://www.usb.org).

4.2.1 EL_2: Signal Rate

A USB 2.0 high-speed transmitter data rate must be 480 Mb/s ± 0.05%.

4.2.2 EL_4: Signal Quality/Eye Diagram Test

An eye diagram provides an intuitive view of jitter. It is a composite view of all the bit periods of a captured waveform superimposed upon each other. A USB 2.0 upstream port on a device, without a captive cable, must meet Template 1 transform waveform requirements measured at a test point close to the port.

4.2.3 EL_6: Rise and Fall Time

A USB 2.0 high-speed driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

4.2.4 EL_7: Monotonic Data Transitions

A USB 2.0 driver must have monotonic data transitions over the vertical openings specified in the appropriate EYE pattern template.

Table 5. Overall Result of the Signal Quality Test

Measurement	Min.	Max.	Mean	pk-pk	Standard Deviation	RMS	Pop.	Status
Eye Diagram Test	-	-	-	-	-	-	-	PASS
Signal Rate	465.5493 Mbps	492.0319 Mbps	480.0509 Mbps	0.0000 bps	4.488669 Mbps	479.8074 Mbps	512	PASS
EOP Width	-	-	16.68762 ns	-	-	-	1	PASS
EOP Width (Bits)	-	-	8.010908	-	-	-	1	PASS
Falling Edge Rate	814.3150 V/µs	951.3559 V/µs	873.3275 V/µs	137.0409 V/µs	26.14228 V/µs	873.7150 V/µs	107	PASS
Rising Edge Rate	826.7541 V/µs	967.2481 V/µs	896.4816 V/µs	140.4940 V/µs	27.33377 V/µs	896.8944 V/µs	108	PASS

Additional Information

- Consecutive Jitter Range: -54.27 ps to 56.81 ps RMS Jitter 22.11 ps
- KJ Paired Jitter Range: -60.14 ps to 56.99 ps RMS Jitter 22.89 ps
- JK Paired Jitter Range: -57.15 ps to 76.99 ps RMS Jitter 21.13 ps

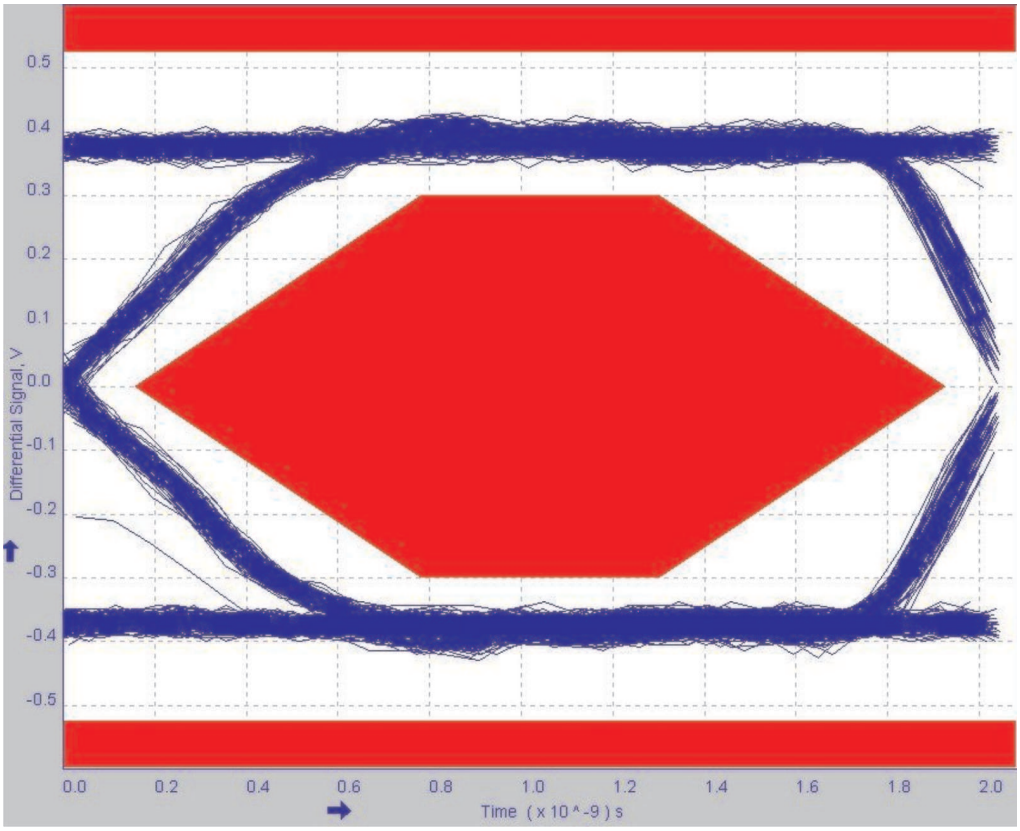

Figure 2. Eye Diagram/Signal Eye

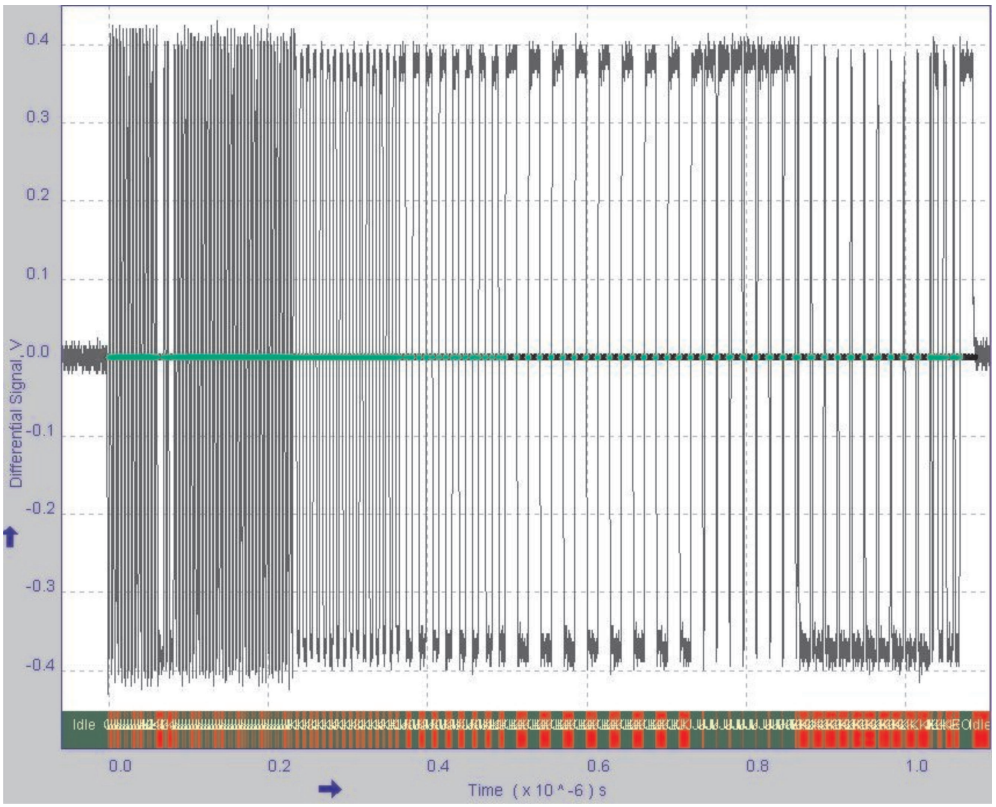

Figure 3. Waveform Plot

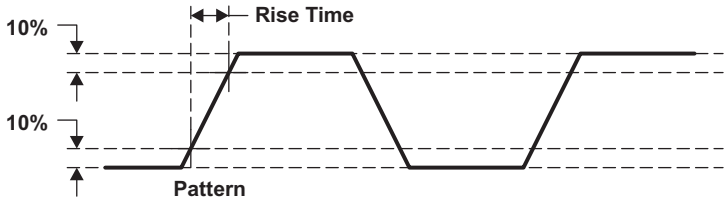

Figure 4. Rise Time

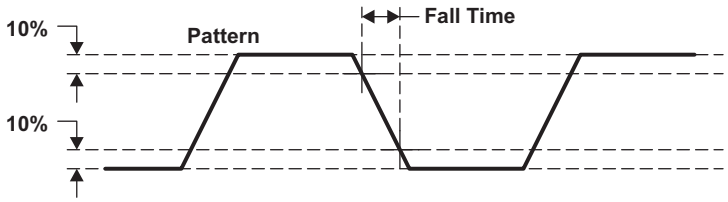

Figure 5. Fall Time

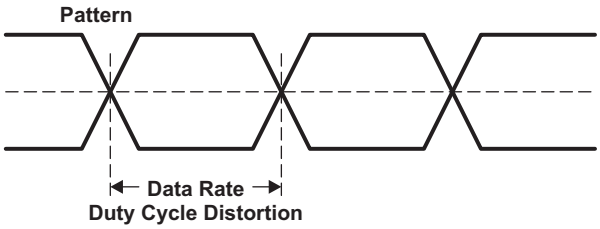

Figure 6. Duty Cycle Distortion (DCD)

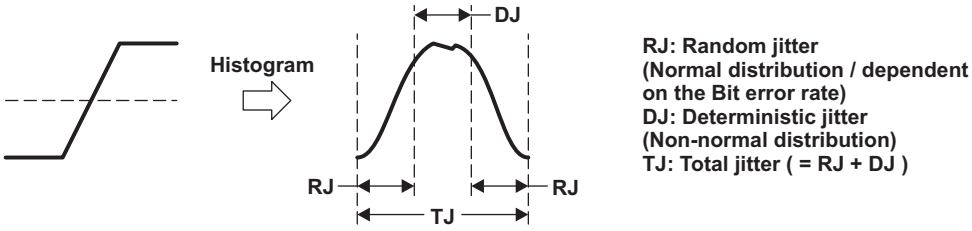

Figure 7. Random Jitter/Deterministic Jitter/Total Jitter

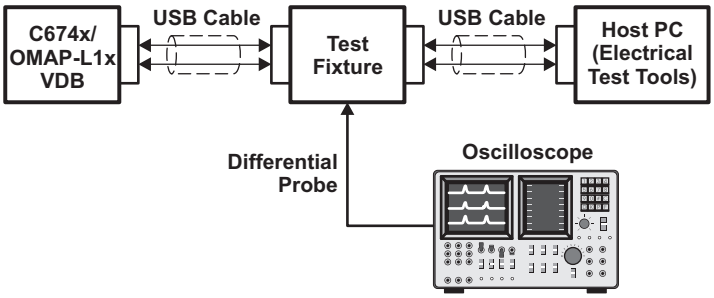

Figure 8. Setup Diagram for Performing HS Upstream Signal Quality Test

Figure 8 is also used for other sets of tests:

- Device Packet Parameters
- Device CHIRP Timing
- Device Suspend/Resume/Reset Timing

4.3 Device Packet Parameters

The device packet parameter tests are comprised of a set of tests related to fields pertaining to a USB transfer. Unlike the signal quality test, the device does not need to enter into a test mode. Instead, the test bed computer invokes a *set feature* control transaction by pausing in between transfers. The *single step set feature* command requires a setup stage and a status stage. The test bed computer invokes the setup stage transaction then pauses until told to continue. The packet delimiter fields, SYNC and EOP, are measured from the handshake packet during the setup stage in the transaction. The STEP button of the electrical test tool is used to continue/finish the *set feature* command. The inter packet gap, the delay between the token packet originating from the Host and the data packet (zero length) originating from the device, is measured from the second half of the transfer.

The same setup file used for the signal quality testing is used to perform device packet parameters tests. Three device parameters are tested from this setup: SYNC, EOP, and inter-packet-gap

4.3.1 EL_21: SYNC (Synchronization) Field

The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

Handshake packet SYNC field: PASS

Note: Measured value: 66.91 ns => 66.91 ns x 480 Mbps = 32.1168 bits

4.3.2 EL_22: Inter-Packet-Gap Field

When transmitting after receiving a packet, hosts and devices must provide an inter-packet-gap of at least 8 bit times and not more than 192 bit times.

Packet gap between Host token packet and device data packet: PASS

Note: Measured value: 240.24 ns => 240.24 ns x 480 Mbps = 115.3152 bits

4.3.3 EL_25: EOP (End-of-Packet) Field

The EOP for all transmitted packets (except state of finish (SOF)) must be an 8-bit non-return to zero inverted (NRZI) byte without bit stuffing.

Handshake packet EOP field: PASS.

Note: Measured value: 16.58 ns => 16.58 ns x 480 Mbps = 7.9584 bits

4.4 Device CHIRP Timing

The device chirp timing is used to validate a high-speed detection handshake and occurs during the time of reset. Some time after the Host resets a high-speed device, the device should indicate its high-speed capability by generating a chirp-K signal. The Host will follow up by generating three sets of chirp-KJ signals in a full-speed signaling environment. The device should disconnect its 1.5KΩ pull-up resistor and enable the 45 Ω termination resistors right after the last chirp-J from the Host.

You can invoke this test using the same setup as the signal quality testing shown in Figure 8, with the two probes replacing the differential probe; however, in this case use the Host test bed computer to enumerate the C6748/46/42 and OMAP-L1x8 device only. You can also invoke the *Enumerate Bus* single-ended from the high-speed electrical test tool to perform the same test.

Note: Make sure your scope is configured and ready for capturing/triggering the enumeration process. Start by disconnecting the USB cable connection between the Host and USB fixture (TDSUSB2F). Have the device side code ready and running. When connecting the USB cable from the Host onto the USB test fixture, the enumeration process takes place and is captured on the scope.

Figure 8 displays the setup used for performing these set of tests.

Note: In place of the differential probe, two single-ended FET probes are used.

4.4.1 EL_28: CHIRP Reset Time

Devices must transmit a chirp handshake no sooner than 2.5 µs and no later than 3 ms when being reset from suspend or a full-speed state.

CHIRP reset time: PASS

Note: Measured value: 5.903741 µs

4.4.2 EL_29: CHIRP-K Duration

The chirp handshake generated by a device must be at least 1ms and not more than 7 ms in duration.

CHIRP-K duration: PASS

Note: Measured value: 1.096818 ms

4.4.3 EL_31: 1.5 K Pull-Up Resistor Disconnection

When a device detects a valid set of chirp-KJ sequences during device speed detection, the device must disconnect its 1.5 K pull-up resistor and enable its high-speed terminations within 500 µs.

1.5K pull-up resistor disconnect: PASS

Note: Measured value: 7 µs

4.5 Device Suspend/Resume/Reset Timing

A device must support suspend state. It is supposed to go through a suspend state when it is forced to go to suspend state by the host or when there is no activity for ≥ 3 ms. A high-speed device indicates its high-speed operation capability when the Host invokes a reset on the device by generating a chirp-K sequence signal.

Figure 8 displays the setup used for performing these set of tests with the two single-ended probes replacing the differential probe.

4.5.1 EL_27: CHIRP Handshake Generation From Non-Suspended State

A device must transmit a chirp handshake no sooner than 3.1 ms and no later than 6 ms when being reset from a non-suspended high-speed mode. The timing is measured from the beginning of the last SOF transmitted and before the reset begins.

Chirp handshake generation when reset from a non-suspended state: PASS

Note: Measured value: 3.102598 ms

4.5.2 EL_28: CHIRP-K Duration From a Suspended State

A device must transmit a chirp handshake (chirp-K) no sooner than 2.5 µs and no later than 3 ms when being reset from suspend or a full-speed mode.

Chirp-K duration from a suspend state: PASS

Note: Measured value: 5.592141 µs

4.5.3 EL_38: CHIRP Reset Time From a Suspended State

A device must revert to full-speed termination no later than 125 µs after there is a 3 ms idle period on the bus.

Chirp reset time when reset is applied from a suspended state. PASS

Note: Measured value: 3.0036 ms

4.5.4 EL_39: Device Support for Suspend State

A device must support suspend state. The device should go into suspend state when forced by the Host.

Device support for suspend state: PASS

Note: No value to measure. Make sure SOF is not present.

4.5.5 EL_40: Device Resuming With High-Speed Operation After Resume Signaling From a Suspend State

A device must transition its operating to a high-speed operation after receiving the resume signal. This is with the assumption that the device was operating at high-speed prior to being suspended.

Device resumes to HS operation at the end of resume signaling: PASS

Note: No value to measure. SOF at a HS signal level is observed.

4.6 Device Test_J/K/SE0_NAK

A USB controller that is USB 2.0 specification compliant requires that the controller support four tests: Test_SE0_NAK, Test_J, Test_K, and Test_Packet. A digital Multimeter is used for the DC voltage level of D+ and D- data lines.

Test_SE0_NAK places the controller to remain in high-speed mode but respond to any valid IN token with a NAK. Test_J places the controller to transmit a continuous J on the bus. Test_K places the controller to transmit a continuous K on the bus.

Figure 9 displays the setup used for performing the tests mentioned in Section 4.6.

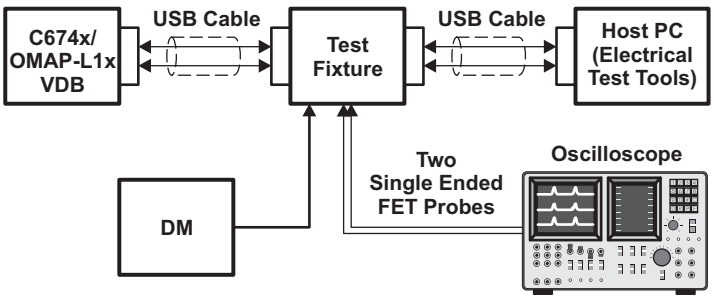

Figure 9. Setup Diagram for Performing HS Test_J/K/SE0_NAK Tests

4.6.1 EL_8: Test_J

When the D+ is driven high, the output voltage must be 400 mV ± 10% when terminated with precision 45 Ω resistor.

D+ data line DC voltage level: PASS

Note: Measured value: 0.391 V

D- data line DC voltage level: PASS

Note: Measured value: 0.002 V

4.6.2 EL_8: Test_K

When the D- is driven high, the output voltage must be 400 mV ± 10% when terminated with precision 45 Ω resistor.

D- data line DC voltage level: PASS

Note: Measured value: 0.388 V

D+ data line DC voltage level: PASS

Note: Measured value: 0.002 V

4.6.3 EL_9: Test_SE0_NAK

When either D+ and D- are not being driven, the output voltage must be 0 V ± 10% when terminated with precision 45 Ω resistors to ground.

D+ data line DC voltage level: PASS

Note: Measured value: 0.001 V

D- data line DC voltage level: PASS

Note: Measured value: 0.001 V

4.7 Receiver Sensitivity Level

The HS receiver sensitivity and squelch test uses the *TEST_SE0_NAK* command. The electrical test tool invokes the *TEST_SE0_NAK* command from the test bed computer to the C6748/46/42 and OMAP-L1x8. Upon receiving this command from the host, the C6748/46/42 and OMAP-L1x8 device enters into a test mode where it continually responds with a NAK upon receiving an IN token.

Once the test setup is done by the host on the test bed computer, the arbitrary waveform replaces the host generating an IN token waveform which forces the device to respond with a NAK. The test fixture has a switch that establishes a link between the device and the Host or the device and the arbitrary waveform generator.

Two waveforms, one with a 32-bit SYNC field and another with a 12-bit SYNC field are used in constructing the IN token to be sent to the device. The waveform with 32-bit SYNC field is used for the receiver and squelch test. The 12-bit field is used for testing device capability on detecting the data transmission.

Figure 10 displays the setup used for performing a receiver sensitivity level test.

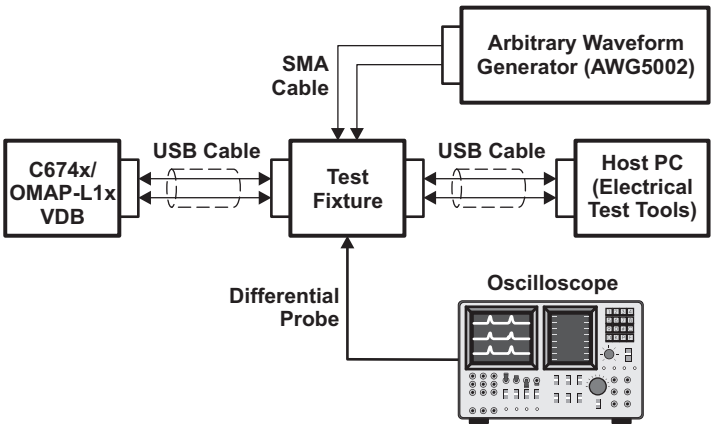

Figure 10. Setup Diagram for Performing Receiver Sensitivity Level Test

4.7.1 EL_16: Squelch Level.

A high-speed capable device must implement a transmission envelope detector that indicates squelch (i.e., never receives packet) when a receiver's input falls below 100 mV differential amplitude.

4.7.2 EL_17: Receiver Level

A high-speed capable device must implement a transmission envelope detector that does not indicate squelch (i.e., reliably receives packets) when a receiver exceeds 150 mV differential amplitude.

4.7.3 EL_18: 12-Bit SYNC Field

The SYNC pattern used for high-speed transmission is required to be 15 KJ pairs followed by 2 K's, for a total of 32 symbols. Hubs are allowed to drop up to 4 bits from the start of the SYNC pattern when repeating packets; however, hubs must not corrupt any repeated bits of the SYNC field. Therefore, after being repeated by five hubs, a packet's SYNC field may be as short as 12 bits. The device attached to the fifth hub should be able to detect the SYNC.

Table 6. Overall Results of 12-Bit SYNC Field

Measurement Name	Positive Peak	Negative Peak	USB Limits	Status	
Receiver Level	136 mV	144 mV	Must receive ≤ 150 mV	Must receive ≤ 200 mV	PASS
Squelch Level	132 mV	136 mV	Must not respond < 100 mV	Must not respond < 50 mV	PASS
EL_18 Level	-	-	Device should respond with minimum 12 bit SYNC field	-	PASS

4.8 USB Checklist

A standard USB checklist from the USB Implementers Forum has been populated with information pertaining to the C6748/46/42 and OMAP-L1x8 devices. For more information, see the TMS320DM64xx USB Compliance Checklist (SPRAAT5).

5 References

- *Device High Speed Electrical Test Procedure* - USB Implementers Forum (http://www.usb.org)
- TMS320DM64xx USB Compliance Checklist (SPRAAT5)

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