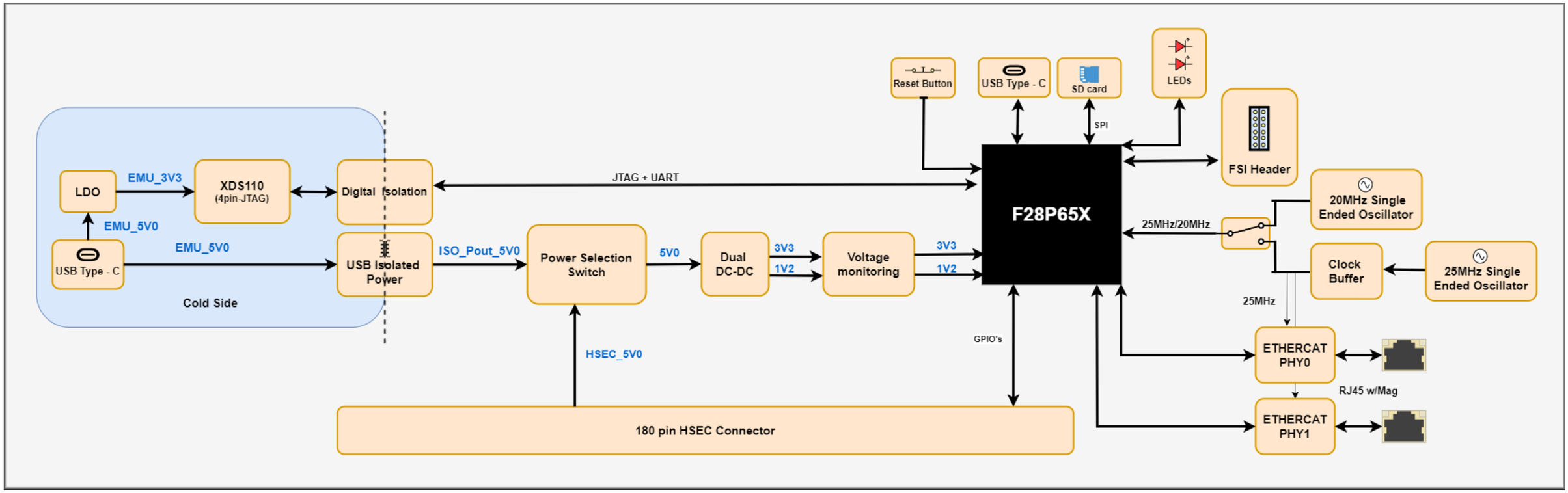
Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	September 12, 2022	UR	Original engineering release
E2	N/A	April 8, 2023	UR	Refer Errata section in the TMDSCNCD28P65X controlCARD Information Guide
A	N/A	June 7, 2023	UR	Cosmetic changes to PCB silk screen
B	N/A	January 2, 2024	UR	Initial F28P650DK9 has ADC issues resolved

1) USB Differential Pairs - 90 Ohm
(A) XDS_D_P and XDS_D_N
(B) USB_D_P (GPIO42) and USB_D_N (GPIO43)

2) ADC Differential pair Impedance Matching - 50 Ohm
(A) HSEC_ADC even pins should match with HSEC_ADC + 1 pin(ie ADC-C2 should match with ADC-C3)
(B) MCU_ADC even pins should match with MCU_ADC + 1 pin(ie MCU_ADC-A0 should match with MCU_ADC-A1)

3) ETHERCAT Differential pairs - 100 Ohm
(A) TD_P and TD_N
(B) RD_P and RD_N

4) CLK Paths - 50 Ohm
(A) F28P65x_25MHz_CLK
(B) PHY0_25MHz_CLK and PHY1_25MHz_CLK



Power to the MCU is either supported by the USB-C on the left or the HSEC 180 pin.

Orderable: TMDSCNCD28P65X		Designed for: Public Release	Mod. Date: 2/26/2024
TID #: N/A		Project Title: F28P65X Control Card	
Number: MCU114	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 002	Sheet: 1 of 11
Drawn By: Uttam Reddy Pailla		File: MCU114B_CoverSheet.SchDoc	Size: B
Engineer: Uttam Reddy Pailla		Contact: http://www.ti.com/support	

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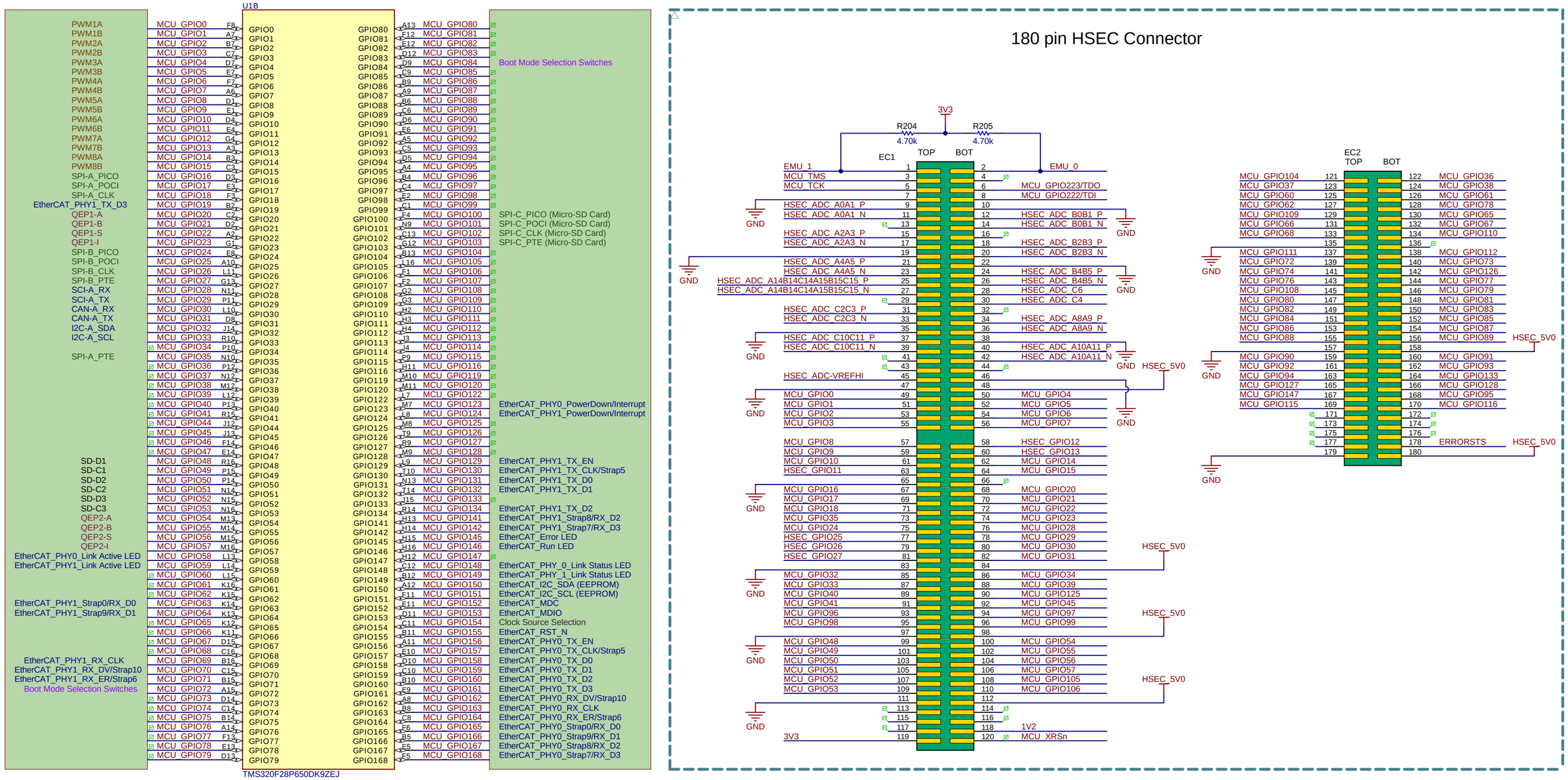

Orderable: TMDSCNCD28P65X		Designed for: Public Release	Mod. Date: 9/27/2023
TID #: N/A		Project Title: F28P65X Control Card	
Number: MCU114	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 002	Sheet: 2 of 11
Drawn By: Uttam Reddy Pailla		File: MCU114B_GPIOs.SchDoc	Size: B
Engineer: Uttam Reddy Pailla		Contact: http://www.ti.com/support	

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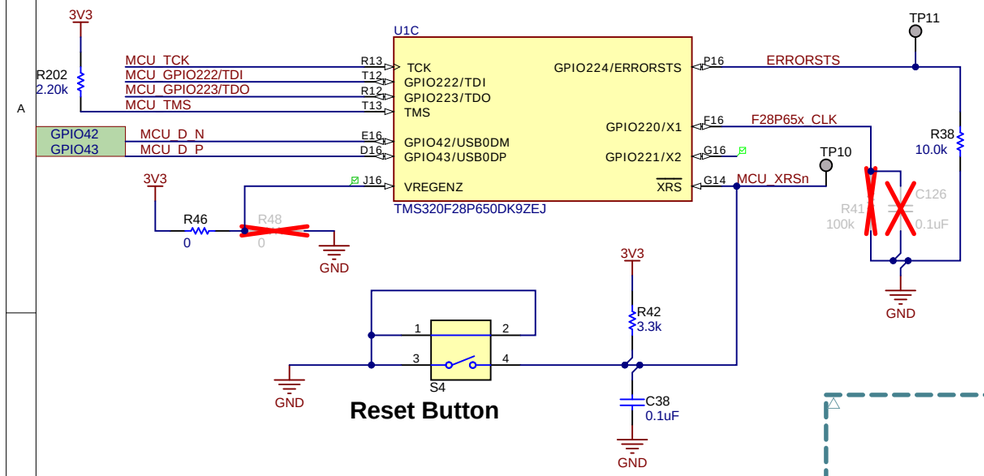
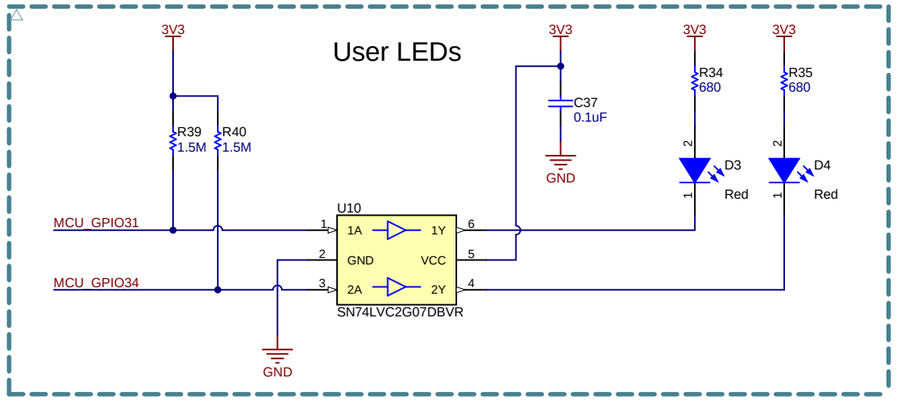
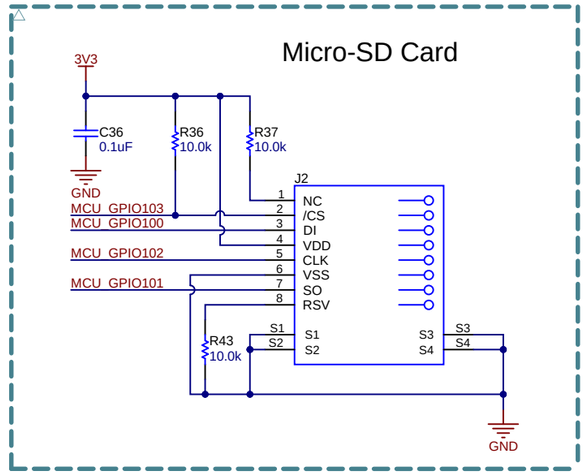
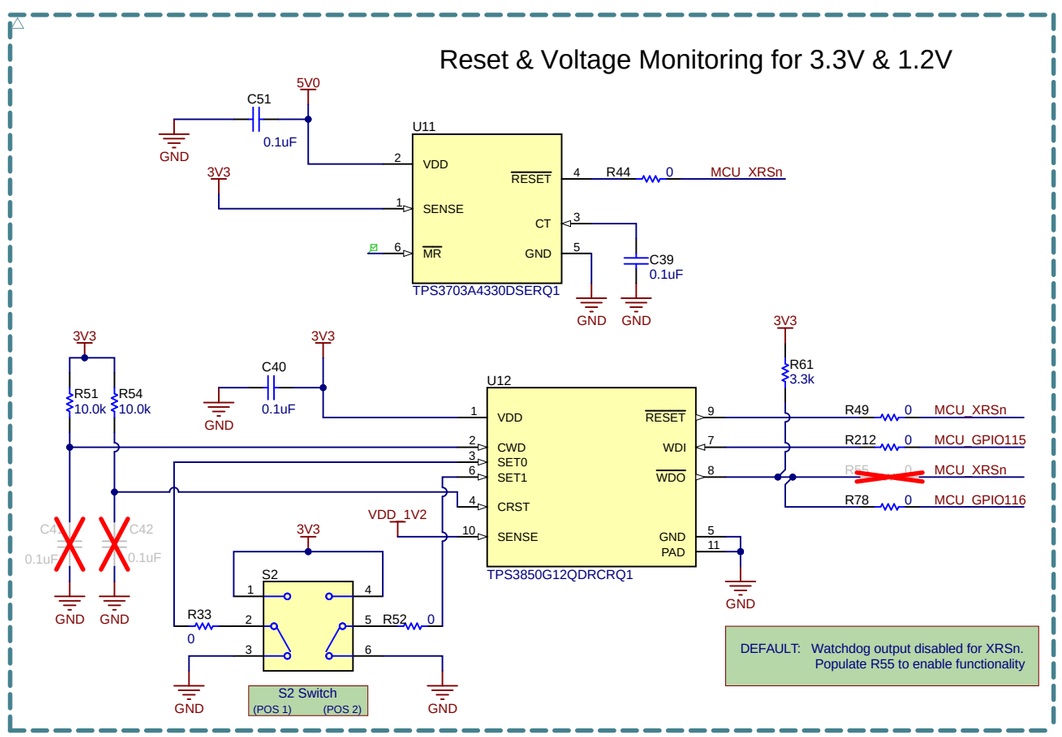
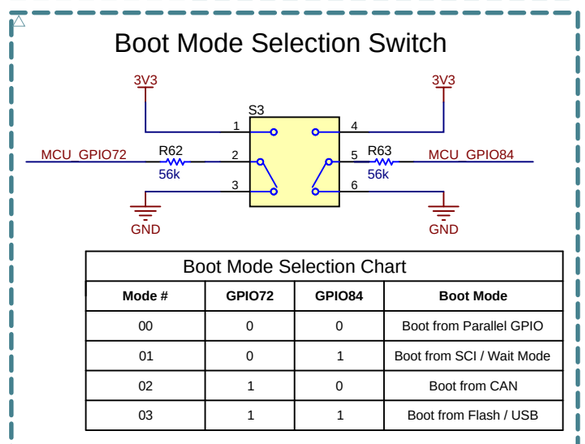








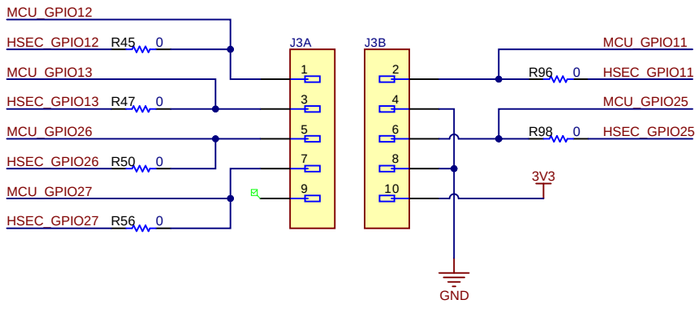


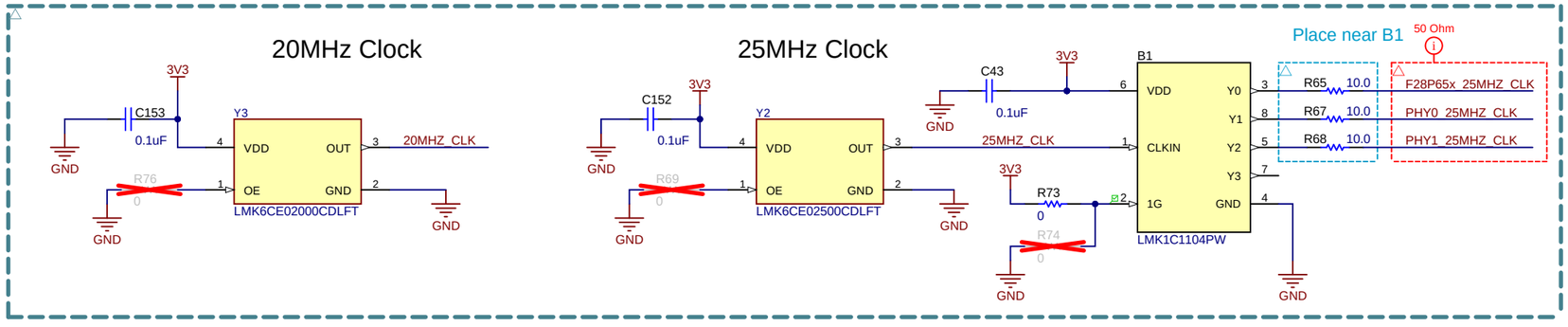
Boot Mode Selection Chart			
Mode #	**GPIO72**	**GPIO84**	**Boot Mode**
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN
03	1	1	Boot from Flash / USB

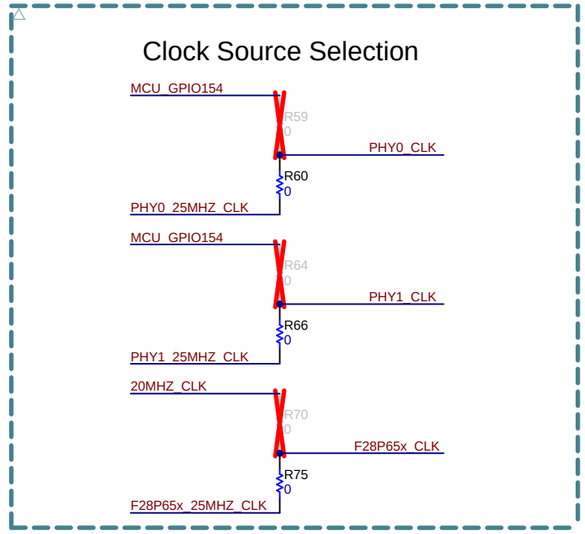
FSI Header

1	FSI-RX_D0	2	FSI-RX_D1/GND
3	FSI-RXCLK	4	GND
5	FSI-TX_D0	6	FSI-TX_D1/GND
7	FSI-TXCLK	8	GND
9	KEY	10	3V3

Pin 9 of J3 is cutoff to key the connector







Orderable: TMDSCNCD28P65X		Designed for: Public Release	Mod. Date: 1/3/2024
TID #: N/A		Project Title: F28P65X Control Card	
Number: MCU114	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 002	Sheet: 3 of 11
Drawn By: Uttam Reddy Pailla		File: MCU114B_Support.SchDoc	Size: B
Engineer: Uttam Reddy Pailla		Contact: http://www.ti.com/support	

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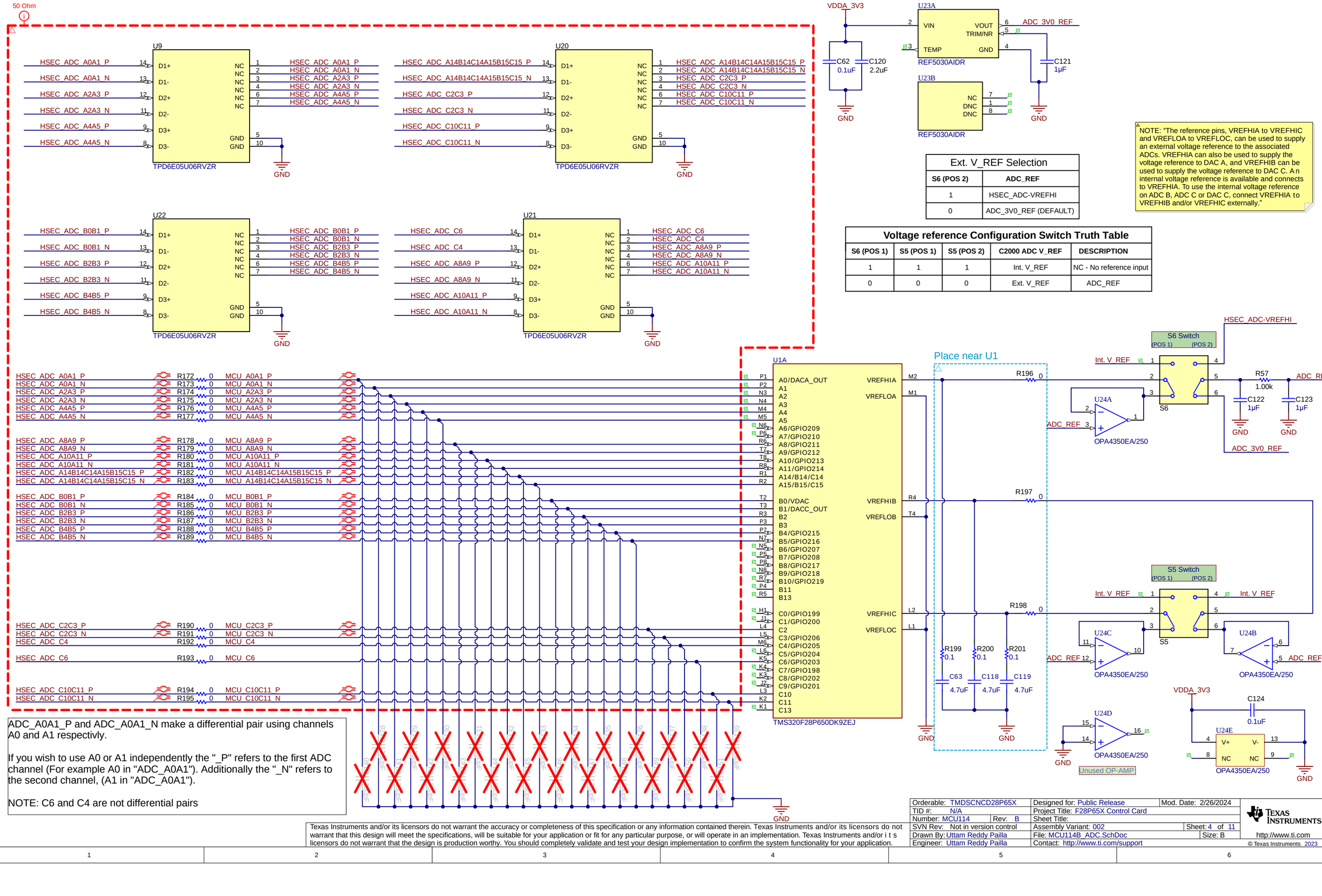
50 Ohm
U9
TPD6E05U06RVZR
U20
TPD6E05U06RVZR
U22
TPD6E05U06RVZR
U21
TPD6E05U06RVZR
GND
HSEC_ADC_A0A1_P
HSEC_ADC_A0A1_N
HSEC_ADC_A2A3_P
HSEC_ADC_A2A3_N
HSEC_ADC_A4A5_P
HSEC_ADC_A4A5_N
HSEC_ADC_A14B14C14A15B15C15_P
HSEC_ADC_A14B14C14A15B15C15_N
HSEC_ADC_C2C3_P
HSEC_ADC_C2C3_N
HSEC_ADC_C10C11_P
HSEC_ADC_C10C11_N
HSEC_ADC_B0B1_P
HSEC_ADC_B0B1_N
HSEC_ADC_B2B3_P
HSEC_ADC_B2B3_N
HSEC_ADC_B4B5_P
HSEC_ADC_B4B5_N
HSEC_ADC_C6
HSEC_ADC_C4
HSEC_ADC_A8A9_P
HSEC_ADC_A8A9_N
HSEC_ADC_A10A11_P
HSEC_ADC_A10A11_N
R172 0 MCU_A0A1_P
R173 0 MCU_A0A1_N
R174 0 MCU_A2A3_P
R175 0 MCU_A2A3_N
R176 0 MCU_A4A5_P
R177 0 MCU_A4A5_N
R178 0 MCU_A8A9_P
R179 0 MCU_A8A9_N
R180 0 MCU_A10A11_P
R181 0 MCU_A10A11_N
R182 0 MCU_A14B14C14A15B15C15_P
R183 0 MCU_A14B14C14A15B15C15_N
R184 0 MCU_B0B1_P
R185 0 MCU_B0B1_N
R186 0 MCU_B2B3_P
R187 0 MCU_B2B3_N
R188 0 MCU_B4B5_P
R189 0 MCU_B4B5_N
R190 0 MCU_C2C3_P
R191 0 MCU_C2C3_N
R192 0 MCU_C4
R193 0 MCU_C6
R194 0 MCU_C10C11_P
R195 0 MCU_C10C11_N
U1A
TMS320F28P650DK9ZEJ
A0/DACA_OUT
A1
A2
A3
A4
A5
A6/GPIO209
A7/GPIO210
A8/GPIO211
A9/GPIO212
A10/GPIO213
A11/GPIO214
A14/B14/C14
A15/B15/C15
B0/VDAC
B1/DACC_OUT
B2
B3
B4/GPIO215
B5/GPIO216
B6/GPIO207
B7/GPIO208
B8/GPIO217
B9/GPIO218
B10/GPIO219
B11
B13
C0/GPIO199
C1/GPIO200
C2
C3/GPIO206
C4/GPIO205
C5/GPIO204
C6/GPIO203
C7/GPIO198
C8/GPIO202
C9/GPIO201
C10
C11
C13
VREFHIA
VREFLOA
VREFHIB
VREFLOB
VREFHIC
VREFLOC
VDDA_3V3
U23A
REF5030AIDR
U23B
REF5030AIDR
C62 0.1uF
C120 2.2uF
C121 1µF
ADC_3V0_REF
NOTE: “The reference pins, VREFHIA to VREFHIC and VREFLOA to VREFLOC, can be used to supply an external voltage reference to the associated ADCs. VREFHIA can also be used to supply the voltage reference to DAC A, and VREFHIB can be used to supply the voltage reference to DAC C. An internal voltage reference is available and connects to VREFHIA. To use the internal voltage reference on ADC B, ADC C or DAC C, connect VREFHIA to VREFHIB and/or VREFHIC externally.”
Ext. V_REF Selection
S6 (POS 2) | ADC_REF
1 | HSEC_ADC-VREFHI
0 | ADC_3V0_REF (DEFAULT)
Voltage reference Configuration Switch Truth Table
S6 (POS 1) | S5 (POS 1) | S5 (POS 2) | C2000 ADC V_REF | DESCRIPTION
1 | 1 | 1 | Int. V_REF | NC - No reference input
0 | 0 | 0 | Ext. V_REF | ADC_REF
Place near U1
R196 0
R197 0
R198 0
R199 0.1
R200 0.1
R201 0.1
C63 4.7uF
C118 4.7uF
C119 4.7uF
S6 Switch
(POS 1) (POS 2)
S5 Switch
(POS 1) (POS 2)
Int. V_REF
HSEC_ADC-VREFHI
R57 1.00k
C122 1µF
C123 1µF
U24A
U24B
U24C
U24D
U24E
OPA4350EA/250
ADC_REF
ADC_3V0_REF
C124 0.1uF
Unused OP-AMP
ADC_A0A1_P and ADC_A0A1_N make a differential pair using channels A0 and A1 respectivly.
If you wish to use A0 or A1 independently the "_P" refers to the first ADC channel (For example A0 in "ADC_A0A1"). Additionally the "_N" refers to the second channel, (A1 in "ADC_A0A1").
NOTE: C6 and C4 are not differential pairs
Orderable: TMDSCNCD28P65X
TID #: N/A
Number: MCU114 Rev: B
SVN Rev: Not in version control
Drawn By: Uttam Reddy Pailla
Engineer: Uttam Reddy Pailla
Designed for: Public Release
Project Title: F28P65X Control Card
Sheet Title:
Assembly Variant: 002
File: MCU114B_ADC.SchDoc
Contact: http://www.ti.com/support
Mod. Date: 2/26/2024
Sheet: 4 of 11
Size: B
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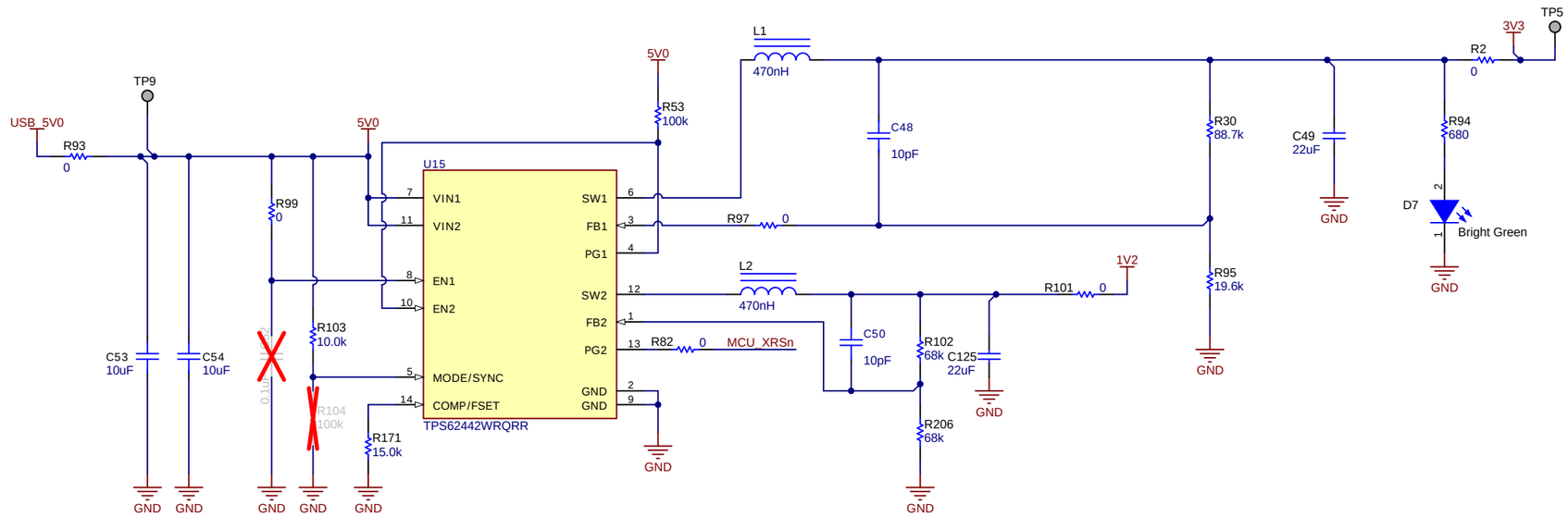
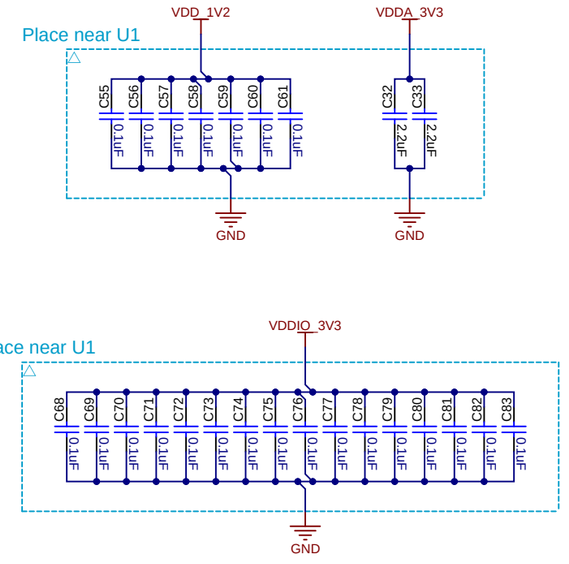
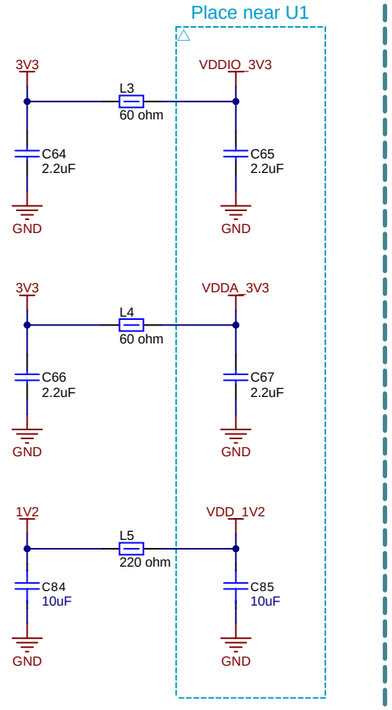
Dual DC-DC (5V to 3.3V & 1.2V)

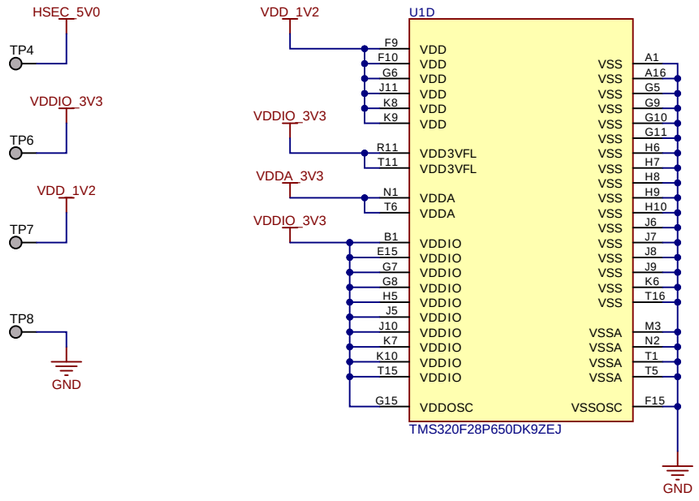


Decoupling Capacitors



Ferrite Beads

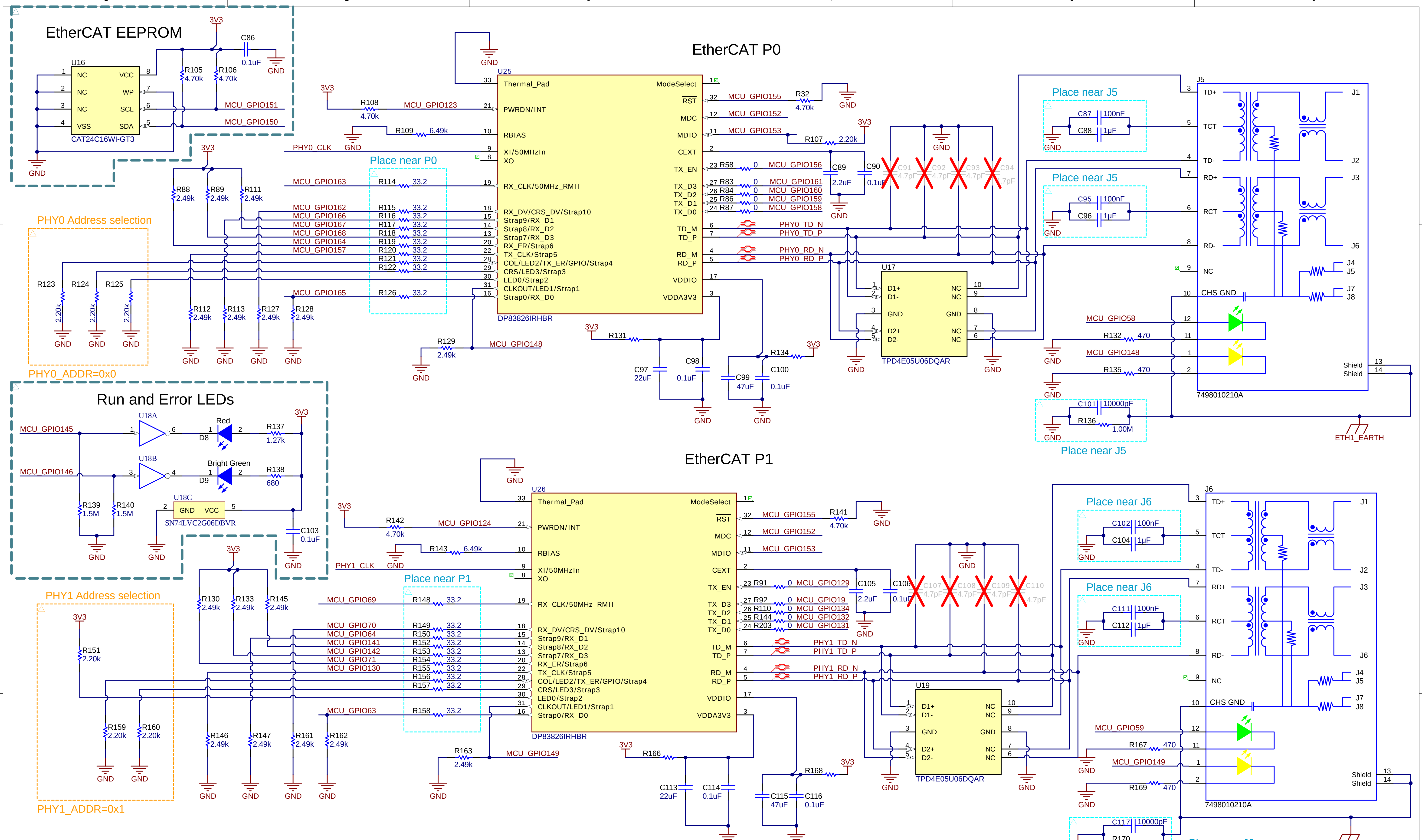




NOTES:

1) TPS62442 Dual DC-DC provides an output current of 2A/2A or 3A/1A, this amount of current capacity should not be necessary for certain applications using F28P65x. This is just necessary for the control card design
2) Alternative part: TPS62441 Dual DC-DC provides an output current of 1A/1A
3) DC-DC can be used without supervisory circuit in specific applications by considering the slew rates of MCU and DC-DC for proper reset.

Orderable: TMDSCNCD28P65X		Designed for: Public Release	Mod. Date: 2/26/2024
TID #: N/A		Project Title: F28P65X Control Card	
Number: MCU114	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 002	Sheet: 5 of 11
Drawn By: Uttam Reddy Pailla		File: MCU114B_Power.SchDoc	Size: B
Engineer: Uttam Reddy Pailla		Contact: http://www.ti.com/support	



Refer Application Notes for PHY boot strapping configuration:
https://www.ti.com/lit/snla344

Orderable: TMDSCNCD28P65X	Designed for: Public Release
TID #: N/A	Mod. Date: 4/5/2023
Number: MCU114	Rev: B
SVN Rev: Not in version control	Project Title: F28P65X Control Card
Drawn By: Uttam Reddy Pailla	Sheet Title:
Engineer: Uttam Reddy Pailla	Assembly Variant: 002
Sheet: 6 of 11	Size: B
File: MCU114B_EtherCAT.SchDoc	Contact: http://www.ti.com/support

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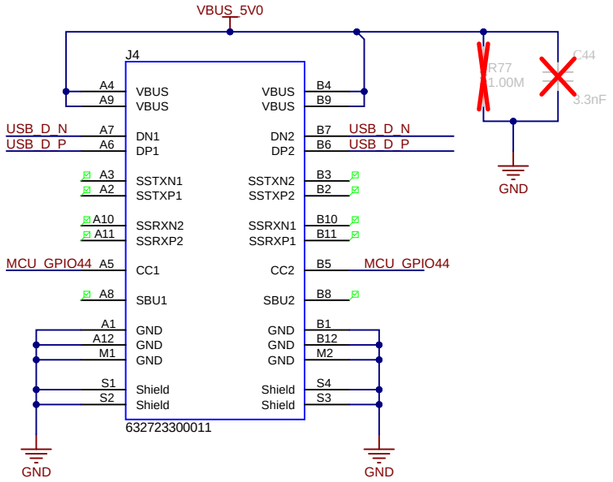
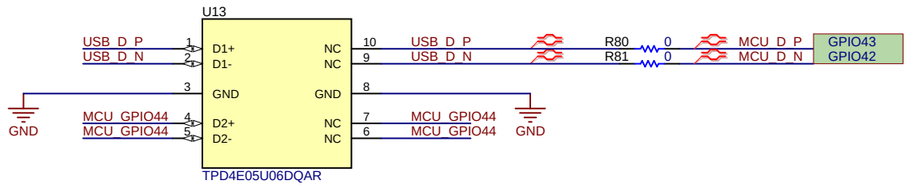
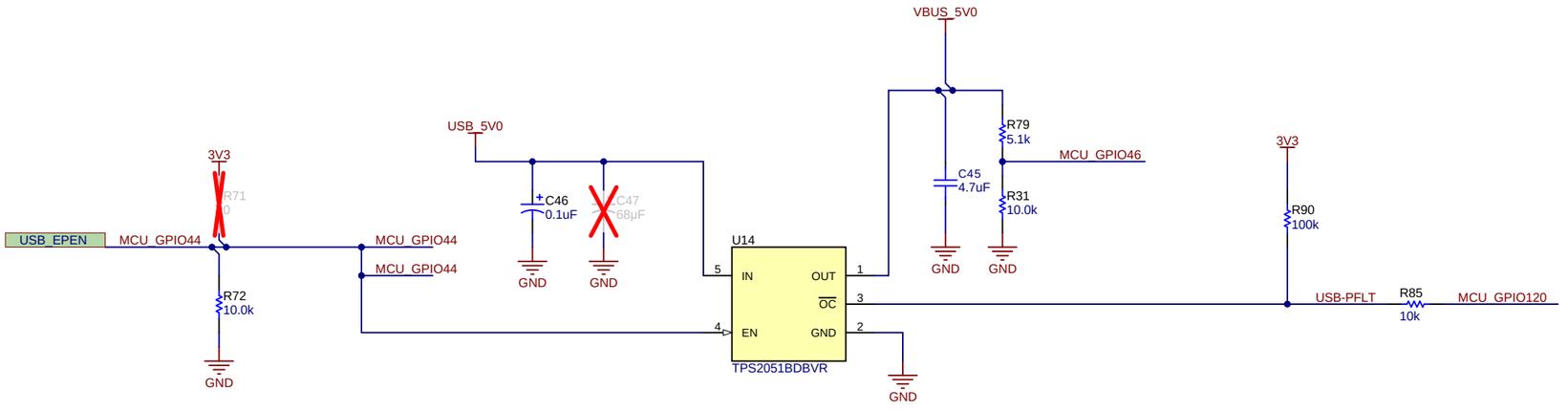
USB- Type C Connector - Data Peripheral to MCU







Switch Truth Table		
MCU_GPIO44 STATUS	DESCRIPTION	USB_MODE
1 (HIGH)	UB_CC1 & USB_CC2 are pulled up	Host mode - DFP
0 (LOW)	UB_CC1 & USB_CC2 are strongly pulled down	Device mode - UFP (DEFAULT)

NOTE: USB VBUS_5V0, PFLT & EPEN do not have a specific mux position in this device.

In this controlCARD, a standard GPIO is used to detect changes to these signals.

NOTE: for TYPE C, the USB2.0 OTG device is referred as a Dual Role Port (DRP)

DRP can function either as a USB host or USB peripheral, the selection choice depends on the channel configuration (CC1/CC2).
1. USB host (DFP) - Use pull-up resistors on CC1/CC2 ; Provides Vbus to the attached peripheral
2. USB peripheral (UFP) -Use pull-down resistors on CC1/CC2 ; monitors Vbus to establish a data connection and/or power on board circuits

Orderable: TMDSCNCD28P65X		Designed for: Public Release	Mod. Date: 2/27/2024
TID #: N/A		Project Title: F28P65X Control Card	
Number: MCU114	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 002	Sheet: 7 of 11
Drawn By: Uttam Reddy Pailla		File: MCU114B_USB.SchDoc	Size: B
Engineer: Uttam Reddy Pailla		Contact: http://www.ti.com/support	

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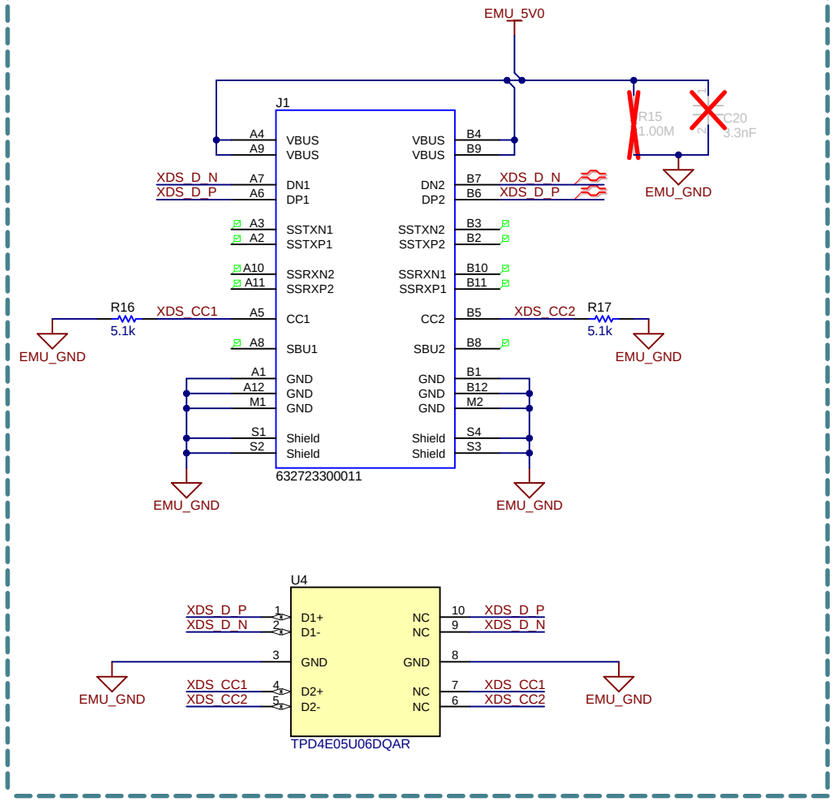
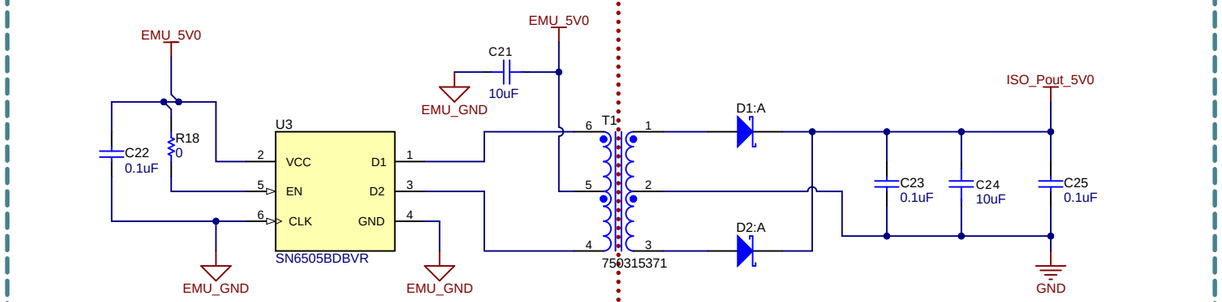
USB- Type C Connector - XDS110

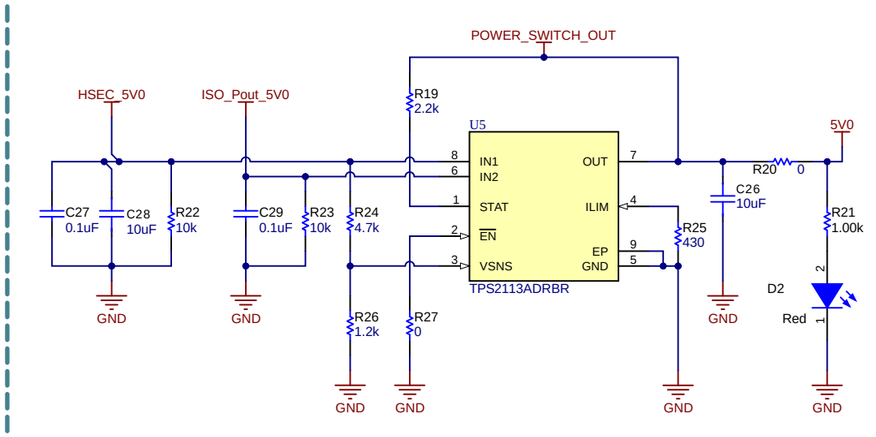


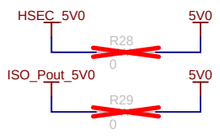
(Cold Side) (Hot Side)

USB Isolated Power



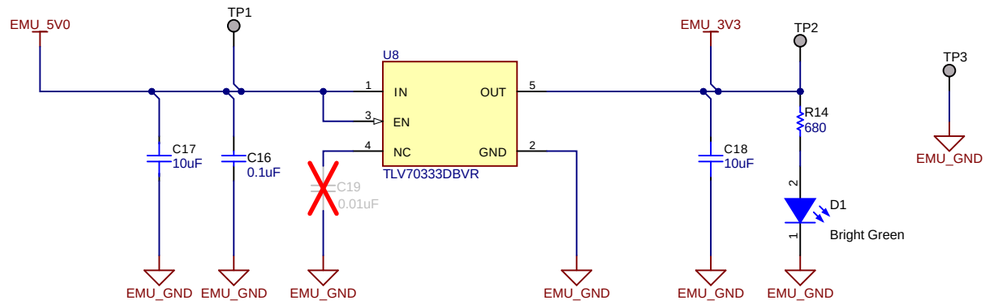
Power Selection Switch





Switch Truth Table		
HSEC_5V0 > 4V	ISO_Pout_5V0 > HSEC_5V0	POWER_SWITCH_OUT
Yes	X	HSEC_5V0
No	No	HSEC_5V0
No	Yes	ISO_Pout_5V0

LDO_5V0_3V3



Orderable: TMDSCNCD28P65X		Designed for: Public Release	Mod. Date: 11/3/2023
TID #: N/A		Project Title: F28P65X Control Card	
Number: MCU114	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 002	Sheet: 8 of 11
Drawn By: Uttam Reddy Pailla		File: MCU114B_XDS110_USB_Power.SchDoc	Size: B
Engineer: Uttam Reddy Pailla		Contact: http://www.ti.com/support	

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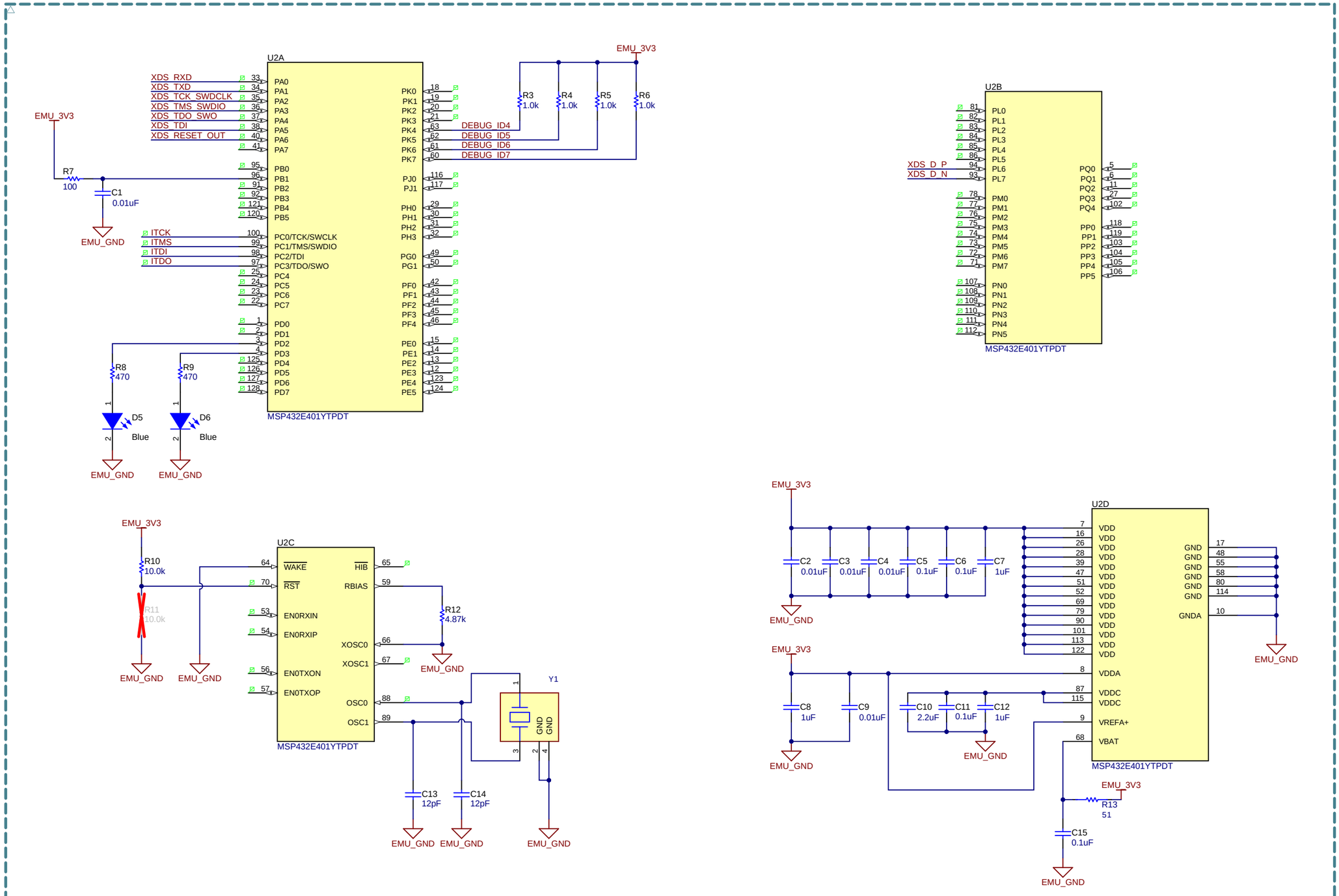

Orderable: TMDSCNCD28P65X		Designed for: Public Release	Mod. Date: 9/27/2023
TID #: N/A		Project Title: F28P65X Control Card	
Number: MCU114	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 002	Sheet: 9 of 11
Drawn By: Uttam Reddy Pailla		File: MCU114B_XDS110_MCU.SchDoc	Size: B
Engineer: Uttam Reddy Pailla		Contact: http://www.ti.com/support	

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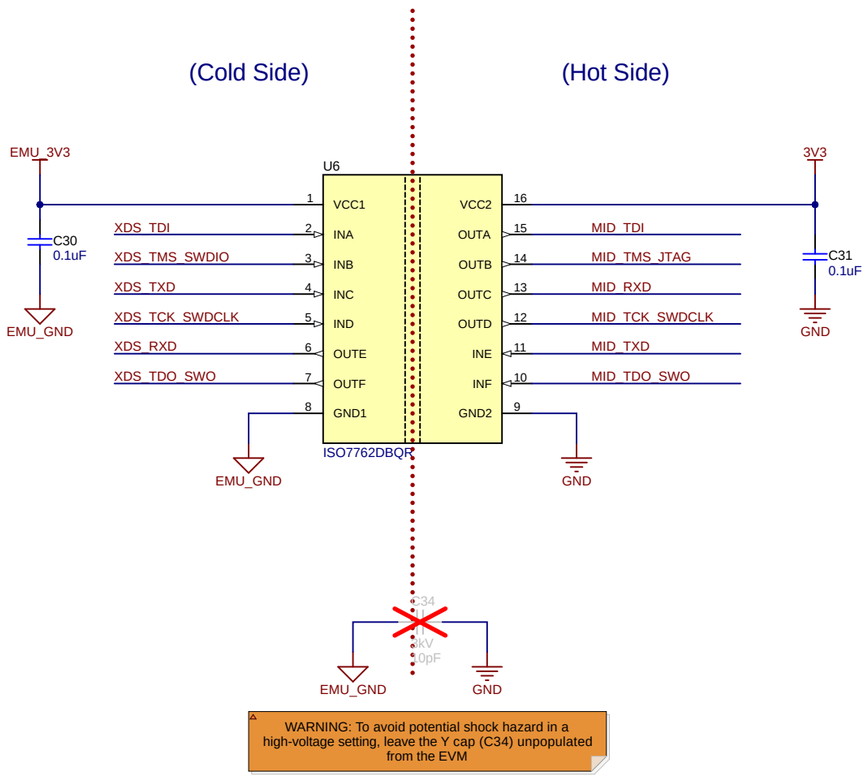
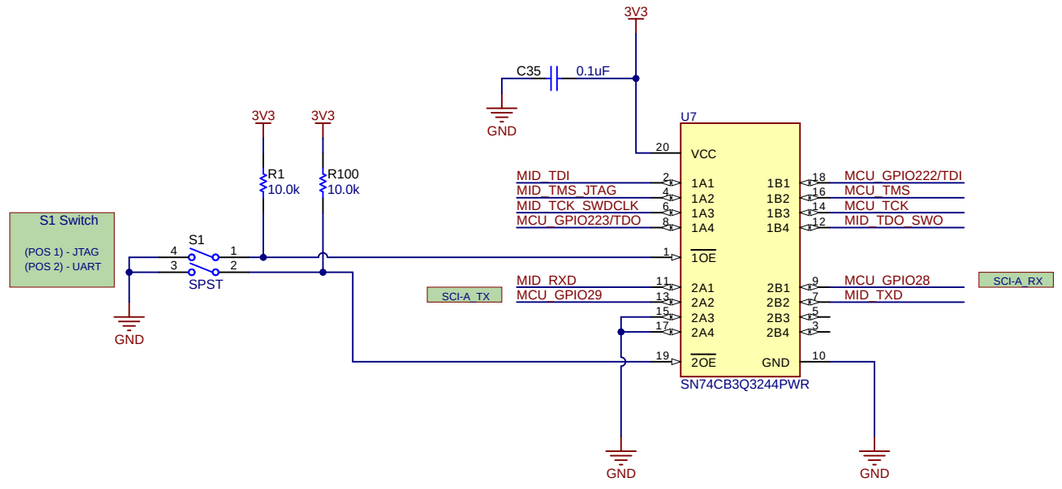
NOTE: In this design JTAG signals are isolated.
cJTAG is not suppported on this control card.



WARNING: To avoid potential shock hazard in a high-voltage setting, leave the Y cap (C34) unpopulated from the EVM

S1 - JTAG Emulation & UART Switch

POS 1 ON: Use XDS110 emulator that is on the cCARD
POS 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard
POS 2 ON: GPIOs 28 & 29 will be connected to the USB-to-UART adapter on the XDS110 emulator
POS 2 OFF: GPIOs 28 & 29 are disconnected from the USB-to-UART adapter on the XDS110 emulator and connected to the HSEC connector pins



Orderable: TMDSCNCD28P65X		Designed for: Public Release	Mod. Date: 11/3/2023
TID #: N/A		Project Title: F28P65X Control Card	
Number: MCU114	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 002	Sheet: 10 of 11
Drawn By: Uttam Reddy Pailla		File: MCU114B_Emulator_Interface.SchDoc	Size: B
Engineer: Uttam Reddy Pailla		Contact: http://www.ti.com/support	

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FID1 FID2 FID3 FID4 FID5 FID6

PCB Number: MCU114
PCB Rev: B

CE Mark

PCB LOGO
Texas Instruments

PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

PCB LOGO
ETHERCAT LABEL

Variant/Label Table	
Variant	Label Text
001	TMDSCNCD28P65X - 20MHz CLK
002	TMDSCNCD28P65X - 25MHz CLK

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: TMDSCNCD28P65X	Designed for: Public Release	Mod. Date: 9/27/2023
TID #: N/A	Project Title: F28P65X Control Card	
Number: MCU114 Rev: B	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 002	Sheet: 11 of 11
Drawn By: Uttam Reddy Pailla	File: MCU114B_EVM_Hardware.SchDoc	Size: B
Engineer: Uttam Reddy Pailla	Contact: http://www.ti.com/support	

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