OMAP5912 Multimedia Processor Clocks Reference Guide

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Preface

Read This First

About This Manual

This document describes the clocking mechanisms of the OMAP5912 multimedia processor.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

The following documents describe the OMAP5910 device and related peripherals. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

OMAP5912 Multimedia Processor Device Overview and Architecture Reference Guide (literature number SPRU748) introduces the setup, components, and features of the OMAP5912 multimedia processor and provides a high-level view of the device architecture.

OMAP5912 Multimedia Processor OMAP 3.2 Subsystem Reference Guide (literature number SPRU749) introduces and briefly defines the main features of the OMAP3.2 subsystem of the OMAP5912 multimedia processor.

OMAP5912 Multimedia Processor DSP Sybsystem Reference Guide (literature number SPRU750) describes the OMAP5912 multimedia processor DSP subsystem. The digital signal processor (DSP) subsystem is built around a core processor and peripherals that interface with: 1) The ARM926EJS via the microprocessor unit interface (MPUI); 2) Various standard memories via the external memory interface (EMIF); 3) Various system peripherals via the TI peripheral bus (TIPB) bridge.

OMAP5912 Multimedia Processor Clocks Reference Guide (literature number SPRU751) describes the clocking mechanisms of the OMAP5912 multimedia processor. In OMAP5912, various clocks are created from special components such as the digital phase locked loop (DPLL) and the analog phase-locked loop (APLL).

OMAP5912 Multimedia Processor Initialization Reference Guide (literature number SPRU752) describes the reset architecture, the configuration, the initialization, and the boot ROM of the OMAP5912 multimedia processor.

OMAP5912 Multimedia Processor Power Management Reference Guide (literature number SPRU753) describes power management in the OMAP5912 multimedia processor. The ultralow-power device (ULPD) generates and manages clocks and reset signals to OMAP3.2 and to some peripherals. It controls chip-level power-down modes and handles chip-level wake-up events. In deep sleep mode, this module is still active to monitor wake-up events.This book describes the ULPD module and outline architecture.

OMAP5912 Multimedia Processor Security Features Reference Guide (literature number SPRU754) describes the security features of teh OMAP5912 multimedia processor. The OMAP5912 security scheme relies on the OMAP3.2 secure mode. The distributed security on the OMAP3.2 platform is a Texas Instruments solution to address m-commerce and security issues within a mobile phone environment. The OMAP3.2 secure mode was developed to bring hardware robustness to the overall OMAP5912 security scheme.

OMAP5912 Multimedia Processor Direct Memory Access (DMA) Support Reference Guide (literature number SPRU755) describes the direct memory access support of the OMAP5912 multimedia processor. The OMAP5912 processor has three DMAs:

- The system DMA is embedded in OMAP3.2. It handles DMA transfers associated with MPU and shared peripherals.
- The DSP DMA is embedded in OMAP3.2. It handles DMA transfers associated with DSP peripherals.
- The generic distributed DMA (GDD) is an OMAP5912 resource attached to the SSI peripheral. It handles only DMA transfers associated with the SSI peripheral.

OMAP5912 Multimedia Processor Memory Interfaces Reference Guide (literature number SPRU756) describes the memory interfaces of the OMAP5912 multimedia processor.

- SDRAM (external memory interface fast, or EMIFF)
- Asynchronous and synchronous burst memory (external memory interface slow, or EMIFS)
- NAND flash (hardware controller or software controller)
- CompactFlash on EMIFS interface
- Internal static RAM

OMAP5912 Multimedia Processor Interrupts Reference Guide (literature number SPRU757) describes the interrupts of the OMAP5912 multimedia processor. Three level 2 interrupt controllers are used in OMAP5912:

- One MPU level 2 interrupt handler (also referred to as MPU interrupt level 2) is implemented outside of OMAP3.2 and can handle 128 interrupts.
- One DSP level 2 interrupt handler (also referred to as DSP interrupt level 2.1) is instantiated outside of OMAP3.2 and can handle 64 interrupts.
- One OMAP3.2 DSP level 2 interrupt handler (referenced as DSP interrupt level 2.0) can handle 16 interrupts.

OMAP5912 Multimedia Processor Peripheral Interconnects Reference Guide (literature number SPRU758) describes various periperal interconnects of the OMAP5912 multimedia processor.

OMAP5912 Multimedia Processor Timers Reference Guide (literature number SPRU759) describes various timers of the OMAP5912 multimedia processor.

OMAP5912 Multimedia Processor Serial Interfaces Reference Guide (literature number SPRU760) describes the serial interfaces of the OMAP5912 multimedia processor.

OMAP5912 Multimedia Processor Universal Serial Bus (USB) Reference Guide (literature number SPRU761) describes the universal serial bus (USB) host on the OMAP5912 multimedia processor. The OMAP5912 processor provides several varieties of USB functionality. Flexible multiplexing of signals from the OMAP5912 USB host controller, the OMAP5912 USB function controller, and other OMAP5912 peripherals allow a wide variety of system-level USB capabilities. Many of the OMAP5912 pins can be used for USB-related signals or for signals from other OMAP5912 peripherals. The OMAP5912 top-level pin multiplexing

controls each pin individually to select one of several possible internal pin signal interconnections. When these shared pins are programmed for use as USB signals, the OMAP5912 USB signal multiplexing selects how the signals associated with the three OMAP5912 USB host ports and the OMAP5912 USB function controller can be brought out to OMAP5912 pins.

OMAP5912 Multimedia Processor Multi-channel Buffered Serial Ports (McBSPs) Reference Guide (literature number SPRU762) describes the three multi-channel buffered serial ports (McBSPs) available on the OMAP5912 device. The OMAP5912 device provides multiple high-speed multichannel buffered serial ports (McBSPs) that allow direct interface to codecs and other devices in a system.

OMAP5912 Multimedia Processor Camera Interface Reference Guide (literature number SPRU763) describes two camera inerfaces implemented in the OMAP5912 multimedia processor: compact serial camera port and camera parallel interface.

OMAP5912 Multimedia Processor Display Interface Reference Guide (literature number SPRU764) describes the display interface of the OMAP5912 multimedia processor.

- LCD module
- LCD data conversion module
- LED pulse generator
- Display interface

OMAP5912 Multimedia Processor Multimedia Card (MMC/SD/SDIO) (literature number SPRU765) describes the multimedia card (MMC) interface of the OMAP5912 multimedia processor. The multimedia card/secure data/secure digital IO (MMC/SD/SDIO) host controller provides an interface between a local host, such as a microprocessor unit (MPU) or digital signal processor (DSP), and either an MMC or SD memory card, plus up to four serial flash cards. The host controller handles MMC/SD/SDIO or serial port interface (SPI) transactions with minimal local host intervention.

OMAP5912 Multimedia Processor Keyboard Interface Reference Guide (literature number SPRU766) describes the keyboard interface of the OMAP5912 multimedia processor. The MPUIO module enables direct I/O communication between the MPU (through the public TIPB) and external devices. Two types of I/O can be used: specific I/Os dedicated for 8 x 8 keyboard connection, and general-purpose I/Os.

OMAP5912 Multimedia Processor General-Purpose Interface Reference Guide (literature number SPRU767) describes the general-purpose in-

terface of the OMAP5912 multimedia processor. There are four GPIO modules in the OMAP5912. Each GPIO peripheral controls 16 dedicated pins configurable either as input or output for general purposes. Each pin has an independent control direction set by a programmable register. The two−edge control registers configure events (rising edge, falling edge, or both edges) on an input pin to trigger interrupts or wake−up requests (depending on the system mode). In addition, an interrupt mask register masks out specified pins. Finally, the GPIO peripherals provide the set and clear capabilities on the data output registers and the interrupt mask registers. After detection, all event sources are merged and a single synchronous interrupt (per module) is generated in active mode, whereas a unique wake−up line is issued in idle mode. Eight data output lines of the GPIO3 are ORed together to generate a global output line at the OMAP5912 boundary. This global output line can be used in conjunction with the SSI to provide a CMT−APE interface to the OMAP5912.

OMAP5912 Multimedia Processor VLYNQ Serial Communications Interface Reference Guide (literature number SPRU768) describes the VLYNQ of the OMAP5912 multimedia processor.

VLYNQ is a serial communications interface that enables the extension of an internal bus segment to one or more external physical devices. The external devices are mapped into local, physical address space and appear as if they are on the internal bus of the OMAP 5912. The external devices must also have a VLYNQ interface. The VLYNQ module serializes bus transactions in one device, transfers the serialized data between devices via a VLYNQ port, and de-serializes the transaction in the external device.

OMAP5912 includes one VLYNQ module connected on OCPT2 target port and OCPI initiator port. These connections are configured via a static switch, which selects either SSI or VLYNQ module. This switch, forbids the simultaneous use of GDD/SSI and VLYNQ. TThe switch is controlled by the VLYNQ_EN bit in the OMAP5912 configuration control register (CONF_5912_CTRL).

OMAP5912 Multimedia Processor Pinout Reference Guide (literature number SPRU769) provides the pinout of the OMAP5912 multimedia processor. After power-up reset, the user can change the configuration of the default interfaces. If another interface is available on top of the default, it is possible to enable a new interface for each ball by setting the corresponding 3-bit field of the associated FUNC_MUX_CTRL register. It is also possible to configure on-chip pullup/pulldown. This document

also describes the various power domains so that the user can apply the different interfaces seamlessly with external components.

OMAP5912 Multimedia Processor Window Tracer (WT) Reference Guide (literature number SPRU770) describes the window tracer module used to capture the memory transactions from four interfaces: EMIFF, EMIFS, OCP-T1, and OCP-T2. This module is located in the OMAP3.2 traffic controller (TC).

OMAP5912 Multimedia Processor Real-Time Clock Reference Guide (literature number SPRUxxx) describes the real-time clock of the OMAP5912 multimedia processor. The real-time clock (RTC) block is an embedded real-time clock module directly accessible from the TIPB bus interface.

Trademarks

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Clocks

This document describes the clocking mechanisms of the OMAP5912 multimedia processor.

1 Overview

In OMAP5912, various clocks are created from special components such as the digital phase locked loop (DPLL) and the analog phase-locked loop (APLL).

- The DPLL converts the input clock (12 MHz–20 MHz) to a high-frequency clock (200 MHz), which is then distributed within OMAP 3.2 gigacell and to the various on-chip peripherals.

  At power-up reset, the DPLL is in bypass mode and acts as a clock divider. The desired frequency for the DPLL output clock is achieved by enabling the DPLL and setting the multiplication and divider ratios.

Note:

At power-up reset, the DPLL, by default, is in divide-by-one mode.

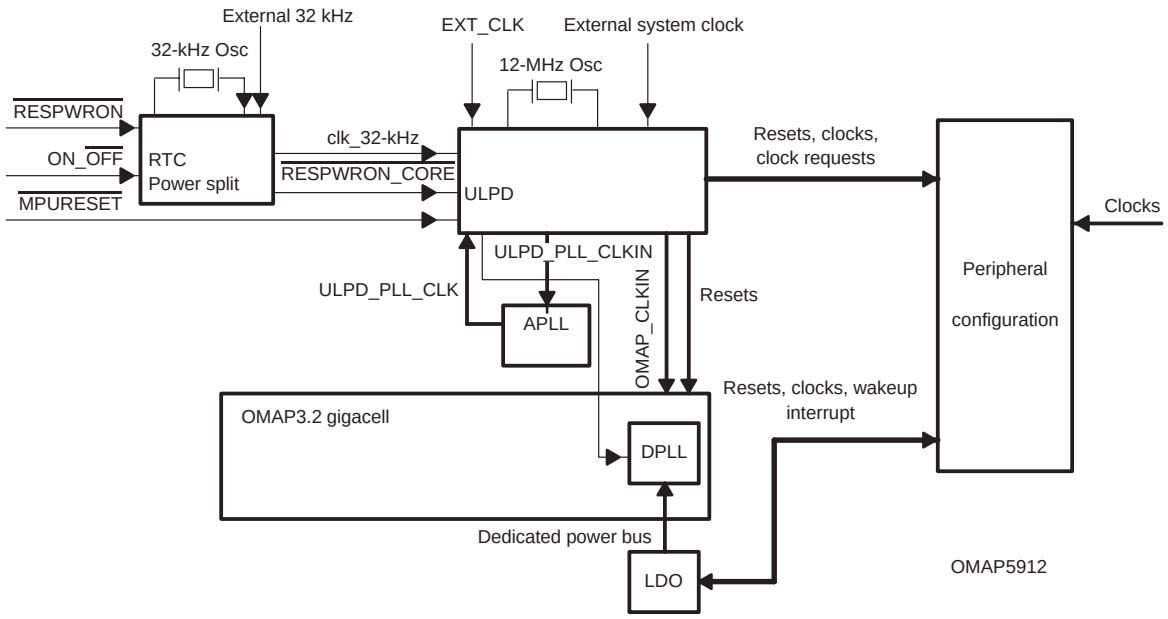
  The input clock is provided by an external device or is derived from the on-chip 12-MHz oscillator. For more details, see Chapter 5, *Initialization*.

  An embedded LDO provides a dedicated power supply to the analog portion of the DPLL to ensure low jitter on the DPLL output clock. The regular core voltage supplies the wrapper of the DPLL. The OMAP5912 configuration modules control the LDO and observe its state.

- The APLL is a clock multiplier that provides a fixed 96-MHz clock from the same input clock used to feed the DPLL. The input clock frequency is 12 MHz, 13 MHz, or 19.2 MHz. The APLL is enabled whenever the ULPD requests a 48-MHz clock. The ULPD_PLL_CTRL_STATUS register is set to ensure the multiplication factor. The 48-MHz frequency is then achieved by a divide-by-2 cell in the ULPD.

Figure 1 shows the OMAP5912 global-clocking environment.

Figure 1. OMAP5912 Clocks



1.1 OMAP5912 Integration

1.1.1 Low-Dropout (LDO) Voltage Regulator

After the power supplies have ramped up and the power-up reset has been released, the LDO ramps up. When its output voltage is no more than 200 mV below its final value, the LDO delivers a steady signal set to 1 to the ULPD. The DPLL is configured in DPLL enable mode, as the LDO output voltage is stable.

Before entering low-power modes such as deep sleep and big sleep, the LDO is put in sleep mode to reduce power dissipation. In that mode, the LDO delivers a voltage derived from the VDD core through a pass-gate transistor. Although the DPLL is in low-power mode, the DPLL settings stay the same. In this configuration, the latency is reduced with returning to active mode.

The LDO can be powered down, where it behaves as a feed-through cell. Power to the DPLL must be provided through an external power supply source. This mode can also be a back-up mode if an external power supply is preferred (see Table 1).

Table 1. LDO Control and Observability

LDO Mode	Signal	Register Bit Description	Notes
LDO in power-down mode	PWRDWN	CONF_LDO_PWRDN_CNTRL_R	OMAP5912 configuration
LDO in sleep mode	SLEEP	SOFT_LDO_SLEEP	ULPD register file
LDO stable	STEADY	LDO_STEADY	ULPD register file

1.1.2 96-MHz APLL

The APLL is enabled whenever a clock request for a 48-MHz clock is active. The clock request can be either hardware or software. The APLL generates a 96-MHz clock, which is then divided by 2 in the ULPD module. An external 48-MHz clock can be selected by software if the APLL is not used.

Table 2 lists the different requests to activate the APLL. When no request is active, the APLL is in power-down mode.

Table 2. Request for 48-MHz Clock

Request	Source	Type of Request	Destination Module
CONF_MOD_UART1_CLK_MODE_R	OMAP5912 configuration	Software	UART1
CONF_MOD_UART2_CLK_MODE_R	OMAP5912 configuration	Software	UART2
CONF_MOD_UART3_CLK_MODE_R	OMAP5912 configuration	Software	UART3
CONF_MOD_USB_HOST_HHC_UHOST_EN_R	OMAP5912 configuration	Software	USB OTG
USB_DPLL_MCLK_REQ	USB OTG	Hardware	USB OTG
CONF_MOD_MMC_SD_CLK_REQ_R	OMAP5912 configuration	Software	MMC/SDIO1
CONF_MOD_MMC_SD2_CLK_REQ_R	OMAP5912 configuration	Software	MMC/SDIO2
CONF_CAM_CLKMUX_R	OMAP 5912 configuration	Software	Camera I/F

The selection of the APLL modes is done in the ULPD module, as shown in Table 3.

Table 3. APLL Mode Selection

APLL SEL2	APLL SEL1	APLL SEL0	CLKIN (MHz)	CLKOUT (MHz)	APLL MODE	ULPD_PLL_CTRL_STATUS[2:0]
L	L	L	19.2	96	Application mode 0	000
L	H	L	13	96	Application mode 2	010
L	H	H	12	96	Application mode 3	011

The reset value is 011, which selects APLL application mode 3. The LOCK_STATUS flag in the ULPD_PLL_CTRL_STATUS register indicates that the APLL has locked.

The internally generated 48-MHz clock or an external 48-MHz clock are selected via the TEST_DBG_CTRL_0 bit in the OMAP5912 configuration. If the TEST_DBG_CTRL_0 bit is set to 1, GPIO_14 becomes the source of the 48 MHz for the device.

1.1.3 OMAP3.2 DPLL

The DPLL is controlled through the DPLL1_CTL_REG, which is mapped in the OMAP3.2 register file. See Section 3, *OMAP3.2 DPLL,* for more detail.

2 Analog Phase-Locked Loop

The APLL is a clock multiplier for creating a 96-MHz clock from 12-MHz, 13-MHz, and 19.2-MHz input frequencies.

It includes an APLL circuit to generate an output clock, which is related to the frequency of the input reference clock. The frequency multiplication factor is an integer (12 MHz/19.2 MHz to 96 MHz) or a fractional (13 MHz−96 MHz):

- In the integer multiplication scheme, the rising edge of the output clock is synchronized to the rising edge of the input clock.
- In the fractional multiplication scheme, the rising edge of the output clock is not synchronized to the rising edge of the input clock for all input clock periods. Nevertheless, the cell produces pulses to notify when the rising edges of the input and output clocks coincide.

This output can be used to decimate the cycles where the phase relationship between input and output clocks is unknown.

Dedicated power supply pins are required to isolate the core analog circuit from the switching noise generated by the core logic that can cause jitter on the clock output signal.

The cell has level shifters on all input ports to avoid through-current when V_{DD} and V_{DDA} are not at the same voltage. Natural level shifting is done at the cell outputs to provide V_{DDA}-compatible CMOS levels.

Three modes of operation and one power-down mode can be selected from the core inputs:

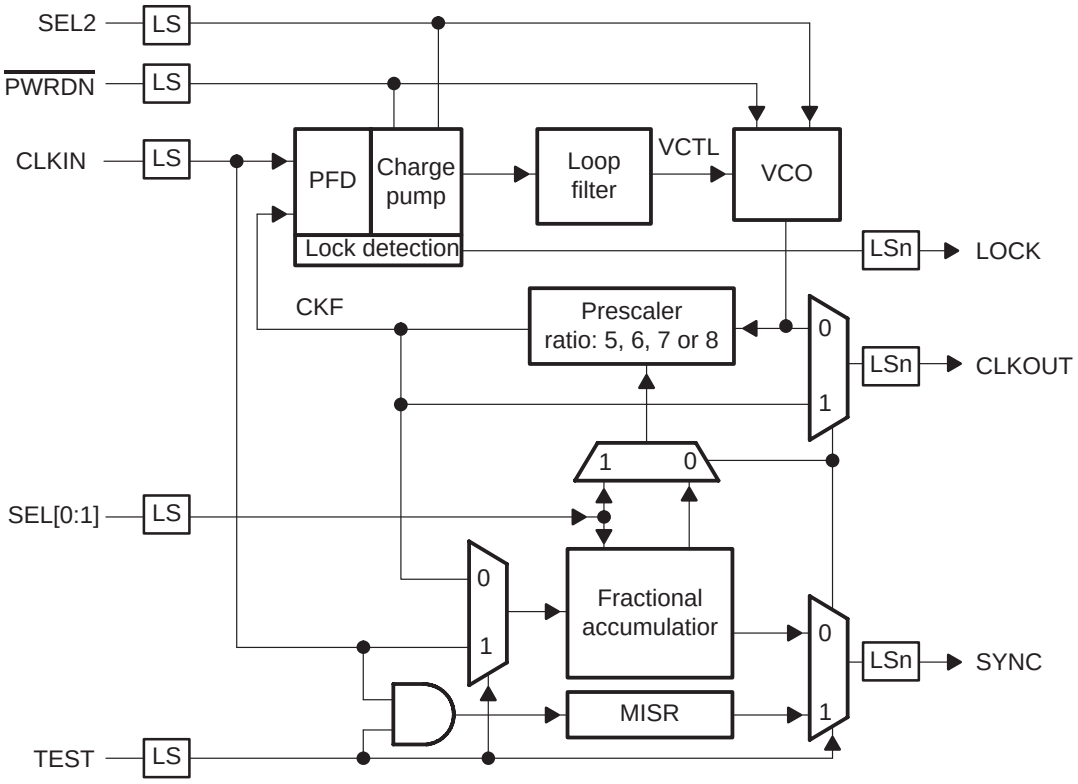
- Application mode 0: The input frequency is 19.2 MHz, and the multiplication factor is 5.
- Application mode 2: The input frequency is 13 MHz, and the multiplication factor is 96/13.
- Application mode 3: The input frequency is 12 MHz, and the multiplication factor is 8.
- Power-down mode: Tests I_{DDQ} on the analog power supply and saves power when the multiplied output clock is not required.

Because the core voltage can vary while V_{DDA} is stable at 1.8 V, the cell is in power-down mode if the voltage on V_{DD} is lower than 200 mV.

Note:

OMAP5912 supports only the above application modes. Although other application modes are possible because of the generic nature of APLL, they are not included in the ULPD architecture.

Figure 2. APLL Block Diagram



- LS: Level shifter
- LSn: Natural level shifter or two successive buffers tied to different supply domains. The usual level-shifting scheme is not suited to the clock output for speed and duty-cycle reasons.
- MISR: Multiple input-shift register for digital test purposes

Table 4. Mode Selection Table

PWRDN	TEST	SEL2	SEL1	SEL0	CLKIN (MHz)	CLKOUT (MHz)	SYNC	MODE
L	-	-	-	-	0	-	-	Power down (1)
H	L	L	L	L	19.2	96	H	Application mode 0
H	L	L	H	L	13	96	Pulsed (1MHz)	Application mode 2
H	L	L	H	H	12	96	H	Application mode 3

Note: Full IDDQ mode is reached when the input clock is not toggling; otherwise, a residual current may be found.

2.1 Application Guidelines

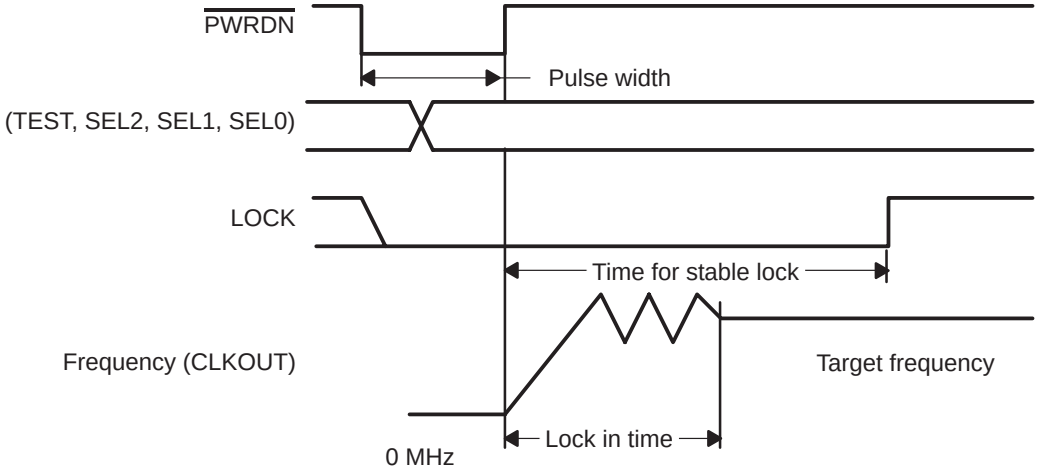
Adhere to the following guidelines to get the best performance from the cell.

Fast Lockup

A fast lockup follows this control sequence (see Figure 3):

1) $\overline{\text{PWRDN}}$ must be set to 0 any time the APLL must be used.
2) $\overline{\text{PWRDN}}$ must stay at low for a minimum time.
3) The mode selection bits (TEST, SEL2, SEL1, SEL0) must be set during the time $\overline{\text{PWRDN}}$ is low.
4) LOCK always falls to 0 when $\overline{\text{PWRDN}}$ is set to low. This may take between several 100 ns and 1 µs.
5) When $\overline{\text{PWRDN}}$ is raised to high, and if the input clock toggles within the specified frequency range, the APLL locks on the target frequency and the lock signal goes to high.
6) Jitter is in specification after LOCK has gone to high.

Figure 3. Fast Lockup



BMode Switching

The fast lockup scheme changes the APLL operation mode. The selection bits must not be changed during normal operation.

If the above condition is not met, be aware that:

- Digital state machines have been designed in such a way to avoid any deadlock condition, but any switching different from the above can lead to unpredictable long transients that differ considerably from case to case.
- The lock signal behavior is not deterministic during mode switching. It goes back to a lower state or it stays high, depending on conditions. Because of the important time-consistent feature of this signal, it is reasonable to expect the APLL to react faster. The lock signal goes low only in major failure conditions, that is, absence of an input clock for a long period of time or a bad frequency range.

Missing Input Clock

A missing input clock is a major concern. It is associated with a lock going low after several 100 µs, depending on mode and condition.

It also causes the output frequency on CLKOUT to decrease quickly because the APLL tries to lock on a 0 frequency signal. However, this is limited to the APLL lock-in range. An unstable frequency can be expected in association with potential beats.

When the input clock is reactivated for a long period of time, the APLL returns to lock condition afterwards. However, this may take longer than usual, up to five times more than the specified lock-in time. In that event, the fast lockup sequence can be used.

One clock source can be switched to another in the same mode without using $\overline{\text{PWRDN}}$. Clock-gating cells must handle this switching to prevent glitches and clock uncertainty. A jitter outside the specification affects this clock switching, especially if a large guard is inserted between the clock source activations with many missing pulses and a large phase jump.

3 OMAP3.2 DPLL

The two most important uses of phase-locked loops are as synthesizers and synchronizers. Synthesizers generate a variable-frequency clock from a fixed-frequency reference clock. The output frequency of the PLL is an integer multiple or a fractional multiple (M/N) of the input reference. Synchronizers

match the on-chip clock to a system clock so that the integrity of the data transfer from one clock to the other is maintained irrespective of the clock skew and timing variations over different process, voltage, and temperature conditions.

Conventional PLLs are analog in nature in the sense that they all use a charge pump/RC filter combination to stabilize the loop. The DPLL, on the other hand, uses a digital control circuitry to stabilize the loop. The feedback control circuit generates digital signals that precisely control the oscillator settings so that the output clock locks-in phase and frequency to the input reference clock.

3.1 Features

The OMAP3.2 DPLL has the following features:

- Frequency-multiplier mode and direct-clock divider mode
- Programmable reset settings
- Idle mode, to save power
- Lock signal, to indicate that the DPLL has locked properly
- Fast lock reacquisition when changed from the idle to active mode, provided the temperature/voltage shifts are not significant
- Automatic switch to the bypass mode during programming/loss of lock
- Support of the TI peripheral bus (TIPB) interface

3.2 Functional Description

The control register is mapped within the MPU space. Writing to the control register causes the DPLL to immediately switch to the bypass mode if not in idle state. If the PLL_ENABLE bit of the control register is set, it begins its sequence to enter the locked mode. This prevents changing the multiple or divide values without reentering the DPLL lock sequence.

Table 5 describes the control register bits. The bit positions are read directly from the TIPB bus. The actual address of the register is programmable to any value. The register has multiple default values depending on the CLKMD pin values.

Table 5. Control Register

Base Address = 0xFFFE CF00, Offset = 0x00				
Bit	**Name**	**Function**	**R/W**	**Reset**
15	LS_DISABLE	Level shifter disable: 0: Level shifter in transparent mode; all signals between wrapper and DPLL core connected. 1: Level shifter in isolated mode; wrapper and DPLL core disconnected. DPLL core power supply turned off: no leakage current between VDD and VDD_DPLL. Power-on value is 0.	R/W	0x0
14	IAI	Initialize after idle: Set high: DPLL starts entire locking sequence after idle is deactivated. Set low: DPLL attempts to lock using internal delay chain setting before entering lock mode. Power-on value is 0. Bit no longer useful and must be set to 0.	R/W	0x0
13	IOB	Initialize on breako When high: DPLL switches to bypass mode and starts new locking sequence if DPLL core indicates lock lost. When low: DPLL continues ro putput synthesized clock even if core indicates lock lost but BREAKLN remains low. Power-on value is 1.	R/W	0x1
12	TEST	Controls test output clock on TCLKOUT pin: Test = 0: TCLKOUT = CLKOUT when in test mode Test = 1: TCLKOUT = CLKOUT/32 when in test mode Test = X: TCLKOUT = 0 when not in test mode	R/W	0x0

Table 5. Control Register (Continued)

Base Address = 0xFFFE CF00, Offset = 0x00				
Bit	**Name**	**Function**	**R/W**	**Reset**
11:7	PLL_MULT (4:0)	DPLL multiple value: 00000: CLKOUT = CLKREF * 1 00001: CLKOUT = CLKREF * 1 00010: CLKOUT = CLKREF * 2 00011: CLKOUT = CLKREF * 3 11111: CLKOUT = CLKREF * 31	R/W	0x0
6:5	PLL_DEV (1:0)	DPLL divide value: 00: CLKOUT = CLKREF 01: CLKOUT = CLKREF/2 10: CLKOUT = CLKREF/3 11: CLKOUT = CLKREF/4 Minimum CLKOUT frequency is 0.25 * CLKREF. When PLL_MULT(4:0) = 0 or 1, CLKOUT is not synthesized by the DPLL, but is simply a divided-down version of CLKREF. Affects lock mode only.	R/R	0x0
4	PLL_ENABLE	DPLL enable: 0: Switched DPLL to bypass mode 1: Requests DPLL to enter lock mode: DPLL starts locking sequence and changes to DPLL synthesized value after locking CLKOUT.	R/W	0x0
3:2	BYPASS_DIV (1:0)	Determines CLKOUT frequency when in bypass mode: 00: CLKOUT = CLKREF 01: CLKOUT = CLKREF/2 1X: CLKOUT = CLKREF/4	R/W	0x0

Table 5. Control Register (Continued)

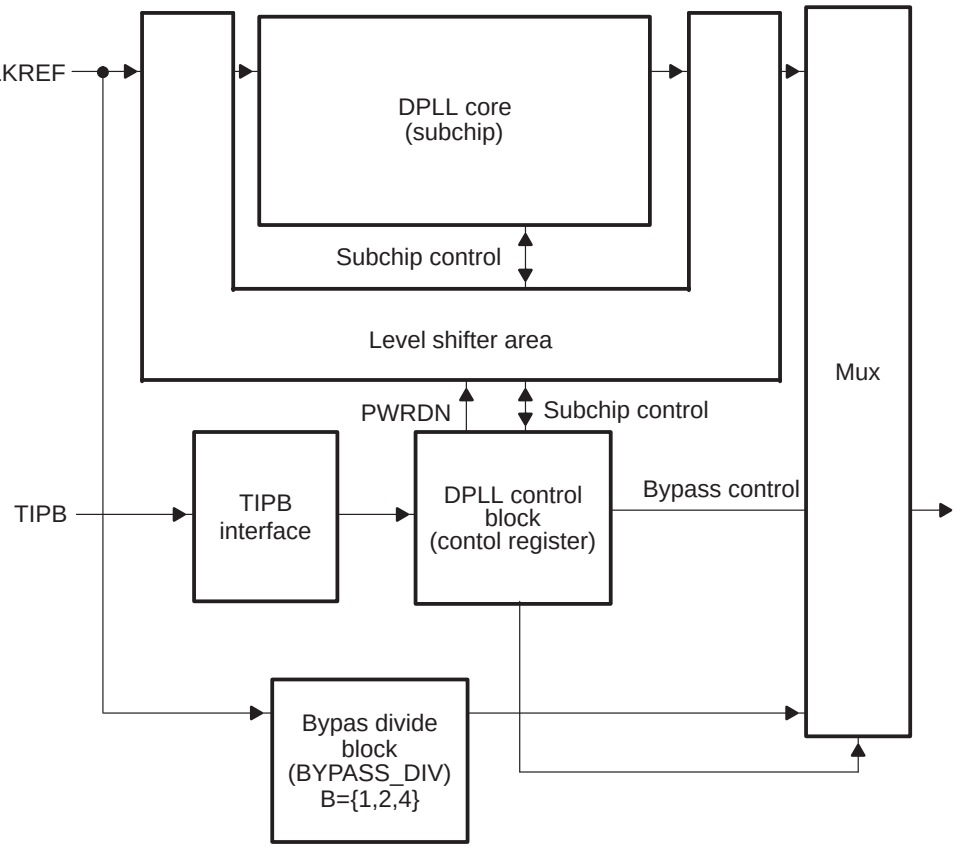
Base Address = 0xFFFE CF00, Offset = 0x00				
Bit	**Name**	**Function**	**R/W**	**Reset**
1	BREAKLN	Indicates break: 0: DPLL has broken lock for some reason. 1: Lock condition has been restored or write to control register has occurred.	R	0x0
0	LOCK	Indicates lock status: 0: DPLL in bypass mode and CLKOUT contains divided-down output clock. 1: DPLL in Lock mode and CLKOUT is desired synthesized clock frequency.	R	0x0

Because the dedicated VDD for the DPLL (VDD_DPLL) is either greater or less than the VDD core, a collar is implemented to isolate the DPLL. This collar includes level shifters that adapt the incoming control signals and the DPLL outputs to the appropriate level (see Figure 4).

- When enabled (LS_DISABLE = 0), the level shifter is seen as a buffer.
- When disabled (LS_DISABLE=1), the level shifter is in isolated mode and its output is grounded.

  LS_DISABLE is a read/write control bit in the DPLL control register. Its reset value is 0.

Figure 4. DPLL



The DPLL has two modes of operation, bypass mode and lock mode.

- In the bypass mode, clkout=clkref divided by 1, 2, or 4. Bypass mode saves power because the DPLL is disabled. This mode also provides an output clock while the DPLL circuitry is locking.
  - clkout = clkref for BYPASS_DIV[1:0] = 00
  - clkout = clkref/2 for BYPASS_DIV[1:0] = 01
  - clkout = clkref/4 for BYPASS_DIV[1:0] = 1X
- In the lock mode, the DPLL provides a synthesized output frequency that is locked to the input reference. Lock mode is entered if the PLL_ENABLE bit of the control register is set and the locking sequence is completed. In this mode, the clkout contains a synthesized clock frequency as defined below:
  - clkout = PLL_MULT / (PLL_DIV+1) * clkref for 1 < PLL_MULT <= 31.
  - clkout = 1 / (PLL_DIV + 1) * clkref for PLL_MULT = 0 or 1

For PLL_MULT = 0 or 1, the clkout is not synthesized. Hence, the output -clock duty cycle (clkout) is directly dependent on the input-clock duty cycle (clkref).

The lock times depend on the values of PLL_MULT and PLL_DIV and the clkout frequency as given below :

Lock time in number of clkref cycles:

clkref clocks=4N(11D+28)

where D=1+$\log_2$(N/(fin*M*xmin)) rounded up to the nearest positive integer (7 max), and fin is the input clock frequency.

The value of xmin in the equation for D is dependent on technology. It must be set to the delay of A with 10 stages in the delay chain measured in min delay conditions.

- 1.5 V xmin = 5.6 ns

Example:

- 1.5 V
- CKref = 10 MHz
- N = 1
- M = 2

D = 1+$\log_2$(1/(2*10E6*5.6E-9)) = 1+$\log_2$(8.93) = 4.158 = 5 (rounded up)

Number of clkref clocks = 4(11(5)+28) = 332

Time = (332)(100 nsec) = 33.2 µsec

Each time the DPLL control register is written to, the mode in which the DPLL operates changes automatically. If the DPLL is operating in the synthesizer mode, it switches automatically to the bypass mode. Depending on the new control register content, the DPLL either initiates a new lock sequence or remains in the bypass mode (see Figure 5).

Figure 5. Operational Flow

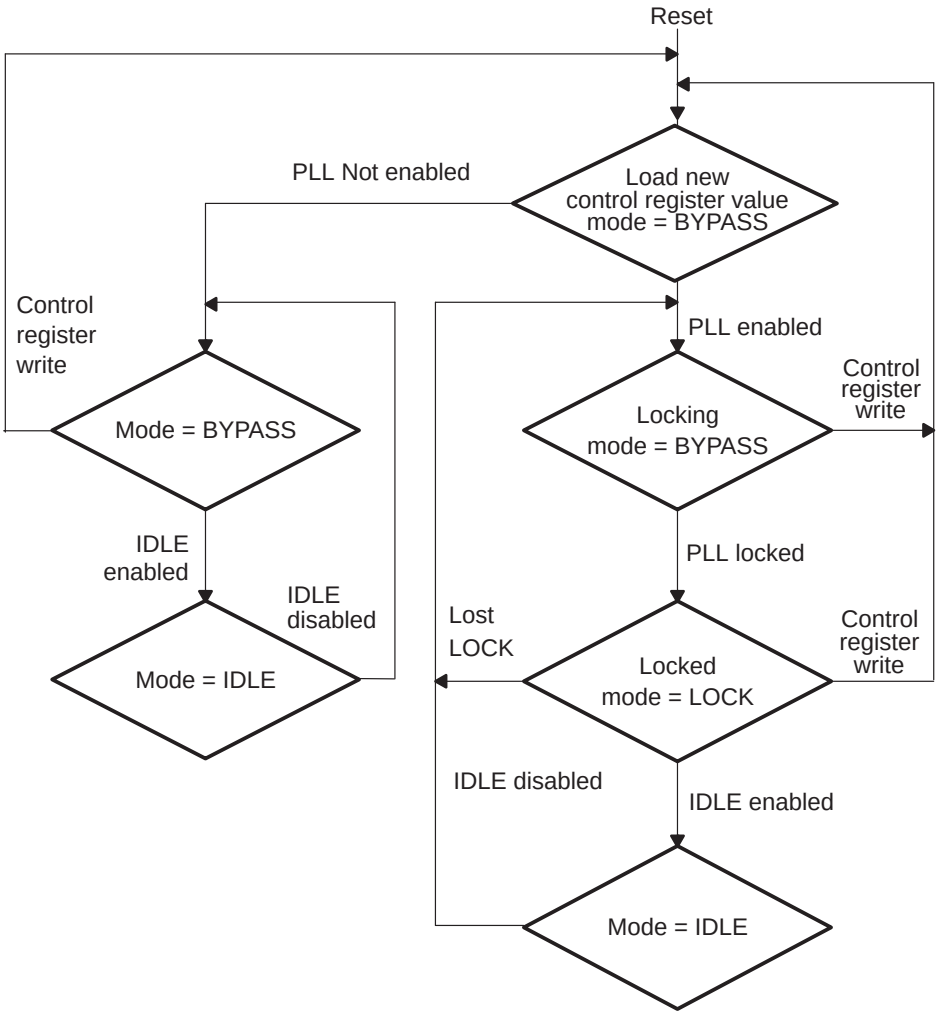


Table 6 lists the clock timings.

Table 6. Clock Timings

Description	Value	Unit
CLKREF duty cycle	From 40 to 60	%
Min CLKREF frequency	2.5	MHz
Max CLKREF frequency	50	MHz
Max CLKOUT frequency	250	MHz

4 Low-Dropout Voltage Regulator

LDO005 is a linear voltage regulator that supplies the OMAP3.2 DPLL macro. This LDO uses peripheral supply input voltage to make the DPLL a quiet power supply.

LDO005 contains:

- Embedded voltage and current reference circuit
- Adaptive biasing error amplifier as voltage regulator
- Offset steady comparator
- Initialization circuit to ensure local powerdown during VDD fast rampup
- Level shifter
- Bypass switch

The regulated supply is delivered to DPLL macros and is available on a unique bond pad. (LDO005 is a complex I/O cell). A decoupling capacitor of 1 µF must be connected externally between the pin of the cell and ground.

The LDO is bypassed when it is in power-down mode because the node VOUT is in high-impedance mode. In this configuration, the DPLL circuit is supplied from the pad (external power supply). To support this mode of operation, the LDO is also in power-down mode after ramp-up of VDD, to avoid potential contention between VDDS and VOUT.

The cell operates in sleep mode when sleep input is high. In this mode, VDD is shorted to VOUT with a resistive switch, and the voltage regulator is kept in power down. This mode retains the status in the registers of the DPLL macros when they are in idle mode (they do not pull current from the power line).

Figure 6 shows the LDO005. Table 7 describes the pins.

Figure 6. LDO005

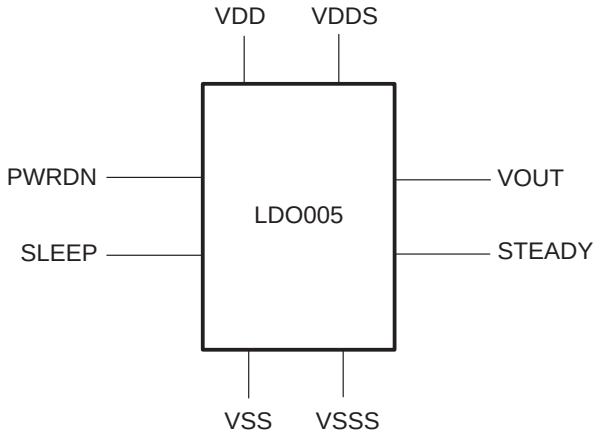
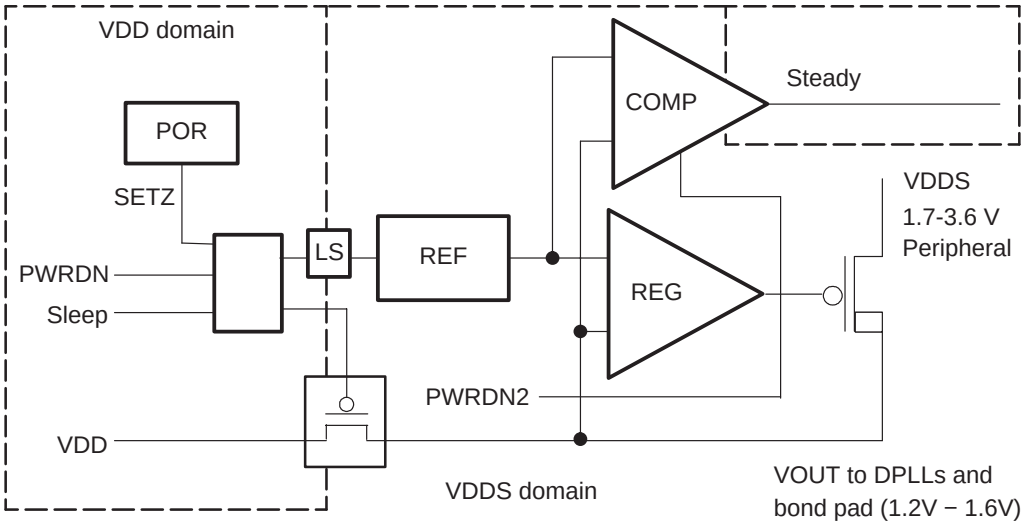


Table 7. LDO005 Pins

Name	Type		Description
VDD	Power signal ring	I/O	Positive core power supply
VDDS	Power signal ring	I/O	Positive periphery power supply input voltage
VOUT	Power signal/pad side	Core	Positive output voltage connected to DPLL power supply and bond pad
VSS	Power signal ring	I/O	Core ground
VSSS	Power signal ring	I/O	Periphery ground connected to DPLLs ground
PWRDN	Digital signal input	Core	Powerdown mode when PWRDN is high
SLEEP	Digital signal input	Core	Control input bypass VDD core voltage to VOUT: active high
STEADY	Digital signal output	Core	Output flag: high when the regulator is active

Figure 7 shows the LDO005 block.

Figure 7. LDO005 Block



The reference is a circuit that delivers voltage and current to the regulator and steady comparator. A local comparator within the reference powers up the regulator and steadies the comparator once the reference is settled using the PWRDN2 signal.

The voltage regulator uses an adaptive biasing technique that has a quiescent current linearly dependent upon the load current.

The voltage comparator has an inherent dc offset. Therefore, the steady signal is logic high when $V_{OUT} > V_{OUTfinal-offset}$ to indicate that the output voltage has almost reached its steady state.

A power-on reset circuit sets the status of the LDO in power down during ramp-up of VDD, before the status of the control inputs PWRDN and SLEEP are in a stable state.

The sleep input signal turns the voltage regulator to power-down mode to cut its quiescient current and turns on the PMOS switch between VDD and VOUT. During the transition from sleep to active modes, the external capacitor holds the voltage on VOUT to the proper level to ensure that the DPLL macros retain the status on the internal registers for fast locking. When sleep input is low, the PMOS switch is off.

Table 8. Mode Selection

PWRDN	SLEEP	Mode
L	L	Application, active
H	Don’t care	Powerdown
L	H	Sleep

4.1 Timing Diagrams

Figure 8. VDD_CORE Ramps First

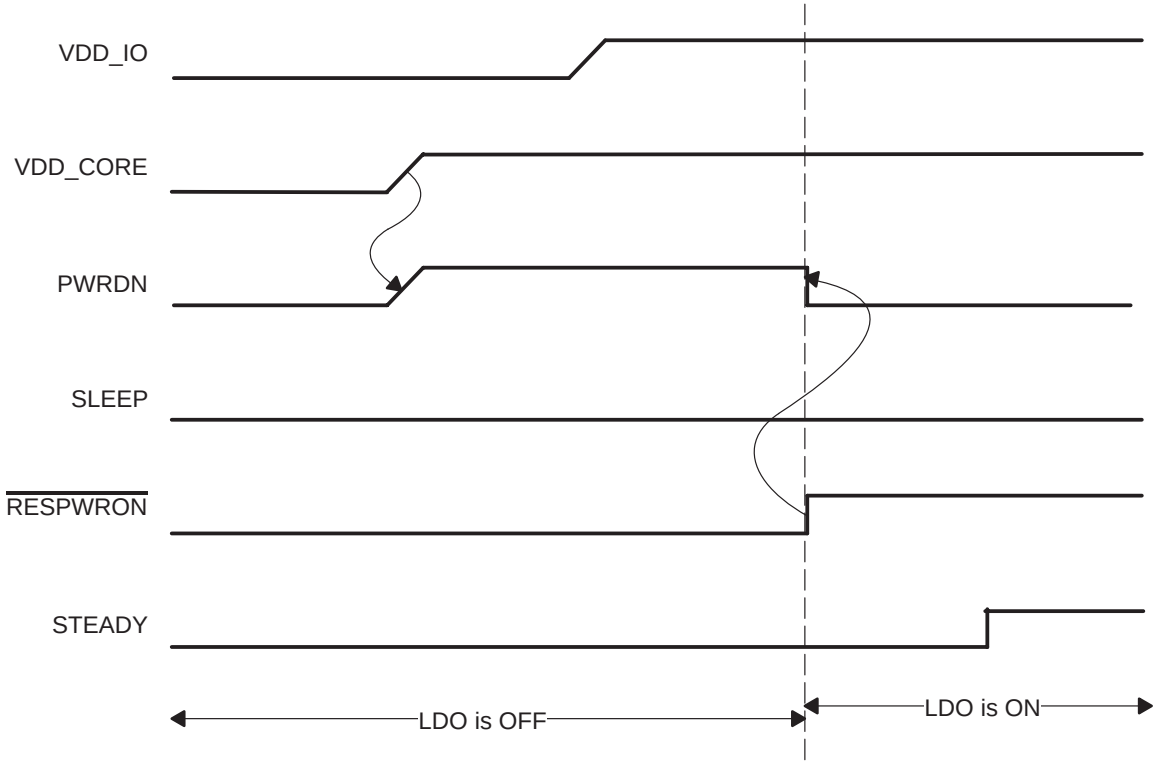
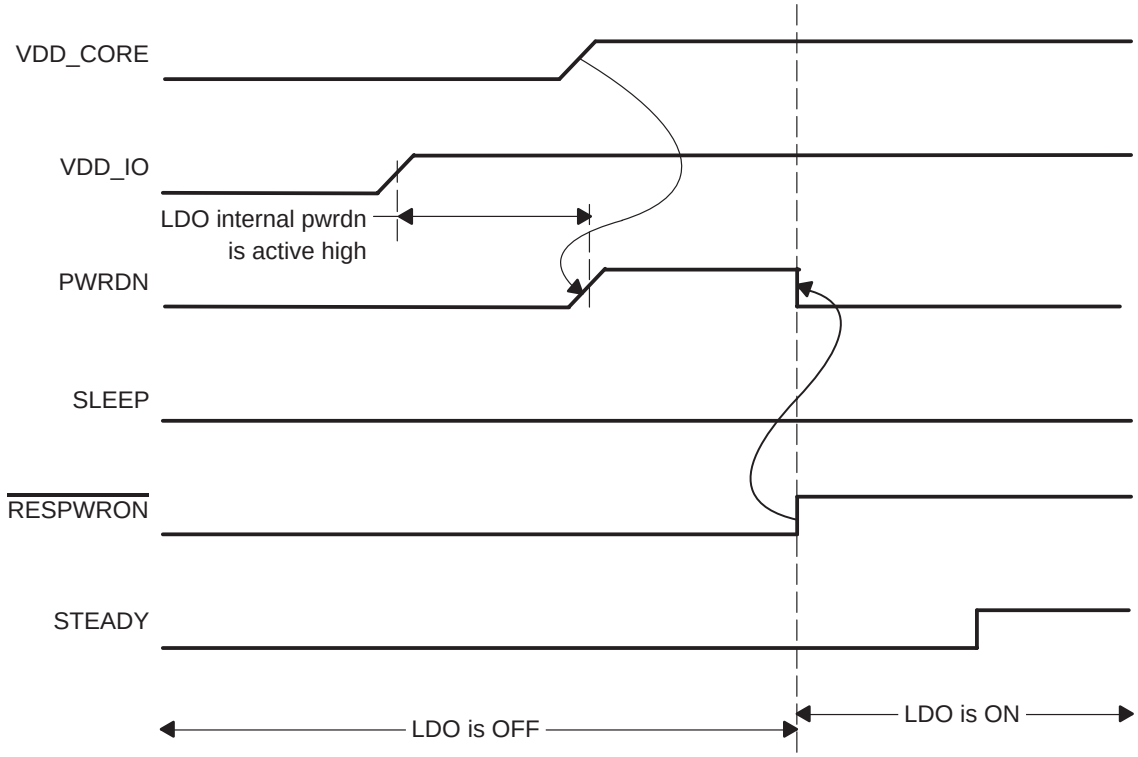


Figure 9. VDD_IO Ramps First



5 OMAP5912 Clock Architecture

The OMAP5912 clock architecture includes the functional and interface clock distribution for the OMAP5912 peripherals.

OMAP5912 receives its system clock from an oscillator or an external squarewave input clock. The system clock first goes through the ultralow-power device module (ULPD), which is responsible for power-mode transitions and clock management. System clock frequencies are 12, 13, or 19.2 MHz. OMAP5912 is also clocked by a 32-kHz clock used by the ULPD finite state machine (FSM) and for specific clocking needs such as the real−time counter (RTC) or the general-purpose timers.

The ULPD output clocks are connected directly to a few peripherals with specific clock requirements. The main system clock output of the ULPD is connected to the MPU subsystem (often referred to as the OMAP 3.2 gigacell). The 32−kHz clock is also one of the ULPD outputs. OMAP 3.2 gigacell is responsible for controlling, multiplying, and distributing clocks to the remaining peripherals.

The ULPD (see chapter 6) manages transitions among deep sleep mode, big sleep mode, and awake mode. Transitions are triggered by external events (resets and clock requests) or by internal events (software reset, watchdog time-out, and software clock requests). Some ULPD outputs can be sent to external power management devices to adjust the OMAP5912 internal corevoltage for optimum power dissipation, versus on-chip activity.

5.1 Reset Modes and Clocking Options

Reset mode 0 has several clocking options while reset mode 1 is much more restrictive.

Table 9. Clocking Options with respect to Reset Modes

Reset Mode = 0	12 MHz	13 MHz	19.2 MHz
OSC1_IN support via crystal?	Yes	Yes	Yes
OSC1_IN support w/external clock source?	Yes	Yes	Yes
SYS_CLK_IN support w/external clock source?	No	No	No
Reset Mode = 1	**12 MHz**	**13 MHz**	**19.2 MHz**
OSC1_IN support via crystal?	No	No	No
OSC1_IN support w/external clock source?	No	No	No
SYS_CLK_IN support w/external clock source?	No	No	Yes

5.2 External System Clock with Reset Mode 0

The OMAP5912 system clock can be driven at 12MHz, 13MHz, or 19.2MHz. For an external system clock, the following hardware connections are used (see Figure 10). Figure 10 applies to reset mode 0 only.

- Hardware considerations:
  - The external clock is applied to the OSC1_IN pin (ball Y2).
  - The OSC1_OUT pin (ball W3) must be left unconnected.
- Software considerations:
  - FUNC_MUX_CTRL_D(2:0) register bits should be 000 to ensure that ball Y4 is *not* pin multiplexed as the SYS_CLK_IN.
  - Set CONF_OSC1_PWRDN_R to 1 in the MOD_CONF_CTRL_1 register so that the oscillator circuit is disabled, reducing power consumption.
  - Set CONF_OSC1_GZ_R to 0 in MOD_CONF_CTRL_1 (when 1, this bit disables square input clocks on the OSC1_IN pin).

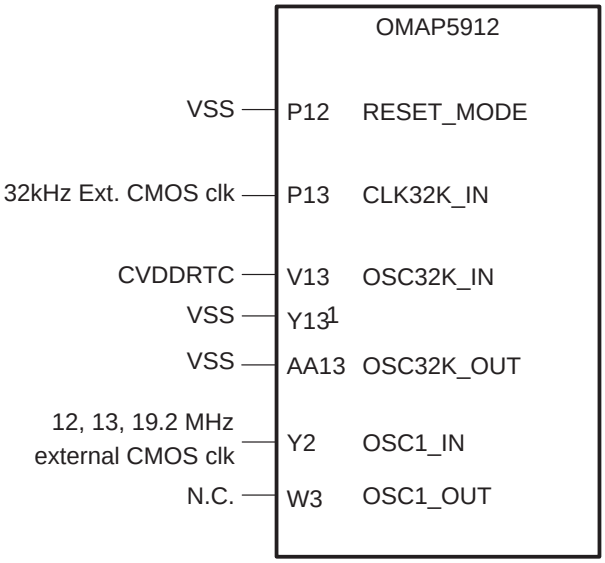
- During power-on reset, the ULPD OSC1 delay timer is reset to 32 ms. Thus, the system clock is not distributed before the timer reaches 0. During this period, the device does not start operation (or transition out of deep sleep state in the FSM of the ULPD). The ULPD OSC1 delay timer can be reprogrammed to 0 in the SETUP_ANALOG_CELL3_REG after the power−on reset has occurred.

5.3 External 32-kHz Clock with Reset Mode 0

The OMAP5912 32-kHz clock can be driven by an external squarewave clock. See Figure 10 for the hardware connections of the external 32-kHz clock. This figure applies to reset mode 0 only.

- Hardware considerations:
  - The external clock is applied to the CLK32K_IN pin (ball P13).
  - OSC32K_IN must be tied to CVDDRTC (see Chapter 22 for a listing of power supply voltages on OMAP5912).
  - OSC32K_OUT must be tied to VSS.
  - Ball Y13 can be connected to board ground (VSS).
- Software considerations:
  - Set OSC32K_PWRDN_R to 1 in RTC_OSC_REG for power-saving purposes.

Figure 10. External CMOS Clock Connections



Notes: 1) Ball Y13 may be connected to board ground.

5.4 Using the Internal Oscillator for the System Clock with Reset Mode 0

The system clock can be 12MHz, 13MHz, or 19.2MHz. To drive the system clock with the internal oscillator circuitry, the following hardware connections are used (see Figure 11). This figure applies to reset mode 0 only.

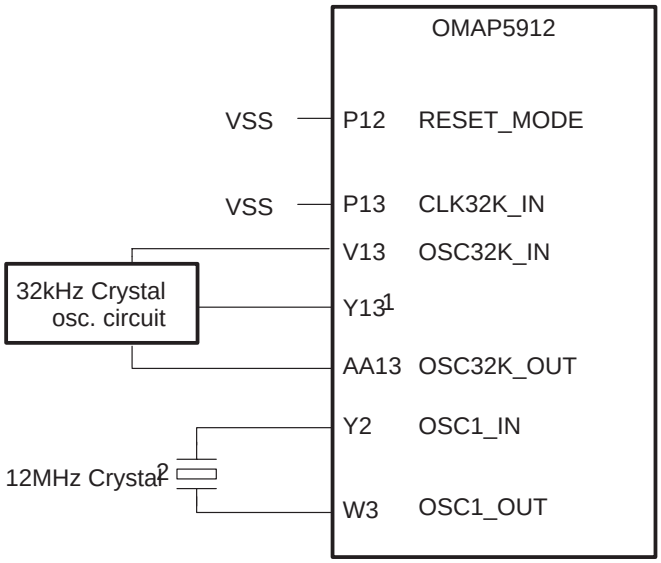
- Hardware considerations:
  - The crystal circuit is applied to the OSC1_IN pin (ball Y2) and the OSC1_OUT pin (ball W3).
- Software considerations:
  - FUNC_MUX_CTRL_D(2:0) register bits should be 000 to ensure that ball Y4 is NOT pin multiplexed as the SYS_CLK_IN.
  - Ensure CONF_OSC1_PWRDN_R is 0 in the MOD_CONF_CTRL_1 register so that the oscillator circuit is enabled.
  - Set CONF_OSC1_GZ_R to 0 in MOD_CONF_CTRL_1 (setting this bit to 1 will also disable the oscillator circuit).

5.5 Using the Internal Oscillator for a 32-kHz Clock with Reset Mode 0

The OMAP5912 32-kHz clock can be driven by an internal oscillator and crystal. See Figure 11 for the hardware connections of the external 32-kHz clock. This figure applies to reset mode 0 only.

- Hardware considerations:
  - The crystal circuit is applied to the OSC32K_IN pin (ball V13) and the OSC32K_OUT pin (ball AA13).
  - Ball Y13 must not be connected to board ground.
  - CLK32K_IN (ball P13) must be tied low directly or with a pulldown. Any activity on this pin will corrupt the 32-kHz clock.
- Software considerations:
  - Ensure OSC32K_PWRDN_R is 0 in the RTC_OSC_REG register.

Figure 11. Internal Oscillator Clock Connections



Notes: 1) Ball Y13 *must not* be connected to board ground (VSS).

2) The crystal may be 12, 13, or 19.2MHz and the full crystal circuit was excluded for the sake of simplicity. Please see the OMAP5912 Data Manual (SPRS231) for more details on clock connections.

The pin Y13 is the oscillator circuit ground pin. This pin must not be connected to board ground when using a 32-kHz oscillator circuit.

5.6 External System Clock with Reset Mode 1

The OMAP5912 system clock is driven at 19.2 MHz only in reset mode 1. For an external system clock, the following hardware connections are used (see Figure 12). Figure 12 applies to reset mode 1 only.

- Hardware considerations:
  - The external clock is applied to the SYS_CLK_IN pin (ball Y4).

- The OSC1_IN pin (ball Y2) must be driven to VSS either by a pulldown or tied directly.
- The OSC1_OUT pin (ball W3) must be left unconnected.

❏ Software considerations:

- Before setting the COMP_MODE_CTRL_0 register to 0x0000EAEF, the FUNC_MUX_CTRL_D(2:0) register bits must be set to 110 to ensure that ball Y4 is pin multiplexed as the SYS_CLK_IN.
- The ULPD OSC1 delay timer is bypassed in reset mode 1. Consequently, there is no delay in the ULPD due to the delay timer.
- If CONF_OSC1_GZ_R = 1, the OSC1_IN pin requires a pulldown, because it is configured as output.

5.7 External 32-kHz Clock with Reset Mode 1

The OMAP5912 32-kHz clock can be driven by an external clock. See Figure 12 for the hardware connections of the external 32-kHz clock. This figure applies to reset mode 1 only.

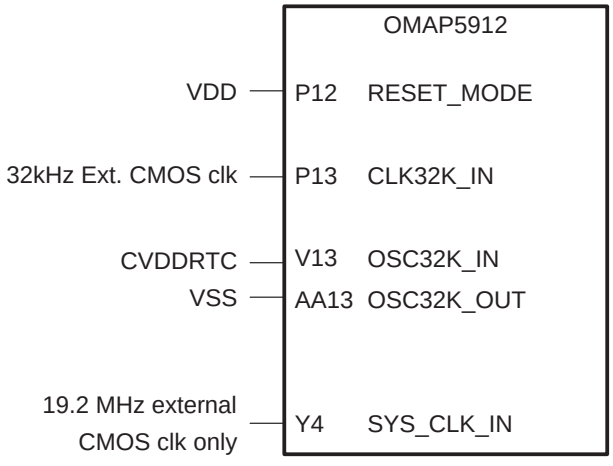
❏ Hardware considerations:

- The external clock is applied to the CLK32K_IN pin (ball P13).
- OSC32K_IN must be tied to CVDDRTC.
- OSC32K_OUT must be tied to VSS.

❏ Software considerations:

- Set OSC32K_PWRDN_R to 1 in RTC_OSC_REG for power-saving purposes.

Figure 12. External CMOS Clock Connections (Reset Mode 1)



5.8 Using the Internal Oscillator for the System Clock with Reset Mode 1

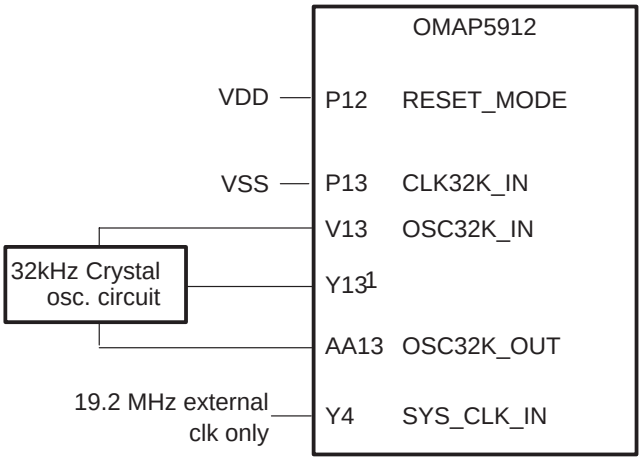
The OMAP5912 system clock cannot be driven by the internal oscillator when reset mode is 1. The internal oscillator is automatically placed in low-power mode when reset mode is 1.

5.9 Using the Internal Oscillator for a 32-kHz Clock with Reset Mode 1

The OMAP5912 32-kHz clock can be driven by an internal oscillator and crystal. See Figure 13 for the hardware connections of the external 32-kHz clock. This figure applies to reset mode 1 only.

- Hardware considerations:
  - The crystal circuit is applied to the OSC32K_IN pin (ball V13) and the OSC32K_OUT pin (ball AA13).
  - CLK32K_IN (ball P13) must be tied low directly or with a pulldown resistor. Any activity on this pin will corrupt the 32-kHz clock.

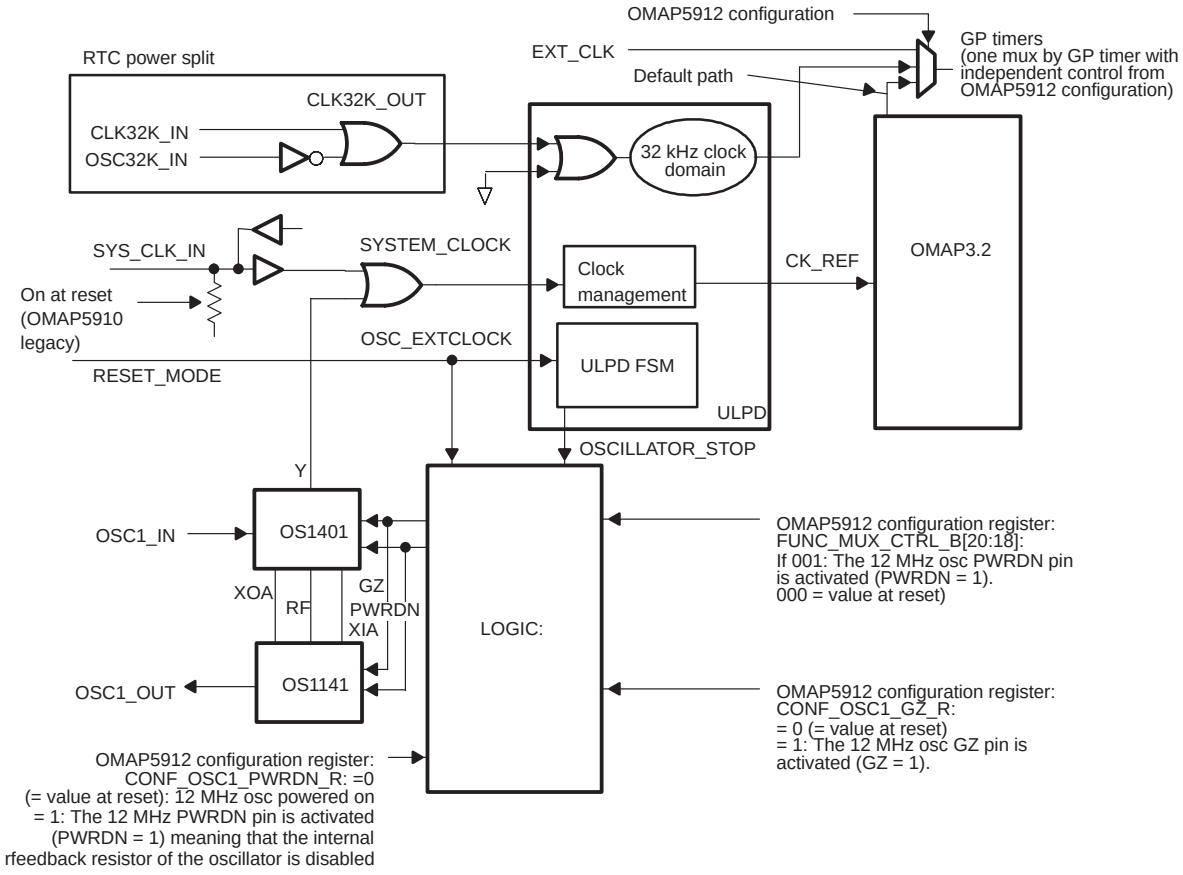
Figure 13. 32-kHz Oscillator Clock Connections (Reset Mode 1)



Notes: 1) Ball Y13 MUST NOT be connected to board ground (VSS). Please see the OMAP5912 Data Manual (SWPS012) for more details on clock connections.

See Figure 14 for a summary of the 32-kHz and system clock internal connections.

Figure 14. 32-kHz and System Clock Scheme



5.10 Clock Distribution in OMAP5912

5.10.1 Clock Inputs to ULPD

The ultralow-power device (ULPD) manages transitions between deep sleep mode, big sleep mode, and awake mode. In each mode, the clocks from the ULPD are gated or ungated either by hardware or by software. The ULPD module is also in charge of managing communication with an external power management device for dynamic voltage scaling. Communication is ensured through $\overline{\text{LOW\_POWER}}$ outputs from OMAP5912.

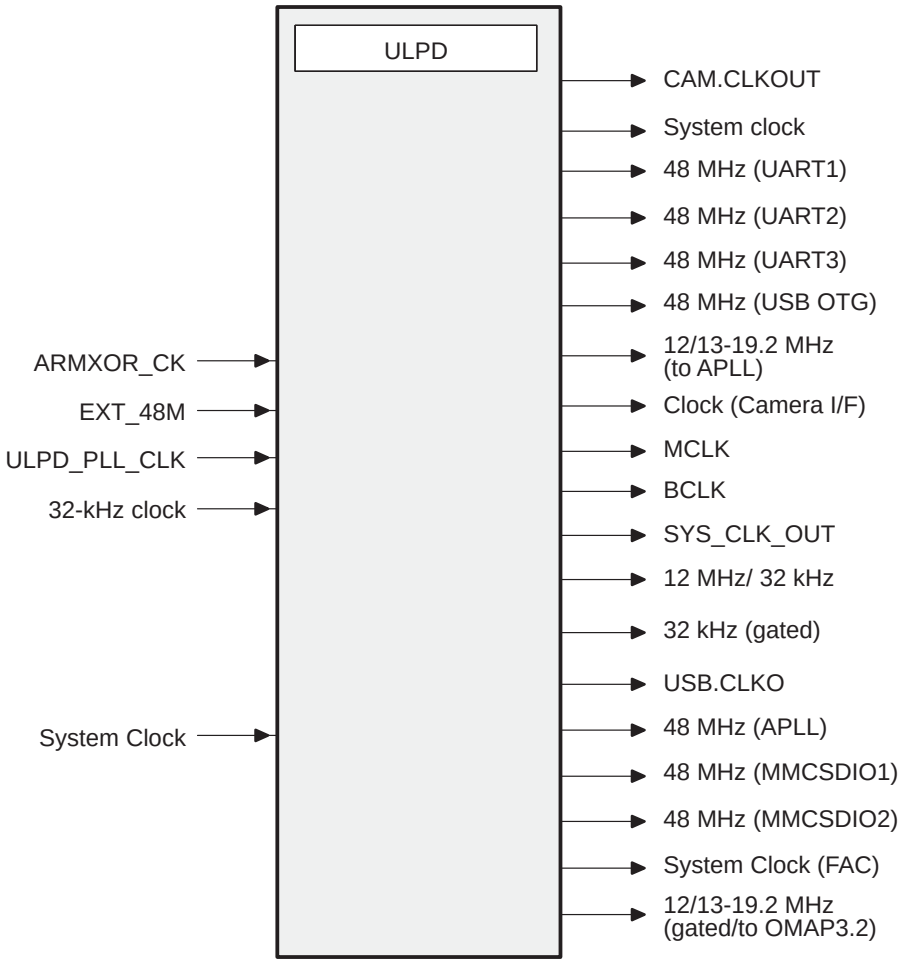
Figure 15 provides an overview of ULPD clocking. See *OMAP5912 Multimedia Processor Power Management Reference Guide* (literature number SPRU753) for further details on the ULPD.

Table 10. ULPD Input Clocks

Input Name	Description	Origin
ARMXOR_CK	MPU peripheral clock	OMAP3.2
EXT_48M	External 48-MHz clock	GPIO_14
ULPD_PLL_CLK	Clock from 96-MHz PLL	APLL
32-kHz Clock	32-kHz clock (either from 32-kHz oscillator or from external 32-kHz clock input)	RTC
System Clock	12- to19.2-MHz system clock (12−19.2-MHz oscillator or from external clock input)	I/O

Figure 15 provides descriptions of the ULPD input clocks.

Figure 15. ULPD Clocking Overview



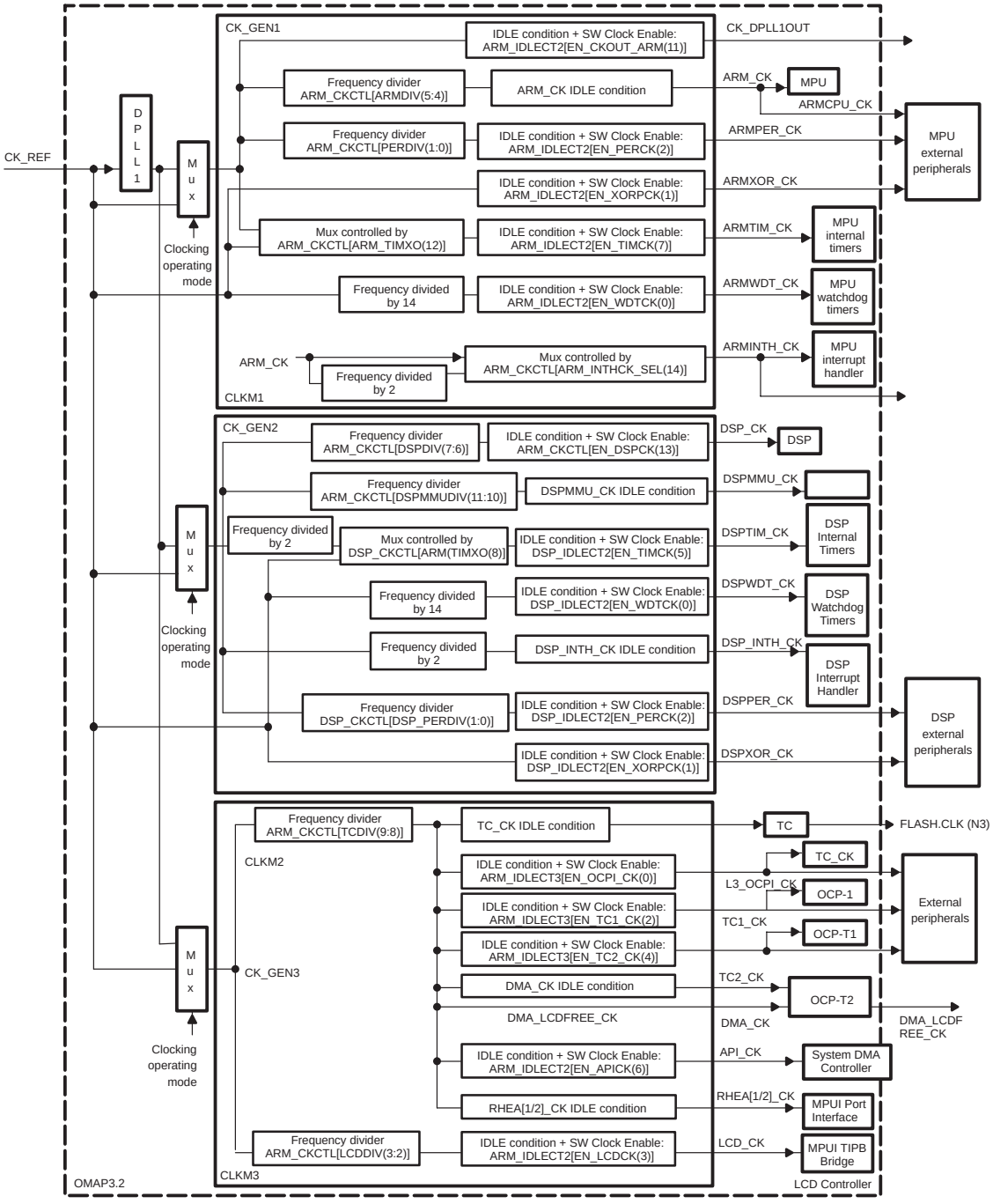
5.11 OMAP 3.2 Clocks

Table 11 describes the OMAP3.2 gigacell clocking distributed to external peripherals.

Table 11. OMAP 3.2 Clocks

Clock Name	Description
CK_REF	System clock, input to DPPL1
CK_DPLL1OUT	Clock from DPPL1, same as MPU clock
ARMCPU_CK	Clock with same frequency as MPU clock, same as ARM_CK
ARMXOR_CK	MPU peripheral clock, fixed, generated from CK_REF, can be gated
ARMPER_CK	MPU peripheral clock, divided from CK_GEN1, can be gated
ARM_INTH_CK	MPU clock interrupt handler
DSPXOR_CK	DSP peripheral clock, fixed, generated from CK_GEN2, can be gated
DSPPER_CK	DSP peripheral clock, divided from CK_GEN2, can be gated
FLASH.CLK (ball N3)	Divided TC_CK clock from EMIFS
TC1_CK	Clocks from OCP-T1
TC2_CK	Clocks from OCP-T2
L3_OCPI_CK	Same frequency as TC clock
DMA_LCDFREE_CK	Interface clock for LCD

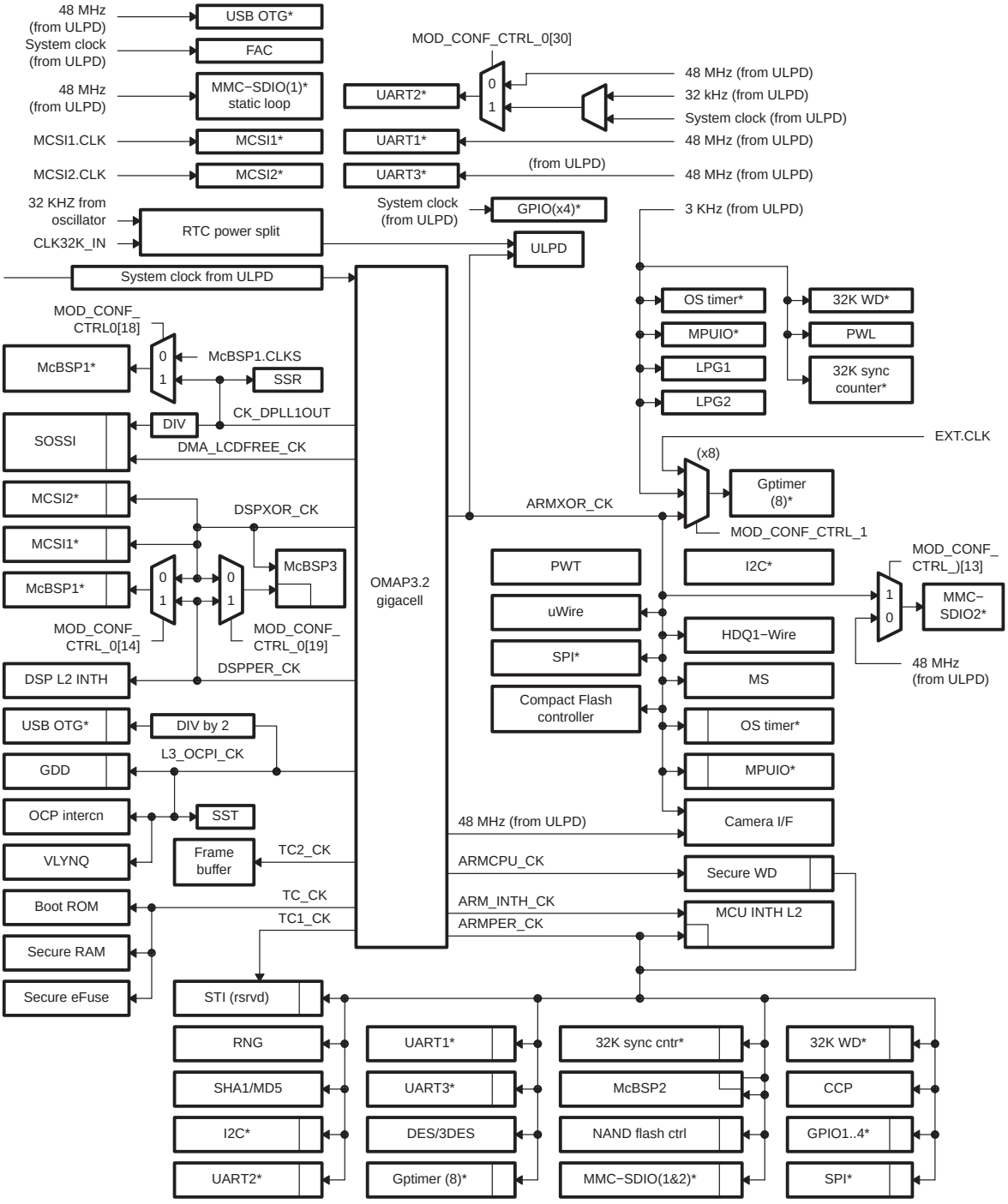
Figure 16. OMAP 3.2 Clock Generation



5.12 Clock Distribution to Peripherals

Figure 17 shows OMAP5912 peripherals (outside of the MPU subsystem) and associated clock distribution.

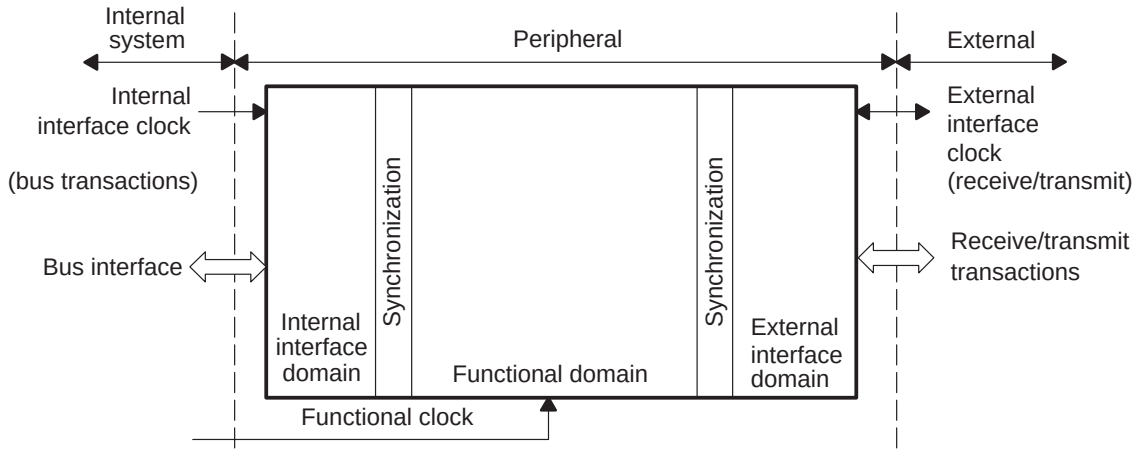
Figure 17. Peripheral Clock Distribution



5.13 Peripheral Module Clocking

Figure 18 shows the peripheral clocking.

Figure 18. Peripheral Clocking



Peripherals can have three types of clocks:

- A functional clock, which is used for peripheral internal logic clocking
- An internal interface clock, which is used for specific register clocking, that is, the OCP clock
- External interface clocks, which are used for transmit/receive protocols, for example (master/slave operation)

See each peripheral specification to better understand how the peripheral uses these clocks.

5.13.1 Peripheral Clocks

Table 12. Peripheral Clocks and Associated Controls

Peripheral Name	**Functional Clock Domain**	**Interface Clock**	**MOD_CONF_ CTRL_0 (OMAP5912 Configuration)**	**MOD_CONF_ CTRL_1 (OMAP5912 Configuration**)
ULPD	32 kHz from RTC			
	ARMXOR_CK			

Notes: 1) The GPIO functional clock is controlled by CAM_CLK_CTRL[2]. If CAM_CLK_CTRL[2] is set , the GPIO functional clock is idle.

2) The SoSSI functional clock can be divided further from 1 to 8 by setting CONF_MODE_CLK_SEL[19:17].

Table 12. Peripheral Clocks and Associated Controls (Continued)

Peripheral Name	Functional Clock Domain	Interface Clock	MOD_CONF_ CTRL_0 (OMAP5912 Configuration)	MOD_CONF_ CTRL_1 (OMAP5912 Configuration)
Boot ROM	TC_CK	Not applicable		
Secure RAM	TC_CK	Not applicable		
STI	TC1_CK	ARMPER_CK		
Secure watchdog	ARMXOR_CK	ARMPER_CK		
Real-time clock (RTC)	Ext 32-kHz clock	Not applicable		
	32-kHz oscillator			
OMAP5912 configuration	Not applicable (TIPB strobe)			
GDD	L3_OCPI_CK	L3_OCPI_CK		
SSR	CK_DPLL1OUT			
SST	L3_OCPI_CK	Not applicable		
OCP interconnect	L3_OCPI_CK	Not applicable		
VLYNQ	L3_OCPI_CK	L3_OCPI_CK		
Frame Buffer	TC2_CK	Not applicable		
General-purpose timer 1	32 kHz from ULPD EXTCLK ARMXOR_CLK	ARMPER_CK		CONF_MODE_ CLK_SEL[1:0]
General-purpose timer 2	32 kHz from ULPD EXTCLK ARMXOR_CLK	ARMPER_CK		CONF_MODE_ CLK_SEL[3:2]
General-purpose timer 3	32 kHz from ULPD EXTCLK ARMXOR_CLK	ARMPER_CK		CONF_MODE_ CLK_SEL[5:4]
General-purpose timer 4	32 kHz from ULPD EXTCLK ARMXOR_CLK	ARMPER_CK		CONF_MODE_ CLK_SEL[7:6]

Notes: 1) The GPIO functional clock is controlled by CAM_CLK_CTRL[2]. If CAM_CLK_CTRL[2] is set , the GPIO functional clock is idle.

2) The SoSSI functional clock can be divided further from 1 to 8 by setting CONF_MODE_CLK_SEL[19:17].

Table 12. Peripheral Clocks and Associated Controls (Continued)

Peripheral Name	Functional Clock Domain	Interface Clock	MOD_CONF_ CTRL_0 (OMAP5912 Configuration)	MOD_CONF_ CTRL_1 (OMAP5912 Configuration)
General-purpose timer 5	32 kHz from ULPD EXTCLK ARMXOR_CLK	ARMPER_CK		CONF_MODE_ CLK_SEL[9:8]
General-purpose timer 6	32 kHz from ULPD EXTCLK ARMXOR_CLK	ARMPER_CK		CONF_MODE_ CLK_SEL[11:10]
I^2C multimaster/slave	ARMXOR_CK	ARMPER_CK		
SPI master/slave	ARMXOR_CK	ARMPER_CK		
32-kHz synchro counter	32 kHz from ULPD	ARMPER_CK		
MMC/SDIO2	ARMXOR_CK 48 MHz from ULPD	ARMPER_CK	CONF_MOD_ MMC2_CLK_ SEL_R	
UART2	32 kHz from ULPD System clock from ULPD 48 MHz from ULPD	ARMPER_CK	CONF_MOD_ UART2_CLK_ MODE_R	
GPIO4	CK_REF	ARMPER_CK		
GPIO1	CK_REF	ARMPER_CK		
GPIO2	CK_REF	ARMPER_CK		
GPIO3	CK_REF	ARMPER_CK		
UART1	48 MHz from ULPD	ARMPER_CK		
UART3	48 MHz from ULPD	ARMPER_CK		
General-purpose timer 7	32 kHz from ULPD EXTCLK ARMXOR_CLK			CONF_MODE_ CLK_SEL[13:12]

Notes: 1) The GPIO functional clock is controlled by CAM_CLK_CTRL[2]. If CAM_CLK_CTRL[2] is set , the GPIO functional clock is idle.

2) The SoSSI functional clock can be divided further from 1 to 8 by setting CONF_MODE_CLK_SEL[19:17].

Table 12. Peripheral Clocks and Associated Controls (Continued)

Peripheral Name	Functional Clock Domain	Interface Clock	MOD_CONF_ CTRL_0 (OMAP5912 Configuration)	MOD_CONF_ CTRL_1 (OMAP5912 Configuration)
General-purpose timer 8	32 kHz from ULPD EXTCLK ARMXOR_CLK			CONF_MODE_ CLK_SEL[15:14]
PWL	32 kHz from ULPD	Not applicable		
LPG1	32 kHz from ULPD	Not applicable		
LPG2	32 kHz from ULPD	Not applicable		
RNG	ARMPER_CK	Not applicable		
SHA1/MD5	ARMPER_CK	Not applicable		
DES/3DES	ARMPER_CK	Not applicable		
CCP	ARMPER_CK	Not applicable		
PWT	ARMXOR_CK	Not applicable		
CompactFlash controller	ARMXOR_CK			
32-kHz watchdog	32 kHz from ULPD	ARMPER_CK		
OS timer	32 kHz from ULPD	ARMXOR_CK		
USB On-The-Go	48 MHz from ULPD	L3_OCPI_CK divided by 2		
µWire	ARMXOR_CK			
HDQ/1-Wire	ARMXOR_CK			
Camera IF	ARMXOR_CK 48 MHz from ULPD			CONF_CAM_ CLKMUX_R
McBSP2	ARMPER_CK	ARMPER_CK		
MPU interrupt handler level 2	ARM_INTH_CK	ARMPER_CK		

Notes: 1) The GPIO functional clock is controlled by CAM_CLK_CTRL[2]. If CAM_CLK_CTRL[2] is set , the GPIO functional clock is idle.

2) The SoSSI functional clock can be divided further from 1 to 8 by setting CONF_MODE_CLK_SEL[19:17].

Table 12. Peripheral Clocks and Associated Controls (Continued)

Peripheral Name	**Functional Clock Domain**	**Interface Clock**	**MOD_CONF_ CTRL_0 (OMAP5912 Configuration)**	**MOD_CONF_ CTRL_1 (OMAP5912 Configuration**)
MMC/SDIO1	48 MHz from ULPD	ARMPER_CK		
FAC	ARMXOR_CK (gated in ULPD)	Not applicable		
MPUIO	32 kHz from ULPD			
DSP interrupt handler 2.1	DSPPER_CK	DSPPER_CK		
McBSP1	MCBS1_CLKS	DSPPER_CK	CONF_MOD_ MCBSP1_CLK_ SEL_R	
	CK_DPLL1OUT	DSPXOR_CK	CONF_MOD_ MCBSP1_CLKS_ SEL_R	
McBSP3	DSPXOR_CK	DSPPER_CK	CONF_MOD_ MCBSP3_CLK_ SEL_R	
		DSPXOR_CK		
MCSI1	MCSI1_BCLK	DSPXOR_CK		
MCSI2	MCSI2_CLK	DSPXOR_CK		
SoSSI	CK_DPLL1OUT	DMA_ LCDFREE_CK		CONF_MODE_ CLK_SEL[16]
				CONF_MODE_ CLK_SEL[19:17][2]

Notes: 1) The GPIO functional clock is controlled by CAM_CLK_CTRL[2]. If CAM_CLK_CTRL[2] is set , the GPIO functional clock is idle.

2) The SoSSI functional clock can be divided further from 1 to 8 by setting CONF_MODE_CLK_SEL[19:17].

5.13.2 Clock Gating in ULPD

Table 13 shows clocks from the ULPD that can be gated or ungated. Clocks can be made active if either one of the respective clock selections is high or if there is a wake-up request. Wake-up requests can be hardware or software and can be disabled by software. For software requests, disables, and associated clocks, see Table 13. In addition, some software requests can be set up in the OMAP5912 configuration module.

Table 13. Hardware Requests

Hardware Request	Clock Requested	Event	Notes
PERIPH_NREQ (internal)	Input clock to OMAP3.2 DPLL	Falling edge detected on the UART2 RX	ULPD state machine transitions to awake.
	UART_MCKO (internal)		UART_MCKO transitions from 32-kHz (deep sleep mode) to system clock.
	CAM.EXCLK		
WAKEUP_NREQ (internal)	Input clock to OMAP3.2 DPLL	Any unmasked interrupt from GPIO	ULPD state machine transitions to awake.
	UART_MCKO		
	CAM.EXCLK		
BCLKREQ	System clock on ball Y15 (BCLK)	External input set high	
MCLKREQ	System clock on ball V5 (MCLK)	External input set high	
USB_MCLK_REQ	System clock	Permanent request. Can be disabled by software.	Interface clock to access USB register file
USB_DPLL_MCLK_REQ	48 MHz for USB	USB cable detection/USB resume	48-MHz USB clock. Refer to USB OTG integration.

By default, USB_MCLK_REQ requests the internal interface clock. When low, it enables the ULPD to enter deep sleep mode, as the USB is in idle mode and USB functionality is no longer required (OTG functionality is no longer used, the idle modes are activated, the USB host is not used, and the USB device is not used, is unconnected, or is put in suspend after the software acknowledgment).

By default, USB_DPLL_MCLK_REQ requests the clock for 48 MHz for the USB core clocks. When low, it enables the ULPD to enter deep sleep mode,

as the USB bus is no longer used and USB functionality is no longer required. (OTG functionality is no longer used, the idle modes are activated, the USB host is not used, and the USB device is not used, is unconnected, or is put in suspend).

Table 14 summarizes software clock requests that are mapped in the OMAP5912 configuration module and in the ULPD module and that differ from the generic ULPD software requests in SOFT_REQ_REG.

Table 14. Software Requests

Software Requests	Clock Requested	Event	Origin
UART1_DPLL_REQ	48 MHz for UART1	MOD_CONF_CTRL0[29] set to 1	OMAP5912 configuration
UART2_DPLL_REQ	48 MHz for UART2	MOD_CONF_CTRL0[30] set to 1	OMAP5912 configuration
UART3_DPLL_REQ	48 MHz for UART3	MOD_CONF_CTRL0[31set to 1]	OMAP5912 configuration
MMC_DPLL_CLK	48 MHz for MMCSDIO1	MOD_CONF_CTRL_0[23] set to 1	OMAP5912 configuration
MMC2_DPLL_CLK	48 MHz for MMCSDIO2	MOD_CONF_CTRL_0[20] set to 1	OMAP5912 configuration
CONF_MOD_USB_ HOST_HHC_ UHOST_EN	48 MHz for USB	CONF_MOD_USB_HOST_HHC_ UHOST_EN_R set to 1	OMAP5912 configuration. Kept in OMAP5912 for software compatibility with OMAP5910
CONF_CAM_ CLKMUX_EN_R	Clock for camera I/F	CONF_ CAM_CLKMUX_R set to 1	OMAP5912 ULPD

As long as at least one of the clock requests is active, the ULPD is prevented from entering deep sleep mode.

In deep sleep mode, all clocks are idle except UART2 UART_MCKO, which is derived from the 32-kHz oscillator.

In big sleep mode, the clocks listed in Table 15 are active as long as their respective requests are enabled.

Table 15. Active Clocks in Big Sleep Mode

Module/ OMAP5912 I/O Destination	Clock Description	Active Request	Notes
BCLK	System clock or 48-MHz clock from APLL	BCLKREQ (see note 5)	When 48MHz clock is selected SDW_CLK_DIV_CTRL_ SEL[7:2] further divides BCLK. See Note 1.
MCLK	System clock or 48-MHz clock from APLL	MCLKREQ (see note 5) SOFT_REQ_REG[6] COM_CLK_DIV_CTRL_SEL[1] SOFT_REQ_REG[1]	When 48MHz clock is selected, COM_RATIO_SEL[7:2] further divides MCLK. See Note 2.
UART2	32-kHz or system clock	WAKEUP_NREQ PERIPH_NREQ SOFT_REQ_REG[5]	
USB.CLK0	EXT_48M divided by 8 48 MHz from ULPD divided by 8	Clock request to ULPD PLL SOFT_REQ_REG[0]	See Note 3.
SYS_CLK_OUT	System clock	MCLKREQ (see note 5) SOFT_REQ_REG[1]	System clock
CAM.D[7]	EXT_48M 48 MHz from ULPD	SOFT_REQ_REG[0] Clock request to ULPD PLL	External source for 48 MHz selected if CONF_DPLL_EXT_SEL=1. See Note 4.
UART1	EXT_48M 48 MHz from ULPD	MOD_CONF_CTRL0[29] SOFT_REQ_REG[9]	
UART2	EXT_48M 48 MHz from ULPD	MOD_CONF_CTRL0[30] SOFT_REQ_REG[10]	
UART3	EXT_48M 48 MHz from ULPD	MOD_CONF_CTRL0[31] SOFT_REQ_REG[11	

Table 15. Active Clocks in Big Sleep Mode (Continued)

Module/ OMAP5912 I/O Destination	Clock Description	Active Request	Notes
USB OTG	EXT_48M 48 MHz from ULPD	USB_DPLL_MCLK_REQ CONF_MOD_USB_HOST_ HHC_UHOST_EN_R SOFT_REQ_REG[8]	
MMC/SDIO1	EXT_48M 48 MHz from ULPD	MOD_CONF_CTRL_0[23] SOFT_REQ_REG[12]	
MMC/SDIO2	EXT_48M 48 MHz from ULPD	MOD_CONF_CTRL_0[20] SOFT_REQ_REG[13]	

Notes: 1) The frequency on the BCLK can be set accordingly: SDW_CLK_DIV_CTRL_SEL[7:2]. The resulting frequency is given in the following table:

SDW_CLK_DIV_CTRL_SEL[7:2] = 0X00000, BCLK = 48 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X00001, BCLK = 32 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X00002, BCLK = 24 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X00003, BCLK = 19.2 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X00004, BCLK = 16 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X00005, BCLK = 13.7 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X00006, BCLK = 12 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X00007, BCLK = 9.6 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X00008, BCLK = 8 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X00009, BCLK = 6.9 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X000012, BCLK = 3 MHz
SDW_CLK_DIV_CTRL_SEL[7:2] = 0X000032, BCLK = 1 MHz

2) The frequency on the MCLK can be set accordingly: COM_RATIO_SEL[7:2]. The resulting frequency is given in the following table:

COM_RATIO_SEL[7:2] = 0X00000, MCLK = 48 MHz
COM_RATIO_SEL[7:2] = 0X00001, MCLK = 32 MHz
COM_RATIO_SEL[7:2] = 0X00002, MCLK = 24 MHz
COM_RATIO_SEL[7:2] = 0X00003, MCLK = 19.2 MHz
COM_RATIO_SEL[7:2] = 0X00004, MCLK = 16 MHz
COM_RATIO_SEL[7:2] = 0X00005, MCLK = 13.7 MHz
COM_RATIO_SEL[7:2] = 0X00006, MCLK = 12 MHz
COM_RATIO_SEL[7:2] = 0X00007, MCLK = 9.6 MHz
COM_RATIO_SEL[7:2] = 0X00008, MCLK = 8 MHz
COM_RATIO_SEL[7:2] = 0X00009, MCLK = 6.9 MHz
COM_RATIO_SEL[7:2] = 0X000012, MCLK = 3 MHz
COM_RATIO_SEL[7:2] = 0X000032, MCLK = 1 MHz

3) EXT_48M is an external 48−MHz input clock multiplexed with GPIO4.
4) The 48 MHz from the APLL, which can be observed on CAM.D[7], if the observability mode is configured.
5) Please refer to section 5.14 for more information on the relationship between activating requests.

5.14 OMAP5912 Output Clocks

There are four OMAP5912 output clocks that can be used to clock external ICs. All of these output clocks are on pins that are multiplexed with other functions. Therefore, the appropriate pin multiplexing must be programmed by software (e.g. MCLK is selected on ball V5, MCLKREQ is selected on ball R10, etc.).

5.14.1 MCLK and MCLKREQ

The hardware request for MCLK, MCLKREQ, is available on ball R10, in multiplexing mode 0. It is active high. Using this request, the user can get the system clock on MCLK.

To get the system clock on MCLK using a hardware request,

- Set the CONF_MOD_COM_MCK_12_48_SEL_R bit to 0 in the MOD_CONF_CTRL_0 register.
- Set the COM_SYSCLK_PLLCLK_SEL bit to 1 in the ULPD COM_CLK_CTRL_DIV_SEL register.
- Set the DIS_COM_MCLK_REQ bit to 0 in the ULPD SOFT_DISABLE_REQ_REG register.
- Set the SOFT_COM_MCKO_REQ bit to 0 in the ULPD SOFT_REQ_REG.

Consequently, setting MCLKREQ (R10) high puts the system clock on MCLK (V5). The software can mask out MCLKREQ, and deactivate MCLK by changing SOFT_DIS_COM_MCLK_REQ. When the system clock is output on

MCLK, the software can also use the ULPD CLOCK_CTRL_REG.COM_MCLK_INV to select the inactive level of MCLK.

A software request for MCLK is also available. Depending on the software request used, MCLK can be:

- 48MHz coming from the ULPD APLL (legacy support)
- 48MHz coming from the ULPD APLL divided by a programmable ratio
- The system clock

For the system clock on MCLK with a software request, the following software procedure must be used:

- Set the CONF_MOD_COM_MCK_12_48_SEL_R bit to 0 in the MOD_CONF_CTRL_0 register.
- Set the COM_SYSCLK_PLLCLK_SEL bit to 1 in the ULPD COM_CLK_CTRL_DIV_SEL register.
- Set the DIS_COM_MCLK_REQ bit to 1 in the ULPD SOFT_DISABLE_REQ_REG register.
- Set the SOFT_COM_MCKO_REQ to 1 in the ULPD SOFT_REQ_REG register.

Consequently, the system clock is available on MCLK. Use SOFT_COM_MCKO_REQ to disable or reenable MCLK. When the system clock is output on MCLK, the software can also use the ULPD CLOCK_CTRL_REG.COM_MCLK_INV to select the inactive level of MCLK.

For a 48-MHz clock on MCLK with a software request (legacy support), the following software procedure must be used:

- Set the CONF_MOD_COM_MCK_12_48_SEL_R bit to 1 in the MOD_CONF_CTRL_0 register.
- Set the COM_SYSCLK_PLLCLK_SEL bit to 1 in the ULPD COM_CLK_CTRL_DIV_SEL register.
- Set the DIS_COM_MCLK_REQ bit to 0 in the ULPD SOFT_DISABLE_REQ_REG register.

The CONF_MOD_COM_MCK_12_48_SEL_R bit acts both as selection for 48MHz on MCLK and as a request for ULPD APLL. This sends the 48-MHz clock to MCLK. Setting DIS_COM_MCLK_REQ to 1 does not gate the output of the APLL or the MCLK clock source selection, but it does disable the APLL clock request associated to CONF_MOD_COM_MCK_12_48_SEL_R.

For a divided 48-MHz clock on MCLK with a software request, the following software procedure must be used:

- Set ULPD COM_CLK_CTRL_DIV_SEL.COM_RATIO_SEL to the desired ratio.
- Set the COM_SYSCLK_PLLCLK_SEL bit to 0 in the ULPD COM_CLK_CTRL_DIV_SEL register.
- Set the COM_ULPD_PLL_CLK_REQ to 1 in the ULPD COM_CLK_CTRL_DIV_SEL register.

Consequently, the 48MHz clock divided by the programmed ratio will be available on MCLK. Use COM_ULPD_PLL_CLK_REQ to disable or re-enable MCLK clock. Note that by setting COM_RATIO_SEL to 00000, 48MHz will be available on MCLK.

5.14.2 BCLK and BCLKREQ

The hardware request for BCLK, BCLKREQ (ball W15), is available in multiplexing mode 0. It is active high. Using this request, the user can get the system clock on BCLK (ball Y15).

To get the system clock on BCLK using a hardware request, the following software procedure is used:

- Set the COM_SYSCLK_PLLCLK_SEL bit to 1 in the ULPD SDW_CLK_CTRL_DIV_SEL register.
- Set the DIS_COM_MCLK_REQ bit to 0 in the ULPD SOFT_DISABLE_REQ_REG register.
- Set the SOFT_SDW_REQ bit to 0 in the ULPD SOFT_REQ_REG.

Consequently, setting BCLKREQ (W15) high puts the system clock on BCLK (Y15). The software can mask out BCLKREQ, and deactivate BCLK by changing SOFT_DIS_SDW_MCLK_REQ. When the system clock is output on MCLK, the software can also use the ULPD CLOCK_CTRL_REG.SDW_MCLK_INV to select the inactive level of BCLK.

A software request for BCLK is also available. Depending on the software request used, BCLK can be:

- 48MHz coming from the ULPD APLL divided by a programmable ratio.
- The system clock.

For the system clock on BCLK with a software request, the following software procedure must be used:

- Set the SDW_SYSCLK_PLLCLK_SEL bit to 1 in the ULPD SDW_CLK_CTRL_DIV_SEL register.
- Set the DIS_SDW_MCLK_REQ bit to 1 in the ULPD SOFT_DISABLE_REQ_REG register.

- Set the SOFT_SDW_REQ bit to 1 in the ULPD SOFT_REQ_REG register.

Consequently, the system clock is available on BCLK. Use SOFT_SDW_REQ to disable or reenable BCLK (regardless of the BCLKREQ pin). When the system clock is output on BCLK, the software can also use the ULPD CLOCK_CTRL_REG.SDW_MCLK_INV to select the inactive level of BCLK.

For a divided 48-MHz clock on BCLK with a software request, the following software procedure must be used. In the ULPD SDW_CLK_CTRL_DIV_SEL register:

- Set SDW_RATIO_SEL to the desired ratio.
- Set the SDW_SYSCLK_PLLCLK_SEL bit to 0.
- Set the SDW_ULPD_PLL_CLK_REQ to 1.

Consequently, the 48MHz clock divided by the programmed ratio will be available on BCLK. Use SDW_ULPD_PLL_CLK_REQ to disable or re-enable BCLK clock. By setting SDW_RATIO_SEL to 00000, 48MHz is made available on BCLK.

5.14.3 CAM_CLK_OUT

Ball Y15 can also be configured to provide an external clock to a camera sensor (CAM_CLK_OUT function, in multiplexing mode 6). The frequency of this external clock is the system clock frequency divided by a programmable ratio. It can only be enabled by software with the following procedure:

- Set the CAM_CLK_DIV field to the appropriate dividing ratio in the ULPD CAM_CLK_CTRL register.
- Set the CAM_CLOCK_ENABLE bit to 1 in the ULPD CAM_CLK_CTRL reigster.

Note:

CAM_CLK_OUT must not be confused with the CAM.EXCLK function: CAM.EXCLK is the output pixel clock of the camera module; CAM_CLK_OUT is merely the system clock divided. These two clocks have different sources, and they are enabled differently

5.14.4 SYS_CLK_OUT

Ball B15 can be configured to function as SYS_CLK_OUT (in multiplexing mode 1). The system clock can be enabled on this ball either by a hardware or a software request.

SYS_CLK_OUT uses the same hardware request as MCLK (MCLKREQ). The pin multiplexing should be setup so that ball R10 acts as MCLKREQ and ball

B15 acts as SYS_CLK_OUT. The procedure to enable SYS_CLK_OUT using a hardware request is:

- Set the TI_RESERVED_EN bit to 1 in the ULPD CLOCK_CTRL_REG register.
- Set the DIS_COM_MCLK_REQ bit to 0 in the ULPD SOFT_DISABLE_REQ_REG register.

Consequently, the system clock is available on ball B15. Modifying the SOFT_DIS_COM_MCLK_REQ or TI_RESERVED_EN bits masks out MCLKREQ and deactivates MCLK clock.

SYS_CLK_OUT uses the same software request as the 48-MHz MCLK. The procedure to enable SYS_CLK_OUT using a software request is:

- Set ULPD CLOCK_CTRL_REG.TI_RESERVED_EN bit to 1
- Set ULPD SOFT_DISABLE_REQ_REG.DIS_COM_MCLK_REQ to 1
- Set ULPD SOFT_REQ_REG.SOFT_COM_REQ to 1

Consequently, the system clock appears on ball B15. By modifying SOFT_COM_REQ or TI_RESERVED_EN bits, the software can deactivate MCLK clock.

5.15 Low-Power Modes

The ULPD module controls transitions to the two low-power modes referred to as big sleep and deep sleep modes. Awake is the only active mode for which OMAP3.2 can fetch instructions.

In addition, if some components are not used, they can be put in low-power mode to reduce power dissipation.

Table 16. Control for Special Components

Components	Software Control	Notes
32-kHz oscillator	OSC32K_PWRDN_R	Control in RTC register file
12-MHz oscillator	CONF_OSC1_PWRDN_R	Control in OMAP5912 configuration register file
LDO	CONF_LDO_PWRDN_CNTRL_R	Dedicated embedded LDO for DPLL control in OMAP5912 configuration register file
	SOFT_LDO_SLEEP	Control in ULPD register file
DPLL	PLL_ENABLE	Converts 12-MHz to19.2-MHz clock input to high-frequency clock used in OMAP3.2 clock tree
		Control in DPLL register file
APLL	None	Converts 12-MHz to 19.2-MHz clock to 48-MHz clock
		APLL active whenever a request for 48-MHz clock is set to 1.

Table 17 details the OMAP5912 sleep modes as they relate to power dissipation and clocks.

Table 17. Mode Description

Modes	Power Dissipation	Clocks
Deep sleep	Lowest	32 kHz for wake-up detection
Big sleep	Caused by gates clocked by 32-kHz clocks and clocks derived from 96-MHz PLL	Each active clock (32-kHz clocks and clocks from 96-MHz PLL) can be gated.
Awake	Nominal	32-kHz clocks and system clocks

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