TMS320C5515/14/05/04/VC05/VC04 DSP General-Purpose Input/Output (GPIO)

User's Guide

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About This Manual

This document describes the general-purpose input/output (GPIO) on the TMS320C5515/14/05/04/VC05/VC04 digital signal processor (DSP).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320C5515/14/05/04 Digital Signal Processor (DSP) Digital Signal Processor (DSP). Copies of these documents are available on the internet at http://www.ti.com.

SWPU073 — TMS320C55x 3.0 CPU Reference Guide. This manual describes the architecture, registers, and operation of the fixed-point TMS320C55x digital signal processor (DSP) CPU.

SPRU652 — TMS320C55x DSP CPU Programmer's Reference Supplement. This document describes functional exceptions to the CPU behavior.

SPRUFO0 — TMS320VC5505/5504 Digital Signal Processor (DSP) Universal Serial Bus 2.0 (USB) User's Guide. This document describes the universal serial bus 2.0 (USB) in the TMS320VC5505/5504 Digital Signal Processor (DSP). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices.

SPRUFO1 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Inter-Integrated Circuit (I2C) Peripheral User's Guide. This document describes the inter-integrated circuit (I2C) peripheral in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The I2C peripheral provides an interface between the device and other devices compliant with Phillips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. This document assumes the reader is familiar with the I2C-bus specification.

SPRUFO2 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Timer/Watchdog Timer User's Guide. This document provides an overview of the three 32-bit timers in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The 32-bit timers of the device are software programmable timers that can be configured as general-purpose (GP) timers. Timer 2 can be configured as a GP, a Watchdog (WD), or both simultaneously.

SPRUFO3 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Serial Peripheral Interface (SPI) User's Guide. This document describes the serial peripheral interface (SPI) in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to four SPI slave devices. The SPI can operate as a master device only.

SPRUFO4 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) General-Purpose Input/Output (GPIO) User's Guide. This document describes the general-purpose input/output (GPIO) on the TMS320VC5505/5504 digital signal processor (DSP). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of an internal register. When configured as an output you can write to an internal register to control the state driven on the output pin.

SPRUFO5 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Universal Asynchronous Receiver/Transmitter (UART) User's Guide. This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU.

SPRUFO6 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Multimedia Card (MMC)/Secure Digital (SD) Card Controller User's Guide. This document describes the Multimedia Card (MMC)/Secure Digital (SD) Card Controller on the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The multimedia card (MMC)/secure digital (SD) card is used in a number of applications to provide removable data storage. The MMC/SD card controller provides an interface to external MMC and SD cards.

SPRUF07 — TMS320VC5505/5504 Digital Signal Processor (DSP) Real-Time Clock (RTC) User's Guide. This document describes the operation of the Real-Time Clock (RTC) module in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The RTC also has the capability to wake-up the power management and apply power to the rest of the device through an alarm, periodic interrupt, or external WAKEUP signal.

SPRUFO8 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) External Memory Interface (EMIF) User's Guide. This document describes the operation of the external memory interface (EMIF) in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The purpose of the EMIF is to provide a means to connect to a variety of external devices.

SPRUFO9 — TMS320VC5505/5504 Digital Signal Processor (DSP) Direct Memory Access (DMA) Controller User's Guide. This document describes the features and operation of the DMA controller that is available on the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The DMA controller is used to move data among internal memory, external memory, and peripherals without intervention from the CPU and in the background of CPU operation.

SPRUFP0 — TMS320VC5505 Digital Signal Processor (DSP) System User's Guide. This document describes various aspects of the TMS320VC5505/5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

SPRUGL6 — TMS320VC5504 Digital Signal Processor (DSP) System User's Guide. This document describes various aspects of the TMS320VC5505/5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

SPRUFP1 — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Successive Approximation (SAR) Analog to Digital Converter (ADC) User's Guide. This document provides an overview of the Successive Approximation (SAR) Analog to Digital Converter (ADC) on the TMS320VC5505/5504 Digital Signal Processor (DSP). The SAR is a 10-bit ADC using a switched capacitor architecture which converts an analog input signal to a digital value.

SPRUFP3 — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Liquid Crystal Display Controller (LCDC) User's Guide. This document describes the liquid crystal display controller (LCDC) in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The LCD controller includes a LCD Interface Display Driver (LIDD) controller.

SPRUFP4 — TMS320VC5505/5504 Digital Signal Processor (DSP) Inter-IC Sound (I2S) Bus User's Guide. This document describes the features and operation of Inter-IC Sound (I2S) Bus in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. This peripheral allows serial transfer of full duplex streaming data, usually streaming audio, between DSP and an external I2S peripheral device such as an audio codec.

General-Purpose Input/Output (GPIO)

1 Introduction

This document describes the general-purpose input/output (GPIO) on the TMS320C5515/14/05/04/VC05/VC04 digital signal processor (DSP).

1.1 Purpose of the peripheral

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of the internal register. The GPIO can also be used to send interrupts to the CPU.

1.2 Features

The GPIO Peripheral consists of the following features:

- 32 GPIOs.
- Output Set/Clear functionality through writing a single output data register.
- All GPIOs can be configured to generate edge detected interrupts to the CPU.

1.3 Industry Standard(s) Compliance Statement

The GPIO peripheral connects to external devices. While it is possible that the software implements some standard connectivity protocol over GPIO, the GPIO peripheral itself is not compliant with any such standards.

2 Peripheral Architecture

The following sections describe the GPIO peripheral.

2.1 Clock Control

The input clock to the GPIO peripheral is driven by the system clock.

2.2 Signal Descriptions

The device supports up to 32 signals, GPIO[31:0]. All GPIO pins are muxed with other signals and have an optional internal pull-down resistor. The mux is controlled in the External Bus Selection Register (EBSR) located at port address 0x1C00h. The routing of the signals take place on the next CPU clock cycle. Before modifying the values of EBSR, you must first clock gated all affected peripherals via the Peripheral Clock Gating Control Register (PCGCR1 and PCGCR2) at addresses 0x1C02h and 0x1C03h. The EBSR can be modified only once after boot process is complete. Continuously switching the EBSR is not supported. Pull-downs are disable or enabled by the Pull-down Inhibit Register (0x1C17h, 0x1C18h and 0x1C19h) located in the data manual. These 32 GPIO are muxed with other signals. For more information on the package pinout and muxing of each GPIO signal, refer to the device-specific data manual.

Due to a variety of different technology devices that can be connected to the GPIO, the levels of logic 0 (low) and logic 1 (high) are not fixed and depend on the supply level. See the device-specific data manual for more information.

Table 1. GPIO Terminal Functions

Signal		Type [1]	Other	Description
Name	NO.			
MMC0_CLK/ I2S0_CLK/ GP[0]	L10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 0 (GP[0]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_CMD/ I2S0_FS/ GP[1]	M11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 1 (GP[1]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_D0/ I2S0_DX/ GP[2]	L9	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 2 (GP[2]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_D1/ I2S0_RX/ GP[3]	M10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 3 (GP[3]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_D2/ GP[4]	L12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0 and GPIO. For GPIO, it is general-purpose input/output pin 4 (GP[4]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_D3/ GP[5]	L11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0 and GPIO. For GPIO, it is general-purpose input/output pin 5 (GP[5]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_CLK/ I2S1_CLK/ GP[6]	M13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, MMC1, I2S1 and GPIO. For GPIO, it is general-purpose input/output pin 6 (GP[6]). Mux control via the SP1MODE bits in the EBSR.
MMC1_CMD/ I2S1_FS/ GP[7]	L14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, MMC1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 7 (GP[7]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_D0/ I2S1_DX/ GP[8]	M14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, MMC1, I2S1 and GPIO. For GPIO, it is general-purpose input/output pin 8 (GP[8]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_D1/ I2S1_RX/ GP[9]	M12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, MMC1, I2S1 and GPIO. For GPIO, it is general-purpose input/output pin 9 (GP[9]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_D2/ GP[10]	K14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1 and GPIO. For GPIO, it is general-purpose input/output pin 10 (GP[10]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_D3/ GP[11]	L13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1 and GPIO. For GPIO, it is general-purpose input/output pin 11 (GP[11]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
LCD_D[2]/ GP[12]	P7	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 12 (GP[12]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[3]/ GP[13]	N7	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 13 (GP[13]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[4]/ GP[14]	N8	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 15 (GP[15]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.

[1] I = Input, O = Output, Z = High Impedance

Table 1. GPIO Terminal Functions (continued)

Signal		Type [1]	Other	Description
Name	NO.			
LCD_D[5]/ GP[15]	P9	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 16 (GP[16]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[6]/ GP[16]	N9	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 17 (GP[17]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[7]/ GP[17]	P10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 18 (GP[18]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D8]/ I2S2_CLK/ GP[18]/ SPI_CLK	N10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 18 (GP[18]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	P11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, LCD Bridge, I2S2, and GPIO. For GPIO, it is general-purpose input/output pin 19 (GP[19]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	N11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO and SPI. For GPIO, it is general-purpose input/output pin 20 (GP[20]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
EM_A[15]/GP[21]	N1	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 21 (GP[21]). Mux control via the A15_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[16]/GP[22]	E2	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 22 (GP[22]). Mux control via the A16_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[17]/GP[23]	GP	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 23 (GP[23]). Mux control via the A17_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[18]/GP[24]	G2	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 24 (GP[24]). Mux control via the A18_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[19]/GP[25]	G4	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 25 (GP[25]). Mux control via the A19_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[20]/GP[26]	J3	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 26 (GP[26]). Mux control via the A20_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	P12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For GPIO, it is general-purpose input/output pin 27 (GP[27]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.

Table 1. GPIO Terminal Functions (continued)

Signal		Type [1]	Other	Description
Name	NO.			
LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	N12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 28 (GP[28]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	P13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 29 (GP[29]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	N13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 30 (GP[30]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	P14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 31 (GP[31]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.

2.3 GPIO Register Structure

The GPIO configuration registers are grouped into two 16-bit registers for each function. Control of the general-purpose I/O is maintained through a set of I/O memory mapped registers. For detailed information on the GPIO registers, see Section 3.

2.4 Using a GPIO Signal as an Output

GPIO signals are configured to operate as inputs or outputs by writing the appropriate value to the GPIO direction registers (IODIR1 and IODIR2). This section describes using the GPIO signal as an output.

2.4.1 Configuring a GPIO Output Signal

To configure a given GPIO signal as an output, set the bit in (IODIR1 and IODIR2) that is associated with the desired GPIO signal. For detailed information on the GPIO direction registers, see Section 3.1.

2.4.2 Controlling the GPIO Output Signal State

The GPIO output is controlled by the setting or clearing the OUT bit in the GPIO data out registers (IODATAOUT1 or IODATAOUT2) for the desired GPIO. When the GPIO is configured for output, a write of "1" will make the output high and a write of "0" will make the output low. For detailed information on in the GPIO data out registers, see Section 3.3.

2.5 Using a GPIO Signal as an Input

GPIO signals are configured to operate as inputs or outputs by writing the appropriate value to the IODIR1 or IODIR2 registers. This section describes using the GPIO signal as an input.

2.5.1 Configuring a GPIO Input Signal

To configure a given GPIO signal as an input, clear the bit in the GPIO direct register (IODIR1 or IODIR2) that is associated with the desired GPIO signal. For detailed information on GPIO direction registers, see Section 3.1.

2.5.2 Controlling the GPIO Input Signal State

The current state of the GPIO signals are read using the GPIO data in registers (IOINDATA1 & IOINDATA2).

- For GPIO signals configured as inputs, reading input data register returns the state of the input signal synchronized to the GPIO peripheral (system clock).

- For GPIO signals configured as outputs, reading input data register returns the output value being driven by the device.

To use GPIO input signals as interrupt sources, see Section 2.7.

2.6 Reset Considerations

The GPIO peripheral is only reset by a hardware reset.

2.6.1 Software Reset Considerations

A software reset does not modify the configuration and state of the GPIO signals. Software resets include reset initiated through the emulator, the device's software reset instruction, and the Peripheral Reset Control Register (PRCR) (1C05h). For a detailed description, see the *TMS320VC5505 Digital Signal Processor (DSP) System User's Guide* (SPRUFP0).

2.6.2 Hardware Reset Considerations

A hardware reset will cause the GPIO configuration to return to the default state, including GPIO pin selection (GPIOs default to input), and data registers to their default states, therefore affecting the configuration and state of the GPIO signals.

2.7 Interrupt Support

GPIO peripheral can individually generate an interrupt. The GPIO interrupts are falling or rising edge triggered interrupts.

2.7.1 Interrupt Events and Requests

The GPIO signals can be configured to generate an interrupt. The device supports interrupts from the GPIO signals. All GPIO are tied a single interrupt. To determine which GPIO caused the interrupt, the GPIO interrupt flag registers (IOINTFLG1 and IOINTFLG2) must be read. For detailed information on the GPIO interrupt flag registers, see Section 3.6.

2.7.2 Enabling GPIO Interrupt Events

GPIO interrupt events are enabled in GPIO interrupt enable registers (IOINTEN1 and IOINTEN2). Interrupts can be enabled for each of the 32 GPIO. Setting a "1" to the appropriate GPIO will enable external interrupts for this pin. For detailed information on GPIO interrupt enable registers, see Section 3.5.

2.7.3 Configuring GPIO Interrupt Edge Triggering

Each GPIO interrupt source can be configured to generate an interrupt on the rising or the falling edge. The edge detection is synchronized to the GPIO peripheral module clock. This is controlled in the GPIO interrupt edge trigger enable registers (IOINTEDG1 and IOINTEDG2). Setting a "1" to this register will use Rising edge to trigger the interrupt and "0" sets it to Falling Edge triggered if interrupts are enabled for this GPIO. For detailed information on the GPIO interrupt edge trigger enable registers, see Section 3.4.

2.7.4 GPIO Interrupt Status

When an interrupt occurs on an enabled GPIO pin, the GPIO interrupt flag registers (IOINTFLG1 and IOINTFLG2) latch the corresponding bit to a "1". The interrupt signal to the CPU will be kept low until all flag bits in the IOINTFLG1 and IOINTFLG2 registers are cleared. To clear the flag you must write a "1" to the corresponding bit.

The status of the GPIO interrupt events can be monitored by reading the IOINTFLG1 and IOINTFLG2 registers. If a GPIO interrupt event has occurred the corresponding bit will be a set to a “1”. In the case of a non-interrupt the corresponding bit will be “0”.

2.7.5 Interrupt Multiplexing

No GPIO interrupts are multiplexed with other interrupt functions on the device.

3 Registers

Table 2 lists the memory-mapped registers for the general-purpose input/output (GPIO).

Table 2. Memory-mapped Registers for the General-purpose Input/Output (GPIO)

CPU Word Address	Acronym	Register Description	Section
1C06h	IODIR1	GPIO Direction Register 1	Section 3.1
1C07h	IODIR2	GPIO Direction Register 2	Section 3.1
1C08h	IOINDATA1	GPIO Data In Register 1	Section 3.2
1C09h	IOINDATA2	GPIO Data In Register 2	Section 3.2
1C0Ah	IODATAOUT1	GPIO Data Out Register 1	Section 3.3
1C0Bh	IODATAOUT2	GPIO Data Out Register 2	Section 3.3
1C0Ch	IOINTEDG1	GPIO Interrupt Edge Trigger Enable Register 1	Section 3.4
1C0Dh	IOINTEDG2	GPIO Interrupt Edge Trigger Enable Register 2	Section 3.4
1C0Eh	IOINTEN1	GPIO Interrupt Enable Register 1	Section 3.5
1C0Fh	IOINTEN2	GPIO Interrupt Enable Register 2	Section 3.5
1C10h	IOINTFLG1	GPIO Interrupt Flag Register 1	Section 3.6
1C11h	IOINTFLG2	GPIO Interrupt Flag Register 2	Section 3.6

3.1 GPIO Direction Registers (IODIR1 and IODIR2)

The device includes two registers for controlling whether the GPIO is set as a general-purpose Input, or Output. Use the GPIO direction register (IODIR1 and IODIR2) to set the GPIO pin as Input or Output. Each of these registers control 16 of the 32 GPIOs. IODIR1 is used for GPIO[15:0] with bit 0 corresponding to GPIO 0 through bit 15 corresponding to GPIO 15. IODIR2 is used for GPIO[31:16] with bit 0 corresponding to GPIO 16 through bit 15 corresponding to GPIO 31. Writing a "1" to these bits configures the pin as an OUTPUT and writing a "0" configures the pin as an INPUT.

The GPIO Direction Registers (IODIR1 and IODIR2) is shown in Figure 1 and Figure 2 and described in Table 3.

Figure 1. GPIO Direction Register 1 (IODIR1)

15		0
DIR		
RW+0		

LEGEND: R/W = Read/Write; n = value at reset

Figure 2. GPIO Direction Register 2 (IODIR2)

15		0
DIR		
RW+0		

LEGEND: R/W = Read/Write; n = value at reset

Table 3. GPIO Direction Register (IODIR1 and IODIR2) Bit Field Description

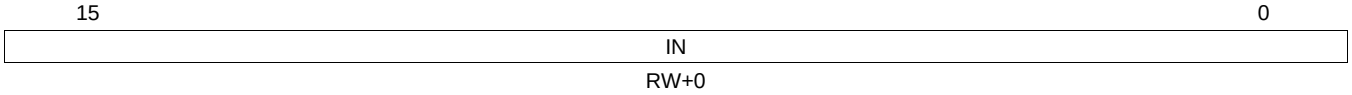
Bit	Field	Value	Description
15-0	DIR	0-FFFFh	Data direction bits that configure the general-purpose IO pins as either inputs or outputs. Bit 0 of IODIR1 corresponds to GPIO 0 and Bit 0 of IODIR2 corresponds to GPIO 16.
		0	Configure corresponding pin as an INPUT
		1	Configure corresponding pin as an OUTPUT.

3.2 GPIO Data In Registers (IOINDATA1 and IOINDATA2)

The device includes two registers for reading in the GPIO values when they are configured as Inputs. Use the GPIO data in registers (IOINDATA1 and IOINDATA2) to read the state of the corresponding GPIO pin. Each of these registers control 16 of the 32 GPIOs. IOINDATA1 is used for GPIO[15:0] with bit 0 corresponding to GPIO 0 through bit 15 corresponding to GPIO15. IOINDATA2 is used for GPIO[31:16] with bit 0 corresponding to GPIO 16 through bit 15 corresponding to GPIO 31.

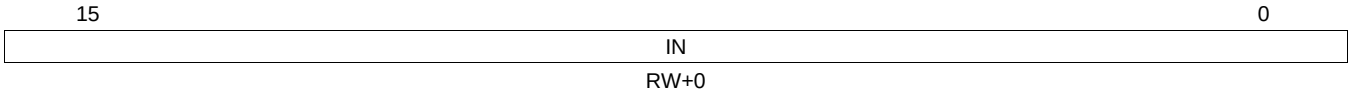
The GPIO Data In Registers (IOINDATA1 and IOINDATA2) is shown in Figure 3 and Figure 4 and described in Table 4.

Figure 3. GPIO Data In Register 1 (IOINDATA1)



LEGEND: R/W = Read/Write; n = value at reset

Figure 4. GPIO Data In Register 2 (IOINDATA2)



LEGEND: R/W = Read/Write; n = value at reset

Table 4. GPIO Data In Register (IOINDATA1 and IOINDATA2) Bit Field Description

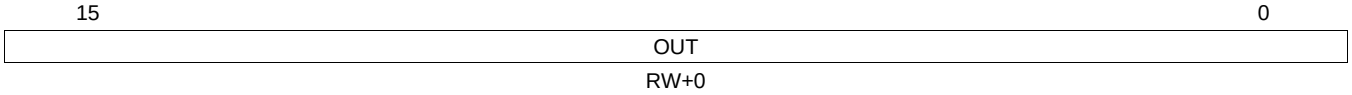
Bit	Field	Value	Description
15-0	IN	0-FFFFh	Data bits that are used to monitor the level of the GPIO pins configured as general-purpose input pins. If DIR = 0, then: • 0 = corresponding I/O pin is read as a LOW. • 1 = corresponding I/O pin is read as a HIGH. If DIR = 1, then: • X = reflects value of output pin.

3.3 GPIO Data Out Registers (IOOUTDATA1 and IOOUTDATA2)

The device includes two registers for writing to the GPIO pins when they are configured as outputs. Use the GPIO data out registers (IOOUTDATA1 and IOOUTDATA2) to change the state of the corresponding GPIO pin. Each of these registers control 16 of the 32 GPIOs. IOOUTDATA1 is used for GPIO[15:0] with bit 0 corresponding to GPIO 0 through bit 15 corresponding to GPIO15. IOOUTDATA2 is used for GPIO[31:16] with bit 0 corresponding to GPIO 16 through bit 15 corresponding to GPIO 31.

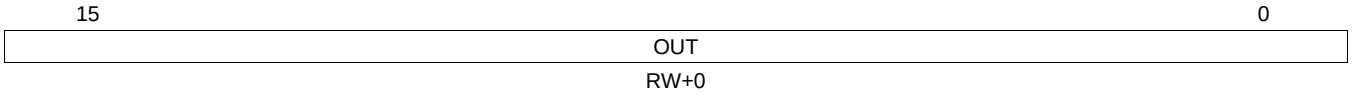
The GPIO Data Out Registers (IOOUTDATA1 and IOOUTDATA2) is shown in Figure 5 and Figure 6 and described in Table 5.

Figure 5. GPIO Data Out Register 1 (IODATAOUT1)



LEGEND: R/W = Read/Write; n = value at reset

Figure 6. GPIO Data Out Register 2 (IODATAOUT2)



LEGEND: R/W = Read/Write; n = value at reset

Table 5. GPIO Data Out Register (IOOUTDATA1 and IOOUTDATA2) Bit Field Description

Bit	Field	Value	Description
15-0	OUT	0-FFFFh	Data bits that are used to control the level of the GPIO pins configured as general-purpose output pins. If DIR = 0, then: • X = value stored on register but not reflected on the output pin. If DIR = 1, then: • 0 = set corresponding I/O pin to LOW. • 1 = set corresponding I/O pin to HIGH.

3.4 GPIO Interrupt Edge Trigger Registers (IOINTEDG1 and IOINTEDG2)

The device has two registers for configuring interrupts to trigger on the rising or falling edge of the input signal to the GPIO pins if they are configured as inputs with Interrupt enabled for the chosen GPIO. Use the GPIO interrupt edge trigger registers (IOINTEDG1 and IOINTEDG2) to enable rising or falling edge trigger for the corresponding GPIO pin. Each of these registers control 16 of the 32 GPIOs. IOINTEDG1 is used for GPIO[15:0] with bit 0 corresponding to GPIO 0 through bit 15 corresponding to GPIO15. IOINTEDG2 is used for GPIO[31:16] with bit 0 corresponding to GPIO 16 through bit 15 corresponding to GPIO 31.

The GPIO Interrupt Edge Trigger Registers (IOINTEDG1 and IOINTEDG2) is shown in Figure 7 and Figure 8 and described in Table 6.

Figure 7. GPIO Interrupt Edge Trigger Enable Register 1 (IOINTEDG1)

15	0
INTEDG	
RW+0	

LEGEND: R/W = Read/Write; n = value at reset

Figure 8. GPIO Interrupt Edge Trigger Enable Register 2 (IOINTEDG2)

15	0
INTEDG	
RW+0	

LEGEND: R/W = Read/Write; n = value at reset

Table 6. GPIO Interrupt Edge Trigger Enable Register (IOINTEDG1 and IOINTEDG2) Bit Field Description

Bit	Field	Value	Description
15-0	INTEDG	0-FFFFh	Configure the GPIO pin for rising or falling edge.
		0	Corresponding I/O pin has rising edge triggered interrupt capability.
		1	Corresponding I/O pin has falling edge triggered interrupt capability.

3.5 GPIO Interrupt Enable Registers (IOINTEN1 and IOINTEN2)

The device has two registers for enabling Interrupts on the GPIO pins if they are configured as Inputs. Use the GPIO interrupt enable registers (IOINTEN1 and IOINTEN2) to enable the interrupt of the corresponding GPIO pin. Each of these registers control 16 of the 32 GPIOs. IOINTEN1 is used for GPIO[15:0] with bit 0 corresponding to GPIO 0 through bit 15 corresponding to GPIO15. IOINTEN2 is used for GPIO[31:16] with bit 0 corresponding to GPIO 16 through bit 15 corresponding to GPIO 31.

The GPIO Interrupt Enable Registers (IOINTEN1 and IOINTEN2) is shown in Figure 9 and Figure 10 and described in Table 7.

Figure 9. GPIO Interrupt Enable Register 1 (IOINTEN1)

15	0
INTEN	
RW+0	

LEGEND: R/W = Read/Write; n = value at reset

Figure 10. GPIO Interrupt Enable Register 2 (IOINTEN2)

15	0
INTEN	
RW+0	

LEGEND: R/W = Read/Write; n = value at reset

Table 7. GPIO Interrupt Enable Register (IOINTEN1 and IOINTEN2) Bit Field Description

Bit	Field	Value	Description
15-0	INTEN	0-FFFFh	Enable or disable interrupt capability of the GPIO:
		0	Corresponding I/O pin has NO interrupt capability.
		1	Corresponding I/O pin is configured as an external interrupt.

3.6 GPIO Interrupt Flag Registers (IOINTFLG1 and IOINTFLG2)

The device has two registers that latch an interrupt that occurred with the corresponding GPIO pin. Use the GPIO interrupt flag registers (IOINTFLG1 and IOINTFLG2) to determine which GPIO pin triggered the interrupt. Also, these registers are used to clear the interrupt sent to the CPU. Each of these registers control 16 of the 32 GPIOs. IOINTFLG1 is used for GPIO[15:0] with bit 0 corresponding to GPIO 0 through bit 15 corresponding to GPIO15. IOINTFLG2 is used for GPIO[31:16] with bit 0 corresponding to GPIO 16 through bit 15 corresponding to GPIO 31.

The GPIO Interrupt Flag Registers (IOINTFLG1 and IOINTFLG2) is shown in Figure 11 and Figure 12 and described in Table 8.

Figure 11. GPIO Interrupt Flag Register 1 (IOINTFLG1)

15	0
INTFLG	
RW+0	

LEGEND: R/W = Read/Write; n = value at reset

Figure 12. GPIO Interrupt Flag Register 2 (IOINTFLG2)

15	0
INTFLG	
RW+0	

LEGEND: R/W = Read/Write; n = value at reset

Table 8. GPIO Interrupt Flag Enable Register (IOINTFLG1 and IOINTFLG2) Bit Field Description

Bit	Field	Value	Description
15-0	INTFLG	0-FFFFh	Register that latches if an interrupt occurred in the corresponding I/O pin, if interrupts were enabled. The flag is cleared by writing a “1” or setting the corresponding bit. The interrupt signal to the CPU will be kept low until all flag bits in this register are cleared.
		0	Corresponding I/O interrupt has not occurred.
		1	Corresponding I/O interrupt occurred. Write of “1” resets the flag.

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