DRA78x-15X15 EVM

User's Guide

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Introduction

The DRA78x evaluation module (EVM) is an evaluation platform designed to speed up development efforts and reduce time-to-market for Radio Signal Processor applications. The EVM is based on the DRA78x SoC, which incorporates a heterogeneous, scalable architecture that includes a mixture of the following:

- TI's fixed and floating-point TMS320C66x Digital Signal Processors (DSPs)
- Vision AccelerationPac with Embedded Vision Engine (EVE)
- Dual ARM® Cortex®-M4 processors

The EVM also integrates a host of peripherals including multicamera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN, and GigB Ethernet AVB. The EVM also integrates key peripherals such as Ethernet, FPD-Link, and HDMI.

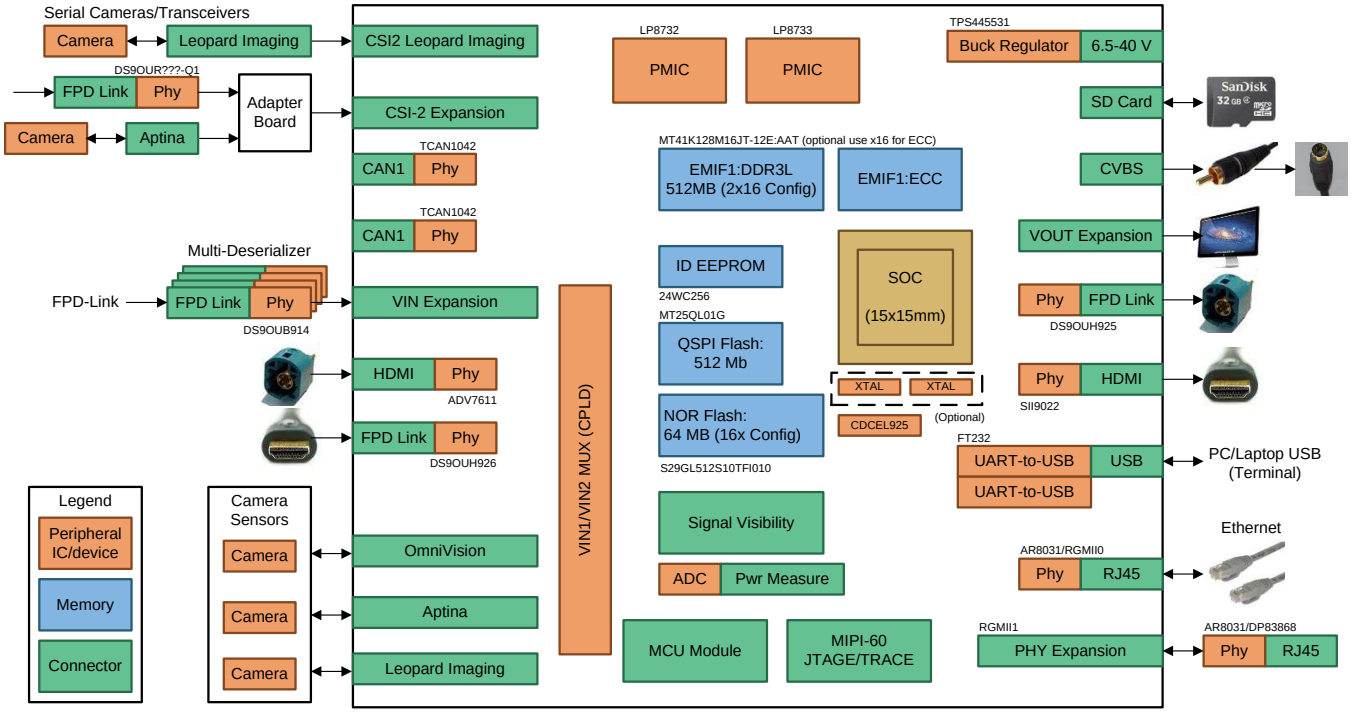
Overview

An EVM system is comprised of a CPU board with various camera interface connectors. The CPU board (see Figure 2-1 for the block diagram and Figure 2-2 for the board photo) can be used as a stand-alone for software debug and development. Each EVM system is designed to let customers evaluate the processor performance and flexibility in Automotive and Radio Signal Processor application markets.

The CPU board contains the TDA3x, DRA78x, and DM50x (superset part) applications processor, a companion power solution (LP8733 and LP8732), DDR3 DRAM, flash memories (QSPI and NOR), and numerous interface ports and expansion connectors. The board provides additional support components that provide software debugging, signal routing, and configuration controls that are not needed in a final product. Different versions of the CPU boards will be built to support the development process that includes the following:

- Socketed processor for wakeup, early software development, and quick and easy chip revision evaluation
- Soldered-down processor for high-performance use cases and evaluations

All other onboard components are soldered-down.



Note: Camera Sensor(s), CSI-2 Expansion, and Phy Expansion connectors will be re-used from J6-Eco.

Figure 2-1. EVM Block Diagram

(1) ARM, Cortex are registered trademarks of ARM Limited.
(2) Micron is a registered trademark of Micron Technology.
(3) MIPI is a registered trademark of Mobile Industry Processor Interface Alliance.

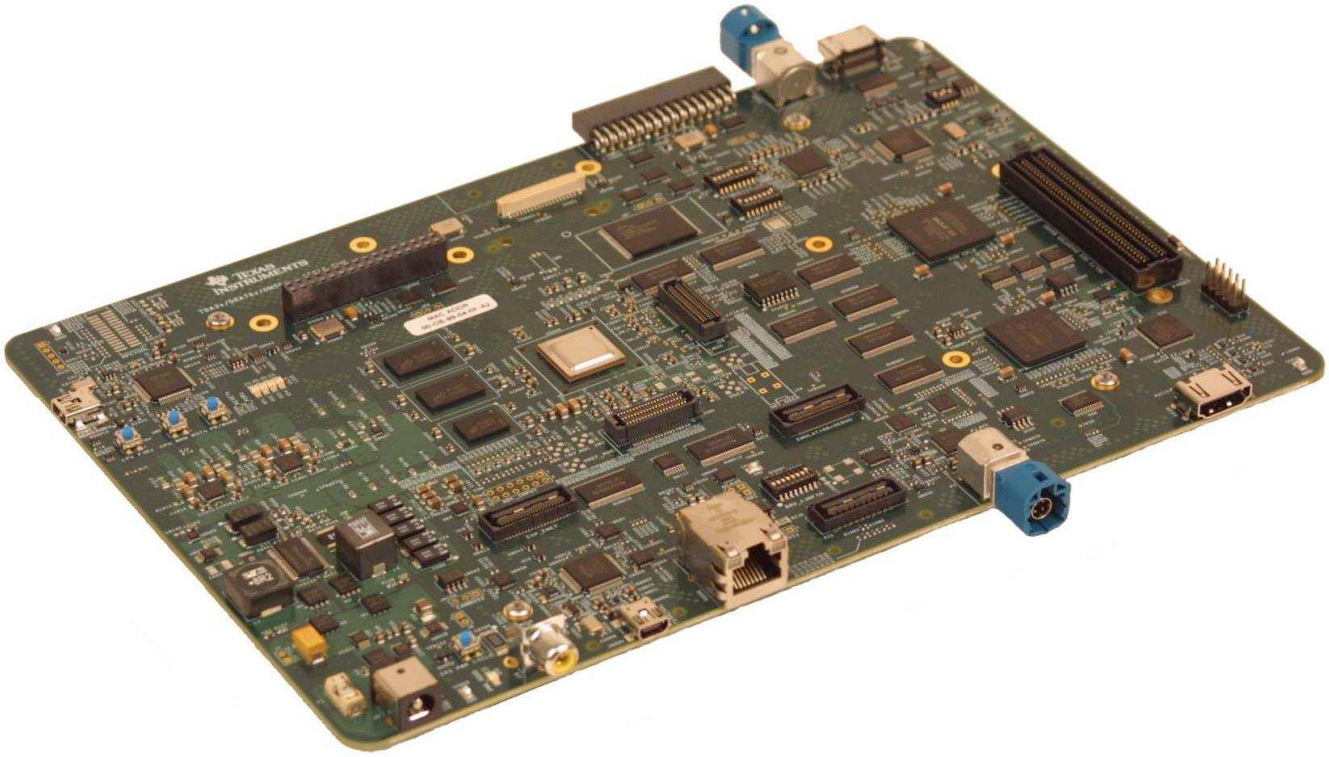


Figure 2-2. EVM Board

2.1 Features

The EVM has the following features:

- Processor:
  - 15-mm × 15-mm package, 0.65-mm pitch (25 × 25 grid)
  - Support for corresponding Ironwood socket
- Power:
  - 12-V DC input
  - Dedicated PMIC solution (LP8733 and LP8732)
  - Power sequencing compliant with SoC requirements
  - Integrated power measurement
  - Power bench support (SVB)
- PCB:
  - Dimension (W × D): 280 mm × 215 mm (11” × 8.5”)
  - 100% PTH technology
- Memory:
  - DRAM (DDR3L-1333): 4Gb + 1Gbit ECC
  - Quad-SPI: 1GB
  - NOR: 512MB
  - I2C EEPROM: 256KB
  - SD/MMC Socket
  - Support for GPMC expansion interface
- Boot mode selection DIP switch
- Signal visibility/expansion interface
- Digital temperature sensor/thermistor
- JTAG/Emulator:
  - 60-pin MIPI® JTAG with up to 20-bit trace
- Modules and Transceivers:
  - CAN interface, 2-wire PHY
  - CAN-FD interface, 2-wire PHY
  - NTSC/PAL composite video (RCA-style)
  - FPD-Link III, serializer and deserializer
  - Support for FPD-Link III multideserializer module
  - HDMI, serializer and deserializer
  - Camera sensor support, including OmniVision, Aptina, and Leopard imaging modules
  - External display panel support
  - Gigabit Ethernet PHY (RJ45), support for the second Ethernet PHY using dedicated expansion
  - *RS-232* using the USB FTDI converter (mini-A/B USB)
  - Support for interfacing with safety MCU EVM

Hardware

3.1 Hardware Architecture

Figure 2-1 shows the EVM block diagram. Table 3-1 lists the targeted orderable EVMs and boards.

Table 3-1. SoC EVMs

Product	Description
EVMTDA3G-02-40-00	TDA3x/DRA78x/DM50x-15X15 EVM Kit (Includes CPU/Vision Board)
EVMTDA3G-02-40-S0	TDA3x/DRA78x/DM50x-15X15 EVM Kit Socketed (Includes CPU/Vision Board)

3.2 TDA3x, DRA78x, and DM50x Processor

The processor is a highly integrated, programmable SoC silicon solution. Figure 3-1 shows the SoC block diagram from the chip specification.

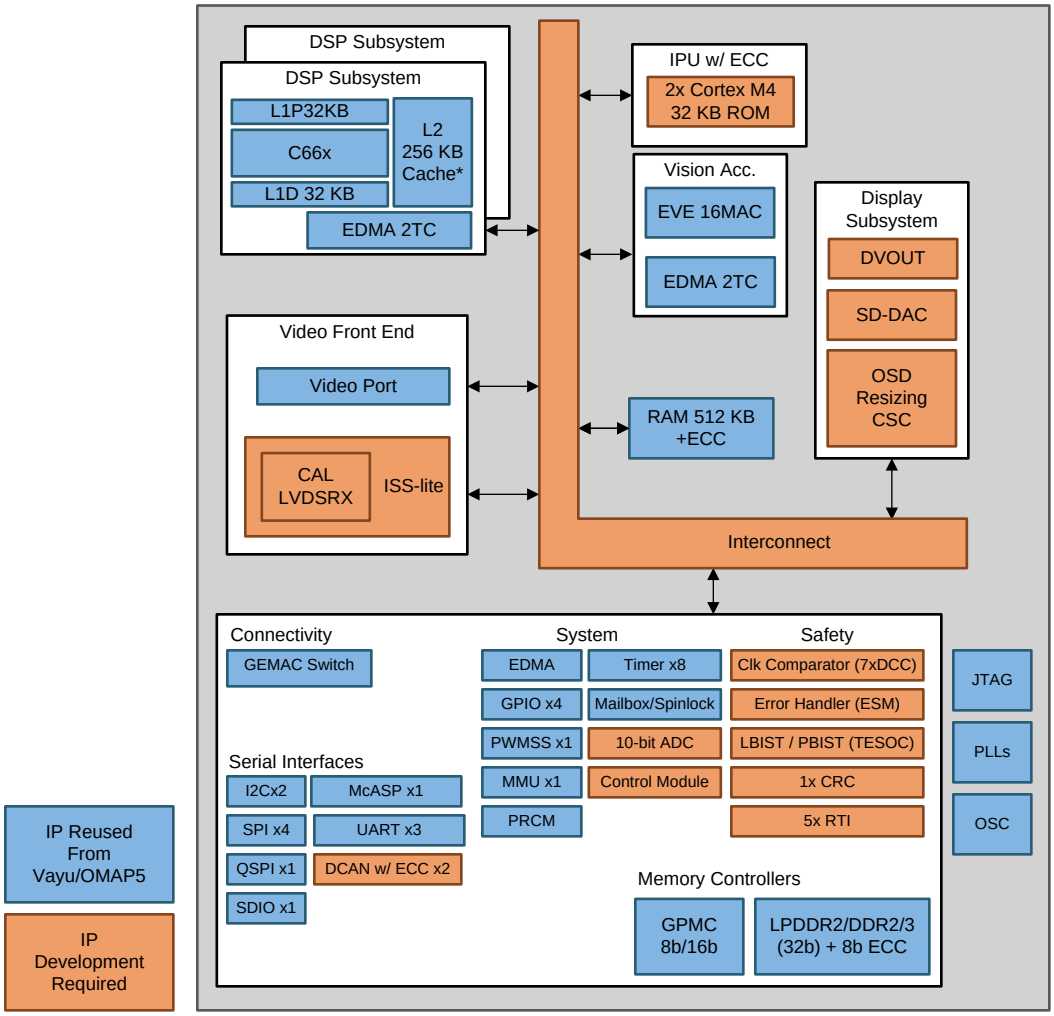


Figure 3-1. Processor Block Diagram

3.3 Power Supply

The companion power management IC (PMIC) for the SoC is a combination of LP8733 and LP8732 devices. The regulators of the PMIC are dedicated for each of the separate power domains of the SoC. The PMIC includes detection of power on and off events as well as power up and down sequencing requirements. A step-down 12 V to 5 V/3.3-V converter (TPS43351) is required to provide a 5 V, 3.3-V DC inputs to the PMIC as well as at the board-level peripherals.

Figure 3-2 shows the high-level block diagram.

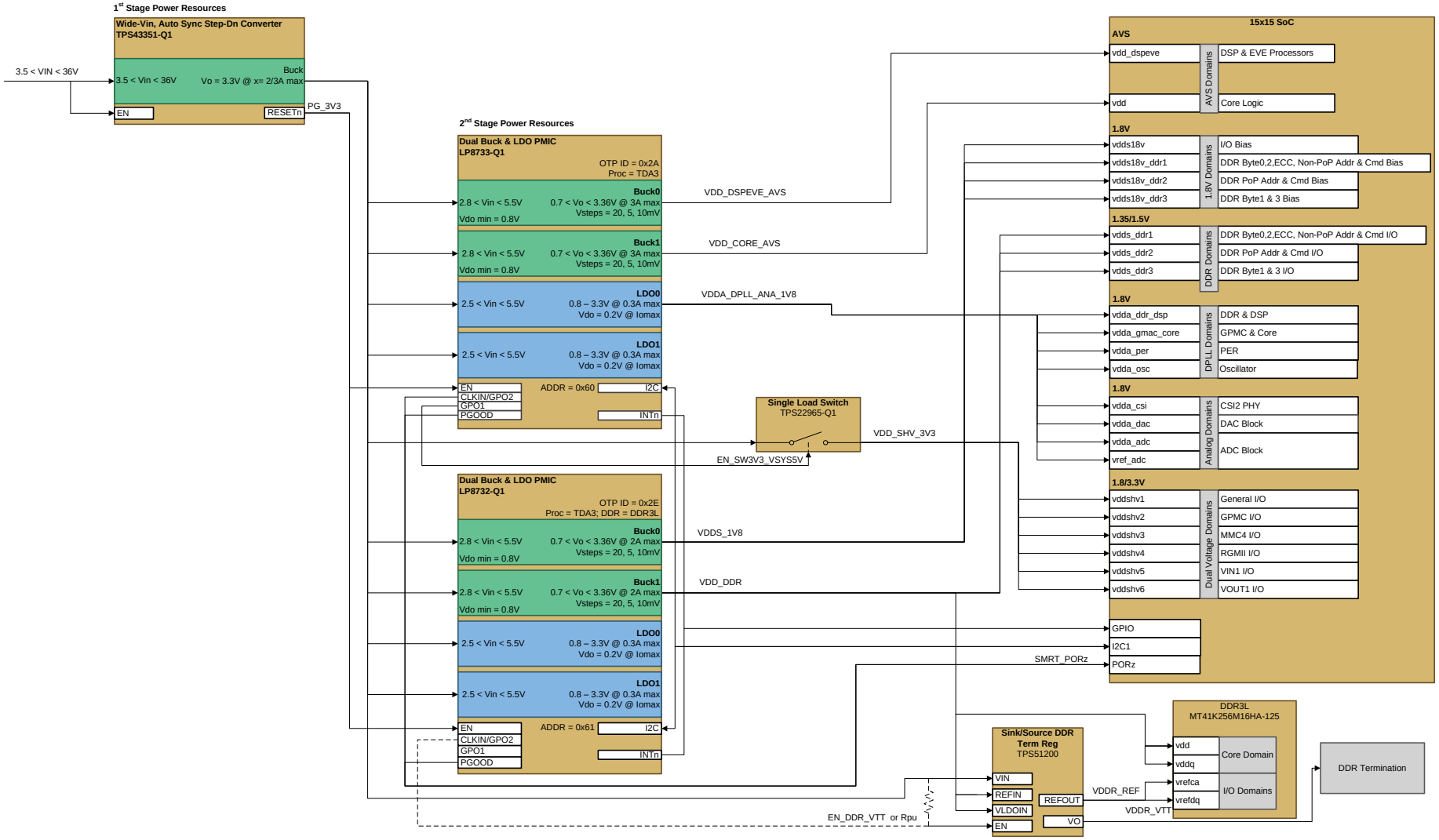


Figure 3-2. High-Level Power Supply Block Diagram

3.4 External Power Supply

An external/wall power supply is not included as a part of the EVM kit. The EVM has the following power requirements:

- Nom voltage: 12 VDC
- Maximum current: 5000 mA
- Efficiency level V

Table 3-2 lists the recommended and tested supplies for use with the EVM.

Table 3-2. Recommended and Tested Supplies for Use With EVM(1)

Digi-Key Part Number	Manufacturer Part Number	Manufacturer	Output Connector	Notes
102-3417-ND	SDI65-12-U-P5	CUI Inc	Barrel plug, 2.1 mm I.D. × 5.5 mm O.D. × 9.5 mm	Required adapter, provided in EVM kit
62-1221-ND	KTPS65-1250DT-3P-VI-C-P1	Volgen America/Kaga Electronics USA	Barrel plug, 2.1 mm I.D. × 5.5 mm O.D. × 9.5 mm	Required adapter, provided in EVM kit
102-3419-ND	SDI65-12-UD-P5	CUI Inc	Barrel plug, 2.1 mm I.D. × 5.5 mm O.D. × 9.5 mm	Required adapter, provided in EVM kit
SDI65-12-U-P6-ND	SDI65-12-U-P6	CUI Inc	Barrel plug, 2.1 mm I.D. × 5.5 mm O.D. × 9.5 mm	
SDI65-12-UD-P6-ND	SDI65-12-UD-P6	CUI Inc	Barrel plug, 2.1 mm I.D. × 5.5 mm O.D. × 9.5 mm	

(1) External power supply regulatory compliance certifications: TI recommends selection and use of an external power supply which meets TI's required minimum electrical ratings in addition to complying with applicable regional product regulatory and safety certification requirements such as UL, CSA, VDE, CCC, PSE, and more.

3.5 Visibility and Expansion Connectors

Two connectors for visibility of the I/O are near the SoC. This interface targets standard CMOS-type signals, and does not include DDR and CSI2 signals. The primary purpose of this interface is to provide direct (and isolated) access to all SoC I/Os for verification and characterization. The connectors can also be used for expansion to interface with other application and validation boards (see Figure 3-3).

Visibility connector used: Samtec SEAF8-20-05.0-S-06-2-K

For signal isolation, a series resistor is placed immediately after the visibility connector for minimal impact.

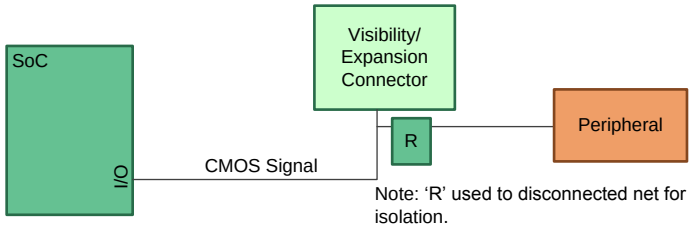


Figure 3-3. System Visibility Diagram

Figure 3-4 and Figure 3-5 show the signal definition for the visibility connectors. Only the primary function is shown. For all muxing options available, see the SoC data manual.

Connector: Samtec SEAF8-20-05.0-S-06-2-K											
Pin	SoC	Pin	SoC	Pin	SoC	Pin	SoC	Pin	SoC	Pin	SoC
1	<open>	2	<open>	3	<open>	4	<open>	5	UART2_CTSN	6	<open>
7	VIN1A_FLD0	8	<open>	9	<open>	10	GND	11	VIN1A_HSYNC0	12	VIN1A_D0
13	UART2_RTSN	14	<open>	15	<open>	16	GND	17	VIN1A_D1	18	VIN1A_VSYNC0
19	VIN1A_DE0	20	<open>	21	<open>	22	GND	23	VIN1A_CLK	24	VIN1A_D2
25	VIN1A_D4	26	<open>	27	<open>	28	GND	29	UART1_CTSN	30	VIN1A_D3
31	VIN1A_D6	32	<open>	33	<open>	34	GND	35	VIN1A_D9	36	VIN1A_D10
37	VIN1A_D7	38	<open>	39	<open>	40	GND	41	VIN1A_D5	42	VIN1A_D15
43	VIN2A_CLK0	44	<open>	45	<open>	46	GND	47	VIN1A_D14	48	VIN1A_D11
49	VIN1A_D8	50	<open>	51	<open>	52	GND	53	VIN2A_FLD0	54	VIN1A_D12
55	VIN1A_D13	56	<open>	57	<open>	58	GND	59	VOUT1_VSYNC	60	VIN1_DE
61	VIN2A_DE0	62	<open>	63	<open>	64	GND	65	VOUT1_D0	66	VOUT1_FLD
67	VOUT1_D1	68	<open>	69	<open>	70	GND	71	VOUT1_D6	72	VOUT1_CLK
73	VOUT1_HSYNC	74	<open>	75	<open>	76	GND	77	VOUT1_D5	78	VOUT1_D2
79	VOUT1_D3	80	<open>	81	<open>	82	GND	83	VOUT1_D8	84	VOUT1_D7
85	VOUT1_D4	86	<open>	87	<open>	88	GND	89	VOUT1_D13	90	VOUT1_D9
91	VOUT1_D11	92	<open>	93	<open>	94	GND	95	VOUT1_D19	96	VOUT1_17
97	VOUT1_D12	98	<open>	99	<open>	100	GND	101	VOUT1_D18	102	VOUT1_D10
103	VOUT1_D15	104	<open>	105	<open>	106	<open>	107	VOUT1_D21	108	VOUT1_D16
109	VOUT1_D14	110	<open>	111	<open>	112	VOUT1_D23	113	VIO	114	DCAN2_TX
115	VOUT1_D20	116	<open>	117	<open>	118	VOUT1_D22	119	VIO	120	DCAN2_RX

Figure 3-4. Signal Assignments: Visibility Connector J1003

Connector: Samtec SEAF8-20-05.0-S-06-2-K											
Pin	SoC	Pin	SoC	Pin	SoC	Pin	SoC	Pin	SoC	Pin	SoC
1	SPI1_CS1	2	SPI2_D0	3		4		5	SPI1_CS0	6	SPI1_D0
7	I2C1_SCL	8	XREF_CLK0	9		10	GND	11	SPI1_SCLK	12	SPI1_D1
13	DCAN1_RX	14		15		16	GND	17	SPI1_SCLK	18	DCAN1_TX
19		20		21		22		23	I2C1_SDA	24	SPI2_D1
25	GPMC_AD12	26	GPMC_AD9	27		28	GND	29	GPMC_AD14	30	SPI2_CS0
31	GPMC_AD15	32	GPMC_AD4	33		34	GND	35	GPMC_AD11	36	I2C2_SDA
37	I2C2_SCL	38	GPMC_AD1	39		40	GND	41	GPMC_AD2	42	GPMC_AD7
43	GPMC_CS6	44	GPMC_AD13	45		46	GND	47	GPMC_AD5	48	GPMC_AD10
49	GPMC_AD8	50	GPMC_CS2	51		52	GND	53	GPMC_AD3	54	GPMC_AD6
55	GPMC_CS4	56		57		58	GND	59	GPMC_AD0	60	GPMC_WAIT0
61	GPMC_WEN	62		63		64	GND	65	GPMC_CS3	66	GPMC_CS5
67	GPMC_OEN	68		69		70	GND	71	GPMC_CS1	72	GPMC_BEN0
73	GPMC_CLK	74		75		76	GND	77	GPMC_CS0	78	
79	GPMC_ADVN	80		81		82	GND	83		84	
85	UART2_RXD	86		87		88	GND	89	UART1_RTSN	90	GPMC_BEN1
91	UART1_TXD	92		93		94	GND	95	RGMII0_TXC	96	UART1_RXD
97	RGMII0_TXD2	98		99		100	GND	101	RGMII0_TXD3	102	UART2_TXD
103	RGMII0_TXCTL	104		105		106		107	RGMII0_RXC	108	RGMII0_TXD1
109	RGMII0_RXD3	110	MDIO_D	111		112	RGMII0_RXD0	113	VIO	114	MDIO_MCLK
115	RGMII0_RXD1	116	RGMII0_RXD2	117		118	RGMII0_TXD0	119	VIO	120	RGMII0_RXCTL

Figure 3-5. Signal Assignments: Visibility Connector J28

3.6 Clocks

The 20-MHz device clock and 22.5792-MHz auxiliary clock are generated by a programmable clock synthesizer, the CDCEL925. Optionally, the frequencies can be generated by external crystals connected directly to the SoC. The platform includes options for an oscillator socket (7 × 5 mm) and MMCX connector to support testing of additional sources and frequencies (not included on most assemblies).

NOTE: The oscillator socket and coax interface connector footprints are available but not populated.

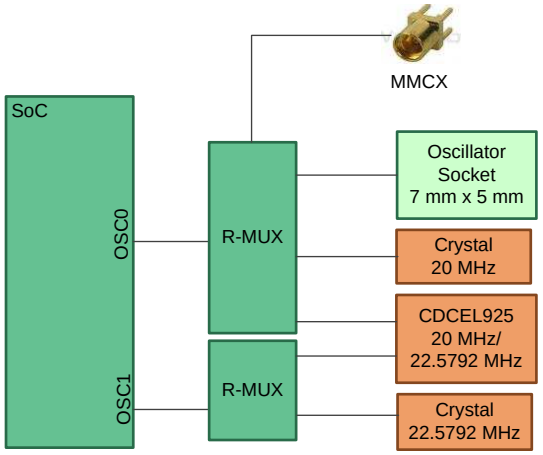


Figure 3-6. SoC Source Clock Diagram

Other IC components may need reference clocks and are locally generated.

3.7 Boot Modes

The SoC supports various boot modes (see Figure 3-7). The selections of the boot modes are accomplished by latching the state of the GPMC_AD[15:8, 6:0] and SPI2_D[0] (muxed with sysboot) signals during device reset. The high and low values latched determines the mode of the device.

DIP switches SW2 and SW3 on the SYSBOOT signals are enabled during reset to ensure the values are properly latched. Setting the switch to the OFF position causes a logic 0 to be latched. Setting the switch to the ON position causes a logic 1.

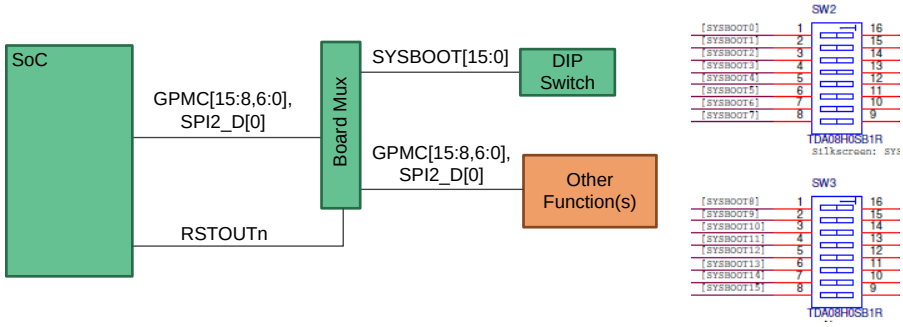


Figure 3-7. SYSBOOT Diagram

In addition to the SoC boot modes, the board also supports hardware configurations that can affect boot operations (see Table 3-3). SW8001 controls the PCB hardware settings.

Table 3-3. PCB Hardware Settings, SW8001

Signals	Default State	Description	I²C Expander
SEL_GPMCn	On	Selects default state for onboard GPMC muxes (GPMC selection is not default)	U8017. P00
I2C_EEPROM_WP		Selects EEPROM writeable state	None
IOEXP2_P[24:20)		User defined	U8006. P24-P20
SW_VPP_EN	Off	Enables software control for VPP programming power supply	U44.P10
SEL_HDMI_INn	Off	Selects access to HDMI EEPROM	U44. P00

3.8 Reset

Power-on reset (PORz) is controlled primarily from the system PMIC (LP8733 and LP8732). For other onboard supplies, supervisors are used and wired-OR with RESET_OUT of the PMIC. There are two push-buttons for reset. One is PORz for a complete system reset and another is for a warm reset (RESETn). The warm reset can also be source from the MIPI-60 Trace connector. Figure 3-8 describes the reset architecture.

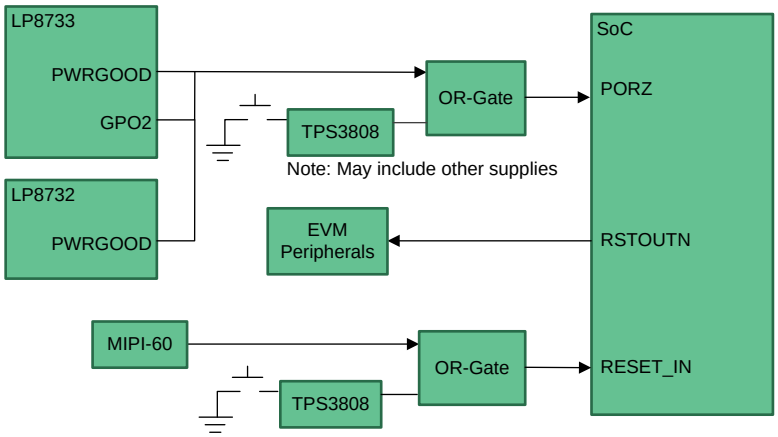


Figure 3-8. System Reset Diagram

Several buttons in the system allow for manual assertion of the various resets. Table 3-4 lists the reset locations.

Table 3-4. Reset Signals

Reset Signals	Switch Location	Description
PB_ON	SW9	Toggles power to the entire board (similar to unplugging power from jack). Resets are reasserted upon power up.
PORZ	SW4	Toggles the PORz reset signals to the system
RESET	SW6	Toggles the RESETN reset signal to the SoC device

There are reset implementations for individual IC components as necessary. The system-level reset must be qualified using the power supervisor chip.

3.9 Memory

3.9.1 DDR3 Memory

The EMIF1 has two 16-bit DDR3L memory devices, plus one 8-bit DDR3L device for ECC. All devices have a density of 2GB. The PCB footprint supports a 4GB DDR3L package. (The ECC memory can be a 16-bit device with 8b unused.)

DDR3L device used: Micron® MT41K128M16JT-125:K (two 16-bit at 2GB each or equivalent).

The power of the DDR3L is set to 1.35 V. The device uses fly-by topology with VTT termination. VTT is generated from a regulated supply, the TPS51200. The memory operates at a maximum rate of 667 MHz (DDR-1333).

For device characterization, the design supports DDR interposers that can be placed between the PCB and the memory components. Figure 3-9 shows the board layout.

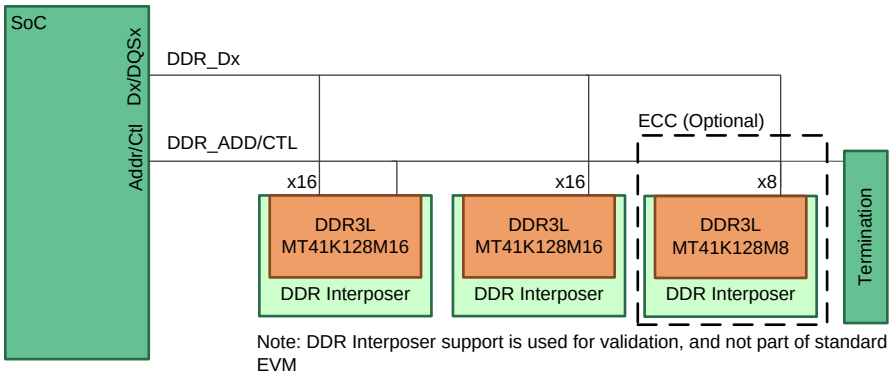


Figure 3-9. DDR3L Memory Diagram

3.9.2 Quad SPI Flash Memory

A 1-GB Quad-SPI (QSPI) flash memory is used as the primary nonvolatile storage/boot device (see Figure 3-10). The PCB footprint supports a wide range of densities (32MB to 1GB).

QSPI device used: Micron MT25QL01GBBB8ESF-0SIT

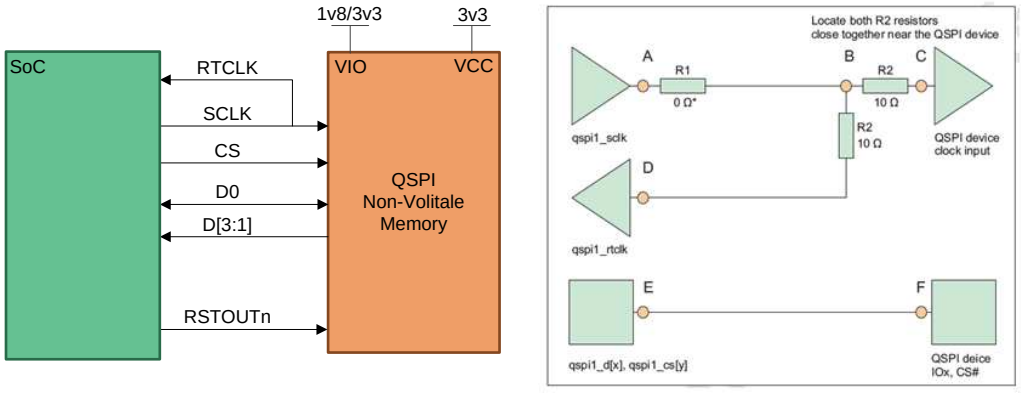


Figure 3-10. QSPI Memory Diagram

3.9.3 GPMC Flash Memory

A 16-bit, 512MB NOR flash memory is implemented in the design. For supporting other memory types (NAND, PSRAM, and so on), the design includes a memory expansion interface. The boot chip select GPMC_CS0 is to be selectable between onboard memory, socket, and expansion through onboard configuration selection (see Figure 3-11).

NOR device used: Spansion S29GL512S10TFI010

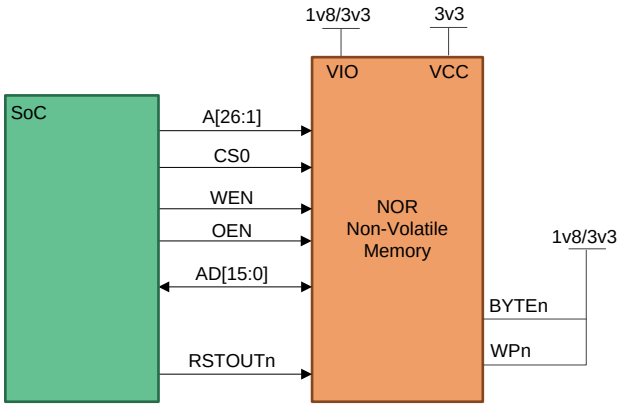


Figure 3-11. NOR Memory Configuration

The expansion interface is to align with previously used memory adapter boards. Figure 3-12 shows the interface.

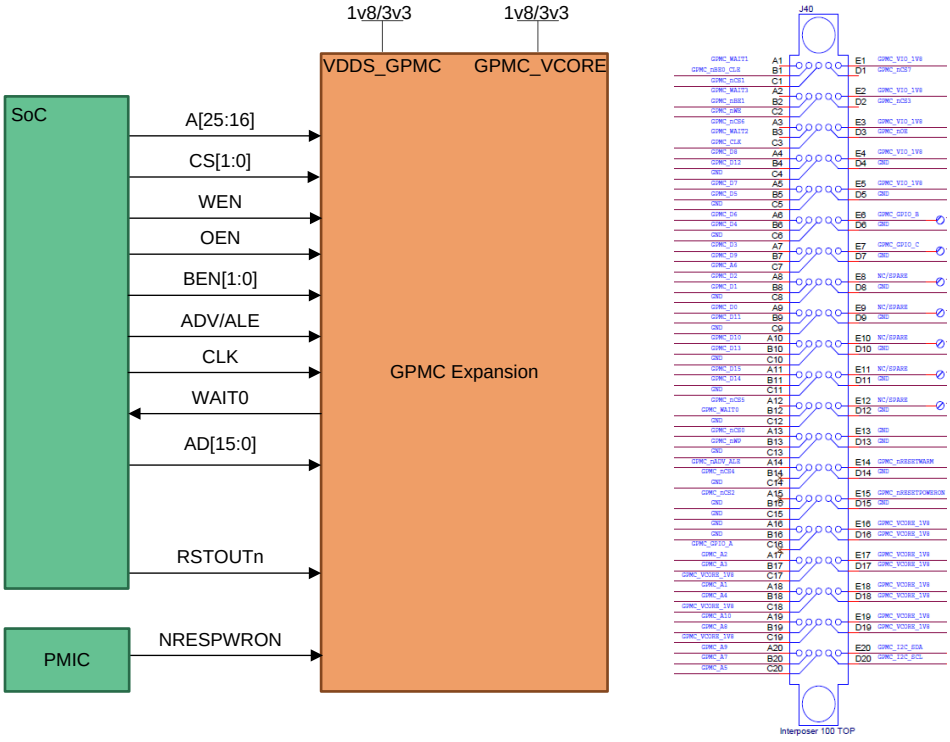


Figure 3-12. GPMC Expansion Interface

3.9.4 I²C EEPROM

An I²C EEPROM device is used (see Figure 3-13). The intended purpose of the 256-KB device is to store the board name and revision tracking information. The EEPROM write protection is controlled with a DIP switch (no software override).

EEPROM device used: Catalyst Semiconductor CAT24C256WI-G

I2C Bus/Address: I2C1, 0x50

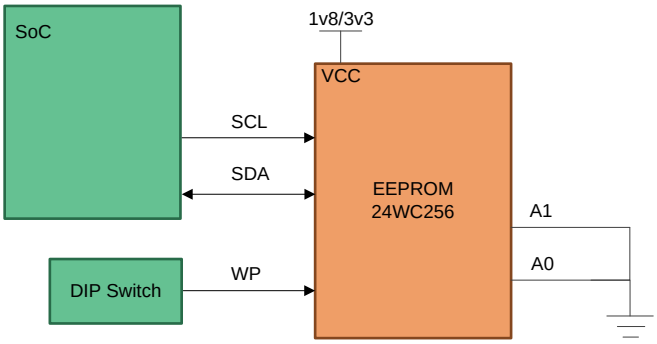


Figure 3-13. EEPROM Memory Configuration

3.10 Digital Temperature Sensor

A digital temperature sensor device is available (see Figure 3-14). The sensor is near the SoC device.

Digital temperature sensor device used: Texas Instruments TMP102AIDRL

I2C Bus/Address: I2C1, 0x48

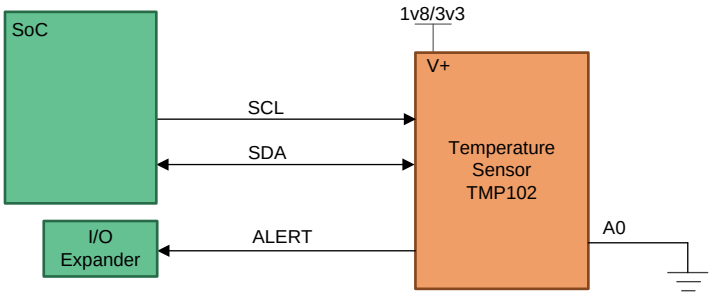


Figure 3-14. Temperature Sensor Configuration

3.11 JTAG and Emulator

The JTAG emulation interface is supported through a standard 60-pin MIPI interface (see Figure 3-15). Reset using the emulator is supported. A DIP switch for EMU0 and EMU1 is supported to enable modes such as wait-in-reset.

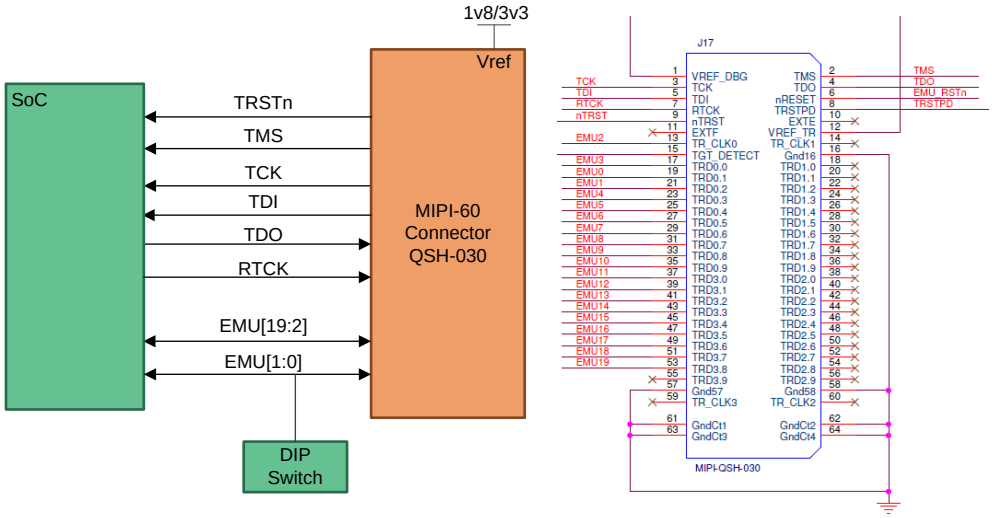


Figure 3-15. JTAG/Trace MIPI-60 Interface

The DIP-2 switch is used to control the emulation boot modes (EMU0 and EMU1), see Table 3-5. For normal operation, these switches should be in the OFF position (logic 1). See the SoC TRM for other supported modes.

Table 3-5. EMU0 and EMU1 Control, DIP-2

Signals	Default State	Description	I2C Expander
EMU1	Off	See the TRM for specific mode support.	None
EMU0	Off	See the TRM for specific mode support.	None

3.12 UART Over USB

The EVM supports three UART connections. An FT4232H device is used to transport the UART information over USB to a host PC. A USB mini-AB receptacle is used to support USB connection. The EVM is designed to use UART3 as the primary terminal connection and is assigned the third terminal port. UART1 and UART2 are assigned to first and second ports. Port four is reserved for future use (see Figure 3-16).

USART device used: FTD Chip FT4232H

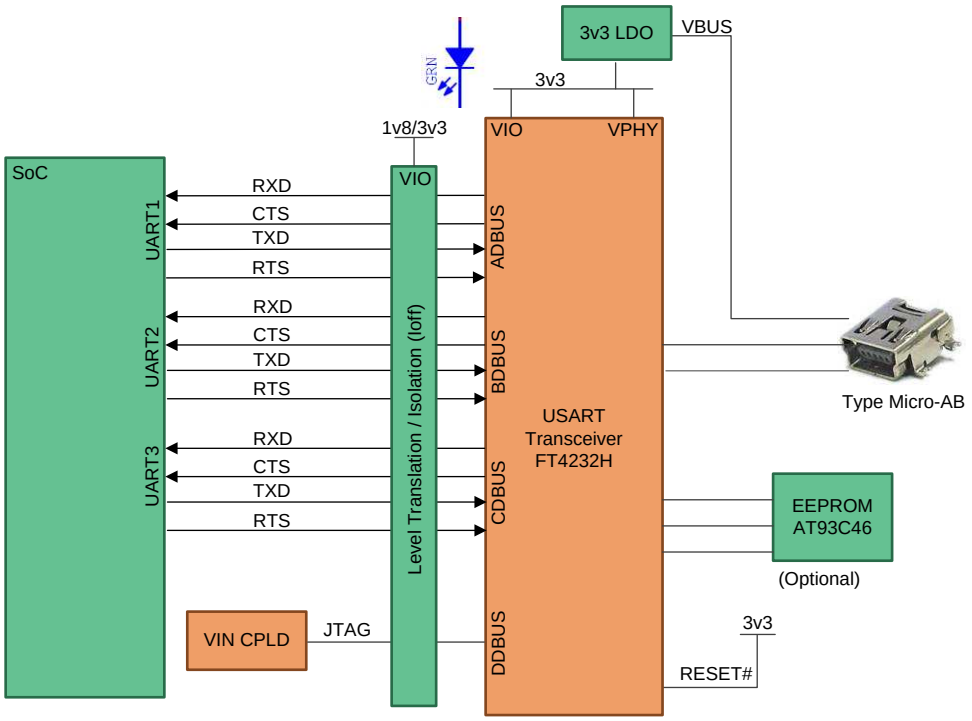


Figure 3-16. UART Over USB Diagram

3.13 CAN and CAN-FD Interfaces

There are two CAN modules within the SoC silicon, with one interface capability of supporting CAN-FD (see Figure 3-17). The TX and RX signals of DCAN1 connect to a header as well as a CAN transceiver supporting a 2-wire CAN bus. MCAN supports CAN-FD, and connects to a 2-pin header and a CAN-FD transceiver.

CAN device used: Texas Instruments TCAN1042

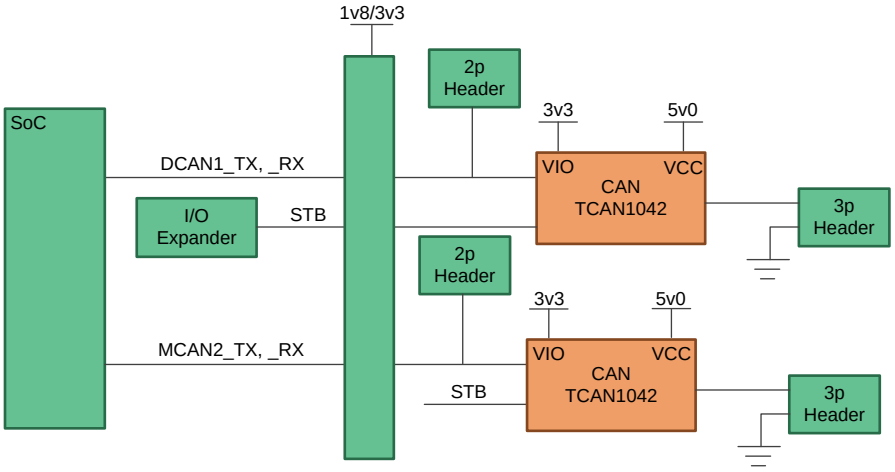


Figure 3-17. DCAN and MCAN Diagram

3.14 Safety MCU Expansion

The EVM provides the mechanism to interface with an external safety MCU (see Figure 3-18). While the interface is generic and can be used with many systems, the TMS570LS04 EVM is specifically targeted because it provides the necessary development support for its dual CAN bus transceivers. Figure 3-18 shows an overview of the connection. It is expected that SPI2 is the primary communication channel between systems. The remaining SPI buses can be configured for GIO.

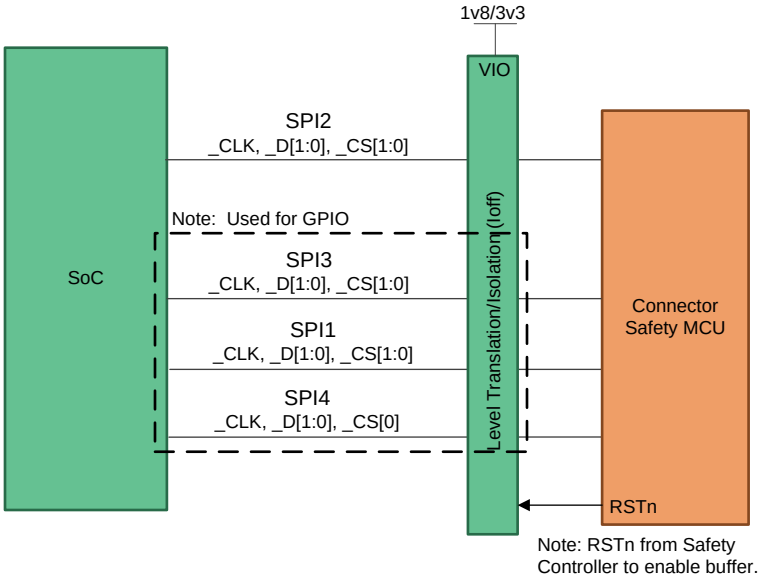


Figure 3-18. Safety MCU Diagram

The SoC/EVM and MCU systems operate from separate power supplies, therefore an isolation buffer is required between the systems. The reset output (RSTn) from the MCU Expansion board can be used to enable the buffer indicating both systems are powered. Figure 3-19 shows the TMS570 EVM interface.

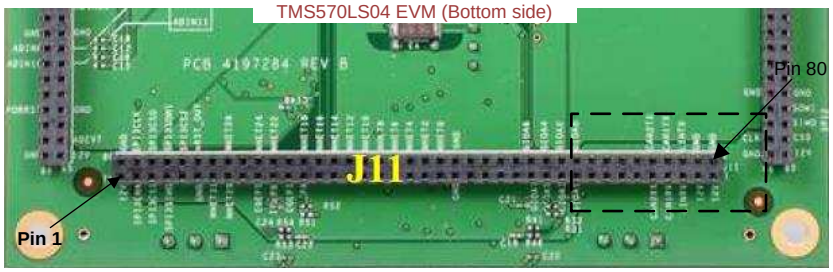


Figure 3-19. Safety MCU EVM Interface

Figure 3-20 shows the SoC signal assignment for the connections that are used.

SoC	TMS570	Pin	SoC	TMS570	Pin
<open>	EQEPA (SPI3_CS0)	57	SPI4_CS0	<open>	58
SPI1_D1	EQEPB (SPI3_ENA)	59	SPI1_CS0	NHET22	60
SPI1_CLK	EQEPS	61	SPI1_CS1	NHET24	62
SPI4_CLK	<open>	63	SPI4_D1	<open>	64
SPI3_D0	GIOA7	65	SPI1_D0	ADEVT_NHET28#	66
SPI3_CLK	GIOA6	67	SPI4_D0	<open>	68
GND	GND	69	(buffer control)	RSTn	70
SPI3_CS0	GIOA0_SPI3CS3	71	SPI3_D1	GIOA1_SPI3CS2	72
SPI2_D1	SPI3_SIMO	73	SPI2_D0	SPI3_SOMI	74
SPI2_CS1	GIOA2_SPI3CS1	75	SPI2_CS0	SPI3_CS0	76
SPI3_CS1	SPI3_ENA	77	SPI2_CLK	SPI3_CLK	78
<open>	12V	79	GND	GND	80

Figure 3-20. MCU Expansion Pin Assignments

3.15 ADC

The SoC device supports eight ADC input channels. ADC channel 0 is connected to the onboard thermistor (100K nominal), as shown in Figure 3-21. ADC channels 2 and 3 are connected to onboard AVS power supplies (CORE and DSP) and have resistor MUX options for connecting to the ADC header. There are footprint population options for connecting coax and ADC headers to the remaining ADC inputs and VREFP to external test equipment.

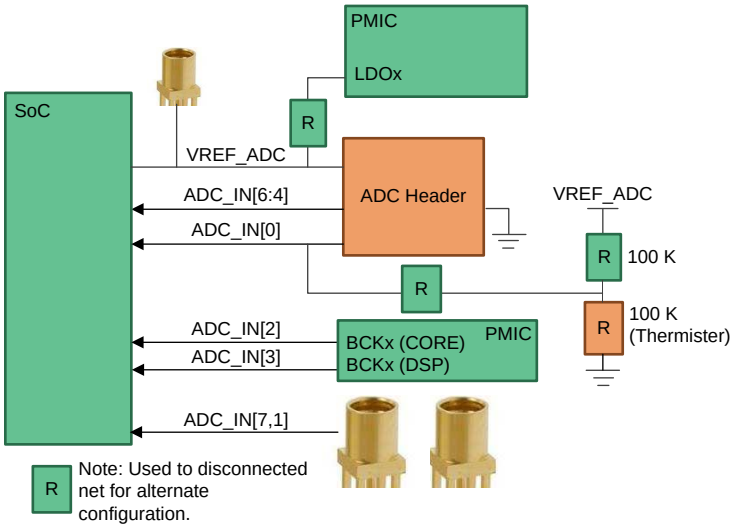


Figure 3-21. ADC Diagram

3.16 Video OUT

The EVM supports four different options for supporting video output. The SoC device does not support multiple video outputs simultaneously, therefore the EVM video out interfaces cannot be used simultaneously.

3.16.1 Display Panel Output/Expansion

The display panel interface supports video from VOUT1 to external LCD display panel (see Figure 3-22). The interface also supports a projected capacitive touchscreen for advanced user interfaces. (A display panel is not included with the EVM, but can be added.)

The VOUT CPLD provides the ability to support additional display modes. Two modes are supported – pass-through and TDM. Pass-through mode assumes a standard 24-bit RGB888 protocol. TDM mode enables the SoC to generate 24-bit RGB data using eight data pins (requires three pixel clocks to transfer each byte of video data). The CPLD concatenates the three separate transfers and generates one 24-bit RGB transfer. This 24-bit output can be output to the Panel/Expansion interfaces. The CPLD assumes the VOUT is configured to output data/syncs on the rising edge, and assumes the attached panel captures data/syncs on the falling edge.

NOTE: The display is not included with EVM.

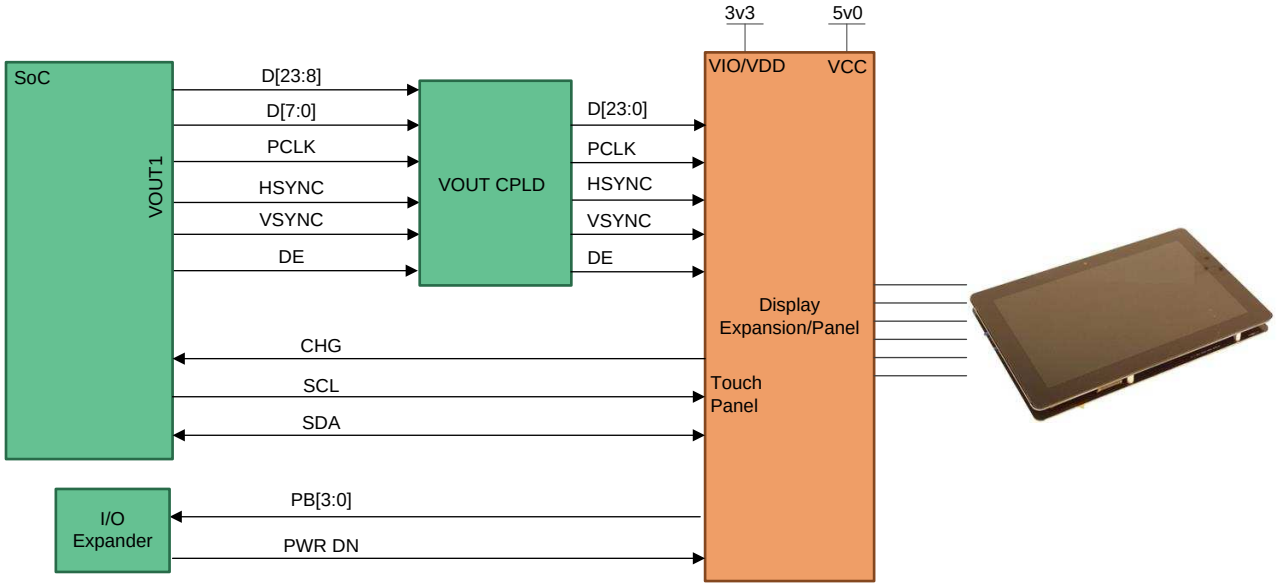


Figure 3-22. Display Panel Output Diagram

Table 3-6 lists the signals used on the display panel output interface.

Table 3-6. Display Panel Connector Pin Assignments

Connector: Molex FFC/FPC 54132-50	
Pin	**Function**
1	Power (5v0)
2	Power (5v0)
3	Power (5v0)
4	Power (3v3)
5	Power (3v3)
6	Power (3v3)
7	Power (1v8)
8	Power (1v8)

Table 3-6. Display Panel Connector Pin Assignments (continued)

Connector: Molex FFC/FPC 54132-50	
Pin	**Function**
9	PB1 / GPIO1
10	PB2 / GPIO2
11	PB3 / GPIO3
12	PB4 / GPIO4
13	GND
14	Power down
15	Touch IRQ
16	I2C SDA
17	I2C SCL
18	GND
19	Pixel data R0
20	Pixel data R1
21	Pixel data R2
22	Pixel data R3
23	Pixel data R4
24	Pixel data R5
25	Pixel data R6
26	Pixel data R7
27	GND
28	Pixel data G0
29	Pixel data G1
30	Pixel data G2
31	Pixel data G3
32	Pixel data G4
33	Pixel data G5
34	Pixel data G6
35	Pixel data G7
36	GND
37	Pixel data B0
38	Pixel data B1
39	Pixel data B2
40	Pixel data B3
41	Pixel data B4
42	Pixel data B5
43	Pixel data B6
44	Pixel data B7
45	GND
46	DE
47	HSYNC
48	VSYNC
49	PCLK
50	GND

3.16.2 Composite Video

The EVM includes composite video through a standard RCA-style connector (see Figure 3-23). The interface can be configured to operate using the internal amplifier (normal or low voltage) or in bypass mode by changing of the RSET and FB resistors. An onboard buffer is provided for test purposes, but is not populated for normal circuit operation.

Optional external filter/buffer device used: Texas Instruments OPA361

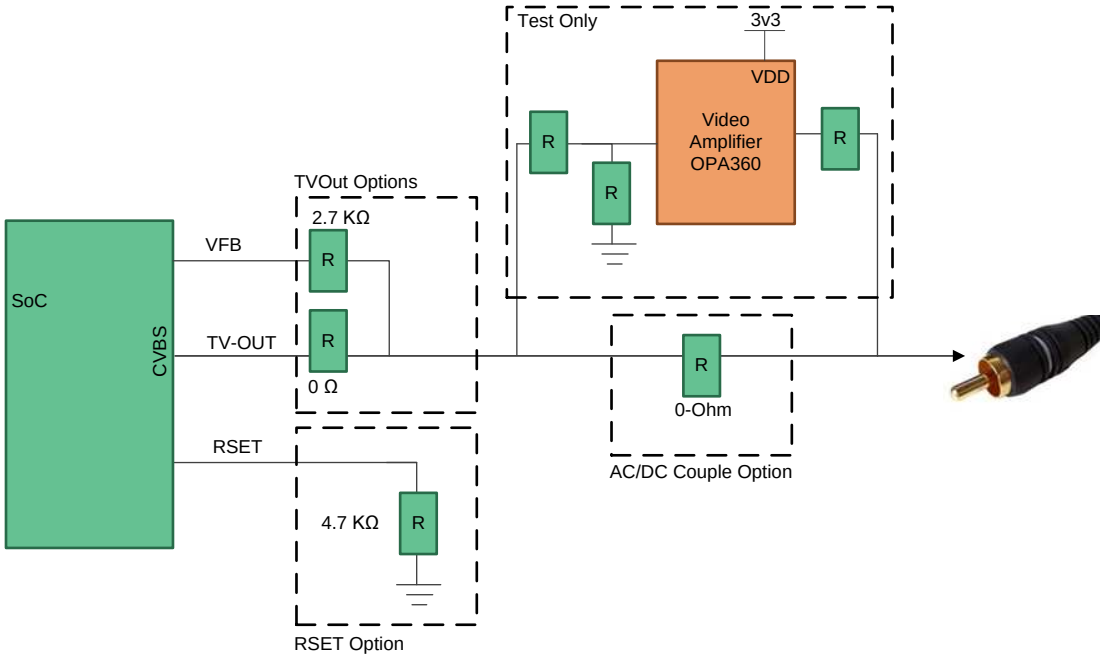


Figure 3-23. Composite Video Output Diagram

3.16.3 FPD-Link III Output

The EVM includes a FPD-Link III parallel to serial interface on VOUT1 (see Figure 3-24). The interface supports up to 24 bits of data and can operate at pixel rates up to 85 MHz. The interrupt is supported to enable back-channel communication, typically needed if supporting a touchscreen.

Serializer device used: Texas Instruments DS90UH925Q

Connector used: Automotive HSD connector, right-angle plug for PCB, Rosenberger D4S20D-40ML5-Z.

The VOUT CPLD provides the ability to support additional display modes. Two modes are supported – pass through and TDM. Pass through assumes a standard 24-bit RGB888 protocol. TDM mode enables the SoC device to generate 24-bit RGB data using eight data pins (requires three pixel clocks to transfer each byte of video data). The CPLD concatenates the three separate transfers and generates one single 24-bit RGB transfer. This 24-bit output can be output to the FPD-Link interfaces. The CPLD assumes the VOUT is configured to output data/syncs on the rising edge, and assumes the attached panel captures data/syncs on the falling edge.

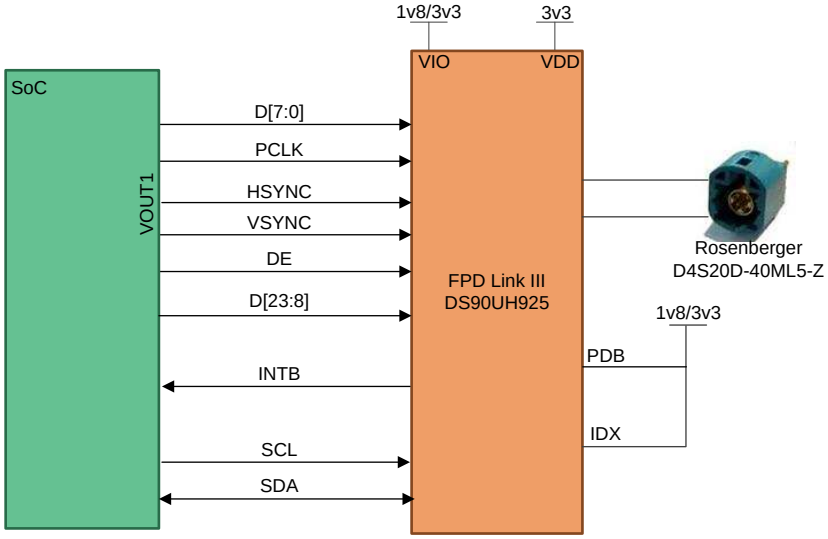


Figure 3-24. Display Panel Output Diagram

3.16.4 HDMI Out

An HDMI external transmitter with an HDMI connector type A is used for the HDMI video output (see Figure 3-25). The transmitter is the *Sil9022A*. The VOUT1 port is the connector to the HDMI, and supports 24b color. Multiple input formats are supported, including RGB24, BT.656, and BT.1120.

Transmitter device used: Silicon Images Sil9022

ESD device used: Texas Instruments TPD12S016-Q1PW

The VOUT CPLD provides the ability to support multiple display modes (RGB24, BT.656, and BT.1120). Two RGB modes are supported – pass through and TDM. Pass through assumes a standard 24-bit RGB888 protocol. TDM mode enables the SoC device to generate 24-bit RGB data using eight data pins (requires three pixel clocks to transfer each byte of video data). The CPLD concatenates the three separate transfers and generates a single 24b RGB transfer. This 24-bit output can be output to the HDMI, FPD-Link, or Panel/Expansion interfaces. The CPLD assumes the VOUT is configured to output data/syncs on rising edge, and assumes the attached panel captures data/syncs on the falling edge.

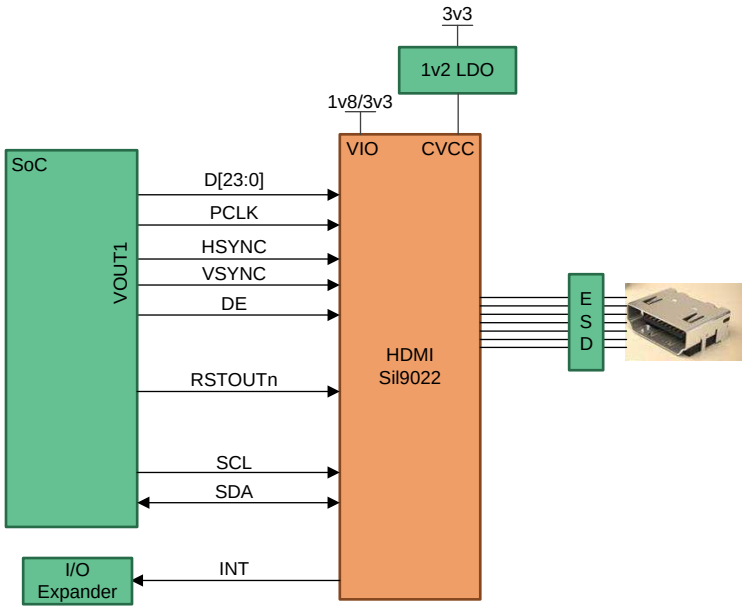


Figure 3-25. HDMI Output Diagram

3.17 Parallel Video In

3.17.1 Leopard Imaging Interface

The EVM includes a connector for interfacing with the camera modules from Leopard Imaging (LI). Figure 3-26 shows the diagram of the implementation. Either VIN1A or VIN2A can be used, depending on the board settings. An optional reference clock is provided, but not supported by default.

LI Camera Connector device used: MOLEX-FPC 36POS, 0.5 mm, Part#: 052559-3679

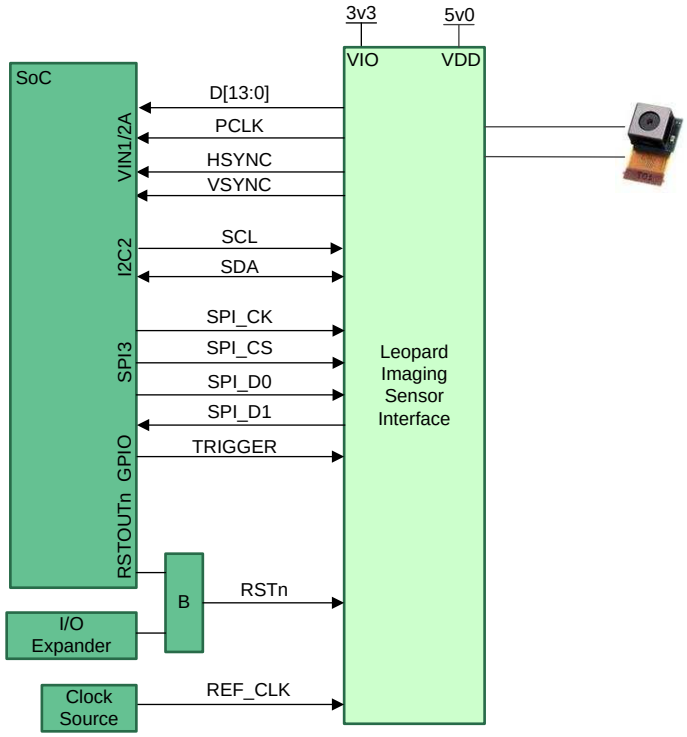


Figure 3-26. Leopard Imaging Diagram

The connector is placed on the board so that the camera image is directed to the side of the PCB for better viewing options. Table 3-7 lists the pinout of the connector. The VIP data assignments of the SoC are not fixed, because the CPLD does provide options for bit shifting.

Table 3-7. Leopard Imaging Pin Assignments

Connector: FPC 36 Pos, 05 mm, Molex 052559-3679		
Pin	**SoC**	**Function**
1	+3.3 V	Power (3v3)
2	+3.3 V	Power (3v3)
3	+3.3 V	Power (3v3)
4	+5.0 V	Power (5v0)
5	+5.0 V	Power (5v0)
6	GND	GND
7	(optional)	External Cam Clk
8	GND	GND
9	VIP_CLK	Cam Pixel Clk
10	GND	GND
11	VIP_VSYNC	Verticle Sync Pulse
12	VIP_HSYNC	Horizontal Sync
13	VIP_D[13]	Cam Data Bit 13
14	VIP_D[12]	Cam Data Bit 12
15	VIP_D[11]	Cam Data Bit 11
16	VIP_D[10]	Cam Data Bit 10
17	VIP_D[9]	Cam Data Bit 9
18	VIP_D[8]	Cam Data Bit 8
19	VIP_D[7]	Cam Data Bit 7
20	VIP_D[6]	Cam Data Bit 6
21	VIP_D[5]	Cam Data Bit 5
22	VIP_D[4]	Cam Data Bit 4
23	VIP_D[3]	Cam Data Bit 3
24	VIP_D[2]	Cam Data Bit 2
25	GND	GND
26	GND	GND
27	VIP_D[1]	Cam Data Bit 1
28	VIP_D[0]	Cam Data Bit 0
29	I2C2_SCL	I2C Serial Clk
30	I2C2_SDA	I2C Serial Data
31	SPI3_D[0]	SPI Bus Master O
32	SPI3_CLK	SPI Bus Clk
33	RSTOUTn	Reset Input
34	SPI3_CS0	SPI Bus Chip Sel
35	*x*	Cam Trigger
36	SPI3_D[1]	SPI Bus Master I

3.17.2 Aptina Interface

The EVM includes a connector for interfacing with the camera modules from Aptina. Figure 3-27 shows the diagram of the implementation. Either VIN1A or VIN2A can be used, depending on the board settings. A 24-MHz reference clock is provided to the module.

Aptina Camera Connector device used: Samtec, Part#: SSQ-116-02-L-D

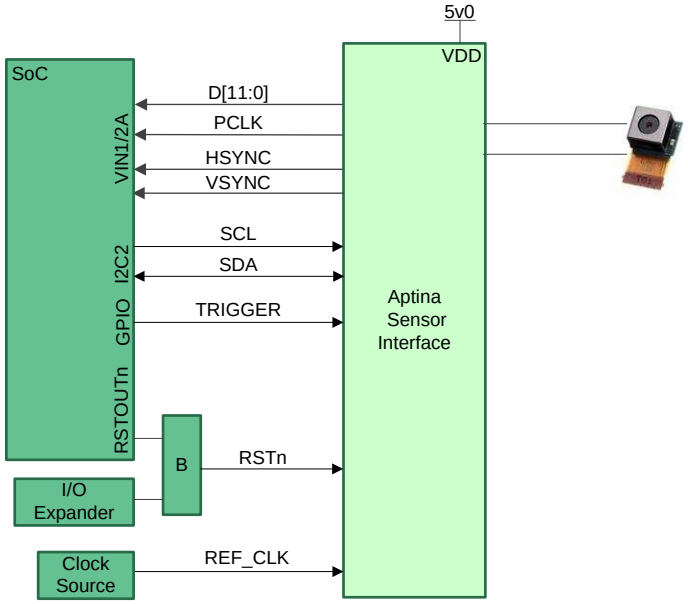


Figure 3-27. Aptina Camera Diagram

The connector is placed on the board so that the camera image is directed to the side of the PCB for better viewing options. Table 3-8 lists the pinout of the connector. The VIP data assignments of the SoC are not fixed, because the CPLD does provide options for bit shifting.

Table 3-8. Aptina Pin Assignments

Connector: Receptacle 32 Pos, 2.54 mm, Samtec SSQ-116-02-L-D		
Pin	**SoC**	**Function**
1	VIP_D[1]	Cam Data Bit 1
2	VIP_D[0]	Cam Data Bit 0
3	VIP_D[4]	Cam Data Bit 4
4	VIP_D[5]	Cam Data Bit 5
5	VIP_D[6]	Cam Data Bit 6
6	VIP_D[7]	Cam Data Bit 7
7	VIP_D[8]	Cam Data Bit 8
8	VIP_D[9]	Cam Data Bit 9
9	VIP_D[10]	Cam Data Bit 10
10	VIP_D[11]	Cam Data Bit 11
11	VIP_D[2]	Cam Data Bit 2
12	VIP_D[3]	Cam Data Bit 3
13	GND	GND
14	GND	GND
15	VIP_HSYNC	Cam Horiz Sync
16		<open>
17		<open>
18	RSTOUTn	Reset Input
19	VIP_VSYNC	Cam Verticle Sync
20	I2C2_SDA	I2C Serial Data
21	I2C2_SCL	I2C Serial Clk
22		<open>
23	+5.0 V	Power (5v0)
24	+5.0 V	Power (5v0)
25	VIP_CLK	Cam Pixel Clk
26	GND	GND
27	GND	GND
28	24 Mhz Clk	External Cam Clk
29	GND	GND
30	GND	GND
31	*x*	Cam Trigger
32	GND	GND

3.17.3 OmniVision Interface

The EVM includes a connector for interfacing with the camera modules from OmniVision. Figure 3-28 shows the diagram of the implementation. Either VIN1A or VIN2A can be used, depending on the board settings. A 24-MHz reference clock is provided to module.

OmniVision Camera Connector device used: Samtec, Part#: SSQ-116-02-L-D-RA

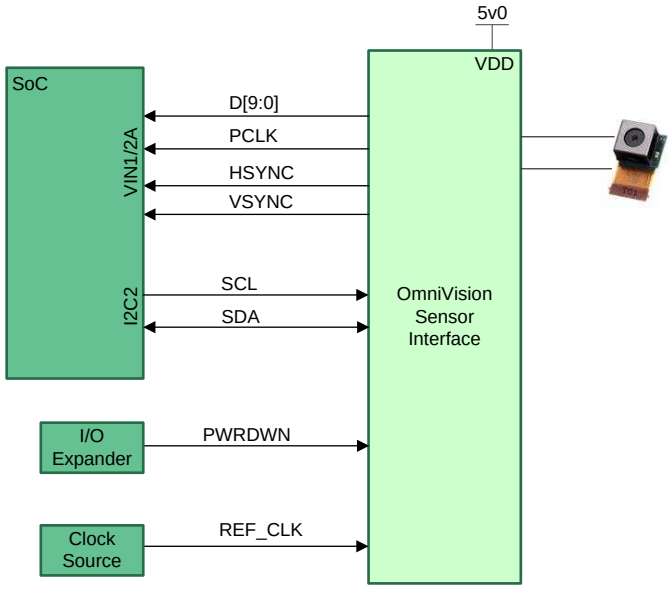


Figure 3-28. OmniVision Diagram

The connector is placed on the board so that the camera image is directed to the side of the PCB for better viewing options. Table 3-9 shows the pinout of the connector. The VIP data assignments of the SoC are not fixed, because the CPLD does provide options for bit shifting.

Table 3-9. OmniVision Camera Pin Assignments

Connector: Receptacle 32 Pos, 2.54-mm, Samtec SSQ-116-02-L-D-RA		
Pin	**SoC**	**Function**
1	VIP_D[3]	Cam data bit 3
2	VIP_D[2]	Cam data bit 2
3	VIP_D[5]	Cam data bit 5
4	VIP_D[4]	Cam data bit 4
5	VIP_D[7]	Cam data bit 7
6	VIP_D[6]	Cam data bit 6
7	VIP_D[9]	Cam data bit 9
8	VIP_D[8]	Cam data bit 8
9		<open>
10	I/O_EXP	Power down
11		<open>
12	I2C2_SDA	I2C Serial data
13	VIP_HSYnC	Cam horizontal sync
14	I2C2_SCL	I2C serial clock
15	VIP_VSYNC	Cam vertical sync
16	GND	GND
17	VIP_CLK	Cam pixel clock
18	GND	GND
19	+5.0 V	Power (5v0)
20	24 MHz clk	External cam clock
21	+5.0 V	Power (5v0)
22	GND	GND
23	VIP_D[1]	Cam data bit 1
24	CAM_D[0]	Cam data bit 0
25		<open>
26		<open>
27		<open>
28		<open>
29		<open>
30		<open>
31	GND	GND
32	GND	GND

3.17.4 HDMI

The EVM supports receiving video input from an external HDMI transmitter using the Analog Devices ADV7611 receiver (see Figure 3-29). Because the EVM does not provide any audio support, the audio input from the receiver is not used. An EEPROM is included to support EDID information.

HDMI Receiver device used: Analog Devices ADV7611BSWZ-P

HDMI Connector used: Type A

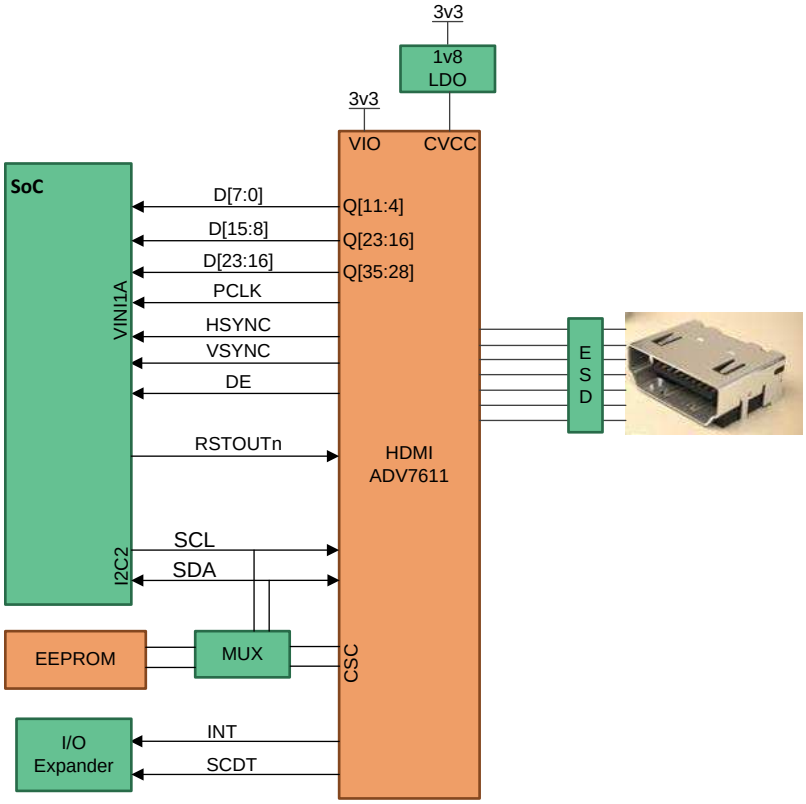


Figure 3-29. HDMI Receiver Diagram

3.17.5 FPD-Link III

The EVM supports receiving video input from an FPD-Link II deserializer (see Figure 3-30). The deserializer supports up to 24 bits at 85 MHz. Because the EVM does not provide any audio support, the audio input from the deserializer is not used.

FPD-Link Receiver device used: Texas Instruments DS90UH926

HDMI Connector used: Rosenberger D4S20D-40ML5-Z

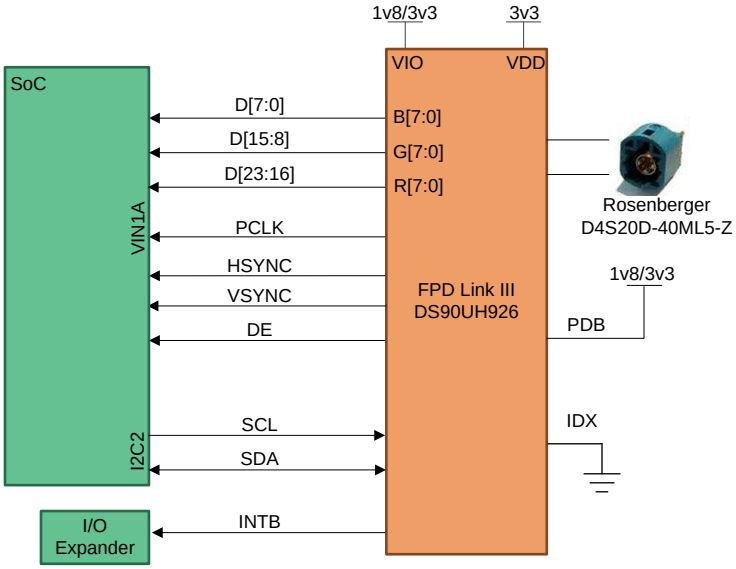


Figure 3-30. FPD-Link III Receiver Diagram

3.17.6 Parallel Camera Expansion

The EVM supports additional video input configurations using the parallel expansion interface. The interface is designed to support the existing FPD-Link III multideserializer board, which provides up to six camera inputs. The SoC and EVM supports only four camera inputs (ports 1 to 4). The connection definition is extended to support higher resolution inputs (reassign pins for cameras 5 and 6). The connector definition is provided as follows.

Connector used: Samtec ASP-127796-01

NOTE: This interface is aligned with the FMC VITA 57 specification (low pin-count version).

When using the expansion interface with the FPD-Link III multideserializer, the deserializer requires 4-channel mode configuration. See the jumper settings in Figure 3-31.

Configuration:

a. The board will be configured to the "4 Channels, 12b data" position – configuration is done via the CN2, CN3 and CN4 headers which should be configured as shown below:

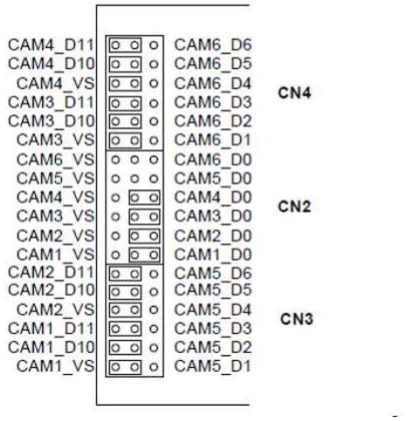


Figure 3-31. Header Configuration for Four Cameras (12 Bits per Camera)

Figure 3-32 shows the parallel camera expansion pin assignments.

Legend			
Camera 1 (24b)		(maps to VIN1A)	
Camera 2 (12b)		(maps to VIN1B)	
Camera 3 (16b)		(maps to VIN2A)	
Camera 4 (12b)		(maps to VIN2B)	

	C		D		G		H	
	Multi-Deserializer	SoC	Multi-Deserializer	SoC	Multi-Deserializer	SoC	Multi-Deserializer	SoC
1	GND	GND	open	GPIO/TIMER4	GND		open	open
2	open	CAM1_D20	GND	GND	CAM5_D1_CAM1_V	CAM1_VS	GND	GND
3	open	CAM1_D21	GND	GND	CAM5_D2_CAM1_D	CAM1_D10	GND	GND
4	GND	GND	open	CAM1_D16	GND	GND	CAM2_D5	
5	GND	GND	open	CAM1_D19	GND	GND	CAM2_D4	
6	open	CAM1_D22	GND	GND	CAM2_PCLK		GND	GND
7	open	CAM1_D23	GND	GND	CAM1_PCLK		CAM2_D9	
8	GND	GND	CAM2_D3		GND	GND	CAM2_D8	
9	GND	GND	CAM2_D2		CAM1_D5		GND	GND
8	CAM3_D3		GND	GND	CAM1_D4		CAM1_D3	
11	CAM3_D2		CAM2_D1		GND	GND	CAM1_D2	
8	GND	GND	CAM2_HS		CAM5_D3_CAM1_D	CAM1_D11	GND	GND
8	GND	GND	GND	GND	CAM5_D6_CAM2_	CAM2_VS	CAM1_D0_CAM1_V	CAM1_D0
8	CAM2_D7		CAM6_D1_CAM3_V	CAM3_VS	GND	GND	CAM2_D0_CAM2_	CAM2_D0
8	CAM2_D6		CAM6_D2_CAM3_	CAM3_D10	CAM1_D1		GND	GND
8	GND	GND	GND	GND	CAM1_HS		CAM6_HS	CAM1_D15
8	GND	GND	CAM1_D3		GND	GND	CAM6_D6_CAM4_	CAM4_D11
8	CAM6_D3_CAM3_	CAM3_D11	CAM1_D8		CAM5_D5_CAM2_D	CAM2_D10	GND	GND
8	CAM6_D4_CAM4_	CAM4_VS	GND	GND	CAM5_D6_CAM2_	CAM2_D11	CAM1_D7	
8	GND	GND	CAM4_PCLK		GND	GND	CAM1_D6	
8	GND	GND	CAM3_PCLK		CAM3_D5		GND	GND
8	CAM6_PCLK	CAM1_D14	GND	GND	CAM3_D4		CAM3_D0_CAM3_	CAM3_D0
8	CAM5_PCLK	CAM1_D13	CAM3_D9		GND	GND	CAM4_D0_CAM4_	CAM4_D0
8	GND	GND	CAM3_D8		CAM3_D7		GND	GND
8	GND	GND	GND	GND	CAM3_D6		CAM5_D0_CAM5_V	CAM1_DE
8	CAM5_HS	CAM1_D17	CAM4_D9		GND	GND	CAM6_D0_CAM6_	CAM3_DE
8	CAM6_D6_CAM4_	CAM4_D10	CAM4_D8		CAM4_D5		GND	GND
8	GND	GND	GND	GND	CAM4_D4		CAM6_D7	CAM1_D12
8	GND	GND	open	GPIO/TIMER1	GND	GND	CAM6_D8	CAM1_D18
8	CAM_SCL	CAM_SCL	BRD_ID1	BRD_ID1	CAM3_D1		GND	GND
8	CAM_SDA	CAM_SDA	BRD_ID2	BRD_ID2	CAM3_HS		CAM4_D7	
8	GND	GND	3v3	3v3	GND	GND	CAM4_D6	
8	GND	GND	open	GPIO/TIMER2	CAM5_D7	CAM3_D12	GND	GND
8	I2C_ADDR_SEL0	I2C_ADDR_SEL0	open	GPIO/TIMER3	CAM5_D8	CAM3_D13	CAM4_D3	
8	12V	12V	I2C_ADDR_SEL1	I2C_ADDR_SEL1	GND	GND	CAM4_D2	
8	GND	GND	3v3	3v3	CAM5_D9	CAM3_D14	GND	GND
8	12V	12V	GND	GND	CAM6_D9	CAM3_D15	CAM4_D1	
8	GND	GND	3v3	3v3	GND	GND	CAM4_HS	
8	open	open	GND	GND	open	open	GND	GND
8	GND	GND	3v3	3v3	GND	GND	open	open

Changes to extend interface for higher resolution sensors and timer inputs.

Figure 3-32. Parallel Camera Expansion Pin Assignments

3.18 Serial Video In

The CSI2 signals are connected directly between the SoC device and the sensor connectors (see Figure 3-33). They are not included as part of the visibility signals (due to performance). Two sensor interfaces are supported: Leopard Imaging and Generic/Expansion.

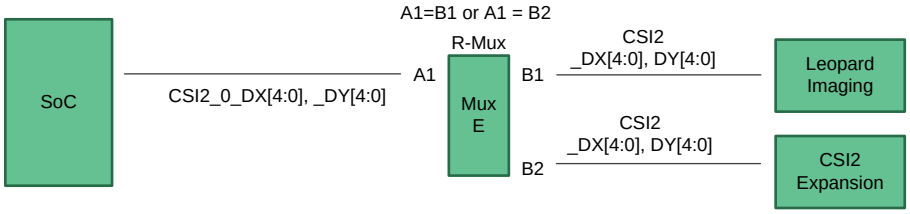


Figure 3-33. Leopard Imaging and Generic/Expansion

Figure 3-34 shows the Leopard Imaging interface.

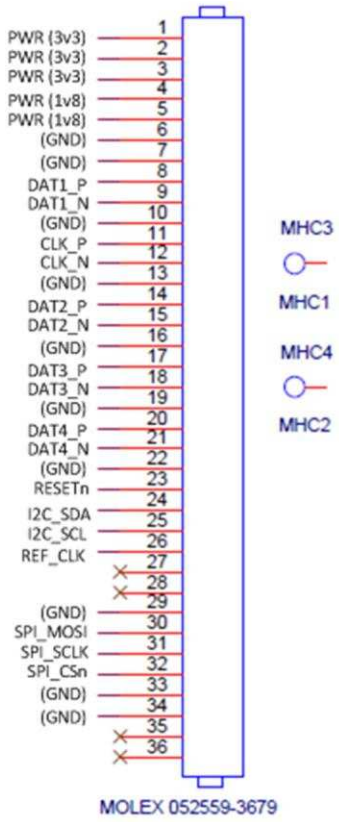


Figure 3-34. Leopard Imaging CSI2 Module Interface

Table 3-10 lists the Leopard imaging connector interface definitions.

Table 3-10. Leopard Imaging Connector Interface Definition

Connector: Molex 052559-3679		
Pin	**SoC**	**Function**
1	+3.3 V	Power (3v3)
2	+3.3 V	Power (3v3)
3	+3.3 V	Power (3v3)
4	+1.8 V	Power - I/O (1v8)
5	+1.8 V	Power - I/O (1v8)
6	GND	GND
7	GND	GND
8	CSI2_0_DX0	DAT1_P
9	CSI2_0_DY0	DAT1_N
10	GND	GND
11	CSI2_0_DX1	CLK_P
12	CSI2_0_DY1	CLK_N
13	GND	GND
14	CSI2_0_DX2	DAT2_P
15	CSI2_0_DY2	DAT2_N
16	GND	GND
17	CSI2_0_DX3	DAT3_P
18	CSI2_0_DY3	DAT3_N
19	GND	GND
20	CSI2_0_DX4	DAT4_P
21	CSI2_0_DY4	DAT4_N
22	GND	GND
23	RSTOUTn	RESETn
24	I2C2_SDA	I2C_SDA
25	I2C2_SCL	I2C_SCL
26	<open>	REF_CLK (opt)
27	<open>	<open>
28	<open>	<open>
29	GND	GND
30	SPI1_D0	SPI_MOSI
31	SPI1_SCLK	SPI_SCK
32	SPI1_CS1	SPI_CS
33	GND	GND
34	GND	GND
35	<open>	<open>
36	<open>	<open>

CSI2 expansion is designed to support third-party add-on modules, like the FPD-Link-to-CSI2 transceiver. The CSI2 expansion has an improved high-speed connector when compared with the LI interface. Table 3-11 lists the CSI2 generic expansion module interface.

Table 3-11. CSI2 Generic Expansion Module Interface

Connector: Samtec QSH-020-01-L-D-DP-A		
Pin	**SoC**	**Function**
1		<open>
2	I2C2_SCL	I2C_SCL
3		<open>
4	I2C2_SDA	I2C_SDA
5	CSI2_0_DX0	DAT0_P
6		<open>
7	CSI2_0_DY0	DAT0_N
8		<open>
9	CSI2_0_DX1	DAT1_P
10	<open>	REF_CLK (opt)
11	CSI2_0_DY1	DAT1_N
12	GND	GND
13	CSI2_0_DX2	DAT2_P
14	RSTOUTn	RESETn
15	CSI2_0_DY2	DAT3_N
16	GND	GND
17	CSI2_0_DX3	DAT3_P
18	SPI1_D0	SPI_MOSI
19	CSI2_0_DY3	DAT3_N
20	SPI1_SCLK	SPI_SCLK
21	CSI2_0_DX4	DAT4_P
22	SPI1_CS1	SPI_CS
23	CSI2_0_DY4	DAT4_N
24	GND	GND
25		<open>
26		<open>
27		<open>
28		<open>
29		<open>
30	+3.3 V	Power (3v3)
31		<open>
32	+3.3 V	Power (3v3)
33		<open>
34	+3.3 V	Power (3v3)
35		<open>
36	+3.3 V	Power (3v3)
37		<open>
38	+1.8 V	Power - IO (1v8)
39		<open>
40	+1.8 V	Power - IO (1v8)

3.19 Ethernet

A Gigabit Ethernet Transceiver is supported on EMAC0 (see Figure 3-35). The RJ45 jack provides seamless connection to an Ethernet network. The physical address for the MD management interface is assigned to 00000b for EMAC0.

Transceiver devices used: Qualcom AR8031

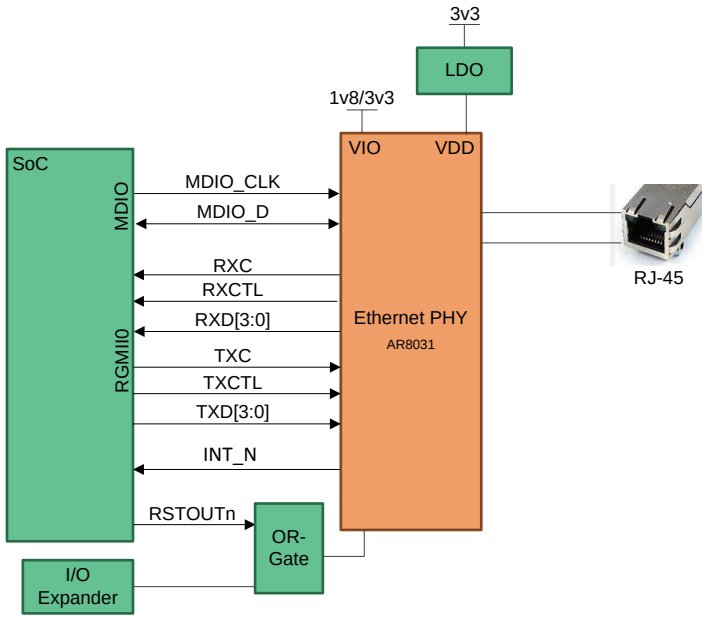


Figure 3-35. Gigabit Ethernet Transceiver

A second Ethernet transceiver can be added through the Ethernet expansion interface (see Figure 3-36). The EMAC0 interface is connected to Port A. The EMAC1 interface is connected to Port B.

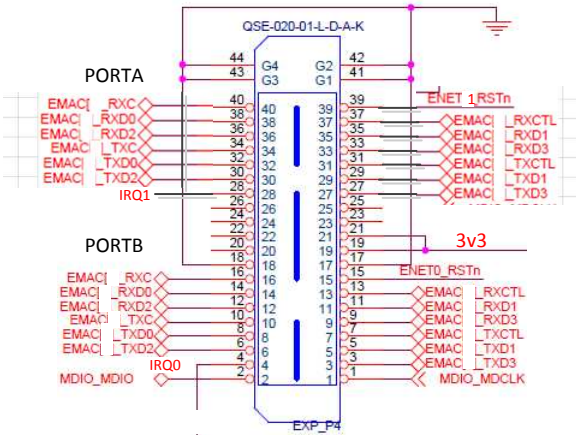


Figure 3-36. Ethernet Expansion Interface

3.20 SD Card Socket

A MicroSD socket is used for the MMC1 interface with 4-bit data width. This connector supports ESD protection.

ESD device used:

- Texas Instruments x3 TPD2E001-Q1
- Texas Instruments x2 TPD1E10B09-Q1
- 8 33-Ω resistors

3.21 I²C Expander

Due to the lack of available GPIOs, the EVM uses three I²C-based I/O expanders (see Figure 3-37). The third I/O expander (address 0x23) is used to control the onboard and CPLD mux configurations. All expanders are controlled using I2C1.

NOTE: All pins power up as inputs.

GPIO Expander devices used: TI TCA6424ARGJR (2x)

GPIO Expander device used: TI TCA6416ARGJR (1x)

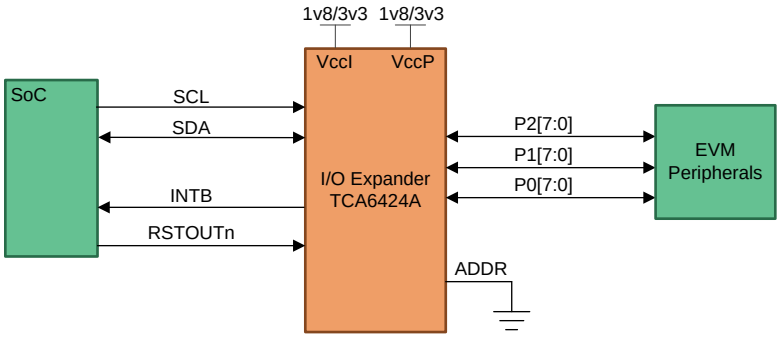


Figure 3-37. I²C-Based I/O Expander Diagram

Table 3-12 provides signals that will be controlled through the I²C I/O expanders.

Bus: I2C1, address: 0x20

Table 3-12. I²C GPIO Expander 1

Port	Bit	Signals	Comments
TCA6416 Port 0	Bit 7	FPD_LINK_DB_DET	Detects if FPD-Link board is assembled.
	Bit 6	DCAN1_STB	Controls DCAN1 transceiver STB signal
	Bit 5	HDMI_CT_HPD	HDMI HPD detect signal
	Bit 4	HDMI_LS_OE	HDMI translator enable
	Bit 3	HDMI_CEC_D	Controls HDMI CEC signal manually
	Bit 2	LI_DUAL_TRIGGER	Leopard imaging GPIO
	Bit 1	APT_TRIGGER	Aptina sensor GPIO
	Bit 0	SEL_HDMI_INn	Controls selection of access to HDMI EEPROM

Table 3-12. I²C GPIO Expander 1 (continued)

Port	Bit	Signals	Comments
TCA6424 Port 1	Bit 7	TS_LCD_GPIO1	GPIO-to-LCD connector
	Bit 6	TS_LCD_GPIO2	GPIO-to-LCD connector
	Bit 5	TS_LCD_GPIO3	GPIO-to-LCD connector
	Bit 4	TS_LCD_GPIO4	GPIO-to-LCD connector
	Bit 3	CON_LCD_PWR_DN	Power down GPIO-to-LCD connector
	Bit 2	<open>	
	Bit 1	HDMI_INT	Interrupt from HDMI receiver
	Bit 0	PCF_VPP_ENn	Enable VPP power supply

Table 3-13 provides signals that will be controlled through the I²C I/O expanders.

Bus: I2C1, address: 0x22

Table 3-13. I²C GPIO Expander 2

Port	Bit	Signals	Comments
TCA6416 Port 0	Bit 0	USR_LED1	Control of user-defined LED (DS1)
	Bit 1	USR_LED2	Control of user-defined LED (DS2)
	Bit 2	USR_LED3	Control of user-defined LED (DS3)
	Bit 3	USR_LED4	Control of user-defined LED (DS4)
	Bit 4	VIP_RSTn	Control of reset signal to VIN CPLD
	Bit 5	VOUT_RSTn	Control of reset signal to VOUT CPLD
	Bit 6	<open>	
	Bit 7	<open>	
TCA6424 Port 1	Bit 0	<open>	
	Bit 1	TMP_ALERT	Onboard temperature sensor alert input
	Bit 2	ENET0_RSTn	Control of onboard GMAC0 PHY reset
	Bit 3	ENET1_EXP_RSTn	Control of expansion board GMAC1 PHY reset
	Bit 4	ENET0_EXP_RSTn	Control of expansion board GMAC0 PHY reset
	Bit 5	SD_CARD_DETn	SD card detect input
	Bit 6	<open>	
	Bit 7	<open>	
TCA6424 Port 2	Bit 0	USR_SW1	User defined input from DIP switch (SW8001)
	Bit 1	USR_SW2	User defined input from DIP switch (SW8001)
	Bit 2	USR_SW3	User defined input from DIP switch (SW8001)
	Bit 3	USR_SW4	User defined input from DIP switch (SW8001)
	Bit 4	USR_SW5	User defined input from DIP switch (SW8001)
	Bit 5	<open>	
	Bit 6	POWERHOLD_CLK	Power off (disabled by default)
	Bit 7	MUX_CNTL13	Onboard M u control bit 13 (see MUX Ctrl Settings)

Table 3-14 provides signals that will be controlled through the I²C I/O expanders.

Bus: I2C1, address: 0x23

Table 3-14. I²C GPIO Expander 3

Port	Bit	Signals	Comments
TCA6416 Port 0	Bit 0	MUX_CNTL0	Onboard MUX Control Bit 0, SEL_GPMCn
	Bit 1	MUX_CNTL1	Onboard MUX control bit 1 (see MUX Ctrl Settings)
	Bit 2	MUX_CNTL2	Onboard MUX control bit 2 (see MUX Ctrl Settings)
	Bit 3	MUX_CNTL3	Onboard MUX control bit 3 (see MUX Ctrl Settings)
	Bit 4	MUX_CNTL4	Onboard MUX control bit 4 (see MUX Ctrl Settings)
	Bit 5	MUX_CNTL5	Onboard MUX control bit 5 (see MUX Ctrl Settings)
	Bit 6	MUX_CNTL6	Onboard MUX control bit 6 (see MUX Ctrl Settings)
	Bit 7	MUX_CNTL7	Onboard MUX control bit 7 (see MUX Ctrl Settings)
TCA6424 Port 1	Bit 0	MUX_CNTL8	Onboard MUX control bit 8 (see MUX Ctrl Settings)
	Bit 1	MUX_CNTL9	Onboard MUX control bit 9 (see MUX Ctrl Settings)
	Bit 2	MUX_CNTL10	Onboard MUX control bit 10 (see MUX Ctrl Settings)
	Bit 3	MUX_CNTL11	Onboard MUX control bit 11 (see MUX Ctrl Settings)
	Bit 4	MUX_CNTL12	Onboard MUX control bit 12 (see MUX Ctrl Settings)
	Bit 5	VOUT_MAP0	VOUT MUX control bit 0 (see VOUT table in MUXCntl)
	Bit 6	VOUT_MAP1	VOUT MUX control bit 1 (see VOUT table in MUX Cntl)
	Bit 7	VOUT_MAP2	VOUT MUX control bit 2 (see VOUT table in MUX Cntl)
TCA6424 Port 2	Bit 0	VIN_MAP0	VIN MUX control bit 0 (see VIN table in MUX Cntl)
	Bit 1	VIN_MAP1	VIN MUX control bit 1 (see VIN table in MUX Cntl)
	Bit 2	VIN_MAP2	VIN MUX control bit 2 (see VIN table in MUX Cntl)
	Bit 3	VIN_MAP3	VIN MUX control bit 3 (see VIN table in MUX Cntl)
	Bit 4	VIN_MAP4	VIN MUX control bit 4 (see VIN table in MUX Cntl)
	Bit 5	VIN_MAP5	VIN MUX control bit 5 (see VIN table in MUX Cntl)
	Bit 6	VIN_MAP6	VIN MUX control bit 6 (see VIN table in MUX Cntl)
	Bit 7	VIN_MAP7	VIN MUX control bit 7 (see VIN table in MUX Cntl)

3.22 I²C Peripheral Mapping

Table 3-15 and Table 3-16 summarize the I²C mapping on the EVM board.

Table 3-15. I2C1 Peripheral Mapping

Peripheral Device	I2C1
ID EEPROM	0x51
Temperature Sensor	0x48
LP8733 (Power)	0x60
LP8732 (Power)	0x61
TCA6416A (GPIO Expander 1)	0x20
TCA6424A (GPIO Expander 2)	0x22
TCA6424A (GPIO Expander 3)	0x23
FPD-Link Serializer	0x1B
HDMI Transmitter (TPI)	0x3B
HDMI Transmitter (CPI)	0x62
HDMI Transmitter (9020 compatible)	0x3F

Table 3-16. I2C2 Peripheral Mapping

Peripheral Device	I2C2
FPD-Link	0x2C
HDMI Receiver (Control 1)	0x31
HDMI Receiver (Color)	0x32
HDMI Receiver (Control 2)	0x35
HDMI Receiver (Test1)	0x48
HDMI Receiver (CES Bus)	0x60
HDMI Receiver (Test2)	0x68
HDMI Receiver (E-DDC)	0x70
HDMI Receiver (Test3)	0x73
HDMI Receiver (EEPROM)	0x50
HDMI Receiver (Base)	0x4C

3.23 Power Monitoring

The EVM is previsioned for power monitoring using the INA226 device. The board can monitor power consumption on the power supplies in Figure 3-38. The measurement system consists of the TI INA226 I^2C current shunt/power monitors. The INA226 device provides both power supply voltage and shunt current measurements as well as calculated power through an I^2C bus. This allows the device to be placed close to the shunt.

Figure 3-38 shows a block diagram of the current monitoring system. The INA226 devices are located at the appropriate shunts for various supplies. These INA226 devices are controlled by an onboard I^2C controller through a USB connection with the host PC. The power rails and I^2C groups are identified in Table 3-17 and Table 3-18.

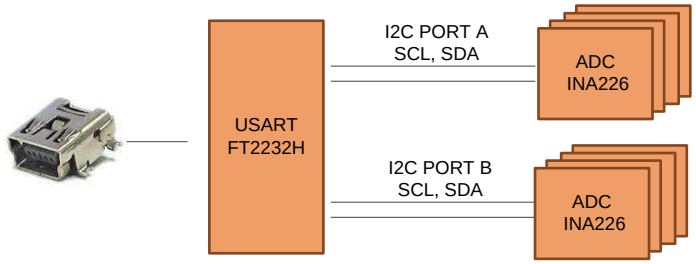


Figure 3-38. Power Monitor Diagram

Table 3-17 lists the power supply pin groups that are monitored in port A.

Table 3-17. Power Monitor Mapping I^2C Port A

I^2C Address	Power Rail
0x40	VPIN_S1_3V3
0x41	VPIN_S2_3V3
0x42	VPIN_S3_3V3
0x43	VPIN_S4_3V3
0x44	VDD_DSPEVE_AVS
0x45	VDD_CORE_AVS
0x46	
0x47	VDDS_DDR_DV
0x48	VDDR_DV
0x49	VSYS_3V3
0x4A	VSYS_5V0

Table 3-17. Power Monitor Mapping I²C Port A (continued)

I²C Address	Power Rail
0x4B	VSYS_12V
0x4C	VPRH_12V

Table 3-18 lists the power supply pin groups that are monitored in port B.

Table 3-18. Power Monitor Mapping I²C Port B

I²C Address	Power Rail
0x40	VDD_SHV (1v8)
0x41	VDD_SHV (3v3)
0x42	VPRH_DV
0x43	VPRH_3V3
0x44	
0x45	
0x46	VPRH_1V8
0x47	VDDS_1V8
0x48	VDDS_DDR_1V8
0x49	VDDA_DPLL_1V8
0x4A	VDDA_ANA_1v8
0x4B	
0x4C	

3.24 GPIO Use

Table 3-19 lists the EVM GPIO assignments.

Table 3-19. List of EVM GPIO Assignments

GPIO	Signal Use
GPIO1_17	MCU SPI Enable
GPIO1_18	PMIC Interrupt
GPIO2_23	Display/Touch Interrupt
GPIO3_31	I/O Expander Interrupt
GPIO4_4	Ethernet Interrupt
GPIO4_15/TIMER3	Camera Expansion
GPIO4_17/TIMER1	Camera Expansion
GPIO4_18/TIMER2	Camera Expansion

Signal Multiplex Logic

Due to the high level of multiplexing on the SoC (17 levels), multiplex control logic is required to use different signals on the same BGA balls with their various functionality. Figure 4-1 provides the relative functions per ball; however, not all available functions are provided.) Figure 4-1 provides the supported onboard multiplexing for each interface.

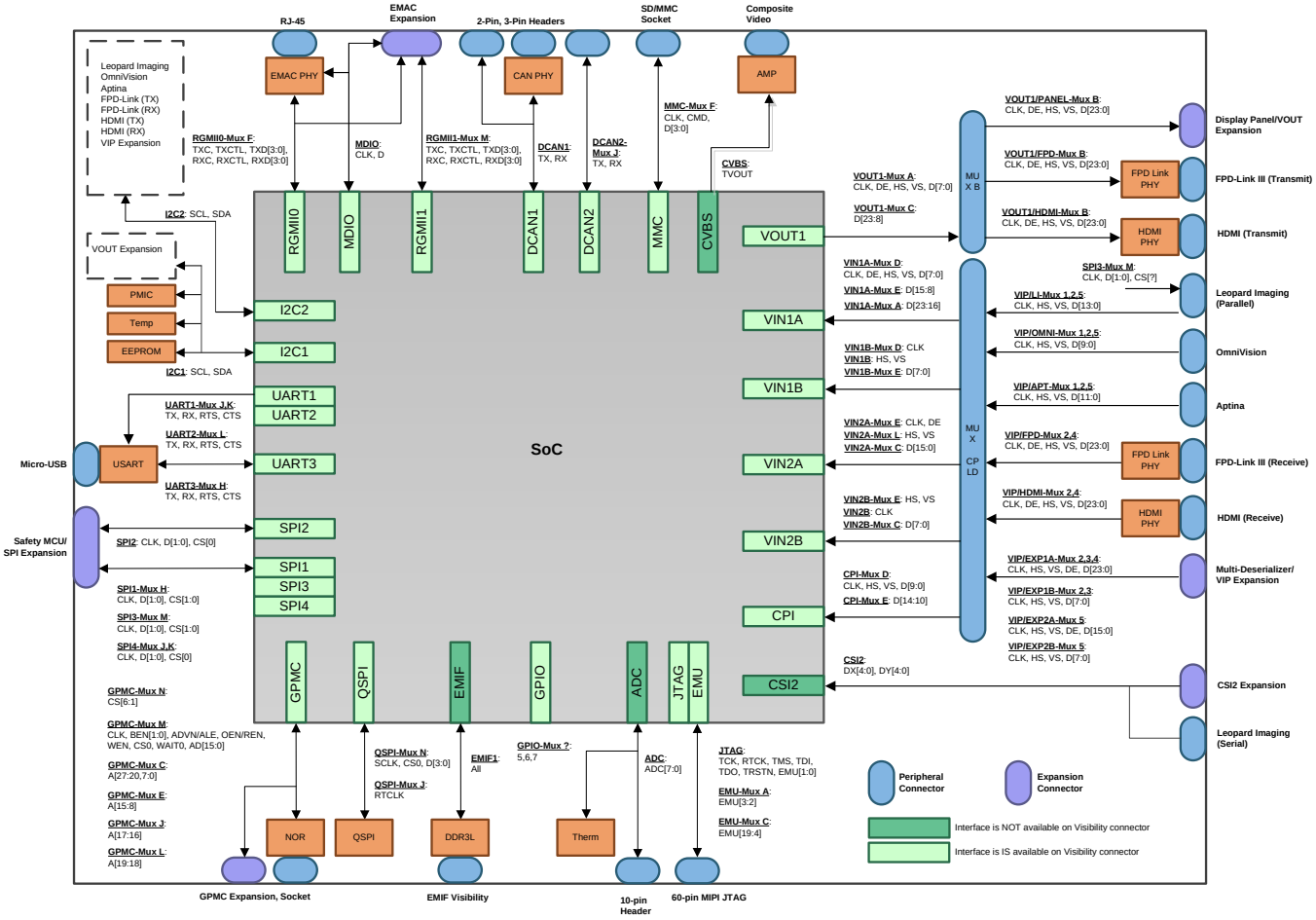
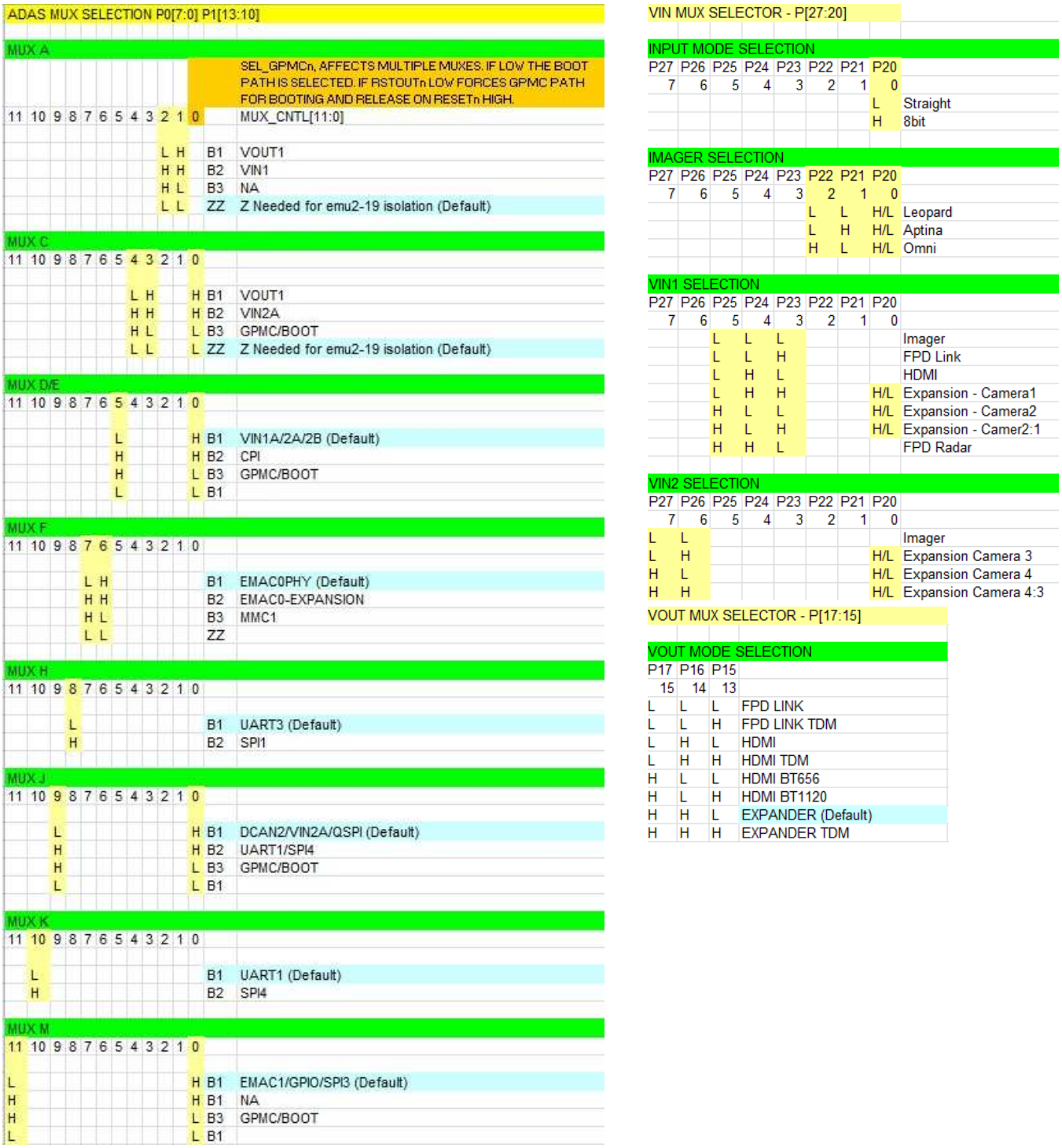


Figure 4-1. Muxing Block Diagram

4.1 MUX Configuration and Control

The I²C-based GPIO expander is used to control all onboard muxes. Figure 4-2 shows the specific bit assigned to each MUX, as well as the specific settings for the various selections.



ADAS MUX SELECTION P0[7:0] P1[13:10]

MUX A

SEL_GPMCn, AFFECTS MULTIPLE MUXES. IF LOW THE BOOT PATH IS SELECTED. IF RSTOUTn LOW FORCES GPMC PATH FOR BOOTING AND RELEASE ON RESETn HIGH.

11	10	9	8	7	6	5	4	3	2	1	0		MUX_CNTL[11:0]
									L	H		B1	VOUT1
									H	H		B2	VIN1
									H	L		B3	NA
									L	L		ZZ	Z Needed for emu2-19 isolation (Default)

MUX C

11	10	9	8	7	6	5	4	3	2	1	0		
							L	H			H	B1	VOUT1
							H	H			H	B2	VIN2A
							H	L			L	B3	GPMC/BOOT
							L	L			L	ZZ	Z Needed for emu2-19 isolation (Default)

MUX D/E

11	10	9	8	7	6	5	4	3	2	1	0		
						L					H	B1	VIN1A/2A/2B (Default)
						H					H	B2	CPI
						H					L	B3	GPMC/BOOT
						L					L	B1	

MUX F

11	10	9	8	7	6	5	4	3	2	1	0		
				L	H							B1	EMAC0PHY (Default)
				H	H							B2	EMAC0-EXPANSION
				H	L							B3	MMC1
				L	L							ZZ	

MUX H

11	10	9	8	7	6	5	4	3	2	1	0		
			L									B1	UART3 (Default)
			H									B2	SPI1

MUX J

11	10	9	8	7	6	5	4	3	2	1	0		
		L									H	B1	DCAN2/VIN2A/QSPI (Default)
		H									H	B2	UART1/SPI4
		H									L	B3	GPMC/BOOT
		L									L	B1	

MUX K

11	10	9	8	7	6	5	4	3	2	1	0		
	L											B1	UART1 (Default)
	H											B2	SPI4

MUX M

11	10	9	8	7	6	5	4	3	2	1	0		
L											H	B1	EMAC1/GPIO/SPI3 (Default)
H											H	B1	NA
H											L	B3	GPMC/BOOT
L											L	B1	

VIN MUX SELECTOR - P[27:20]

INPUT MODE SELECTION

P27	P26	P25	P24	P23	P22	P21	P20	
7	6	5	4	3	2	1	0	
							L	Straight
							H	8bit

IMAGER SELECTION

P27	P26	P25	P24	P23	P22	P21	P20	
7	6	5	4	3	2	1	0	
					L	L	H/L	Leopard
					L	H	H/L	Aptina
					H	L	H/L	Omni

VIN1 SELECTION

P27	P26	P25	P24	P23	P22	P21	P20	
7	6	5	4	3	2	1	0	
		L	L	L				Imager
		L	L	H				FPD Link
		L	H	L				HDMI
		L	H	H			H/L	Expansion - Camera1
		H	L	L			H/L	Expansion - Camera2
		H	L	H			H/L	Expansion - Camer2:1
		H	H	L				FPD Radar

VIN2 SELECTION

P27	P26	P25	P24	P23	P22	P21	P20	
7	6	5	4	3	2	1	0	
L	L							Imager
L	H						H/L	Expansion Camera 3
H	L						H/L	Expansion Camera 4
H	H						H/L	Expansion Camera 4:3

VOUT MUX SELECTOR - P[17:15]

VOUT MODE SELECTION

P17	P16	P15	
15	14	13	
L	L	L	FPD LINK
L	L	H	FPD LINK TDM
L	H	L	HDMI
L	H	H	HDMI TDM
H	L	L	HDMI BT656
H	L	H	HDMI BT1120
H	H	L	EXPANDER (Default)
H	H	H	EXPANDER TDM

Figure 4-2. I/O Expander MUX Settings

4.2 Display Multiplex

Figure 4-3 shows a part of the display section of the SoC pinmux table. The device supports additional functions not shown in the figure. The functions shown are intended to reflex those supported on the EVM. These functions include the following:

- Video Out (VOUT1): CLK, DE, FLD, HSYNC, VSYNC, D[23:0]
- Video In (VIN1A): D[23:16]
- Video In (VIN2A): D[15:0]
- Video In (VIN2B): D[7:0]
- Memory Bus (GPMC): A[27:20, 7:0]
- EMU/Trace (EMU): EMU[19:2]

Function 1			Function 3			Function 4			Function 6			Function 7		
Display														
DSS	vout1_clk	O	VIP1	vin1a_d[12]										
DSS	vout1_de	O	VIP1	vin1a_d[13]										
DSS	vout1_fld	O	VIP1	vin1a_d[14]										
DSS	vout1_hsync	O	VIP1	vin1a_d[15]										
DSS	vout1_vsync	O	VIP1	vin1a_d[16]	I									
DSS	vout1_d[0]	O	VIP1	vin1a_d[17]	I				MMC	mmc_clk	IO			
DSS	vout1_d[1]	O	VIP1	vin1a_d[18]	I				MMC	mmc_cmd	IO			
DSS	vout1_d[2]	O	VIP1	vin1a_d[19]	I				MMC	mmc_dat[0]	IO			
DSS	vout1_d[3]	O	VIP1	vin1a_d[20]	I				MMC	mmc_dat[1]	IO			
DSS	vout1_d[4]	O	VIP1	vin1a_d[21]	I				MMC	mmc_dat[2]	IO			
DSS	vout1_d[5]	O	VIP1	vin1a_d[22]	I				MMC	mmc_dat[3]	IO			
DSS	vout1_d[6]	O	VIP1	vin1a_d[23]	I				ESM	esm_error	IO	DEBUGSS	emu2	O
DSS	vout1_d[7]	O				PWMSS1	eCAP1_in_PV	IO				DEBUGSS	emu3	O
DSS	vout1_d[8]	O	VIP1	vin2a_d[0]	I	GPMC	gpmc_a[20]	O				DEBUGSS	emu4	O
DSS	vout1_d[9]	O	VIP1	vin2a_d[1]	I	GPMC	gpmc_a[21]	O				DEBUGSS	emu5	O
DSS	vout1_d[10]	O	VIP1	vin2a_d[2]	I	GPMC	gpmc_a[22]	O				DEBUGSS	emu6	O
DSS	vout1_d[11]	O	VIP1	vin2a_d[3]	I	GPMC	gpmc_a[23]	O				DEBUGSS	emu7	O
DSS	vout1_d[12]	O	VIP1	vin2a_d[4]	I	GPMC	gpmc_a[24]	O				DEBUGSS	emu8	O
DSS	vout1_d[13]	O	VIP1	vin2a_d[5]	I	GPMC	gpmc_a[25]	O				DEBUGSS	emu9	O
DSS	vout1_d[14]	O	VIP1	vin2a_d[6]	I	GPMC	gpmc_a[26]	O				DEBUGSS	emu10	O
DSS	vout1_d[15]	O	VIP1	vin2a_d[7]	I	GPMC	gpmc_a[27]	O				DEBUGSS	emu11	O
DSS	vout1_d[16]	O	VIP1	vin2a_d[8]	I	GPMC	gpmc_a[0]	O	VIP1	vin2b_d[0]	I	DEBUGSS	emu12	O
DSS	vout1_d[17]	O	VIP1	vin2a_d[9]	I	GPMC	gpmc_a[1]	O	VIP1	vin2b_d[1]	I	DEBUGSS	emu13	O
DSS	vout1_d[18]	O	VIP1	vin2a_d[10]	I	GPMC	gpmc_a[2]	O	VIP1	vin2b_d[2]	I	DEBUGSS	emu14	O
DSS	vout1_d[19]	O	VIP1	vin2a_d[11]	I	GPMC	gpmc_a[3]	O	VIP1	vin2b_d[3]	I	DEBUGSS	emu15	O
DSS	vout1_d[20]	O	VIP1	vin2a_d[12]	I	GPMC	gpmc_a[4]	O	VIP1	vin2b_d[4]	I	DEBUGSS	emu16	O
DSS	vout1_d[21]	O	VIP1	vin2a_d[13]	I	GPMC	gpmc_a[5]	O	VIP1	vin2b_d[5]	I	DEBUGSS	emu17	O
DSS	vout1_d[22]	O	VIP1	vin2a_d[14]	I	GPMC	gpmc_a[6]	O	VIP1	vin2b_d[6]	I	DEBUGSS	emu18	O
DSS	vout1_d[23]	O	VIP1	vin2a_d[15]	I	GPMC	gpmc_a[7]	O	VIP1	vin2b_d[7]	I	DEBUGSS	emu19	O

Figure 4-3. Signals Muxed With VOUT1

Mux A: Selects between 8-bit VOUT support and 24-bit VIN1 support. Also supports DISCONNECT for Trace/EMU.

Mux B: Selects one of the three 24-bit VOUT peripherals (FPD-Link III, HDMI, or Panel). Note: For BT656 support using HDMI, data lanes [9:2] are used for transmitting [7:0].

Mux C: Selects between > 8-bit VOUT support, VIN2A/B, and GPMC. Also supports DISCONNECT for Trace/EMU.

NOTE: VIN CPLD and NOR/GPMC implementations are shown in other diagrams.

Figure 4-4 shows muxing diagram for VOUT1

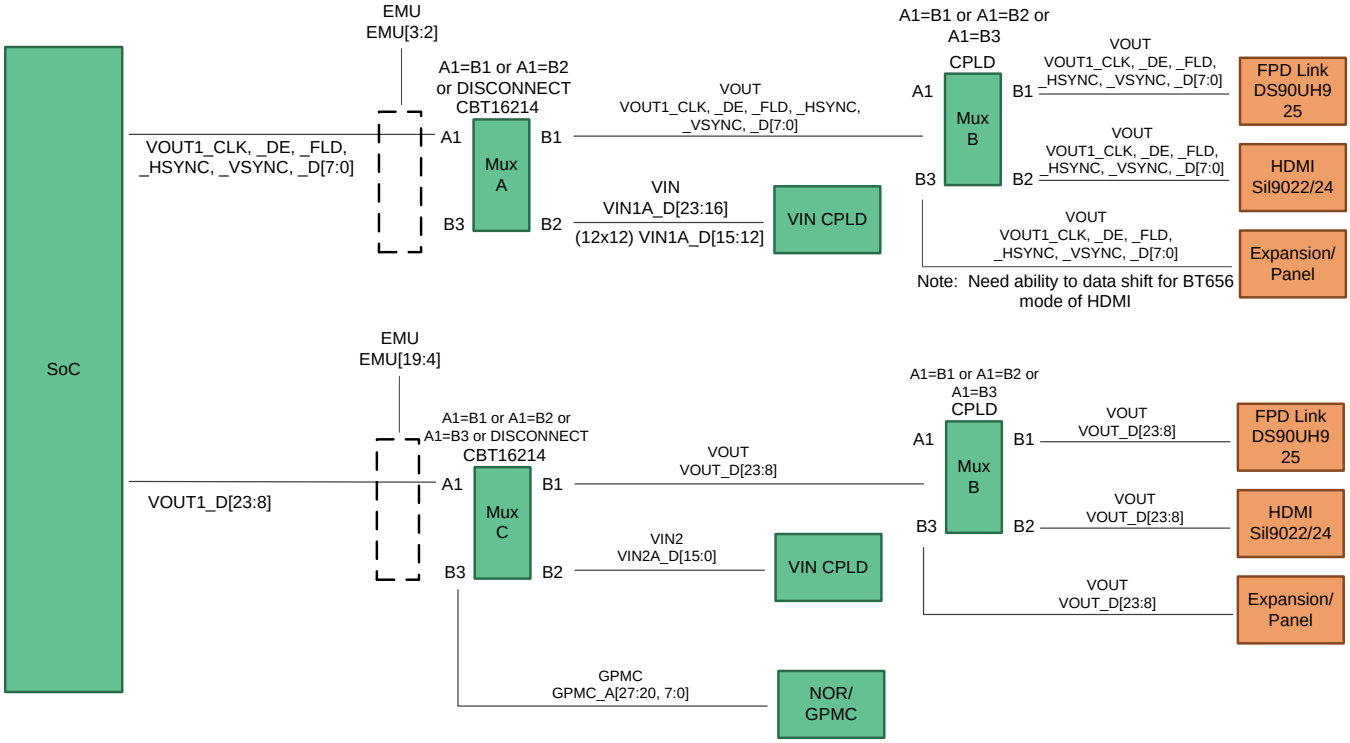


Figure 4-4. Muxing Diagram for VOUT1

4.3 VIP Multiplex

Figure 4-5 shows a part of the display section of the SoC pinmux table. The device supports additional functions not shown in the figure. The functions shown are intended to reflect those supported on the EVM. These functions include the following:

- Video In (VIN1A): CLK, DE, HSYNC, VSYNC, D[15:0]
- Video In (VIN1B): CLK, D[7:0]
- Video In (VIN2A): CLK
- Video In (VIN2B): CLK, HSYNC, VSYNC
- Memory Bus (GPMC): A[15:8]

Function 1			Function 2			Function 3			Function 4	
VIP1										
VIP1	vin1a_clk0	I	ISS	cpi_pclk	I					
VIP1	vin1a_de0	I	ISS	cpi_hsync	IO	VIP1	vin1b_clk1	I		
VIP1	vin1a_fld0	I	ISS	cpi_vsync	IO	VIP1	vin2b_clk1	I		
VIP1	vin1a_hsync0	I	ISS	cpi_data0	I	VIP1	vin1a_de0	I		
VIP1	vin1a_vsync0	I	ISS	cpi_data1	I					
VIP1	vin1a_d[0]	I	ISS	cpi_data2	I					
VIP1	vin1a_d[1]	I	ISS	cpi_data3	I					
VIP1	vin1a_d[2]	I	ISS	cpi_data4	I					
VIP1	vin1a_d[3]	I	ISS	cpi_data5	I					
VIP1	vin1a_d[4]	I	ISS	cpi_data6	I					
VIP1	vin1a_d[5]	I	ISS	cpi_data7	I					
VIP1	vin1a_d[6]	I	ISS	cpi_data8	I					
VIP1	vin1a_d[7]	I	ISS	cpi_data9	I					
VIP1	vin1a_d[8]	I	ISS	cpi_data10	I	VIP1	vin1b_d[0]	I	GPMC	gpmc_a[8]
VIP1	vin1a_d[9]	I	ISS	cpi_data11	I	VIP1	vin1b_d[1]	I	GPMC	gpmc_a[9]
VIP1	vin1a_d[10]	I	ISS	cpi_data12	I	VIP1	vin1b_d[2]	I	GPMC	gpmc_a[10]
VIP1	vin1a_d[11]	I	ISS	cpi_data13	I	VIP1	vin1b_d[3]	I	GPMC	gpmc_a[11]
VIP1	vin1a_d[12]	I	ISS	cpi_data14	I	VIP1	vin1b_d[4]	I	GPMC	gpmc_a[12]
VIP1	vin1a_d[13]	I	ISS	cpi_wen	I	VIP1	vin1b_d[5]	I	GPMC	gpmc_a[13]
VIP1	vin1a_d[14]	I	ISS	cpi_fid	IO	VIP1	vin1b_d[6]	I	GPMC	gpmc_a[14]
VIP1	vin1a_d[15]	I	ISS	cpi_data15	I	VIP1	vin1b_d[7]	I	GPMC	gpmc_a[15]
VIP1	vin2a_clk0	I								
VIP1	vin2a_de0	I	ISS	cam_strobe	O	VIP1	vin2b_hsync1	I		
VIP1	vin2a_fld0	I	ISS	cam_shutter	O	VIP1	vin2b_vsync1	I		

Figure 4-5. Signals Muxed With VIN1A and VIN2A

Mux D: Selects between 8-bit VIP support and ISS Camera support.

Mux E: Selects between > 8-bit VIP support, ISS Camera, and GPMC bus.

NOTE: VIN CPLD and NOR/GPMC implementations are shown in other diagrams.

Figure 4-6 shows the muxing diagram for VIN1A and VIN2A.

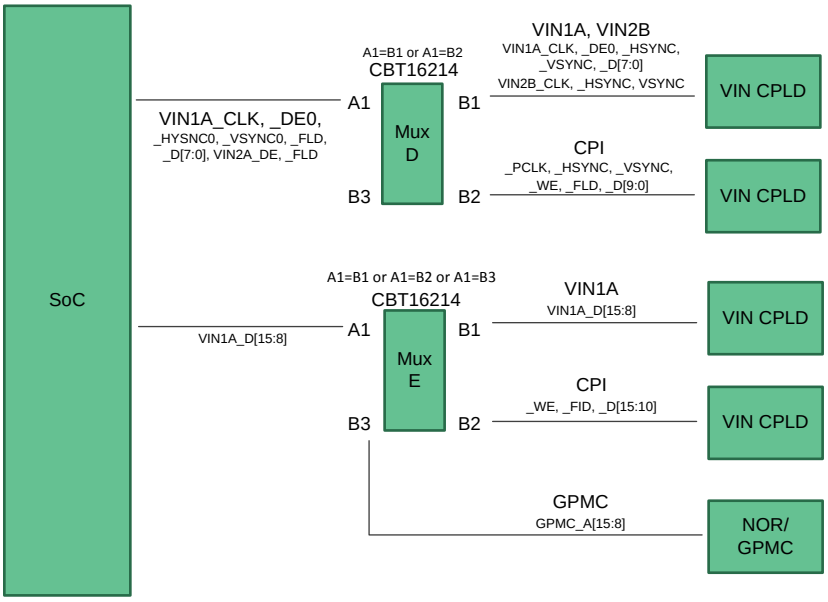


Figure 4-6. Muxing Diagram for VIN1A and VIN2A

4.4 EMAC Multiplex

Figure 4-7 shows a part of the display section of the SoC pinmux table. The device supports additional functions not shown in the figure. The functions shown are intended to reflect those supported on the EVM. These functions include the following:

- Management Data (MDIO): CLK, D
- EMAC (RGMII): TXC, TXCTL, TXD[3:0], RXC, RXCTL, RXD[3:0]
- MMC/SD (MMC): CLK, CMD, D[3:0]

				Z	AA	AB
Function 1				Function 6		
EMAC	mdio_mclk	O				
EMAC	mdio_d	IO		ESM	esm_error	IO
EMAC	rgmii0_txc	O		MMC	mmc_clk	IO
EMAC	rgmii0_txctl	O		MMC	mmc_cmd	IO
EMAC	rgmii0_txd[3]	O		MMC	mmc_dat[0]	IO
EMAC	rgmii0_txd[2]	O		MMC	mmc_dat[1]	IO
EMAC	rgmii0_txd[1]	O		MMC	mmc_dat[2]	IO
EMAC	rgmii0_txd[0]	O		MMC	mmc_dat[3]	IO
EMAC	rgmii0_rxc	I		MMC	mmc_clk	IO
EMAC	rgmii0_rxctl	I		MMC	mmc_cmd	IO
EMAC	rgmii0_rxd[3]	I		MMC	mmc_dat[0]	IO
EMAC	rgmii0_rxd[2]	I		MMC	mmc_dat[1]	IO
EMAC	rgmii0_rxd[1]	I		MMC	mmc_dat[2]	IO
EMAC	rgmii0_rxd[0]	I		MMC	mmc_dat[3]	IO

Figure 4-7. Signals Muxed With EMAC

Mux F: Selects between EMAC/RGMII0 support and MMC support.

Mux G: Selects MDIO to both or either Ethernet PHY (onboard and Expansion)

NOTE: This is expected to be resistor mux with both selected by default.

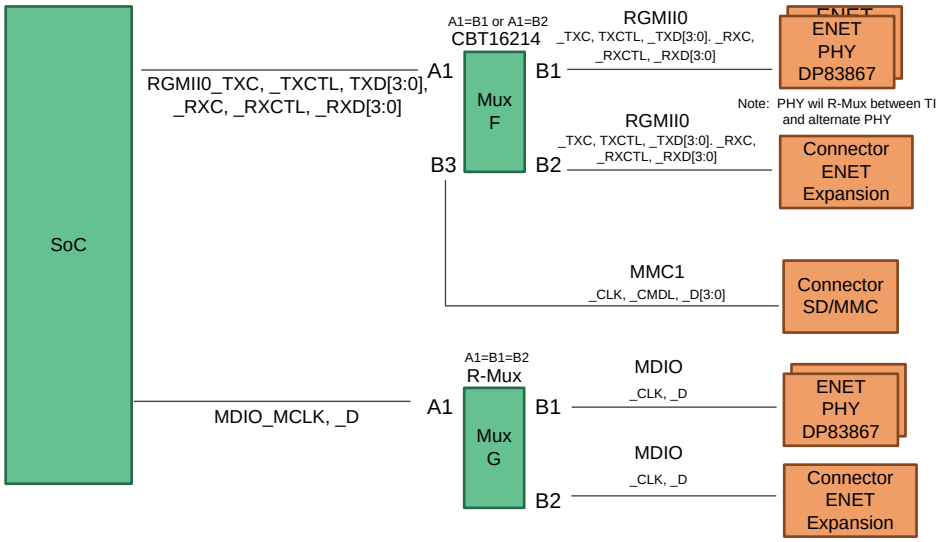


Figure 4-8. Muxing Diagram for EMAC

4.5 SPI1 and SPI2 Multiplex

Figure 4-9 shows a part of the display section of the SoC pinmux table. The device supports additional functions not shown in the figure. The functions shown are intended to reflect those supported on the EVM. These functions include the following:

- SPI1: CLK, D0, D1, CS[1:0]
- SPI2: CLK, D0, D1, CS[0]
- UART (UART3): TXD, RXD, RTSN, CTSN

Function 1			Function 2			Function 15		
SPI1	spi1_sclk	IO	UART3	uart3_rxd	I	GPIO4	gpio4_0	IO
SPI1	spi1_d[1]	IO	UART3	uart3_ctsn	I	GPIO4	gpio4_1	IO
SPI1	spi1_d[0]	IO	UART3	uart3_rtsn	O	GPIO4	gpio4_2	IO
SPI1	spi1_cs[0]	IO	UART3	uart3_txd	O	GPIO4	gpio4_3	IO
SPI1	spi1_cs[1]	IO	SPI3	spi3_cs[1]	IO	GPIO4	gpio4_4	IO

Function 1		
SPI2	spi2_sclk	IO
SPI2	spi2_d[1]	IO
SPI2	spi2_d[0]	IO
SPI2	spi2_cs[0]	IO

Figure 4-9. Signals Muxed With SPI1 and SPI2

Mux H: Selects between UART and MCU expansion support.

Figure 4-10 shows the muxing diagram for SPI1 and SPI2.

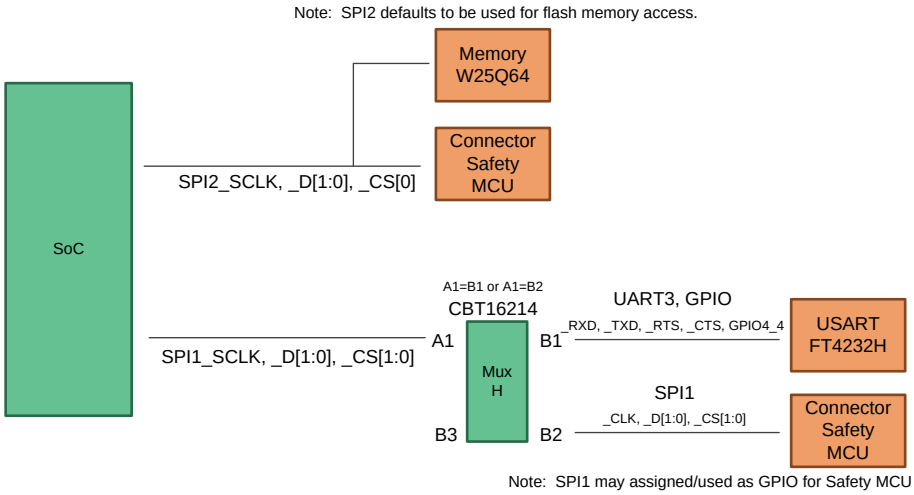


Figure 4-10. Muxing Diagram for SPI1 and SPI2

4.6 UART1 and UART2 Multiplex

Figure 4-11 shows a part of the display section of the SoC pinmux table. The device supports additional functions not shown in the figure. The functions shown are intended to reflect those supported on the EVM. These functions include the following:

- UART (UART1): TXD, RXD, RTSN, CTSN
- UART (UART2): TXD, RXD, RTSN, CTSN
- Memory Bus (GPMC): A[19:16]
- Memory Bus (QSPI): RTCLK
- Serial Periph Interface (SPI4): CLK, D0, D1, CS[0]
- Digital CAN (DCAN2): TX, RX
- Video In (VIN2A): HSYNC, VSYNC

Function 1			Function 2			Function 4			Function 5			Function 9			
UART	uart1_ctsn	I	PRCM	xref_clk1	I	GPMC	gpmc_a[16]	O	SPI4	spi4_sclk	IO	PRCM	clkout0	O	
UART	uart1_rtsn	O				GPMC	gpmc_a[17]	O	SPI4	spi4_cs[0]	IO	QSPI1	qspi1_rtclk	I	

Function 1			Function 2			Function 4			Function 5			Function 13		
UART1														
UART	uart1_rxd	I							SPI4	spi4_d[1]	IO	DCAN1	dcan2_tx	IO
UART	uart1_txd	O							SPI4	spi4_d[0]	IO	DCAN1	dcan2_rx	IO

Function 1			Function 4			Function 10		
UART	uart2_rxd	I						
UART	uart2_txd	O						
UART	uart2_ctsn	I	GPMC	gpmc_a[18	O	VIP1	vin2a_hsync0	I
UART	uart2_rtsn	O	GPMC	gpmc_a[19	O	VIP1	vin2a_vsync0	I

Figure 4-11. Signals Muxed With UART1 and UART2

Mux J: Selects between primary functions (QSPI, DCAN, Video In, GPIO), validation functions (SPI, UART), and GPMC bus.

Mux K: Selects between UART and MCU expansion support.

Figure 4-12 shows the muxing diagram for UART1 and UART2.

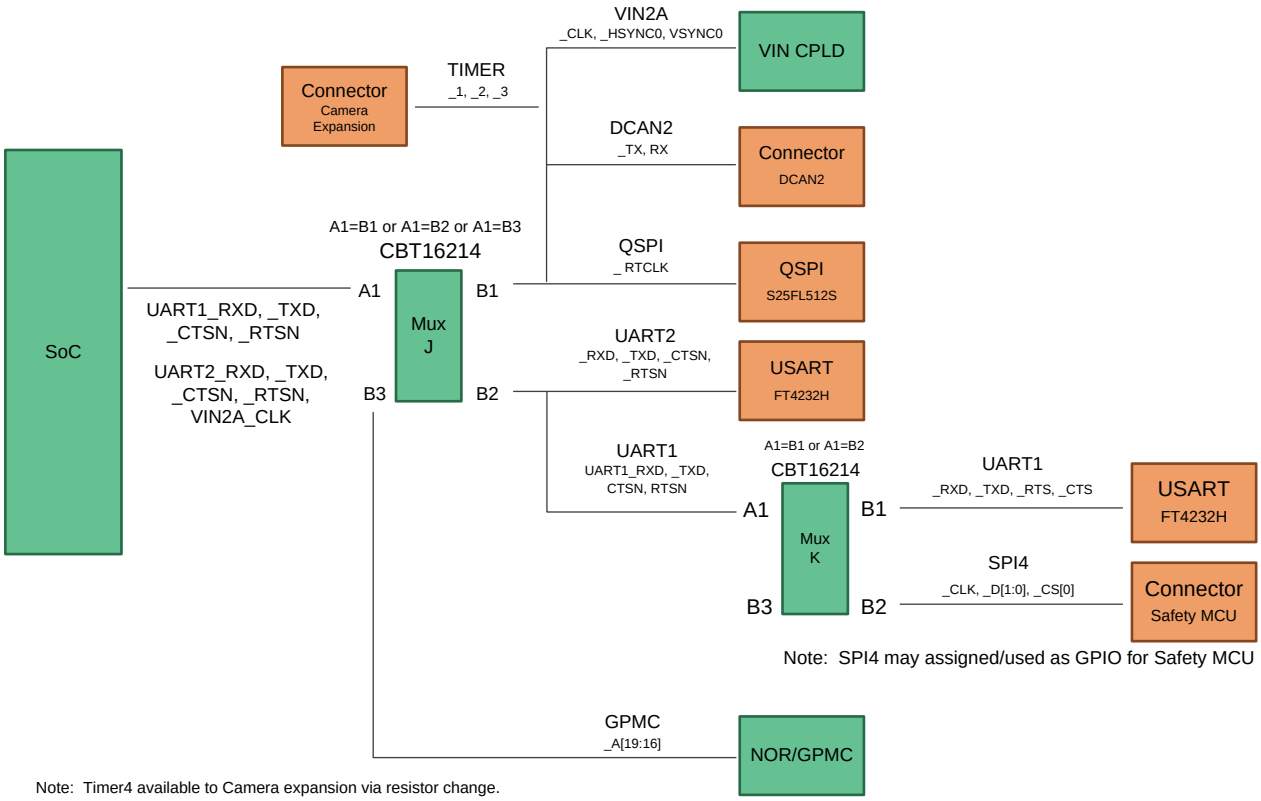


Figure 4-12. Muxing Diagram for UART1 and UART2

4.7 GPMC Multiplex

Figure 4-13 shows a part of the display section of the SoC pinmux table. The device supports additional functions not shown in the figure. The functions shown are intended to reflect those supported on the EVM. These functions include the following:

- Memory Bus (GPMC): CLK, BE[1:0], ADV/ALE, OEN, WE, CS[6:0], WAIT0, AD[15:0]
- Memory Bus (QSPI): CLK, CS0, D[3:0]
- System Boot (SYSBOOT): SYSBOOT [15:0]
- EMAC (RGMII1): TXC, TXCTL, TXD[3:0], RXC, RXCTL, RXD[3:0]
- Serial Periph Interface (SPI3): CLK, D0, D1, CS[1:0]
- General I/O (GPIO): GPIO1_[29:18]

Figure 4-13 shows the signals muxed With GPMC.

Function 1			Function 2			Function 5			Function 15			Function 16		
GPMC	gpmc_clk	IO	EMAC	rgmii1_txc	O				GPIO1	gpio1_0	IO			
GPMC	gpmc_ben[0]	O	EMAC	rgmii1_txctl	O	PWMSS1	ehrpwm1A	O	GPIO1	gpio1_1	IO			
GPMC	gpmc_ben[1]	O	EMAC	rgmii1_txd[3]	O	PWMSS1	ehrpwm1B	O	GPIO1	gpio1_2	IO			
GPMC	gpmc_advn_a	O	EMAC	rgmii1_txd[2]	O	PWMSS1	ehrpwm1_tripzor	IO	GPIO1	gpio1_3	IO			
GPMC	gpmc_oen_re	O	EMAC	rgmii1_txd[1]	O	PWMSS1	ehrpwm1_synci	I	GPIO1	gpio1_4	IO			
GPMC	gpmc_wen	O	EMAC	rgmii1_txd[0]	O	PWMSS1	ehrpwm1_synco	O	GPIO1	gpio1_5	IO			
GPMC	gpmc_cs[0]	O	EMAC	rgmii1_rxctl	I				GPIO1	gpio1_6	IO			
GPMC	gpmc_cs[1]	O	QSPI1	qspi1_cs[0]	IO				GPIO1	gpio1_7	IO			
GPMC	gpmc_cs[2]	O	QSPI1	qspi1_d[3]	IO				GPIO1	gpio1_8	IO			
GPMC	gpmc_cs[3]	O	QSPI1	qspi1_d[2]	IO				GPIO1	gpio1_9	IO			
GPMC	gpmc_cs[4]	O	QSPI1	qspi1_d[1]	IO				GPIO1	gpio1_10	IO			
GPMC	gpmc_cs[5]	O	QSPI1	qspi1_d[0]	IO				GPIO1	gpio1_11	IO			
GPMC	gpmc_cs[6]	O	QSPI1	qspi1_sclk	O				GPIO1	gpio1_12	IO			
GPMC	gpmc_wait0	I	EMAC	rgmii1_rxd[3]	I				GPIO1	gpio1_13	IO			
GPMC	gpmc_ad[0]	IO	EMAC	rgmii1_rxd[2]	I				GPIO1	gpio1_14	IO	CHIPGLL	sysboot0	I
GPMC	gpmc_ad[1]	IO	EMAC	rgmii1_rxd[1]	I				GPIO1	gpio1_15	IO	CHIPGLL	sysboot1	I
GPMC	gpmc_ad[2]	IO	EMAC	rgmii1_rxd[0]	I				GPIO1	gpio1_16	IO	CHIPGLL	sysboot2	I
GPMC	gpmc_ad[3]	IO	QSPI1	qspi1_rtclk	I				GPIO1	gpio1_17	IO	CHIPGLL	sysboot3	I
GPMC	gpmc_ad[4]	IO	ISS	cam_strobe	O				GPIO1	gpio1_18	IO	CHIPGLL	sysboot4	I
GPMC	gpmc_ad[5]	IO				SPI3	spi3_d[1]		GPIO1	gpio1_19	IO	CHIPGLL	sysboot5	I
GPMC	gpmc_ad[6]	IO				SPI3	spi3_d[0]		GPIO1	gpio1_20	IO	CHIPGLL	sysboot6	I
GPMC	gpmc_ad[7]	IO	ISS	cam_shutter	O	SPI3	spi3_sclk		GPIO1	gpio1_21	IO	CHIPGLL	sysboot7	I
GPMC	gpmc_ad[8]	IO				SPI3	spi3_cs[0]		GPIO1	gpio1_22	IO	CHIPGLL	sysboot8	I
GPMC	gpmc_ad[9]	IO				SPI3	spi3_cs[1]		GPIO1	gpio1_23	IO	CHIPGLL	sysboot9	I
GPMC	gpmc_ad[10]	IO							GPIO1	gpio1_24	IO	CHIPGLL	sysboot10	I
GPMC	gpmc_ad[11]	IO							GPIO1	gpio1_25	IO	CHIPGLL	sysboot11	I
GPMC	gpmc_ad[12]	IO							GPIO1	gpio1_26	IO	CHIPGLL	sysboot12	I
GPMC	gpmc_ad[13]	IO	EMAC	rgmii1_rxc	I				GPIO1	gpio1_27	IO	CHIPGLL	sysboot13	I
GPMC	gpmc_ad[14]	IO				SPI2	spi2_cs[1]		GPIO1	gpio1_28	IO	CHIPGLL	sysboot14	I
GPMC	gpmc_ad[15]	IO				SPI2	spi2_cs[0]		GPIO1	gpio1_29	IO	CHIPGLL	sysboot15	I

Figure 4-13. Signals Muxed With GPMC

Mux M: Selects between GPMC, Ethernet (using expansion), and MCU expansion (SPI3).

Mux N: Selects GPMC chip selects and QSPI memory.

NOTE: NOR/GPMC implementation is shown in other diagrams.

Figure 4-14 shows the muxing diagram for GPMC.

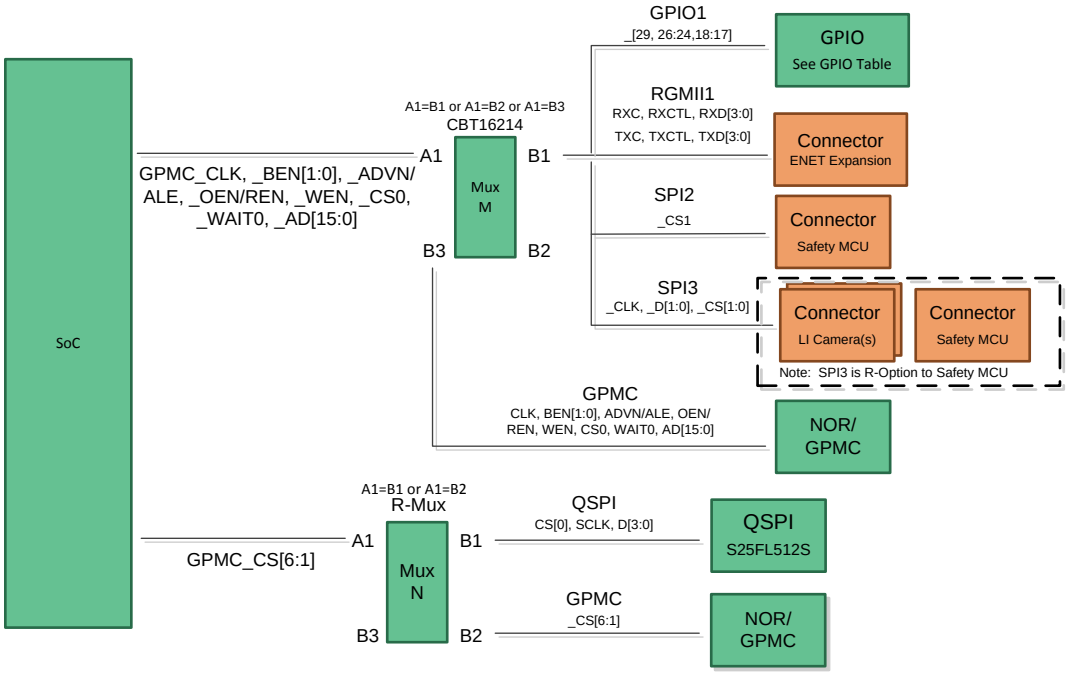
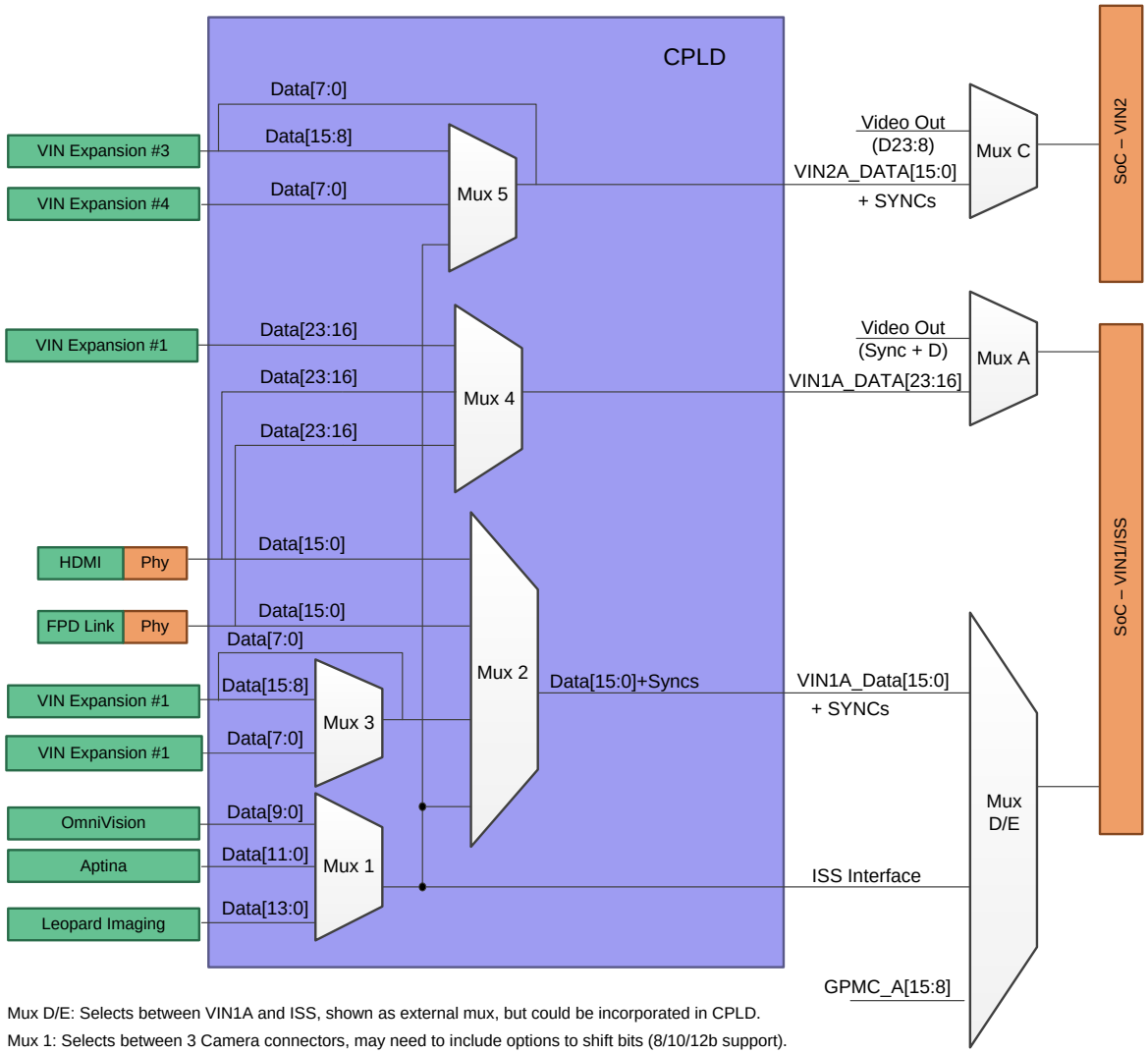


Figure 4-14. Muxing Diagram for GPMC

Programmable Logic

Due to the high level of VIP/ISS multiplexing on the SoC (17 levels), multiplex control logic is required to use different signals on the same BGA balls with their various functionality (see Figure 5-1).



Mux D/E: Selects between VIN1A and ISS, shown as external mux, but could be incorporated in CPLD.

Mux 1: Selects between 3 Camera connectors, may need to include options to shift bits (8/10/12b support).

Mux 2: Selects between 4 VIN inputs (Camera, Expansion, FPD Link, HDMI)

Mux 3: Selects between 16b support (Exp #1) and dual 8b support (Exp #1 + Exp #2).

Mux 4: Could be considered part of Mux 2, expect only 2 VIN inputs support 24b

Mux 5: Selects between 16b support (Exp #3) and dual 8b support (Exp #3 +Exp #4). Similar to Mux 3, but for VIN2

Note: I/O should be oriented such that voltage levels on left of diagram can be adjusted independent of those on the right.
For example, camera interface may need to be operated at 1v8 levels, with processor at 3v3 levels.

Figure 5-1. VIN CPLD Muxing Diagram

PCB Board With Components Identification

6.1 Top Side Components

Figure 6-1 shows the top-side components.

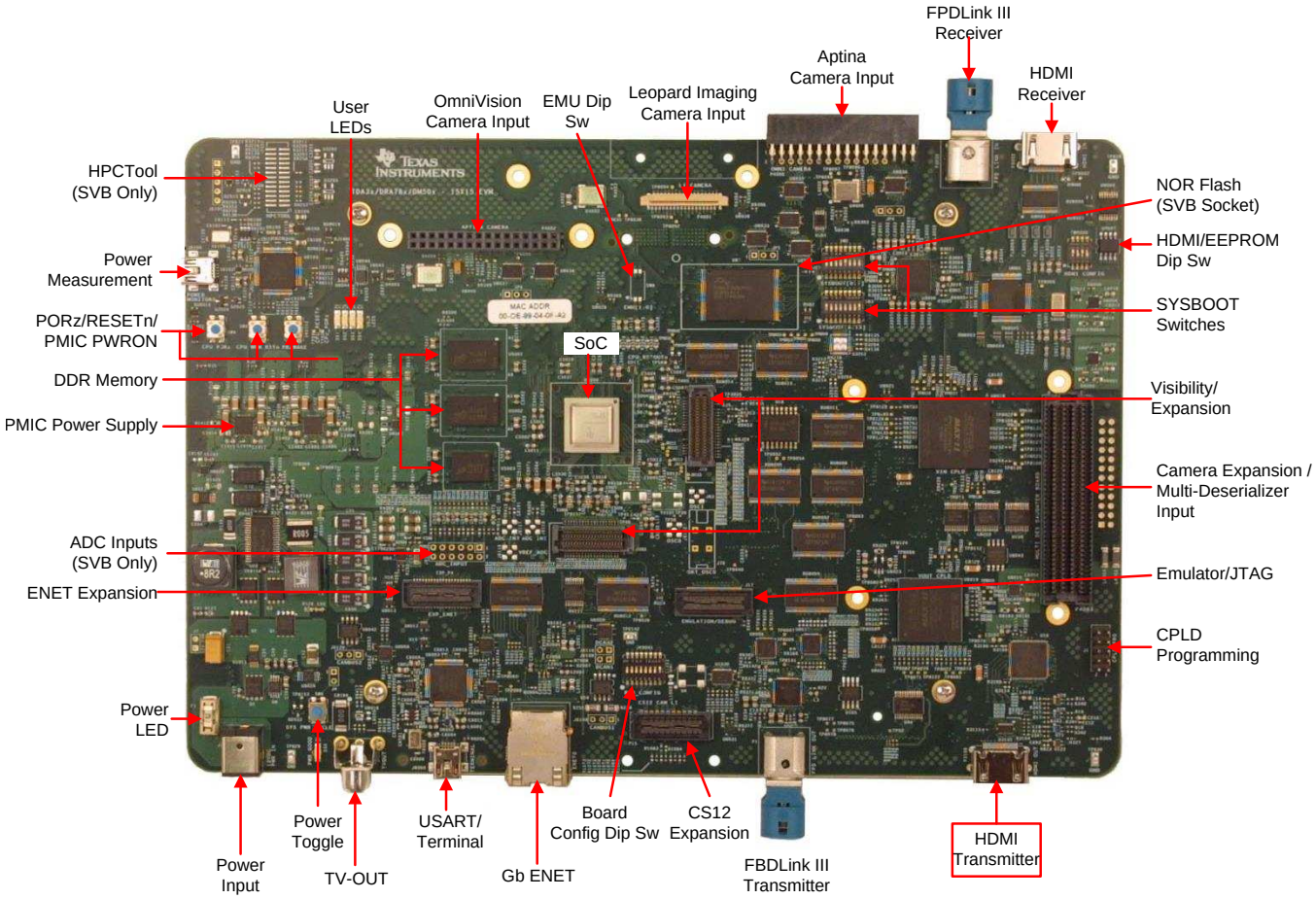


Figure 6-1. Top-Side Components Diagram

6.2 Bottom Side Components

Figure 6-2 shows the bottom-side components.

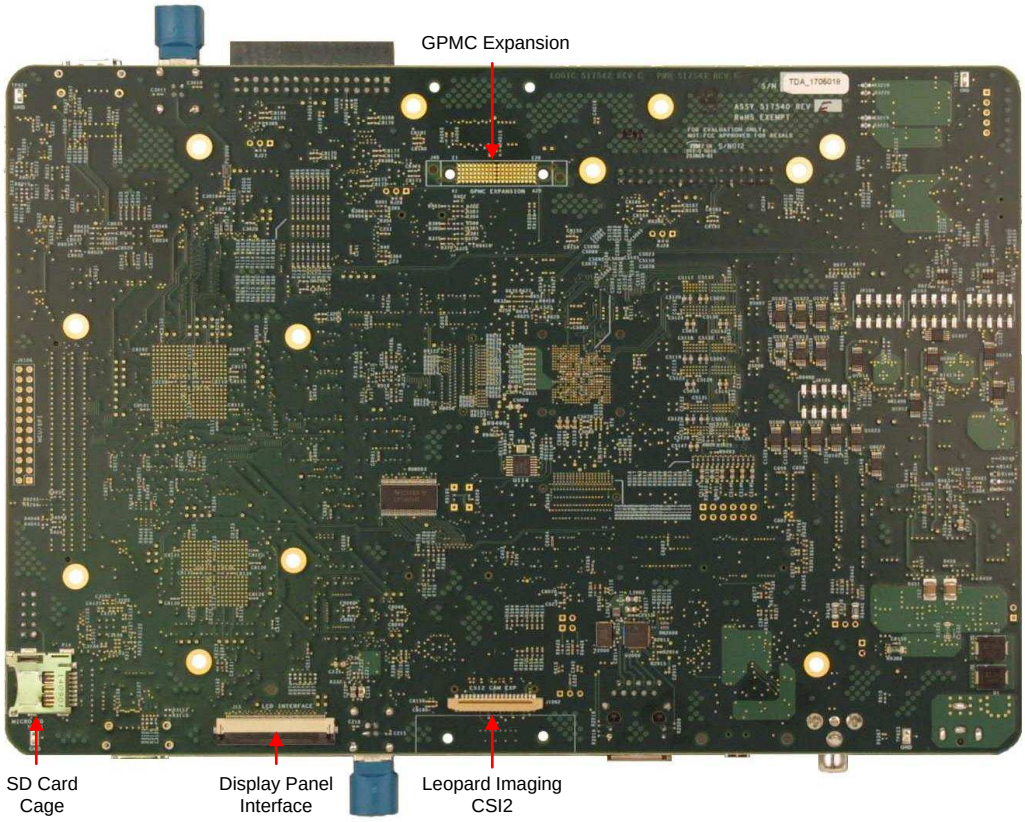


Figure 6-2. Bottom-Side Components Diagram

References

- Texas Instruments, TDA3x, DRA78x, and DM50x-15X15 CPU Board PCB Rev E
- Texas Instruments, TDA3x, DRA78x, and DM50x-15X15 CPU Board Schematic Rev E1
- Texas Instruments, TDA3x, DRA78x, and DM50x-15X15 CPU Board BOM Rev E
- Texas Instruments, TDA3x, DRA78x, and DM50x-15X15 CPU Board Assembly Drawing Rev E
- Texas Instruments, TDA3x, DRA78x, and DM50x-15X15 CPU Board PCB Drawing Rev E

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