User's Guide

Jacinto7 EVM Gateway/Ethernet Switch Expansion

ABSTRACT

This user's guide describes the hardware architecture of the Jacinto7 EVM - Gateway/Ethernet Switch/Industrial (GESI) Boards. GESI is one of the Expansion boards, which shall be interfaced with Jacinto7 common processor board.

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Trademarks

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1 Introduction

The Jacinto7 EVMs are development and evaluation systems that enable developers to write software and develop hardware around the Jacinto7 family of processors. The main elements of the system are available on the base board(s) of the EVM. This gives developers the basic resources needed for most general-purpose type projects that encompass the Jacinto7 processor.

The Jacinto7 EVM is comprised of two boards:

- Jacinto7 System on Module (SOM) – which includes Jacinto7 processor, its power solution, and non-volatile memory.
- Jacinto7 Common Processor Board (CPB) – which includes wide variety of memories, peripherals, and debug tools supporting by the Jacinto7 processor.

Beyond the basic resources provided, additional functionality can be added via expansion cards.

This technical user's guide describes the hardware architecture and functionality of the Gateway/Ethernet Switch/Industrial (GESI) expansion board.

1.1 Key Features

Below are the key features of the expansion board:

- Ethernet:
  - 4x 10/100/1000Mbps - RGMII ports (DP83867E)
  - 1x 10/100Mbps - RMII port (DP83822I)
- 6x CAN interface
- 6x LIN interface
- PROFI BUS/RS485 port (DB9)
- USS/IMU Sensor header
- Motor Control header
- Booster pack Interface header
- Board ID EEPROM

2 GESI Expansion Board Overview

Jacinto7 EVM can support different types of expansion boards. Not all of the expansion boards are supported on each Jacinto7 EVMs.

To determine which version Jacinto7 EVM supports the GESI expansion board, see Appendix A.

Figure 2-1 shows the overall architecture of Jacinto7 EVM.

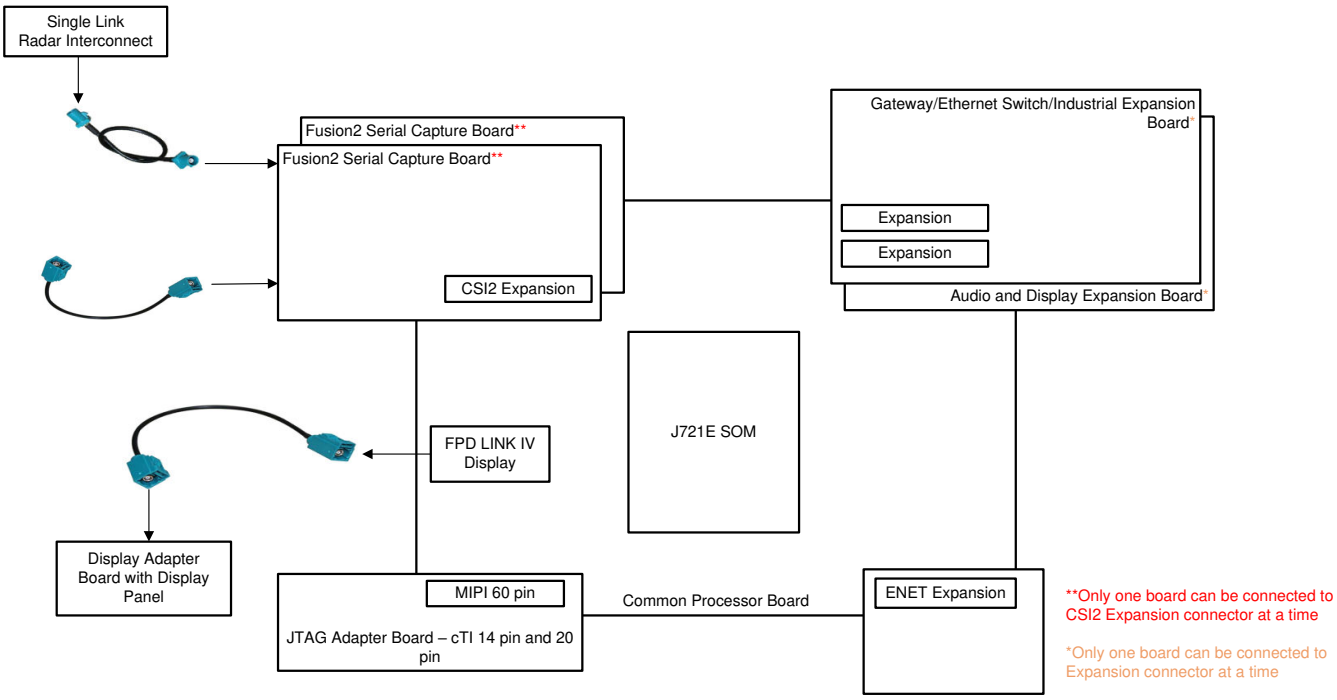


Figure 2-1. System Architecture Interface

2.1 GESI Expansion Board Identification

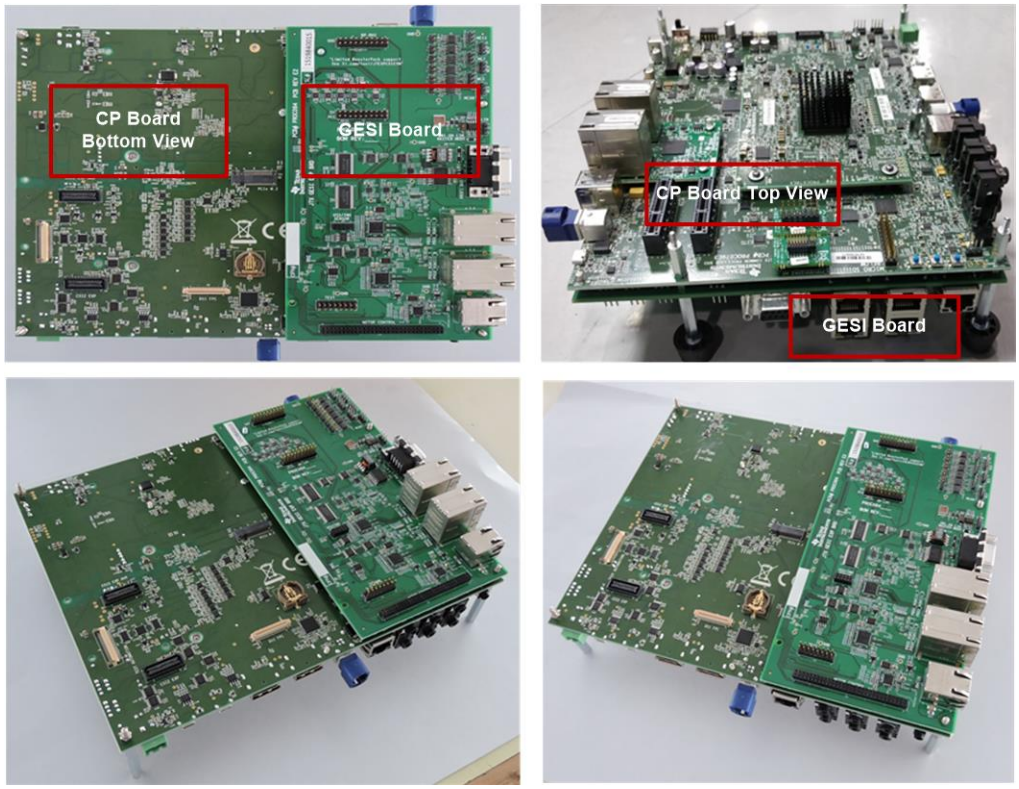
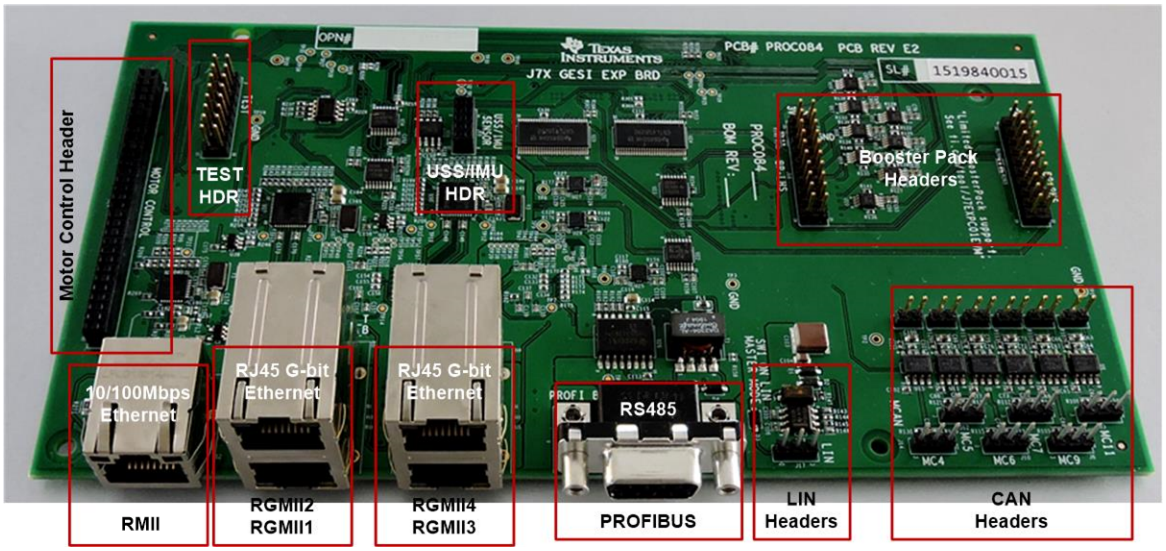


Figure 2-2. System Assembly Image

2.2 GESI Expansion Board Component Identification



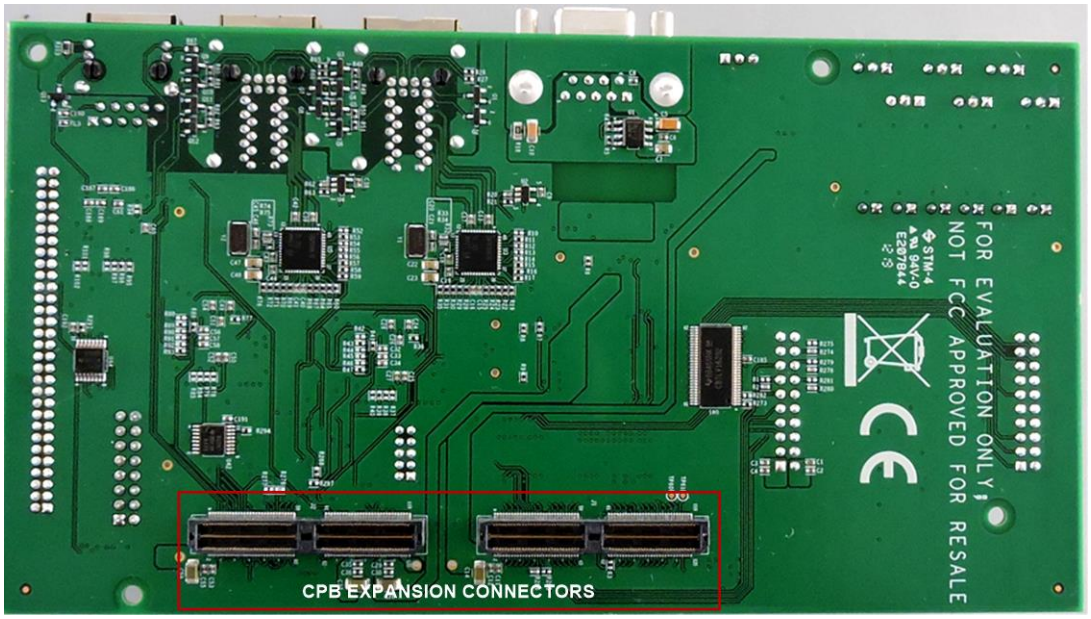


Figure 2-3. Infotainment Expansion Board Component Identification

3 GESI Expansion Board - User Setup/Configuration

3.1 GESI Infotainment Expansion Board With CP Board

GESI expansion boards should be interfaced with Jacinto7 EVM CP Board in bottom mating. Two expansion connectors J1 and J2 on the GESI will be mated to the EVM CPB Expansion connectors J46 and J51.

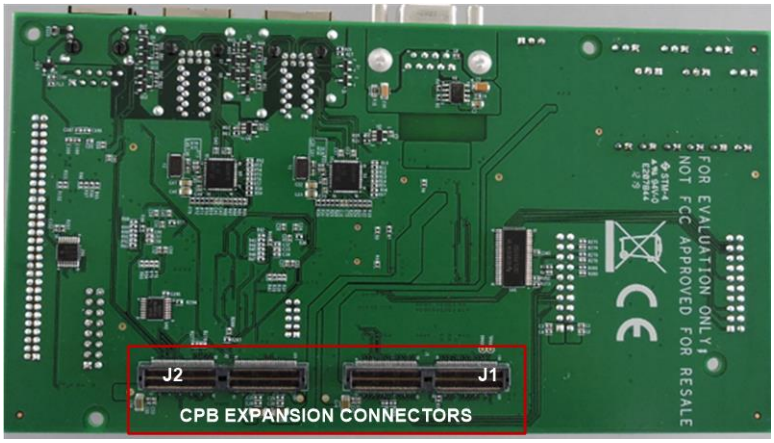


Figure 3-1. Expansion Connectors on INFO Exp Board Top Side

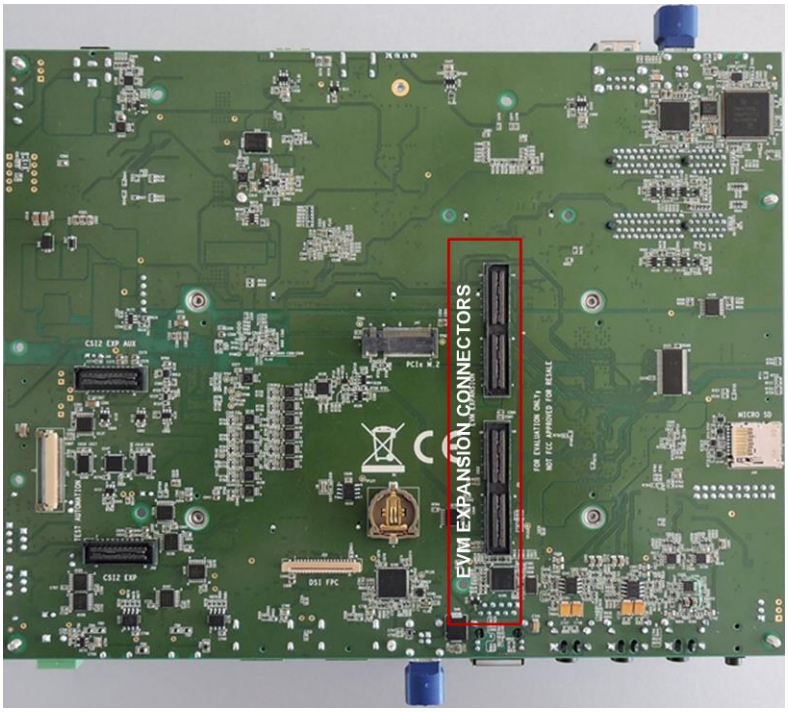


Figure 3-2. Expansion Connectors on Jacinto7 CP Board Bottom Side

3.1.1 Board Assembly Procedures

1. Take the Assembled CP board Kit
2. Remove the spacers from CP board and mate the infotainment board on CP board left side B-B connectors.
3. Add 2 mm thick washer (PART NUMBER : RWM100A) on the four stand offs in case no CSI Expansion Board connected.
4. Fix all the eight stand offs.

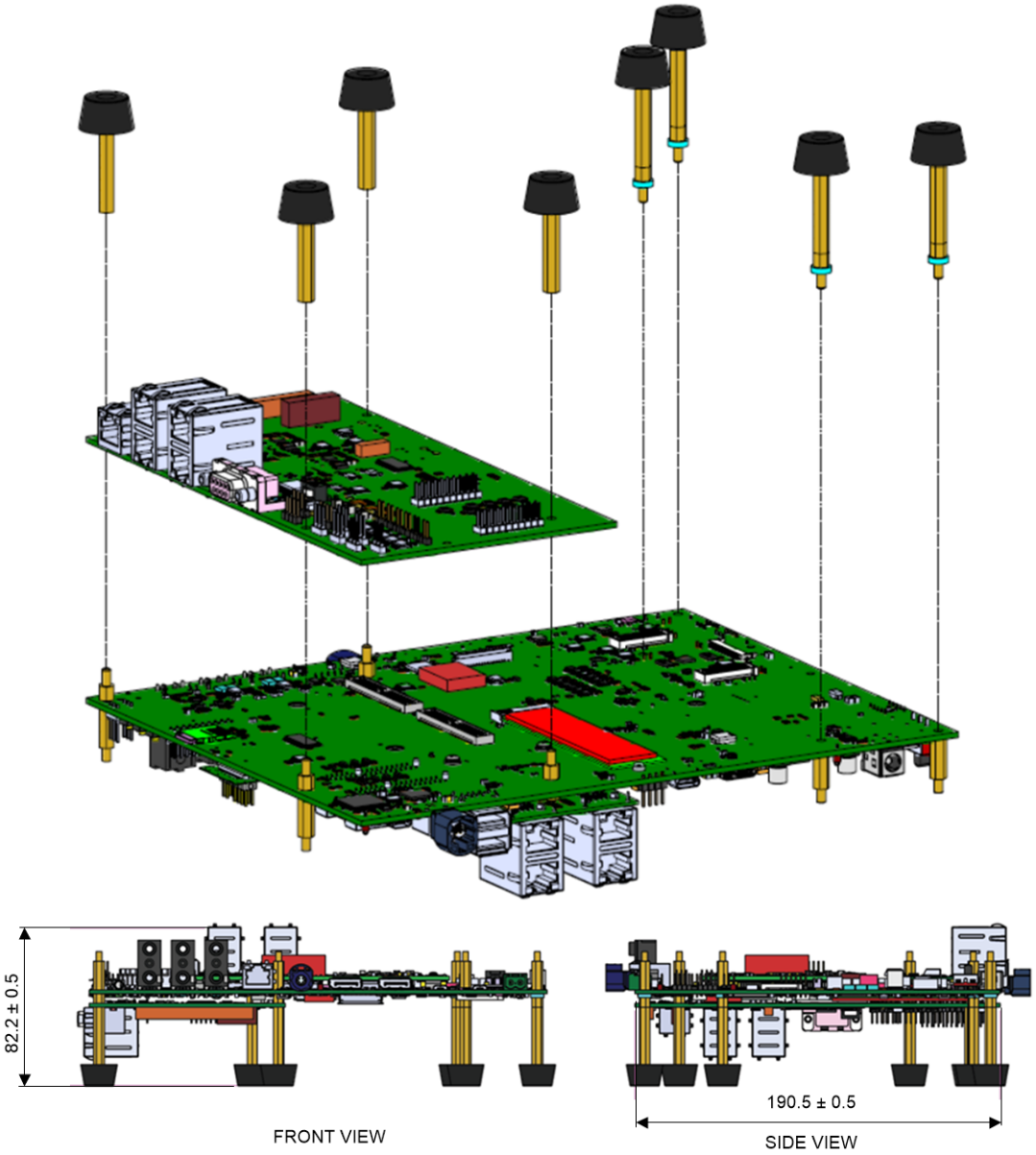


Figure 3-3. Board Assembly Procedure

3.2 Power Requirements

External power supply is not required since GESI board takes power from Jacinto7 EVM Common Processor Board. 12 V, 5 V, 3.3 V and 3.3 V_IO are tapped from CPB.

Power to the Ethernet PHY's 2.5 V, 1.8 V and 1 V are generated locally on GESI board using LDO circuits.

No Power ON indication LEDs are provided in the GESI expansion board.

3.3 EVM Reset/Interrupt Push Buttons

Jacinto7 EVM supports multiple User Push buttons for providing Reset inputs and User Interrupts to the processor. For their location and function, see the device-specific user's manual.

There are no Specific Reset/Interrupt Push Buttons available on the infotainment expansion board.

3.4 EVM Configuration DIP Switch

Common processor board has dedicated EVM configuration switch (SW3) shown in Figure 3-4 to set the various functions of EVM peripherals. The Configuration DIP Switch (SW3) is placed on Top side of CPB right below the USB Type C port.

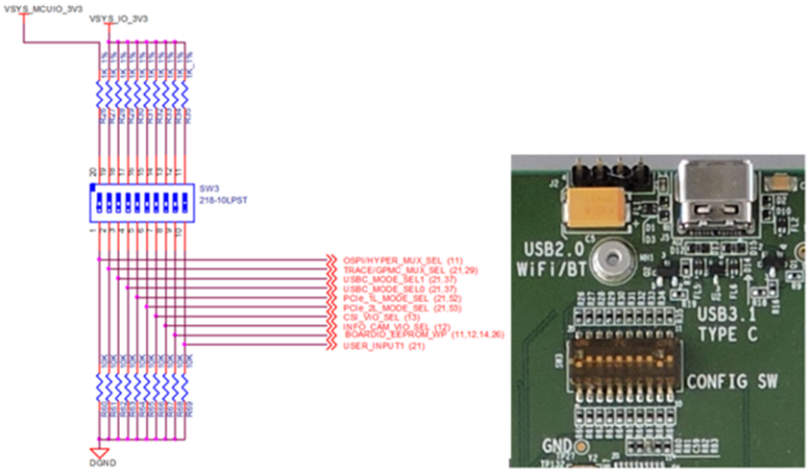


Figure 3-4. EVM Configuration DIP Switch

This switch includes configuration options for the expansion board. EVM Board ID EEPROM Write Protect function and Motor Control/Boosterpack Mux selection is defined by EVM Configuration DIP Switch SW3 Bit 9 and 8, respectively, as described in Table 3-1.

Table 3-1. EVM Configuration Switch Function

Switch Name	Default Condition	Signal	Operation
SW3.8	ON	INFO_CAM_VIO_SEL	'0' (OFF) = PWM Signals connects to "Motor Control Header" '1' (ON) = PWM Signals connects to "Boosterpack Header"
SW3.9	ON	BOARDID_EEPROM_WP	Sets EVM's configuration EEPROM Write Protection '0' (OFF) = Configuration EEPROM can be updated 1' (ON) = Configuration EEPROM cannot be updated/protected

4 GESI Expansion Board Hardware Architecture

This section explains the hardware architecture of GESI expansion board in detail.

4.1 GESI Expansion Board Hardware Top Level Diagram

Figure 4-1 shows the functional block diagram of the GESI expansion board

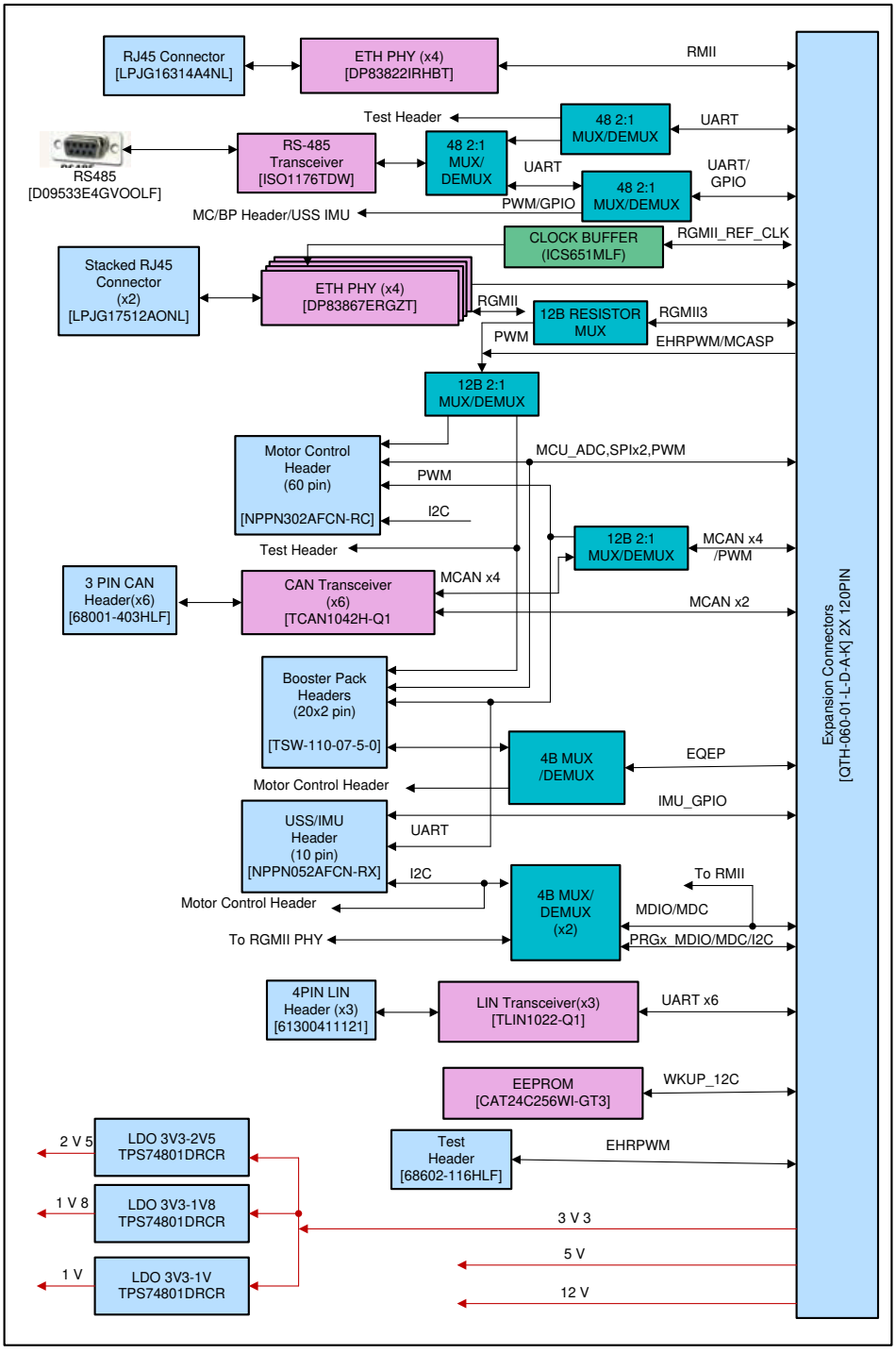


Figure 4-1. Functional Block Diagram of Infotainment Expansion Board

Few of the interfaces shown in the above diagram are specific EVM dependency. All may not be supported in all the Jacinto7 EVM.

For supported interfaces on the specific EVM platform, see Appendix A.

4.2 Expansion Connectors

There are two expansion connectors J1 and J2 (120 pin Samtec connector) for connecting it to Jacinto7 EVM Common processor board. All GESI interfaces, power and control signals are provided with these connectors.

Table 4-1 and Table 4-2 contain the pin out/signal mapping GESI expansion connectors.

Table 4-1. Pinouts of J1 Expansion Connector

Pin	Net Name	Pin	Net Name	Pin	Net Name	Pin	Net Name
1	DGND	31	PRG1_PRU1_GPO10	61	PROFI_UART_SEL/IMU_ GPIO1	91	PRG0_RGMII2_TX_ CTL
2	VCC_12V0	32	SPI6_CS1/ PRG1_PWM3_TZ_IN /PRG1_UART0_CTSn	62	NC	92	EXP_PRG1_RGMII1 _RX_CTL
3	DGND	33	SPI6_D0/PRG1_ECAP0_ SYNC_IN	63	WKUP_I2C0_SDA	93	PRG0_RGMII2_TD3
4	VCC_12V0	34	SPI6_CLK/PRG1_ECAP0_ SYNC_OUT	64	SOC_PORZ_OUT	94	EXP_PRG1_RGMII1 _RD2
5	DGND	35	NC	65	WKUP_I2C0_SCL	95	DGND
6	VCC_12V0	36	SPI6_D1/PRG1_ECAP0_IN_ APWM_OUT	66	GPIO_PRG1_RGMII_RST	96	DGND
7	PRG0_RGMII2_RXC	37	DGND	67	DGND	97	MDIO0_MDC
8	PRG1_RGMII2_TX_CTL	38	DGND	68	DGND	98	EXP_PRG0_MDIO0 _MDC
9	PRG0_RGMII2_RD3	39	PRG1_RGMII2_RD0	69	PRG0_RGMII1_RD0	99	MDIO0_MDIO
10	PRG1_RGMII2_TD3	40	EXP_PRG1_RGMII1_TD3	70	PRG0_RGMII1_TD1	100	EXP_PRG0_MDIO0 _MDIO
11	PRG0_RGMII2_RX_CTL	41	PRG1_RGMII2_RD2	71	PRG0_RGMII1_RX_CTL	101	SPI3_D0
12	PRG1_RGMII2_TXC	42	EXP_PRG1_RGMII1_TD0	72	PRG0_RGMII1_TD0	102	CAN_STB
13	PRG0_RGMII2_RD0	43	PRG1_RGMII2_RD1	73	PRG0_RGMII1_RXC	103	SPI3_D1
14	PRG1_RGMII2_TD0	44	EXP_PRG1_RGMII1_TX_CTL	74	PRG0_RGMII1_TX_CTL	104	NC
15	PRG0_RGMII2_RD1	45	PRG1_RGMII2_RD3	75	PRG0_RGMII1_RD2	105	SPI3_CLK
16	PRG1_RGMII2_TD2	46	EXP_PRG1_RGMII1_TD2	76	PRG0_RGMII1_TD3	106	RGMII_REF_ CLOCK
17	PRG0_RGMII2_RD2	47	PRG1_RGMII2_RX_CTL	77	PRG0_RGMII1_RD1	107	DGND
18	PRG1_RGMII2_TD1	48	EXP_PRG1_RGMII1_TXC	78	PRG0_RGMII1_TD2	108	DGND
19	DGND	49	PRG1_RGMII2_RXC	79	PRG0_RGMII1_RD3	109	I2C0_SCL
20	DGND	50	EXP_PRG1_RGMII1_TD1	80	PRG0_RGMII1_TXC	110	GPIO_LIN_EN
21	EXP_MCAN6_TX	51	DGND	81	DGND	111	I2C0_SDA
22	EXP_MCAN5_TX	52	DGND	82	DGND	112	SOC_I2C2_SCL
23	EXP_MCAN6_RX	53	MCAN9_TX	83	PRG0_RGMII2_TD1	113	I2C1_SCL
24	EXP_MCAN5_RX	54	EXP_PRG1_MDIO0_MDC	84	EXP_PRG1_RGMII1_RD0	114	SOC_I2C2_ SDA
25	EXP_MCAN7_TX	55	MCAN9_RX	85	PRG0_RGMII2_TD0	115	I2C1_SDA
26	EXP_MCAN4_TX	56	EXP_PRG1_MDIO0_MDIO	86	EXP_PRG1_RGMII1_RXC	116	NC
27	EXP_MCAN7_RX	57	SPI3_CS1	87	PRG0_RGMII2_TXC	117	NC
28	EXP_MCAN4_RX	58	MCAN11_TX	88	EXP_PRG1_RGMII1_RD1	118	EXP_RSTZ

Table 4-1. Pinouts of J1 Expansion Connector (continued)

Pin	Net Name	Pin	Net Name	Pin	Net Name	Pin	Net Name
29	PRG1_PRU1_GPO9	59	SPI3_CS2	89	PRG0_RGMII2_TD2	119	DGND
30	PRG1_PRU0_GPO10	60	MCAN11_RX	90	EXP_PRG1_RGMII1_RD3	120	DGND

Table 4-2. Pinouts of J2 Expansion Connector

Pin	Net Name	Pin	Net Name	Pin	Net Name	Pin	Net Name
1	DGND	31	NC	61	EHRPWM2_B	91	CON_MCU_ ADC1_AIN4
2	VCC_3V3	32	MCAN/PWM_SEL	62	RMII8_TX_EN	92	LIN4_UART_ RXD
3	DGND	33	NC	63	RMII8_PHY_RESET	93	CON_MCU_ ADC1_AIN5
4	VCC_3V3	34	MDIO_MDC_SEL0	64	RMII8_CRS_DV	94	LIN4_UART_ TXD
5	DGND	35	NC	65	NC	95	CON_MCU_ ADC1_AIN6
6	VCC_3V3	36	MDIO_MDC_SEL1	66	NC	96	LIN5_UART_ RXD
7	LIN1_UART_RXD	37	NC	67	DGND	97	CON_MCU_ ADC1_AIN7
8	I2C3_SCL	38	NC	68	DGND	98	LIN5_UART_ TXD
9	LIN1_UART_TXD	39	DGND	69	NC	99	NC
10	I2C3_SDA	40	DGND	70	NC	100	VSYS_IO_3V3
11	EQEP0_A	41	EHRPWM0_SYNCI/MCASP10_ ACLKX	71	NC	101	NC
12	EQEP0_I	42	MAIN_UART4_RTSN	72	NC	102	VSYS_IO_3V3
13	EQEP0_B	43	EHRPWM0_SYNCO/MCASP10_ AFSX	73	NC	103	MCU_ADC_ EXT_TRIGGER1
14	EQEP0_S	44	RMII8_RXD0	74	NC	104	VSYS_IO_3V3
15	PRG0_RGMII_INT#	45	EHRPWM_TZN_IN0/MCASP10_ AXR0	75	NC	105	DGND
16	NC	46	RMII8_TXD1	76	NC	106	LIN6_UART_ RXD
17	PRG1_RGMII_INT#	47	EHRPWM0_A/MCASP10_AXR1	77	DGND	107	I2C6_SCL
18	NC	48	RMII8_RXD1	78	VCC_5V0	108	LIN6_UART_ TXD
19	EEPROM_A0	49	EHRPWM0_B	79	DGND	109	I2C6_SDA
20	MUX_MC/BP_SEL	50	MAIN_UART4_TXD	80	VCC_5V0	110	Test Point
21	EEPROM_A1	51	EHRPWM1_B	81	DGND	111	NC
22	EXP_REFCLK	52	MAIN_UART4_CTSn/ IMU_GPIO0	82	VCC_5V0	112	Test Point
23	EEPROM_A2	53	EHRPWM1_A	83	CON_MCU_ADC1_AIN0	113	NC
24	NC	54	MAIN_UART4_RXD	84	LIN2_UART_RXD	114	VSYS_IO_1V8
25	EEPROM_WP	55	EHRPWM2_A	85	CON_MCU_ADC1_AIN1	115	NC
26	PRG1_IEP0_EDIO_ OUTVALID	56	RMII8_PHY_INTN	86	LIN2_UART_TXD	116	VSYS_IO_1V8
27	PRG1_PWM3_B2	57	EHRPWM_TZN_IN2	87	CON_MCU_ADC1_AIN2	117	NC
28	PERIPH_RSTZ	58	RMII8_RX_ER	88	LIN3_UART_RXD	118	VSYS_IO_1V8
29	GPIO_PRG0_RGMII_ RST	59	EHRPWM_TZN_IN1	89	CON_MCU_ADC1_AIN3	119	DGND
30	RESETSTATZ	60	RMII8_TXD0	90	LIN3_UART_TXD	120	DGND

4.3 Board ID EEPROM

The Jacinto7 EVM – GESI is identified by its version and serial number, which are stored in the onboard EEPROM. The EEPROM CAT24C256WI-GT3 is accessible on the address 0x52 on WKUP_I2C0 I2C BUS.

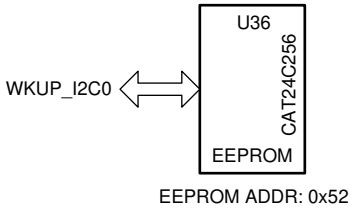


Figure 4-2. Board ID EEPROM

Table 4-3. Board ID Memory Header Information

Header	Field Name	Size (bytes)	Description	Value Written to EEPROM
	MAGIC	4	Magic Number	0xEE3355AA
	TYPE	1	Fixed length and variable position board ID header	0x1
		2	Size of payload	0xF7
BRD_ INFO	TYPE	1	payload type	0x10
	Length	2	offset to next header	0x002E
	Board_Name	16	Name of the board	“J7X-GESI-EXP”
	Design_Rev	2	Revision number of the design	Variable
	PROC_Nbr	4	PROC number	“0084”
	Variant	2	Design variant number	Variable
	PCB_Rev	2	Revision number of the PCB	Variable
	SCHBOM_Rev	2	Revision number of the schematic	Variable
	SWR_Rev	2	first software release number	Variable
	VendorID	2	Vendor ID	Variable
	Build_Week	2	week of the year of production	Variable
	Build_Year	2	year of production	Variable
	BoardID	6	Reserved. Not populated with any value	NA
	Serial_Nbr	4	incrementing board number	Variable
MAC_ADD R	TYPE	1	Payload type	0x13
	Length	2	Size of payload	0xC2
	MAC control	2	MAC header control word	0x20
	MAC_addrs	192	MAC address. Contains 5 valid MAC addresses. Four MAC addresses for RGMII ports and one MAC address for RMII port.	Variable
END_LIST	TYPE	1	End Marker	0xFE

Above board ID details will be programmed on the EEPROM from the address 0x0h.

4.4 Ethernet Interface

The Jacinto7 EVM – GESI Expansion board provides an option to the users to validate the Jacinto7 SoC's RGMII and RMII controllers.

GESI supports 4 RGMII interfaces using Four DP83867 Gigabit Ethernet. It is connected to 2x stacked RJ45 connector J20A & J20B and J21A & J21B. Default Configurations of these PHYs can be determined by Resistor Straps on configuration pins of PHY.

Table 4-4. RGMII PHY Strap Configuration

Ports	RGMII Port1	RGMII Port2	RGMII Port3	RGMII Port4
Connectors	J21A	J21B	J20A	J20B
PHY Address	00000	00011	01100	01111
Auto Negotiation	Enabled	Enabled	Enabled	Enabled
ANEGSel	10/100/1000	10/100/1000	10/100/1000	10/100/1000
RGMII Clock Skew TX	0 ns	0 ns	0 ns	0 ns
RGMII Clock Skew RX	2 ns	2 ns	2 ns	2 ns

On these RGMII PHYs either CPSWxG or Main domain RGMII interface of Jacinto7 processor can be validated by software configuration. It is specific to the processor.

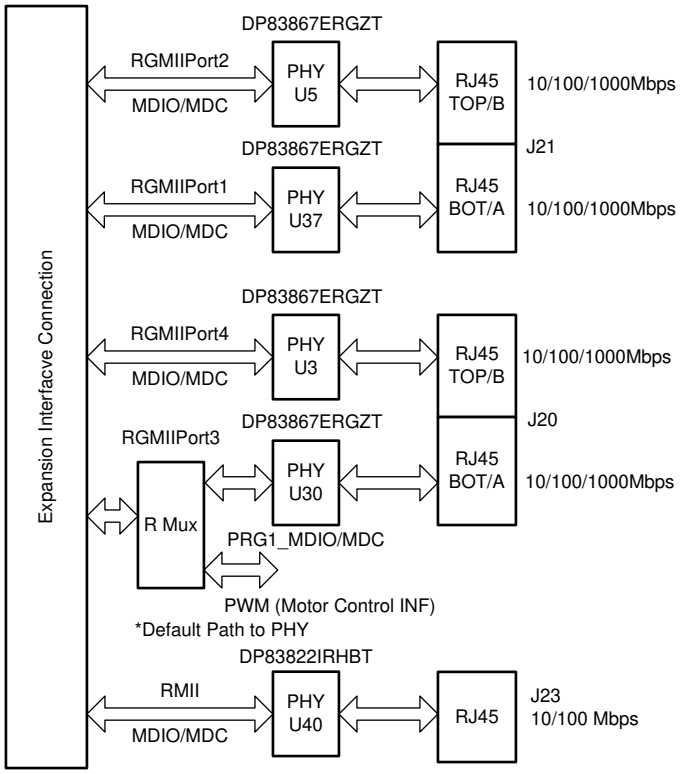


Figure 4-3. Ethernet Interface

Ethernet PHY management bus, MDIO-MDC is wired through 2:1 mux SN74CB3Q3257PWR. For Mux selection GPIO details, see Appendix B.

RMII connection of DP83822IRHBT provides a 10/100 Mbps port (J23).

4.4.1 RGMII Clocking Scheme

Reference clock for Ethernet PHY DP83867 is provided by a 25 MHz Crystal attached to the each PHY chip. Also, the system has an option to source the reference clock to the Ethernet PHY from CP Board Clock Generator with the low skew 1:4 clock buffer ICS651MLF on GESI Expansion board.

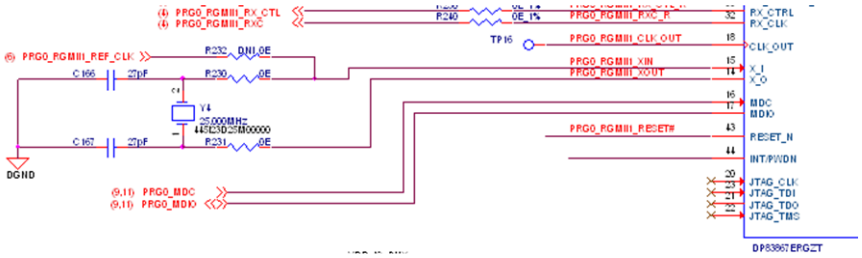


Figure 4-4. RGMII PHY Default Reference Clock Source

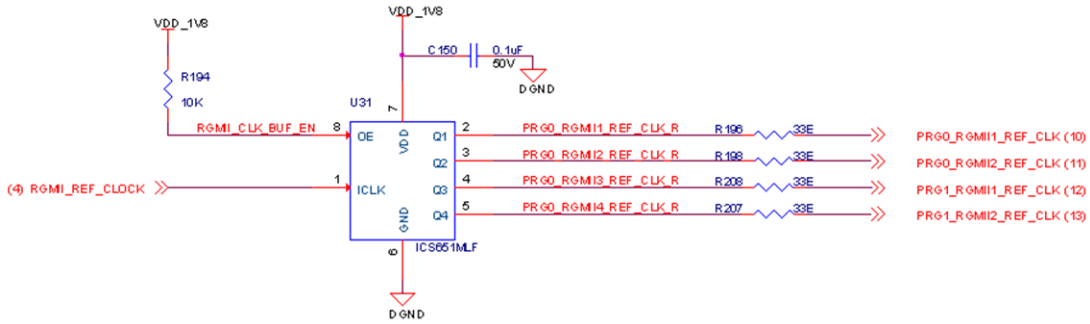


Figure 4-5. Ethernet PHY Reference Clock buffer (Optional)

4.4.2 Ethernet Port LED Indication

Table 4-5 and Table 4-6 show the LED function of the RGMII ports and RMII port RJ45 connectors.

Table 4-5. RGMII Ports LED Function

RGMII Port RJ45-LED	Function
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

Table 4-6. RMII Port LED Function

RMII PORT RJ45-LED	Function
RIGHT - GREEN	ACTIVITY
LEFT - YELLOW	100Mbps Speed

4.5 PROFI BUS / RS485

A 12-Mbps PROFIBUS port (J18 – DB9) is available in GESI board. Figure 4-6 shows the DB-9 (RS485) Connector on GESI Expansion Board.

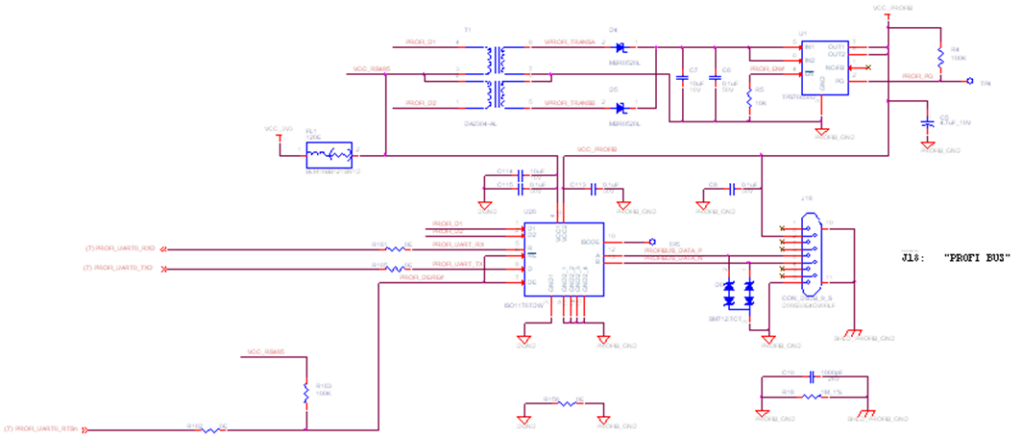


Figure 4-6. PROFIBus Interface

4.6 LIN Interface

There are six LIN interfaces present in the GESI Expansion Board (3x Dual Port LIN). A Dual pin Switch (SW2, SW3 and SW4) is provided for each LIN Port to select the mode of Corresponding LIN Port as a Slave or Master. To set the LIN port as Master CLOSE the corresponding Switch and to set LIN ports as Slave OPEN the Corresponding Switch.

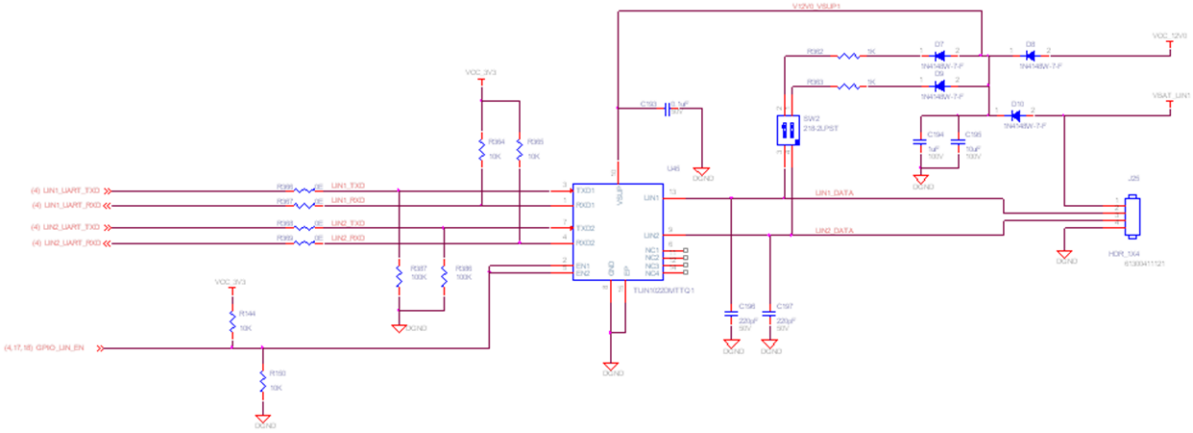


Figure 4-7. Dual Port LIN Interface

4.7 MCAN

6x MCAN ports are available in GESI board. For each port a 3-pin header has been provided. J3, J6, J8, J10, J12 and J14 are the MCAN interface connectors. Toggling CAN_STB to high keeps the MCAN ports in standby state. For specific GPIO assignment, see Appendix B.

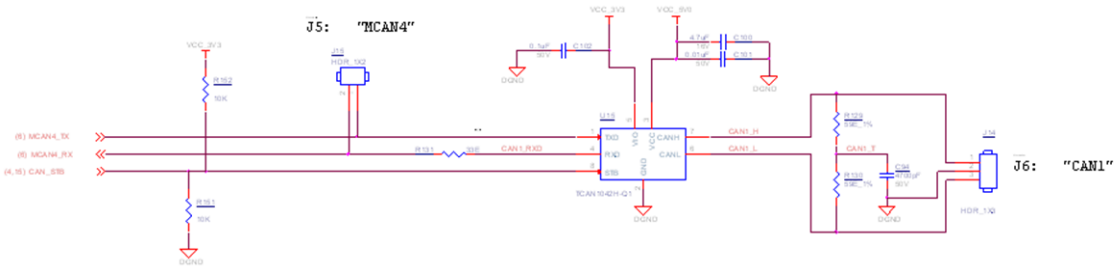


Figure 4-8. MCAN Interface

Figure 4-9 shows the MCAN Headers on GESI Expansion Board.

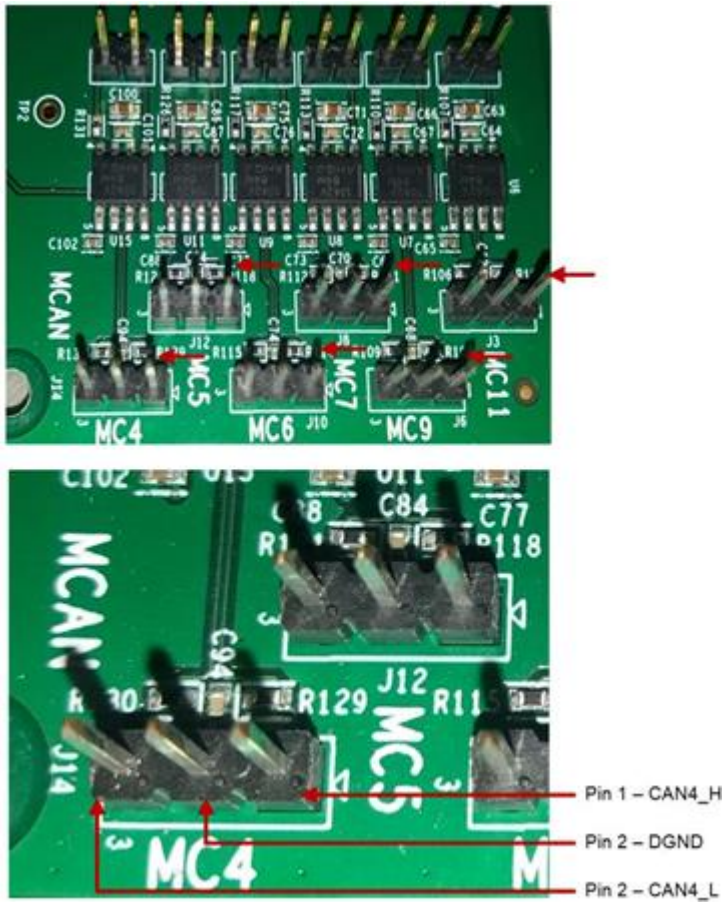


Figure 4-9. MCAN Headers

4.8 MUX Selection

4.8.1 MUX – PRGx_MDIO/MDC, CPSW9G_MDIO/MDC

J721E SoC supports common MDIO/MDC lines from CPSWxG domain and MAIN_ MDIO/MDC control to the RGMII PHYs through Mux IC U34 and U35. I2C5 interface of J721E SoC muxed with PRG0_MDIO0_MDC/ MDIO signals.

Mux channel selection is done by toggling the MDIO_MDC_SEL0 and MDIO_MDC_SEL1 signals from Jacinto7 EVM CPB IO Expander I2C0/0x20 Port 15 and 16. For more information, see Appendix B.

4.8.2 MUX – PRG1_RGMII1/PRG1_PWM

PRG1_RGMII1 and PWM signals of J721E SoC is interfaced on the GESI Expansion board using Resistor Mux as shown in Figure 4-10. J721E signals go to either Ethernet PHY or Motor Control interface on the GESI expansion board. The default path is provided to Ethernet.

Users are required to change the Resistor population option when they need to interface with Motor Control Interface (PWM).

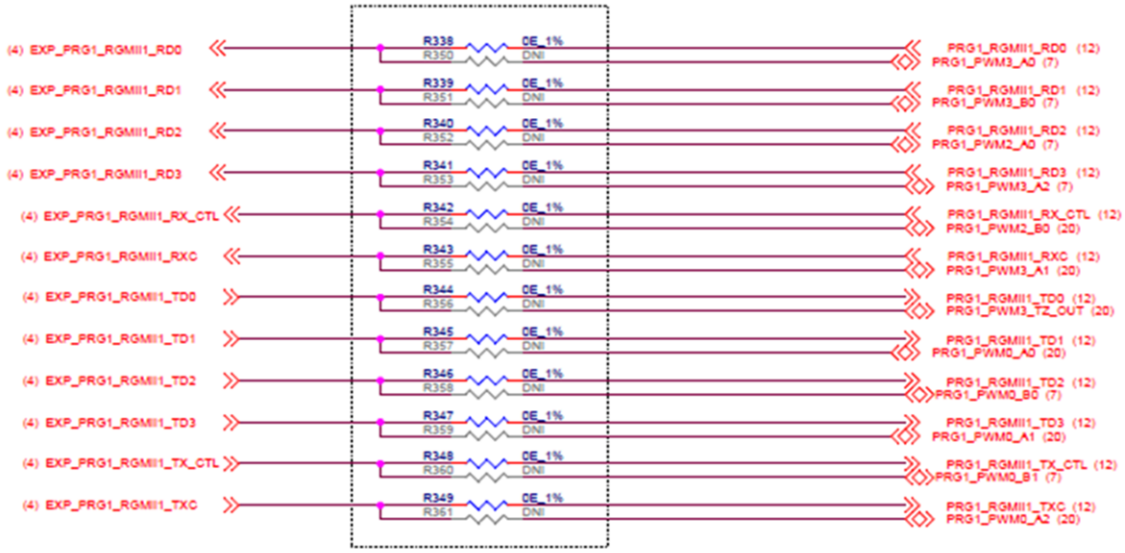


Figure 4-10. Resistor MUX for EXP_PRG1_RGMII1 Signal

4.8.3 MUX – PRG1_PWM/MCAN

EXP_MCAN [4:7] signals of J721E SoC is connected to 1:2 mux U29 on GESI. By toggling the signal MCAN/PWM_SEL from Jacinto7 EVM CPB I2C0 GPIO expander – U126, P14, the EXP_MCAN [4:7] signals either connect to MCAN interface or to Motor Control interface. For more information, see Appendix B.

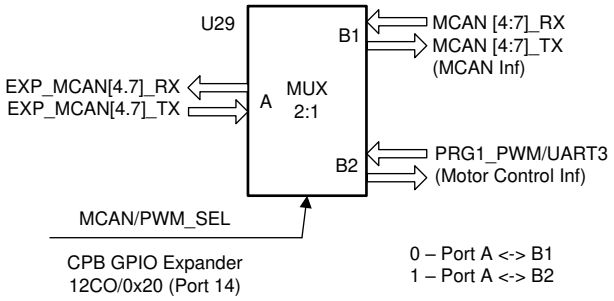


Figure 4-11. G1_PWM/MCAN Mux

4.8.4 MUX_MC/BP_SEL

Signals PRG1_PWM (output from U29) and McASP10 (from Expansion Connector) are input to 2:1 mux U41. MUX_MC/BP_SE, control signal for mux U41 connects the input signals, either to Motor Control interface or to Booster pack interface. MUX_MC/BP_SE is set high or low by Jacinto7 EVM CP Board Configuration Switch SW3 position 8.

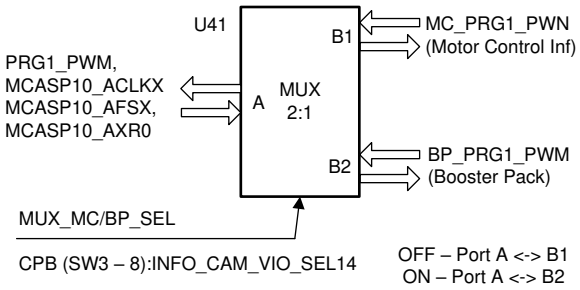


Figure 4-12. MC_PRG1_PWM/BP_PRG1_PWM Mux

4.9 GESI LaunchPad-Booster Pack Interface

A GESI Launchpad connectors (J5 and J16) provided in GESI board to interface with Boosterpack modules. BoosterPack plug-in modules shall be plugged in to extend the functionality like wireless connectivity, capacitive touch, temperature sensing, displays and much more. Table 4-7 contains the pin out details of both connectors.

Except BOOST-DRV8848, all other BP interfaces listed below are supported similar to Maxwell EVM:

- BOOSTXL-ULN2003
- BOOST-DRV8711
- BOOSTXL-DRV8301
- CC3100BOOST
- BOOST-CC2564MODA

For resistor population option to support specific Boosterpack module, see Figure 4-13.

Table 4-7. Pinouts of Booster Pack Interfacing Connectors

J16 – LHS			J5 – RHS		
Pin	**Net Name**	**Function**	**Pin**	**Net Name**	**Function**
1	VCC_3V3_BP		1	BP_PRG1_PWM3_A0	PWM/GPIO
2	VCC_5V0_BP		2	DGND	
3	MCU_ADC1_AIN7	GPIO/ADC_IN	3	BP_PRG1_PWM3_B0	PWM/GPIO
4	DGND		4	SPI3_CS1	GPIO/SPI_CS
5	BP/MC_PRG1_UART0_RXD	GPIO/UART_RXD	5	BP_PRG1_PWM3_A2	PWM/GPIO
6	MCU_ADC1_AIN0	ADC_IN	6	SPI3_CS2	GPIO/SPI_CS
7	BP/MC_PRG1_UART0_TXD	GPIO/UART_TXD	7	PRG1_PWM2_B1	PWM/UART_RTS
8	MCU_ADC1_AIN1	ADC_IN	8	NC	
9	BP_GPIO2	GPIO	9	BP_PRG1_PWM3_B1	PWM/UART_CTS
10	MCU_ADC1_AIN2	ADC_IN	10	PERIPH_RSTz	RESET
11	UART3_RX	GPIO/UART_RXD	11	BP_PRG1_PWM0_B0	PWM/GPIO
12	MCU_ADC1_AIN3	ADC_IN	12	SPI3_D0	SPI_MOSI
13	SPI3_CLK	SPI_CLK/UART_TXD	13	UART3_RTSn	UART_RTS
14	MCU_ADC1_AIN4	ADC_IN/I2S_WCLK	14	SPI3_D1	SPI_MISO
15	BP_GPIO3	GPIO	15	UART3_CTSn	UART_CTS
16	MCU_ADC1_AIN5	ADC_IN/I2S_BCLK	16	BP_PRG1_PWM0_B1	GPIO/PWM
17	BP_PRG1_PWM2_A0	PWM/GPIO	17	NC	
18	MCU_ADC1_AIN6	ADC_IN/I2S_DOUT	18	BP_PRG1_PWM0_B2	GPIO/PWM
19	BP_PRG1_PWM2_A1	PWM/GPIO	19	NC	
20	BP_MCASP10_AXR1	I2S_DIN	20	BP_GPIO4	GPIO

Figure 4-13 shows the BoosterPack headers on GESI Expansion Board.

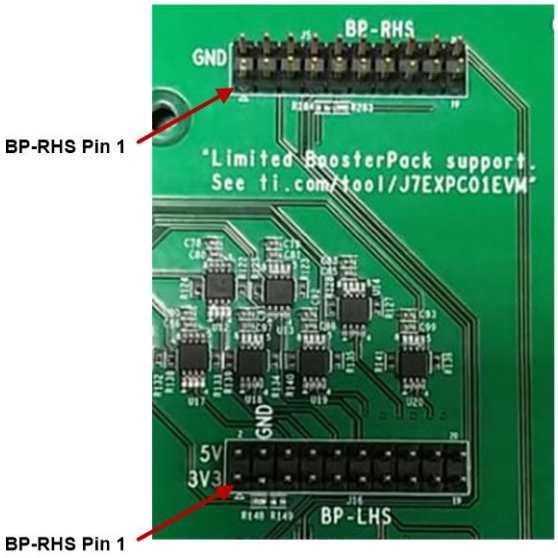


Figure 4-13. BoosterPack Headers

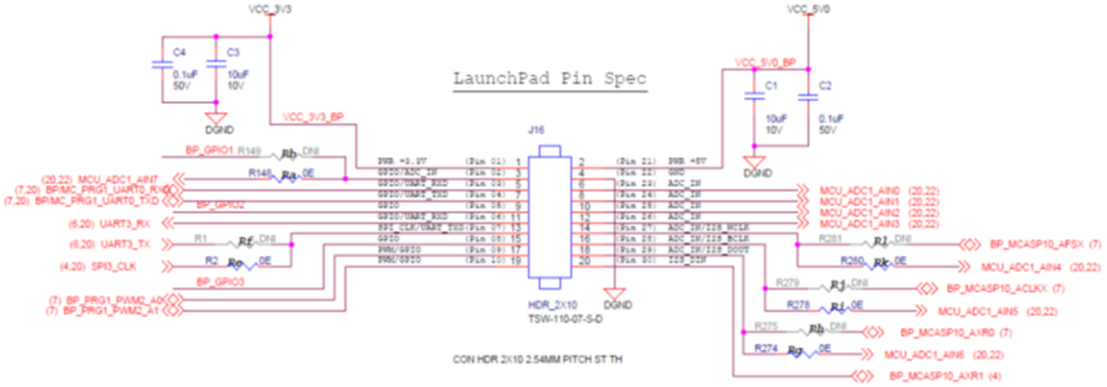


Figure 4-14. BoosterPack I/F LHS Headers

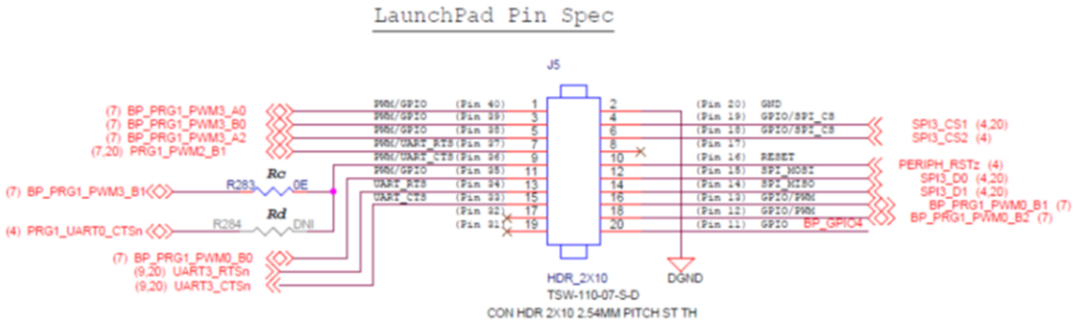


Figure 4-15. BoosterPack I/F RHS Headers

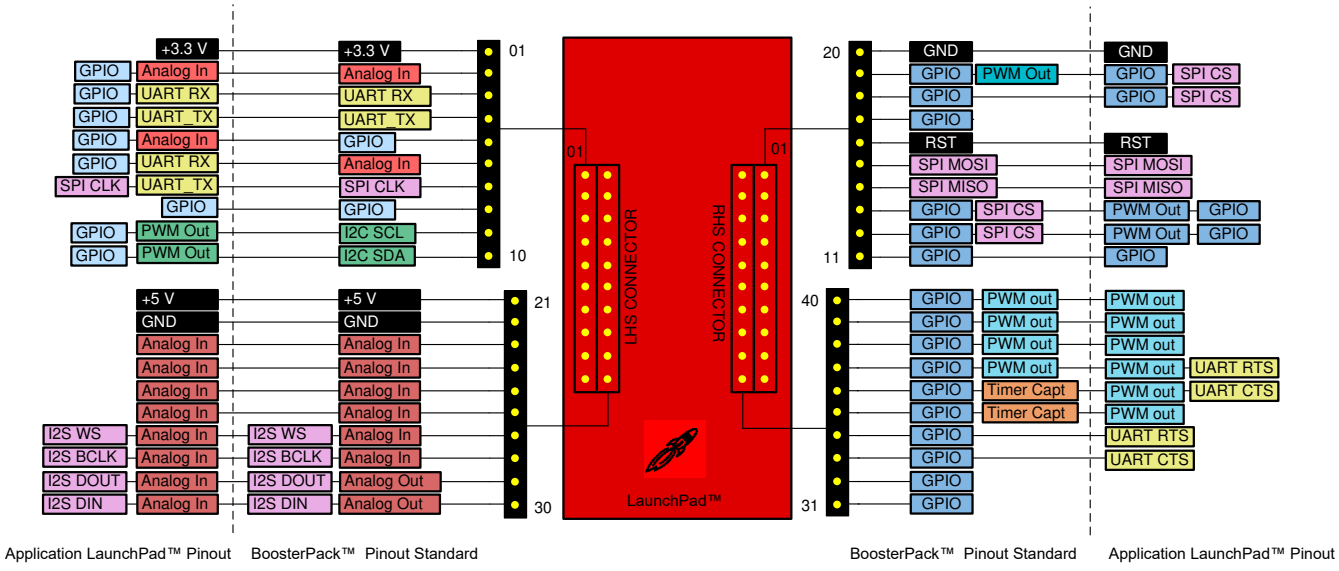


Figure 4-16. GESI launchpad-Booster Pack Pinout

4.10 Motor Control Interface

Motor control interface signals are terminated to 2x30 pin female connector. Figure 4-17 shows the Motor Control Header on GESI Expansion Board.

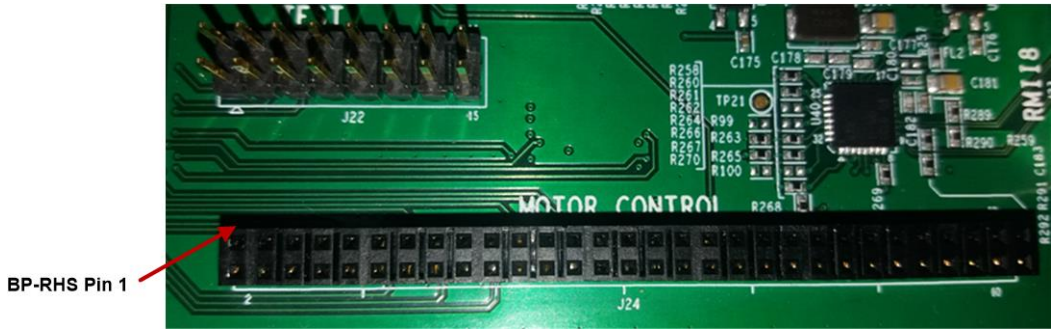


Figure 4-17. Motor Control Header

Table 4-8 contains the Pin Out details of motor Control Header.

Table 4-8. Pin Outs of J24 (Motor Control Header) Connector

J24 Connector Pin Outs			
Pin	**Net Name**	**Pin**	**Net Name**
1	VCC_3V3	31	NC
2	VCC_5V0	32	NC
3	SPI3_CS1	33	NC
4	PRG1_PWM0_A0	34	NC
5	MC_PRG1_PWM0_B0	35	NC
6	PRG1_PWM0_A1	36	SPI6_D1/PRG1_ECAP0_IN_APWM_OUT
7	MC_PRG1_PWM0_B1	37	BP/MC_PRG1_UART0_TXD
8	PRG1_PWM0_A2	38	PRG1_PWM3_B2
9	PRG1_PRU1_GPO5	39	DGND
10	PRG1_PWM0_TZ_OUT	40	DGND
11	PRG1_PWM0_TZ_IN	41	PRG1_IEP0_EDIO_OUTVALID
12	MC_PRG1_PWM0_B2	42	MC_EQEP0_I
13	MC_PRG1_PWM2_A1	43	NC
14	SPI6_D0/PRG1_ECAP0_SYNC_IN	44	MC_EQEP0_S
15	PRG1_PWM3_TZ_OUT	45	NC
16	MC_PRG1_PWM3_B1	46	MC_EQEP0_A
17	PRG1_PWM3_A1	47	I2C5_SCL
18	SPI6_CLK/PRG1_ECAP0_SYNC_OUT	48	MC_EQEP0_B
19	PRG1_PWM2_B0	49	MCU_ADC1_AIN7
20	MC_PRG1_PWM3_A2	50	I2C5_SDA
21	MC_PRG1_PWM2_A0	51	MCU_ADC1_AIN0
22	DGND	52	MCU_ADC1_AIN6
23	MC_PRG1_PWM3_B0	53	MCU_ADC1_AIN1
24	SPI3_CLK	54	MCU_ADC1_AIN5
25	MC_PRG1_PWM3_A0	55	MCU_ADC1_AIN2
26	SPI3_D0	56	MCU_ADC1_AIN4
27	BP/MC_PRG1_UART0_RXD	57	MCU_ADC1_AIN3
28	SPI3_D1	58	MCU_ADC_EXT_TRIGGER1
29	PRG1_PWM2_B1	59	DGND

Table 4-8. Pin Outs of J24 (Motor Control Header) Connector (continued)

J24 Connector Pin Outs			
Pin	**Net Name**	**Pin**	**Net Name**
30	SPI6_CS1/PRG1_PWM3_TZ_IN	60	DGND

4.11 USS/IMU Header

Table 4-9 contains the pin out details of USS/IMU header. USS/IMU Header on GESI Expansion Board is shown in Figure 4-18.

Table 4-9. Pin Outs of J19 (USS/IMU Header) Connector

Pin outs of J19	
Pin	**Net Name**
1	I2C5_SDA
2	UART3_TX
3	I2C5_SCL
4	UART3_RX
5	DGND
6	DGND
7	IMU_GPIO0
8	UART3_RTSn
9	IMU_GPIO1
10	UART3_CTSn

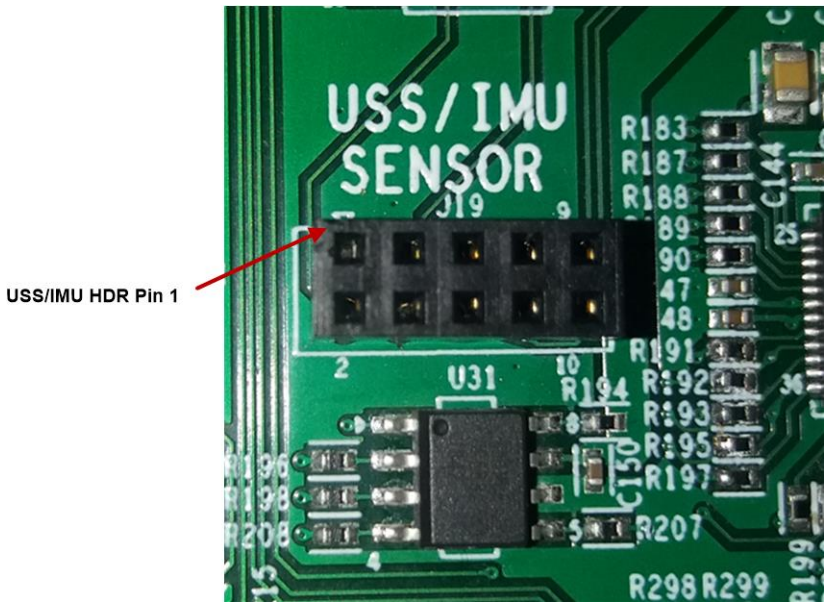


Figure 4-18. USS/IMU Header

4.12 Test Header

Table 4-10 contains the pin out details of Test header. Test Header on GESI Board is shown in Figure 4-19.

Table 4-10. Pin Outs of J22 (Test Header) Connector

J22 Connector Pin Outs			
Pin	**Net Name**	**Pin**	**Net Name**
1	TH_EHRPWM0_SYNCI	9	EHRPWM0_B
2	EHRPWM1_B	10	EHRPWM_TZn_IN2
3	TH_EHRPWM0_SYNCO	11	EHRPWM1_A
4	EHRPWM_TZn_IN1	12	TH_UART4_RTSn
5	TH_EHRPWM_TZn_IN0	13	TH_UART4_TXD
6	EHRPWM2_A	14	TH_UART4_RXD
7	EHRPWM0_A	15	TH_UART4_CTSn
8	EHRPWM2_B	16	DGND

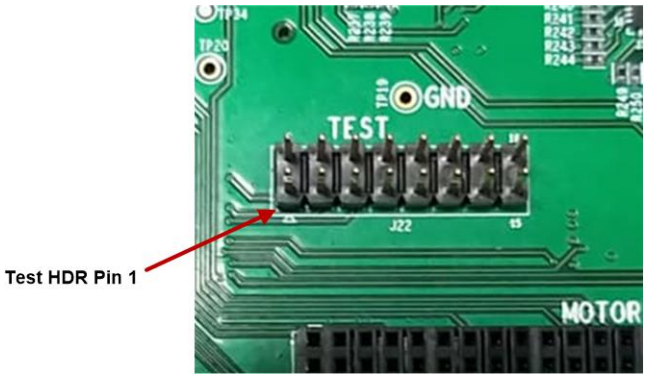


Figure 4-19. Test Header

A Interface Mapping

J721E EVM & J7VCL EVM Interface Mapping on GESI Expansion is provided in Table A-1.

Table A-1. Interface Mapping (1)

GESI Peripheral	GESI Interface	J721E Connectivity	J7200 Connectivity
RGMII Port 1 (U37, J21 Bottom)	RGMII Port (Net name PRG0_RGMII1_*)	RGMII3 / PRG0_RMGII1	RGMII2
	MDIO (Net name PRG0_M*)	(see mux selection) MDIO0 or PRG0_MDIO	MDIO0
RGMII Port 2 (U5, J21 Top)	RGMII Port (Net name PRG0_RGMII2_*)	RGMII4 /PRG0_RGMII2	<not supported>
	MDIO (Net name PRG0_M*)	(see mux selection) MDIO0 or PRG0_MDIO	<not supported>
RGMII Port 3 (U30, J20 Bottom)	RGMII Port (Net name PRG1_RGMII1_*)	RGMII1 / PRG1_RMGII1	<not supported>
	MDIO (Net name PRG1_M*)	(see mux selection) MDIO0 or PRG1_MDIO	<not supported>
RGMII Port 4 (U3, J20 Top)	RGMII Port (Net name PRG1_RGMII2_*)	RGMII8 /PRG1_RGMII2	<not supported>
	MDIO (Net name PRG1_M*)	(see mux selection) MDIO0 or PRG1_MDIO	<not supported>
RMII Port (U40, J23)	RMII (Net name RMII8_*)	RMII8	<not supported>
	MDIO (Net name MDIO0_M*)	MDIO0	<not supported>
CAN Port 1(U15, J14)	CAN (Net name MCAN4_*)	MCAN4	MCAN4
CAN Port 2(U11, J12)	CAN (Net name MCAN5_*)	MCAN5	MCAN5
CAN Port 3(U9, J10)	CAN (Net name MCAN6_*)	MCAN6	MCAN6
CAN Port 4 (U8, J8)	CAN (Net name MCAN7_*)	MCAN7	MCAN7
CAN Port 5 (U7, J6)	CAN (Net name MCAN9_*)	MCAN9	MCAN8
CAN Port 6 (U6, J3)	CAN (Net name MCAN11_*)	MCAN11	MCAN10
LIN Port 1 (U45, J25)	UART (Net name LIN1_UART_*)	UART8	UART5
LIN Port 2 (U45, J25)	UART (Net name LIN2_UART_*)	<not supported>	UART6
LIN Port 3 (U46, J26)	UART (Net name LIN3_UART_*)	<not supported>	UART9
LIN Port 4 (U46, J26)	UART (Net name LIN4_UART_*)	<not supported>	UART3
LIN Port 5 (U47, J27)	UART (Net name LIN5_UART_*)	<not supported>	UART7
LIN Port 6 (U47, J27)	UART (Net name LIN6_UART_*)	<not supported>	UART1
Config EEPROM(U36)	I2C0 (Net name WKUP_I2C0_*)	WKUP_I2C0	WKUP_I2C0
ProfiBus(U26, J18)	UART (Net Name MAIN_UART4_*)	(see mux selection) UART4 Or PRG1_UART0	UART3
USS/IMU Header (J19)	UART4 (Net name UART3_*)	UART3	<not supported>
	I2C5 (Net name I2C5_*)	(see mux selection) I2C5	<not supported>
BoosterPack Header (J5, J16)	UART3 (Net name UART3_*)	UART3	<not supported>
	SPI3 (Net name SPI3_*)	SPI3	<not supported>
Test Connector (J22)	UART4(Net Name MAIN_UART4_*)	(see mux selection) UART4 Or PRG1_UART0	<not supported>
Motor Control Header (J24)	I2C5(Net name I2C5_*)	(see mux selection) I2C5	<not supported>
	SPI3(Net name SPI3_*)	SPI3	<not supported>
	SPI6(Net name SPI6_*)	SPI6	<not supported>

(1) Header and expansion interfaces can support a variety of modes and signals for testing and interfacing to external components. All supported modes are not documented in Table B-1. To determine the complete list of supported signals/interfaces, see device DM and EVM schematics.

B GESI Board GPIO Mapping

GESI GPIO mapping is shown in Table B-1.

Table B-1. GPIO Mapping (1)

GESI Peripheral	Peripheral I/O	Direction (for SoC)	Default	Active State	J721E Connectivity	J7VCL Connectivity
RGMII Port 1, Port2	Interrupt	Input	PU (2)	Active Low	GPIO1_23	GPIO0_27
	Reset	Output	PU	Active Low	GPIO0_61	GPIO0_28
RGMII Port 1, Port2	Interrupt	Input	PU	Active Low	GPIO1_24	<not supported >
	Reset	Output	PU	Active Low	GPIO0_62	Pulled down
RMII Port	Interrupt	Input	PU	Active Low	GPIO0_104	N/A
	Reset	Output	PU	Active Low	GPIO0_96	N/A
CAN Bus (All Ports)	Standby	Output	PD	Active Low	GPIO0_60	IO Expander P7,(I2C0: 0X21 on SOM)
LIN Bus (All Ports)	Enable	Output	PD	Active High	GPIO0_68	IO Expander P6,(I2C0: 0X21 on SOM)
IMU Sensor Header	IMU_GPIO0	I/O	NA	NA	GPIO0_105	N/A
	IMU_GPIO1	I/O	NA	NA	GPIO0_48	N/A
Boosterpack Header	BP_GPIO1	I/O	NA	NA	GPIO1_0	N/A
	BP_GPIO2	I/O	NA	NA	GPIO0_127	N/A
	BP_GPIO3	I/O	NA	NA	GPIO0_123	N/A
	BP_GPIO4	I/O	NA	NA	GPIO0_124	N/A
MCAN/PWM Mux	Select	Output	PD	‘0’ – MCAN ‘1’ - PWM	I2C0 (0x20), P14	I2C0 (0x20), P14
MDIO PRG0 Mux	Select	Output	PU	‘0’ – PRG0_MDIO ‘1’ – MDIO, I2C5	I2C0 (0x20), P15	I2C0 (0x20), P15
MDIO PRG1 Mux	Select	Output	PU	‘0’ – PRG1_MDIO ‘1’ – MDIO, UART3	I2C0 (0x20), P16	I2C0 (0x20), P16

(1) Header and expansion interfaces can support a variety of modes and signals for testing and interfacing to external components. All supported GPIO are not documented in Table B-1. To determine the complete list of supported signals/GPIO, see device-specific DM and EVM schematics.

(2) ‘PU’ refers to default state of Pull-up. ‘PD’ refers to default state of Pull-down.

C I2C Address Mapping

Table C-1 provides the complete I2C address mapping details on GESI Expansion.

Table C-1. J7ES EVM – GESI Expansion I2C Table

I2C Bus	Device/Function	Part Ref#	I2C Address
WKUP_I2C0	Board ID EEPROM	U36	0x52
SoC_I2C5	USS/IMU Sensor control Header	J19 (RECP_2X5)	TBD
SoC_I2C5	Motor Control Header	J24 (RECP_30X2)	TBD
I2C0	Reserved	TP60, TP61	NA
I2C1	Reserved	TP25, TP26	NA
I2C2	Reserved	TP22, TP23	NA
I2C3	Reserved	TP34, TP35	NA
I2C6	Reserved	TP31, TP32	NA

D Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2020) to Revision B (November 2020) **Page**

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