TMS320C6410/C6413/C6418 DSP Inter-Integrated Circuit (I2C) Module

Addendum to TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide

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Preface

Read This First

About This Manual

This addendum, to be used in conjunction with the *TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU175), describes the additional features of the inter-integrated circuit (I2C) module included in the TMS320C6410, TMS320C6413, and TMS320C6418 digital signal processors (DSPs) of the TMS320C6000™ DSP family. These features include general-purpose input/output (GPIO) capability for the I2C pins, and new interrupts and status bits.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide (literature number SPRU175) describes the I2C module that provides an interface between a TMS320C6000™ digital signal processor (DSP) and any I^2C-bus-compatible device that connects by way of an I^2C bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the C6000™ DSP through the I2C module. This document assumes the reader is familiar with the I^2C-bus specification.

TMS320C6000 CPU and Instruction Set Reference Guide (literature number SPRU189) describes the TMS320C6000™ CPU architecture, instruction set, pipeline, and interrupts for these digital signal processors.

TMS320C6000 DSP Peripherals Overview Reference Guide (literature number SPRU190) describes the peripherals available on the TMS320C6000™ DSPs.

TMS320C64x Technical Overview (SPRU395) gives an introduction to the TMS320C64x™ DSP and discusses the application areas that are enhanced by the TMS320C64x VelociTI™.

TMS320C6000 Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code for the TMS320C6000™ DSPs and includes application program examples.

TMS320C6000 Code Composer Studio Tutorial (literature number SPRU301) introduces the Code Composer Studio™ integrated development environment and software tools.

Code Composer Studio Application Programming Interface Reference Guide (literature number SPRU321) describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

TMS320C6x Peripheral Support Library Programmer's Reference (literature number SPRU273) describes the contents of the TMS320C6000™ peripheral support library of functions and macros. It lists functions and macros both by header file and alphabetically, provides a complete description of each, and gives code examples to show how they are used.

TMS320C6000 Chip Support Library API Reference Guide (literature number SPRU401) describes a set of application programming interfaces (APIs) used to configure and control the on-chip peripherals.

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Inter-Integrated Circuit (I2C) Module

This addendum to the *TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU175) describes the additional features of the inter-integrated circuit (I2C) module included in the TMS320C6410, TMS320C6413, and TMS320C6418 digital signal processors (DSPs) of the TMS320C6000™ DSP family. These features include general-purpose input/output (GPIO) capability for the I2C pins, and new interrupts and status bits.

The inter-integrated circuit (I2C) module provides an interface between a C6000™ DSP and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus) specification version 2.1 and connected by way of an I^2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the C6000 DSP through the I2C module. To determine whether a particular C6000 DSP has an I2C module, see your device-specific datasheet.

1 Features

The I2C module of the C6410/C6413/C6418 DSP offers the following additional features:

- The SDA and SCL pins can be used for general-purpose input/output (GPIO) through the use of six additional registers:
  - I2C pin function register (I2CPFUNC)
  - I2C pin direction register (I2CPDIR)
  - I2C pin data input register (I2CPDIN)
  - I2C pin data output register (I2CPDOUT)
  - I2C pin data set register (I2CPDSET)
  - I2C pin data clear register (I2CPDCLR)
- Two additional status bits in the I2C status register (I2CSTR):
  - Slave direction (SDIR) bit
  - Stop condition detected (SCD) bit
- Two additional interrupts enabled in the I2C interrupt enable register (I2CIER):
  - Addressed as slave (AAS) interrupt
  - Stop condition detected (SCD) interrupt

- Two different ways to generate a transmit data ready interrupt when operating in slave-transmitter mode and enabled by the I2C extended mode register (I2CEMDR):
  - When the master requests more data by sending an acknowledge signal after the transmission of the last data.
  - When the data in I2CDXR is copied to I2CXSR.

2 Transmit Data Ready Interrupt/DMA Event Generation

The C6410/C6413/C6418 DSP generates the transmit data ready interrupt in two different ways when operating in slave-transmitter mode through the use of the transmit data ready interrupt mode (XRDYM) bit in the I2C extended mode register (I2CEMDR). The I2C module enters slave-transmitter mode, if the slave address transmitted on the I2C bus is the same as its own address (in I2COAR) and the master has transmitted R/$\overline{W}$ = 1. After the I2C has entered slave-transmitter mode, it generates transmit data ready interrupts (if enabled in I2CIER) to the CPU and DMA events based on the setting specified through the XRDYM bit.

When XRDYM = 1, the first transmit data ready interrupt and event are generated after the I2C module has recognized its slave address and R/$\overline{W}$ was transmitted as 1 by the master device. All subsequent transmit data ready interrupts and events are generated when the data in the data transmit register (I2CDXR) is copied to the transmit shift register (I2CXSR). The I2C module keeps copying data from I2CDXR to I2CXSR as long as the master keeps generating acknowledge signals to request more data. Figure 1 shows the operation of the transmit data ready interrupt when XRDYM = 1.

When the XRDYM = 0, the first transmit data ready interrupt and event are generated after the I2C module has recognized its slave address and R/$\overline{W}$ was transmitted as 1 by the master device. All subsequent transmit data ready interrupts and events are generated when the master generates an acknowledge signal to request more data. Figure 2 shows the operation of the transmit data ready interrupt when XRDYM = 0.

The XRDYM bit only has an effect when the I2C module is operating in slave-transmitter mode.

Code Compatibility

Devices other than the C6410/C6413/C6418 DSP operate as if the XRDYM bit is set to 1. Clearing the XRDYM bit to 0 may have an undesired effect when porting I2C module code from other devices. The XRDYM bit should remain as 1 when code compatibility is desired.

Figure 1. Interrupt Generation When XRDYM = 1

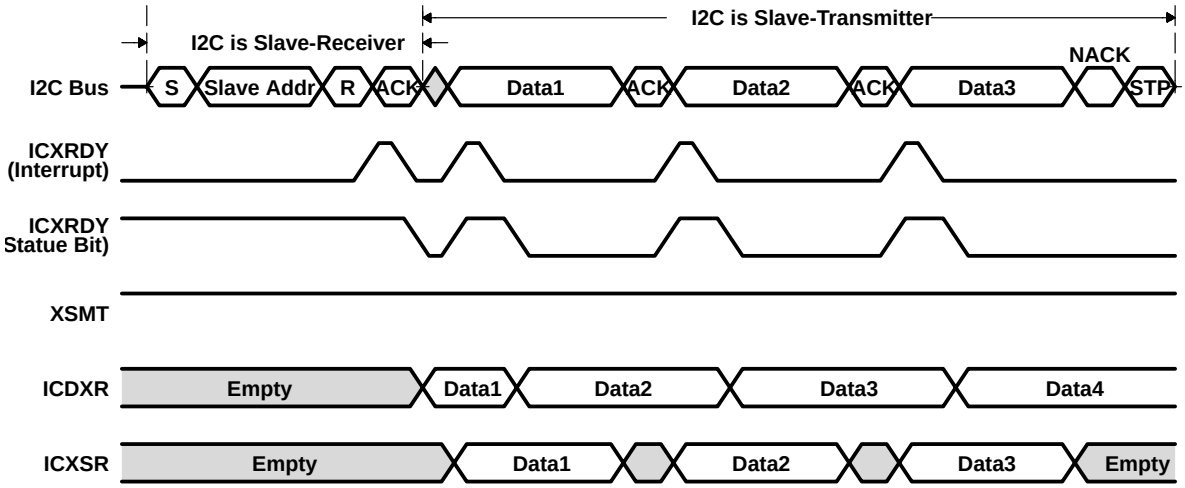
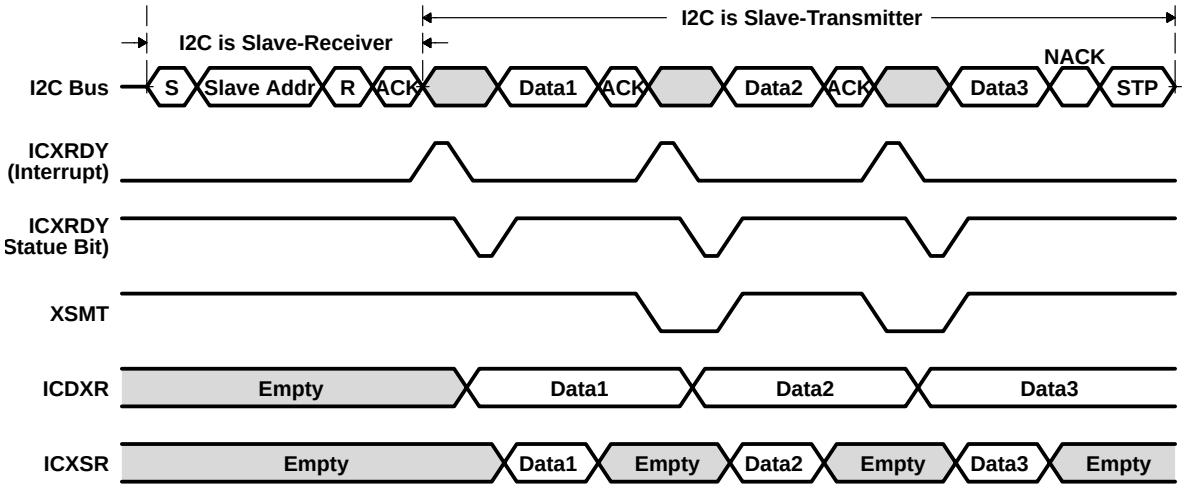


Figure 2. Interrupt Generation When XRDYM = 0



3 GPIO Pin Control

The SDA and SCL pins of the I2C module can be used for general-purpose input/output (GPIO). To use the GPIO mode of the I2C pins:

1) Place the I2C module in reset by clearing the IRS bit to 0 in the I2C mode register (I2CMDR).

2) Enable the GPIO mode by setting the GPMODE bit to 1 in the I2C pin function register (I2CPFUNC).

Some DSPs may require pullup resistors on the SDA and SCL pins in order to use the GPIO mode. See your device-specific datasheet to determine if pullup resistors are necessary for your DSP.

4 Registers

Table 1 lists the I2C module registers. All but the data registers (I2CRSR and I2CXSR) are accessible to the CPU. Only the additional registers available on the C6410/C6413/C6418 DSP are described in this section. For a description of all the other registers, see *TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU175). See the device-specific datasheet for the memory address of these registers.

Table 1. I2C Module Registers

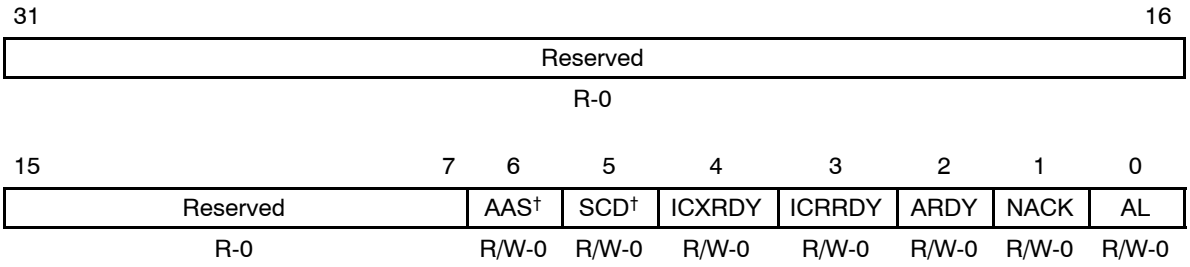
Acronym	Register Name	Address Offset (hex)	Section
I2COAR	I2C own address register	00	—
I2CIER	I2C interrupt enable register	04	4.1
I2CSTR	I2C status register	08	4.2
I2CCLKL	I2C clock low-time divider register	0C	—
I2CCLKH	I2C clock high-time divider register	10	—
I2CCNT	I2C data count register	14	—
I2CDRR	I2C data receive register	18	—
I2CSAR	I2C slave address register	1C	—
I2CDXR	I2C data transmit register	20	—
I2CMDR	I2C mode register	24	—
I2CISRC	I2C interrupt source register	28	—
I2CEMDR†	I2C extended mode register	2C	4.3
I2CPSC	I2C prescaler register	30	—
I2CPID1	I2C peripheral identification register 1	34	—
I2CPID2	I2C peripheral identification register 2	38	—
I2CPFUNC†	I2C pin function register	48	4.4
I2CPDIR†	I2C pin direction register	4C	4.5
I2CPDIN†	I2C pin data input register	50	4.6
I2CPDOUT†	I2C pin data output register	54	4.7
I2CPDSET†	I2C pin data set register	58	4.8
I2CPDCLR†	I2C pin data clear register	5C	4.9
I2CRSR	I2C receive shift register (not accessible to the CPU or EDMA)	—	—
I2CXSR	I2C transmit shift register (not accessible to the CPU or EDMA)	—	—

† Available only on C6410/C6413/C6418 DSP.

4.1 I2C Interrupt Enable Register (I2CIER)

The I2C interrupt enable register (I2CIER) is used by the CPU to individually enable or disable I2C interrupt requests. The I2CIER is shown in Figure 3. The two additional bits on the C6410/C6413/C6418 DSP, AAS and SCD, are described in Table 2. For a description of all the other bits, see *TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU175).

Figure 3. I2C Interrupt Enable Register (I2CIER)



Legend: R = Read only; R/W = Read/write; *-n* = value after reset
† Available only on C6410/C6413/C6418 DSP, reserved on all other devices.

Table 2. I2C Interrupt Enable Register (I2CIER) Field Descriptions

Bit	*field*†	*symval*†	Value	Description
31–7	Reserved	–	0	These reserved bit locations are always read as 0. A value written to this field has no effect.
6	AAS	OF(*value*)		Address as slave interrupt enable bit.
		DEFAULT MSK	0	Interrupt request is disabled.
		UNMSK	1	Interrupt request is enabled.
5	SCD	OF(*value*)		Stop condition detected interrupt enable bit.
		DEFAULT MSK	0	Interrupt request is disabled.
		UNMSK	1	Interrupt request is enabled.
4–0				See *TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU175).

† For CSL C macro implementation, use the notation I2C_I2CIER_*field_symval*

4.2 I2C Status Register (I2CSTR)

The I2C status register (I2CSTR) is used by the CPU to determine which interrupt has occurred and to read status information. The I2CSTR is shown in Figure 4. The two additional bits on the C6410/C6413/C6418 DSP, SDIR and SCD, are described in Table 3. For a description of all the other bits, see *TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU175).

Figure 4. I2C Status Register (I2CSTR)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8
Reserved	SDIR†	NACKSNT	BB	RSFULL	XSMT	AAS	AD0
R-0	R/W1C-0	R/W1C-0	R/W1C-0	R-0	R-1	R-0	R-0

7	6	5	4	3	2	1	0
Reserved		SCD†	ICXRDY	ICRRDY	ARDY	NACK	AL
R-0		R/W-0	R/W1C-1	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0

Legend: R = Read; W1C = Write 1 to clear (writing 0 has no effect); -*n* = value after reset
† Available only on C6410/C6413/C6418 DSP, reserved on all other devices.

Table 3. I2C Status Register (I2CSTR) Field Descriptions

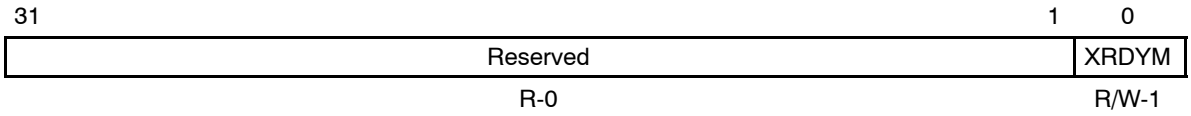
Bit	*field*†	*symval*†	Value	Description
31–15	Reserved	–	0	These reserved bit locations are always read as 0. A value written to this field has no effect.
14	SDIR	OF(*value*)		Slave direction bit. In digital-loopback mode, the SDIR bit is cleared to 0.
		DEFAULT NONE	0	I2C module is acting as a master-transmitter/receiver or a slave-receiver. SDIR is cleared by any one of the following events: ❑ A STOP or a START condition. ❑ SDIR is manually cleared. To clear this bit, write a 1 to it.
		INT CLR	1	I2C module is acting as a slave-transmitter.
13–8				See *TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU175).
7–6	Reserved	–	0	These reserved bit locations are always read as 0. A value written to this field has no effect.
5	SCD	OF(*value*)		Stop condition detected bit. SCD indicates when a STOP condition has been detected on the I2C bus. The STOP condition could be generated by the I2C module or by another I2C device connected to the bus.
		DEFAULT NONE	0	No STOP condition has been detected. SCD is cleared by any one of the following events: ❑ By reading INCODE bits in I2CICR as 110b. ❑ SCD is manually cleared. To clear this bit, write a 1 to it.
		INT CLR	1	A STOP condition has been detected.
4–0				See *TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU175).

† For CSL C macro implementation, use the notation I2C_I2CSTR_*field_symval*

4.3 I2C Extended Mode Register (I2CEMDR)

The I2C extended mode register (I2CEMDR) is used to indicate which condition generates a transmit data ready interrupt. The I2CEMDR is shown in Figure 5 and described in Table 4.

Figure 5. I2C Extended Mode Register (I2CEMDR)



Legend: R = Read only; R/W = Read/write; -*n* = value after reset

Table 4. I2C Extended Mode Register (I2CEMDR) Field Descriptions

Bit	Field	*symval*†	Value	Description
31–1	Reserved	–	0	These reserved bit locations are always read as 0. A value written to this field has no effect.
0	XRDYM	OF(*value*)		Transmit data ready interrupt mode bit. Determines which condition generates a transmit data ready interrupt. The XRDYM bit only has an effect when the I2C module is operating as a slave-transmitter.
		MSTACK	0	The transmit data ready interrupt is generated when the master requests more data by sending an acknowledge signal after the transmission of the last data.
		DEFAULT DXRCPY	1	The transmit data ready interrupt is generated when the data in I2CDXR is copied to I2CXSR.

† For CSL C macro implementation, use the notation I2C_I2CEMDR_XRDYM_*symval*

4.4 I2C Pin Function Register (I2CPFUNC)

The I2C pin function register (I2CPFUNC) selects the SDA and SCL pins as GPIO. The I2CPFUNC is shown in Figure 6 and described in Table 5.

Figure 6. I2C Pin Function Register (I2CPFUNC)

31	1	0
Reserved		GPMODE
R-0		R/W-0

Legend: R = Read only; R/W = Read/write; -*n* = value after reset

Table 5. I2C Pin Function Register (I2CPFUNC) Field Descriptions

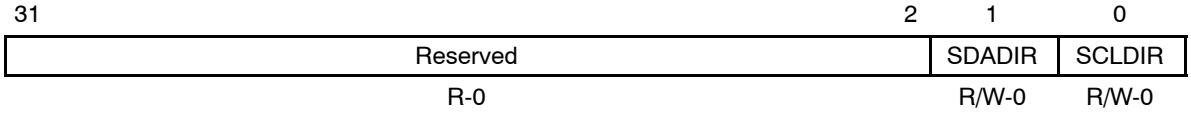
Bit	Field	*symval*†	Value	Description
31–1	Reserved	–	0	These reserved bit locations have an indeterminate value when read. A value written to this field has no effect.
0	GPMODE	OF(*value*)		GPIO mode enable bit for SCL and SDA pins. The I2C module must be placed in reset (IRS = 0 in I2CMDR) before enabling the GPIO function of the SCL and SDA pins.
		DEFAULT DISABLED	0	GPIO mode is disabled; SCL and SDA pins have I2C functionality.
		ENABLED	1	GPIO mode is enabled; SCL and SDA pins have GPIO functionality.

† For CSL C macro implementation, use the notation I2C_I2CPFUNC_GPMODE_*symval*

4.5 I2C Pin Direction Register (I2CPDIR)

The I2C pin direction register (I2CPDIR) controls the direction of the SDA and SCL pins. The I2CPDIR is shown in Figure 7 and described in Table 6. If a bit is set to 1, the pin functions as an output; if a bit is cleared to 0, the pin functions as an input.

Figure 7. I2C Pin Direction Register (I2CPDIR)



Legend: R = Read only; R/W = Read/write; -*n* = value after reset

Table 6. I2C Pin Direction Register (I2CPDIR) Field Descriptions

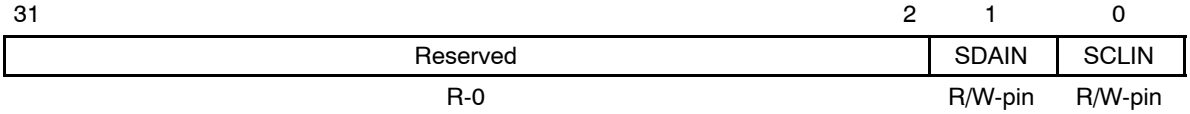
Bit	*field*†	*symval*†	Value	Description
31–2	Reserved	–	0	These reserved bit locations have an indeterminate value when read. A value written to this field has no effect.
1	SDADIR	OF(*value*)		SDA direction bit. Controls the direction of the SDA pin when configured as GPIO.
		DEFAULT	0	SDA pin functions as input.
		INPUT		
		OUTPUT	1	SDA pin functions as output.
0	SCLDIR	OF(*value*)		SCL direction bit. Controls the direction of the SCL pin when configured as GPIO.
		DEFAULT	0	SCL pin functions as input.
		INPUT		
		OUTPUT	1	SCL pin functions as output.

† For CSL C macro implementation, use the notation I2C_I2CPDIR_*field_symval*

4.6 I2C Pin Data Input Register (I2CPDIN)

The I2C pin data input register (I2CPDIN) reflects the state of the SDA and SCL pins. The I2CPDIN is shown in Figure 8 and described in Table 7. When read, I2CPDIN returns the value from the pin's input buffer regardless of the state of the corresponding I2CPFUNC or I2CPDIR bits.

Figure 8. I2C Pin Data Input Register (I2CPDIN)



Legend: R = Read only; R/W = Read/write; -*n* = value after reset;-pin = external pin value after reset

Table 7. I2C Pin Data Input Register (I2CPDIN) Field Descriptions

Bit	*field*†	*symval*†	Value	Description
31–2	Reserved	–	0	These reserved bit locations have an indeterminate value when read. A value written to this field has no effect.
1	SDAIN	OF(*value*)		Indicates the logic level present on the SDA pin. SDAIN is set regardless of the GPMODE setting. A value written to this bit has no effect.
		LOW	0	A logic low is present at the SDA pin.
		HIGH	1	A logic high is present at the SDA pin.
0	SCLIN	OF(*value*)		Indicates the logic level present on the SCL pin. SCLIN is set regardless of the GPMODE setting. A value written to this bit has no effect.
		LOW	0	A logic low is present at the SCL pin.
		HIGH	1	A logic high is present at the SCL pin.

† For CSL C macro implementation, use the notation I2C_I2CPDIN_*field_symval*

4.7 I2C Pin Data Output Register (I2CPDOUT)

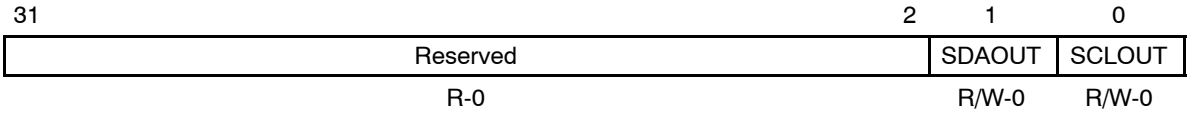
The I2C pin data output register (I2CPDOUT) determines the value driven on the SDA and SCL pins, if the pin is configured as an output. The I2CPDOUT is shown in Figure 9 and described in Table 8. Writes do not affect pins not configured as GPIO outputs.

The I2CPDOUT bits are set or cleared by writing to this register directly. A read of I2CPDOUT returns the value of the register not the value at the pin (that might be configured as an input). An alternative way to set bits in I2CPDOUT is to write a 1 to the corresponding bit of I2CPDSET. An alternative way to clear bits in I2CPDOUT is to write a 1 to the corresponding bit of I2CPDCLR.

I2CPDOUT has these aliases:

- I2CPDSET — writing a 1 to a bit in I2CPDSET sets the corresponding bit in I2CPDOUT to 1; writing a 0 has no effect and keeps the bits in I2CPDOUT unchanged.
- I2CPDCLR — writing a 1 to a bit in I2CPDCLR clears the corresponding bit in I2CPDOUT to 0; writing a 0 has no effect and keeps the bits in I2CPDOUT unchanged.

Figure 9. I2C Pin Data Output Register (I2CPDOUT)



Legend: R = Read only; R/W = Read/write; -*n* = value after reset

Table 8. I2C Pin Data Output Register (I2CPDOUT) Field Descriptions

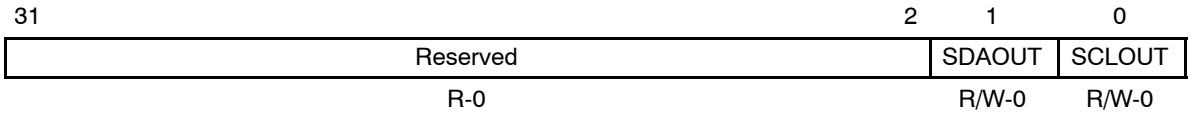
Bit	*field*†	*symval*†	Value	Description
31–2	Reserved	_	0	These reserved bit locations have an indeterminate value when read. A value written to this field has no effect.
1	SDAOUT	OF(*value*)		Controls the value driven on the SDA pin when the pin is configured as an output (GPIO mode must be enabled by setting GPMODE = 1). When reading data, returns the value in the SDAOUT bit, does not return the level on the pin. When writing data, writes to the SDAOUT bit.
		DEFAULT LOW	0	SDA pin is driven to a logic low.
		HIGH	1	SDA pin is driven to a logic high.
0	SCLOUT	OF(*value*)		Controls the value driven on the SCL pin when the pin is configured as an output (GPIO mode must be enabled by setting GPMODE = 1). When reading data, returns the value in the SCLOUT bit, does not return the level on the pin. When writing data, writes to the SCLOUT bit.
		DEFAULT LOW	0	SCL pin is driven to a logic low.
		HIGH	1	SCL pin is driven to a logic high.

† For CSL C macro implementation, use the notation I2C_I2CPDOUT_*field_symval*

4.8 I2C Pin Data Set Register (I2CPDSET)

The I2C pin data set register (I2CPDSET) is shown in Figure 10 and described in Table 9. I2CPDSET is an alias of the I2C pin data output register (I2CPDOUT) for writes only and provides an alternate means of driving GPIO outputs high. Writing a 1 to a bit of I2CPDSET sets the corresponding bit in I2CPDOUT. Writing a 0 has no effect. Register reads are indeterminate.

Figure 10. I2C Pin Data Set Register (I2CPDSET)



Legend: R = Read only; R/W = Read/write; -*n* = value after reset

Table 9. I2C Pin Data Set Register (I2CPDSET) Field Descriptions

Bit	*field*†	*symval*†	Value	Description
31–2	Reserved	_	0	These reserved bit locations have an indeterminate value when read. A value written to this field has no effect.
1	SDAOUT	OF(*value*)		Sets the value of the SDAOUT bit in I2CPDOUT. A write of 0 to this bit has no effect. This bit location has an indeterminate value when read.
		DEFAULT UNCHGN	0	No effect.
		SET	1	Sets the SDAOUT bit in I2CPDOUT to 1.
0	SCLOUT	OF(*value*)		Sets the value of the SCLOUT bit in I2CPDOUT. A write of 0 to this bit has no effect. This bit location has an indeterminate value when read.
		DEFAULT UNCHGN	0	No effect.
		SET	1	Sets the SCLOUT bit in I2CPDOUT to 1.

† For CSL C macro implementation, use the notation I2C_I2CPDSET_*field_symval*

4.9 I2C Pin Data Clear Register (I2CPDCLR)

The I2C pin data clear register (I2CPDCLR) is shown in Figure 11 and described in Table 10. I2CPDCLR is an alias of the I2C pin data output register (I2CPDOUT) for writes only and provides an alternate means of driving GPIO outputs low. Writing a 1 to a bit of I2CPDCLR clears the corresponding bit in I2CPDOUT. Writing a 0 has no effect. Register reads are indeterminate.

Figure 11. I2C Pin Data Clear Register (I2CPDCLR)

31	2	1	0
Reserved		SDAOUT	SCLOUT
R-0		R/W-0	R/W-0

Legend: R = Read only; R/W = Read/write; -*n* = value after reset

Table 10. I2C Pin Data Clear Register (I2CPDCLR) Field Descriptions

Bit	*field*†	*symval*†	Value	Description
31–2	Reserved	_	0	These reserved bit locations have an indeterminate value when read. A value written to this field has no effect.
1	SDAOUT	OF(*value*)		Clears the value of the SDAOUT bit in I2CPDOUT. A write of 0 to this bit has no effect. This bit location has an indeterminate value when read.
		DEFAULT UNCHGN	0	No effect.
		CLR	1	Clears the SDAOUT bit in I2CPDOUT to 0.
0	SCLOUT	OF(*value*)		Clears the value of the SCLOUT bit in I2CPDOUT. A write of 0 to this bit has no effect. This bit location has an indeterminate value when read.
		DEFAULT UNCHGN	0	No effect.
		CLR	1	Clears the SCLOUT bit in I2CPDOUT to 0.

† For CSL C macro implementation, use the notation I2C_I2CPDCLR_*field_symval*

Revision History

Table 11 lists the changes made since the previous version of this document.

Table 11. Document Revision History

Page	Additions/Modifications/Deletions
All	Added C6418 to document.
12–22	Updated symbolic values (*symval*) of the bits in Table 2 through Table 10.

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