Technical Article

SoC Power Design: 3 Steps to a Thermally Optimized Power Supply

Kelvin Odom

This year marks the 35th anniversary of the Applied Power Electronics Conference (APEC). It's a perfect reason to take a trip down memory lane when it comes to power-supply design for system-on-chip (SoC) applications, such as communication base stations, test and measurement equipment or data centers.

While designing thermally optimized power supplies has never been an easy task, the power requirements of modern SoCs have made doing so increasingly challenging. When the first integrated field-effect transistor (FET) buck converters hit the market about 20 years ago, they sought to solve a major challenge emerging in the industry: the need to supply increasing amounts of power at point of load in an increasingly limited amount of board space.

Tackling that challenge is still a top priority, but today's power designers also face trends that make managing thermals even more critical: continually rising SoC power requirements, higher ambient temperatures and higher converter switching frequencies. If your power-supply design doesn't adequately account for these constraints, you run the risk that it won't be able to supply the power you need. Here are three steps you can take to ensure your power supply adequately addresses the needs of your SoC.

1. Understand your processor's power needs.

Reducing solution size and external component count has always been a goal for power designers. Integrating FETs into the package with a buck controller is one good way to do that, and the industry has continued to use this approach to increase power density in the face of rising SoC power requirements. Because of this trend, selecting a converter that's properly rated for your application need is especially critical.

There are many heuristics that you can use to determine if a converter's power rating will fit your application need, but a good place to start is to understand the power loss at the current level where you'll use the converter. Figure 1 is a power-loss curve for the TPS546D24A, a buck converter rated for 40-A output current. Since this converter's package has a large ground pad and its integrated FETs have low $R_{DS(on)}$, its power loss is relatively low, even at a high output current. Carefully considering the power loss under your load condition for any device you're designing with is a good way to ensure that your converter is properly derated to match the application's thermal environment.

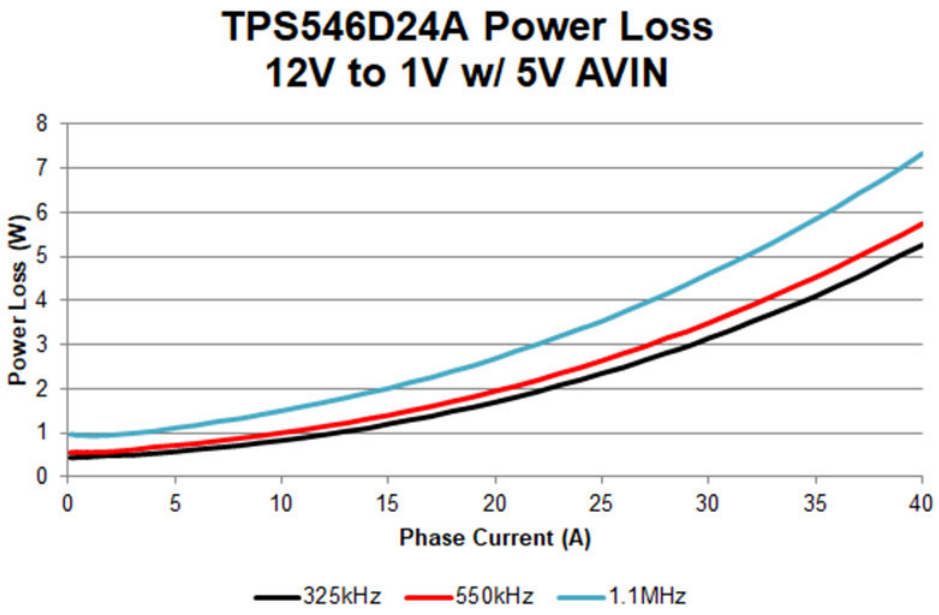

Figure 1. TPS546D24A power loss

2. Ensure that your design can handle higher temperatures.

Using a buck converter with high power loss can be especially problematic in applications with higher ambient temperatures (T_A). To tackle this challenge, TI has developed converter solutions that can operate over a wider range of temperatures, typically specified as a maximum junction temperature (T_J). Consider the increasingly common condition where the environment in which your device will be operating is at 60°C or greater. In this condition, it doesn't take much power loss for a traditional 105°C T_J-rated buck converter to enter thermal shutdown.

While efficiency or power-loss curves can be a helpful starting point, to understand the true operating range of your power supply, ask to see its safe operating area (SOA) curves. For the TPS546D24A, these curves are shown in Figure 2. SOA curves are a good way to understand what power level your converter can realistically deliver over its full operating lifetime based on the ambient temperature in which it will be operating.

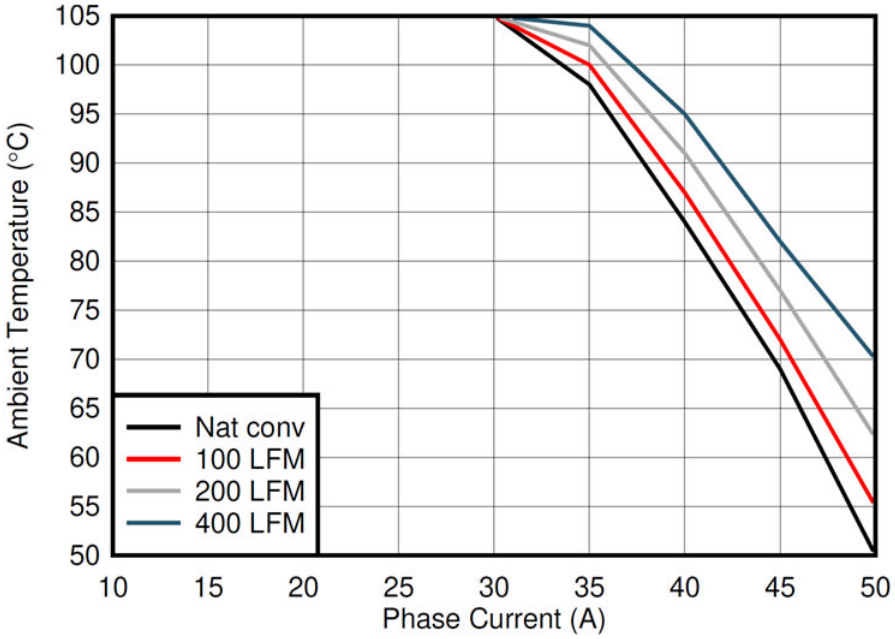

Figure 2. TPS546D24A SOA curves

3. Balance the benefits and drawbacks of high switching frequency operation.

The correlation between higher switching frequency (F_{SW}), higher switching losses and higher total power loss is well understood, but requirements for smaller solution size and faster transient response have pushed more power designers to accept lower-efficiency power solutions. One major factor contributing to this are the power requirements of common processor core rails, which may only allow a total output-voltage deviation of a few percent over changes in line voltage, load voltage and operating temperature. Switching to converters with a higher F_{SW} will allow your design to react more quickly to voltage transients and regulate them more effectively. This principle has driven many power designers to use converters that can switch at frequencies above 1 MHz, even for very high-power applications. Ultimately, the value of operating your converter at a high F_{SW} will depend on your specific application conditions, but choosing a device with a resistor-adjustable or pin-selectable F_{SW} will enable the greatest flexibility for tackling thermal challenges in the face of shifting load requirements.

These are just a few of many considerations when designing a point-of-load power solution, but keeping these in mind when choosing power devices will make optimizing the thermal performance of your applications much more manageable.

Additional resources:

- For further reading on the correlation between F_{SW} and solution size/efficiency, see “Choosing the optimum switching frequency of your DC/DC converter.”
- To learn more about safe operating area, read the application report, “Method of Graphing Safe Operating Area Curves in DC/DC Converters.”

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265