TPS659108 User Guide For i.MX508

This document can be used as a reference for connectivity between the TPS659108 power-management integrated circuit (PMIC) and the Freescale i.MX508.

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1 Introduction

This document can be used as a reference for connectivity between the TPS659108 PMIC and the Freescale i.MX508. For information about the power resources or the functionality of the device, see the device data sheet. For information about Freescale processors, see the official information from Freescale.

2 Platform Connection

Figure 1 shows the power supply connections between TPS659108 and i.MX508.

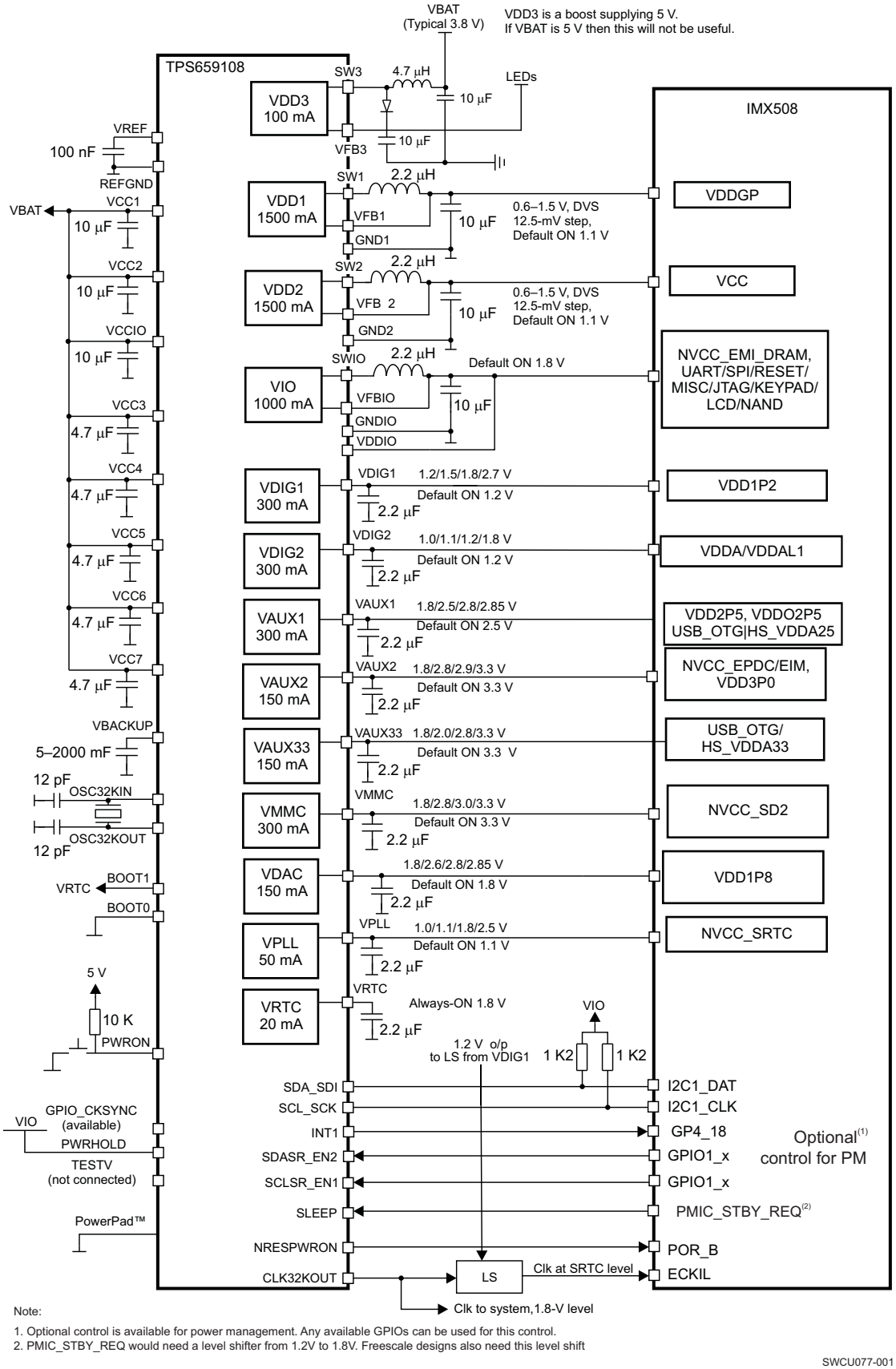

Figure 1. i.MX508 Power Supply Connections With TPS659108

3 Power-Up Sequencing

Table 1 lists the power domain mapping along with the current and voltage specifications.

Table 1. Power Domain Mapping

Sequence	i.MX508	Current Rating (mA)	Voltage Rating (V)	TPS659108	Current (mA)	Voltage (V)	Comments
3	VDDGP	1250	0.8–1.05	VDD1	1500	1.1	
2	VCC	400	1– 1.175	VDD2	1500	1.1	
3	VDDA/VDDAL1	250	1.15–1.27	VDIG2	300	1.2	
5	NVCC_EMI_DRAM, UART/SPI/RESET/MISC/JTAG/KEYPAD/LCD/NAND	55	1.8	VIO	1000	1.8	
3	NVCC_EPDC/EIM	10	2.7–3.3	VAUX2	300	3.3	
1	NVCC_SRTC	10	1.1–1.3	VPLL	50	1.1	
3	VDD3P0	10	2.7–3.3	VAUX2	300	3.3	
4	VDD2P5	10	2.38–2.62	VAUX1	300	2.5	
6	VDD1P8	10	1.75–1.95	VDAC	150	1.8	
7	VDD1P2	10	1.15–1.35	VDIG1	300	1.2	
4	VDDO2P5	150	2.38–2.63	VAUX1	300	2.5	
	Out of power-up sequence						
	USB_OTG_VDDA33	8	3–3.6	VAUX33			
	USB_OTG_VDDA25	25	2.25–2.75				
	USB_H1_VDDA33	8	3–3.6	VAUX33			
	USB_H1_VDDA25	25	2.25–2.75				
	NVCC_SD2	2.7 - 3.3	205	VMCC	300	3.3	
	NVCC_SD1						

Figure 2 shows the TPS659108 power-up sequence for the i.MX508.

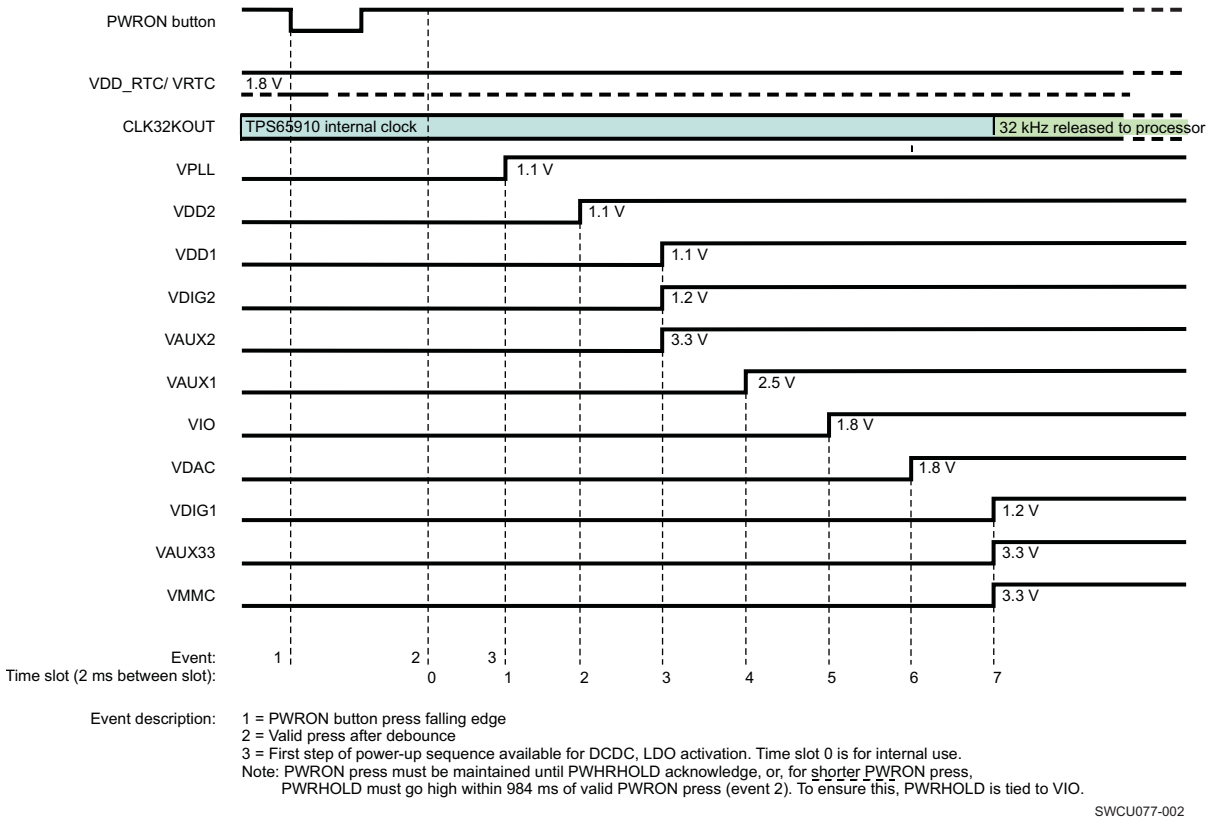

Figure 2. TPS659108 Power-Up Sequence for i.MX508

Table 1 describes the EEPROM values for TPS659108 and the EEPROM setup defining the power-up sequence for the power rails.

Table 2. EEPROM Configuration for TPS659108

Register	Bit	Description	Option Selected
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.1 V
VDD1_REG	VGAIN_SEL	VDD1 gain selection (x1 or x2)	x1
EEPROM		VDD1 time slot selection	3
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG/VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.1 V
VDD2_REG	VGAIN_SEL	VDD2 gain selection (x1 or x3)	x1
EEPROM		VDD2 time slot selection	2
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	5
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled
EEPROM		VDD3 time slot	0
VDIG1_REG	SEL	LDO voltage selection	1.2 V
EEPROM		LDO time slot	7
VDIG2_REG	SEL	LDO voltage selection	1.2 V
EEPROM		LDO time slot	3
VDAC_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	6

Table 2. EEPROM Configuration for TPS659108 (continued)

Register	Bit	Description	Option Selected
VPLL_REG	SEL	LDO voltage selection	1.1
EEPROM		LDO time slot	1
VAUX1_REG	SEL	LDO voltage selection	2.5 V
EEPROM		LDO time slot	4
VMMC_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	7
VAUX33_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	7
VAUX2_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	3
CLK32KOUT pin		CLK32KOUT time slot	7
NRESPWRON pin		NRESPWRON time slot	7+1
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO is in low-power mode during OFF state. 1 = VRC LDO is in full-power mode during OFF state.	Low-power mode
DEVCTRL_REG	RTC_PWDN	0 = RTC is in normal power mode. 1 = Clock gating of RTC register and logic (low-power mode)	1
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is the crystal/external clock. 1 = Clock source is the internal RC oscillator.	Crystal (0)
DEVCTRL2_REG	TSLOT_LENGTH	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	2 ms
DEVCTRL2_REG	IT_POL	0 = INT1 signal is active low. 1 = INT1 signal is active high.	Active low
INT_MSK_REG	VMBHI_IT_MSK	0 = Device automatically switches on at NOSUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = Start-up reason is required before switch on.	0
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	3 V

4 Getting Started With TPS659108 (Basic Software Information)

4.1 First Initialization

4.1.1 I/O Polarity/Muxing Configuration

Program the DEVCTRL2_REG.SLEEPSIG_POL register based on the GPIO signal from the processor. This can be set to active low or active high for SLEEP transition. Software configuration allows specific power resources to enter low consumption state.

Set DEVCTRL_REG.DEV_SLP = 1 to allow SLEEP transition when requested.

Update the GPIO0 configuration (GPIO0_REG) as desired.

4.1.2 Define Wakeup/Interrupt Event (SLEEP or OFF)

Select the appropriate bits in the INT_MSK_REG and INT_MSK2_REG registers to activate an interrupt to the processor on the INT1 line.

4.1.3 Backup Battery Configuration

If a backup battery is used, set BBCH_REG[BBCHEN] = 1 to enable backup battery charging. The maximum voltage can be set by the backup battery specifications (BBSEL).

4.1.4 DCDC and Voltage Scaling Resource Configuration

Configure two operating voltages for DCDC1 and DCDC2:

- VDDx_OP_REG.SEL= roof voltage (Enx ball High)
- VDDx_SR_REG.SEL = floor voltage (Enx ball Low)

Assign control of DCDC1 to SCLSR_EN1 and DCDC2 to SCLSR_EN2:

- Set EN1_SMPS_ASS_REG.VDD1_EN1 = 1.
- Set EN2_SMPS_ASS_REG.VDD2_EN2 = 1.
- Set SLEEP_KEEP_RES_ON_REG.VDD2_KEEPON = 1 (allows low-power mode).
- Set SLEEP_KEEP_RES_ON_REG.VDD1_KEEPON = 1 (allows low-power mode).

4.1.5 Sleep Platform Configuration

Configure the state of LDOs when the SLEEP signal is used. By default, all resources go to SLEEP state. In SLEEP state the LDO voltage is maintained but transient and load capability is reduced.

Resources that provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG register.

Resources that can be set off in SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG register.

NOTE: VDD3P0, VDD2P5, and USB_OTG/H1_VDDA25 should be off.

4.2 Event Management Through Interrupt

4.2.1 INT_STS_REG.VMBHI_IT

INT_STS_REG.VMBHI_IT indicates that the supply (VBAT) is connected. Leaving BACKUP or NO SUPPLY state, the system must be initialized (see Section 4.1, *First Initialization*).

4.2.2 INT_STS_REG.PWRON_IT

INT_STS_REG.PWRON_IT is triggered by pressing the PWRON button. If the device is in OFF or SLEEP state, then this acts as a wake-up event and resources are reinitialized.

4.2.3 INT_STS_REG.PWRON_LP_IT

INT_STS_REG.PWRON_LP_IT is the PWRON long-press interrupt and is generated when the PWRON switch is pressed for 6 seconds. The application processor can decide to acknowledge the interrupt. If this interrupt is not acknowledged in the next 2 seconds, then the device interprets this as a power-down event.

4.2.4 INT_STS_REG.HOTDIE_IT

INT_STS_REG.HOTDIE_IT indicates that the temperature of die is reaching the limit. Software must decrease the power consumption before automatic shutdown.

4.2.5 INT_STS_REG.VMBDCH_IT

INT_STS_REG.VMBDCH_IT indicates that the input supply is low and the processor must prepare to shut down to avoid losing data.

This interrupt is linked to VBAT but is not applicable in a system in which PMIC is connected to 5-V rails and not connected directly to VBAT.

4.2.6 INT_STS2_REG.GPIO_R/F_IT

INT_STS2_REG.GPIO_R/F_IT can be used to wake up the device from SLEEP state. This interrupt event can come from any peripheral or similar device. This wake-up event is not valid for a transition from OFF state.

4.2.7 INT_STS_REG.RTC_ALARM_IT

INT_STS_REG.RTC_ALARM_IT is triggered when the RTC alarm set time is reached.

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