# TPS659114 for Freescale i.MX6 Dual/Quad User's Guide

## 1 Introduction

This document is an application note describing the EEPROM configuration and the power-up sequence of the TPS659114 power-management integrated circuit (PMIC). For details of the PMIC features and performance, refer to the full specification document TPS65911 data manual (SWCS049).

## 2 Platform Connection

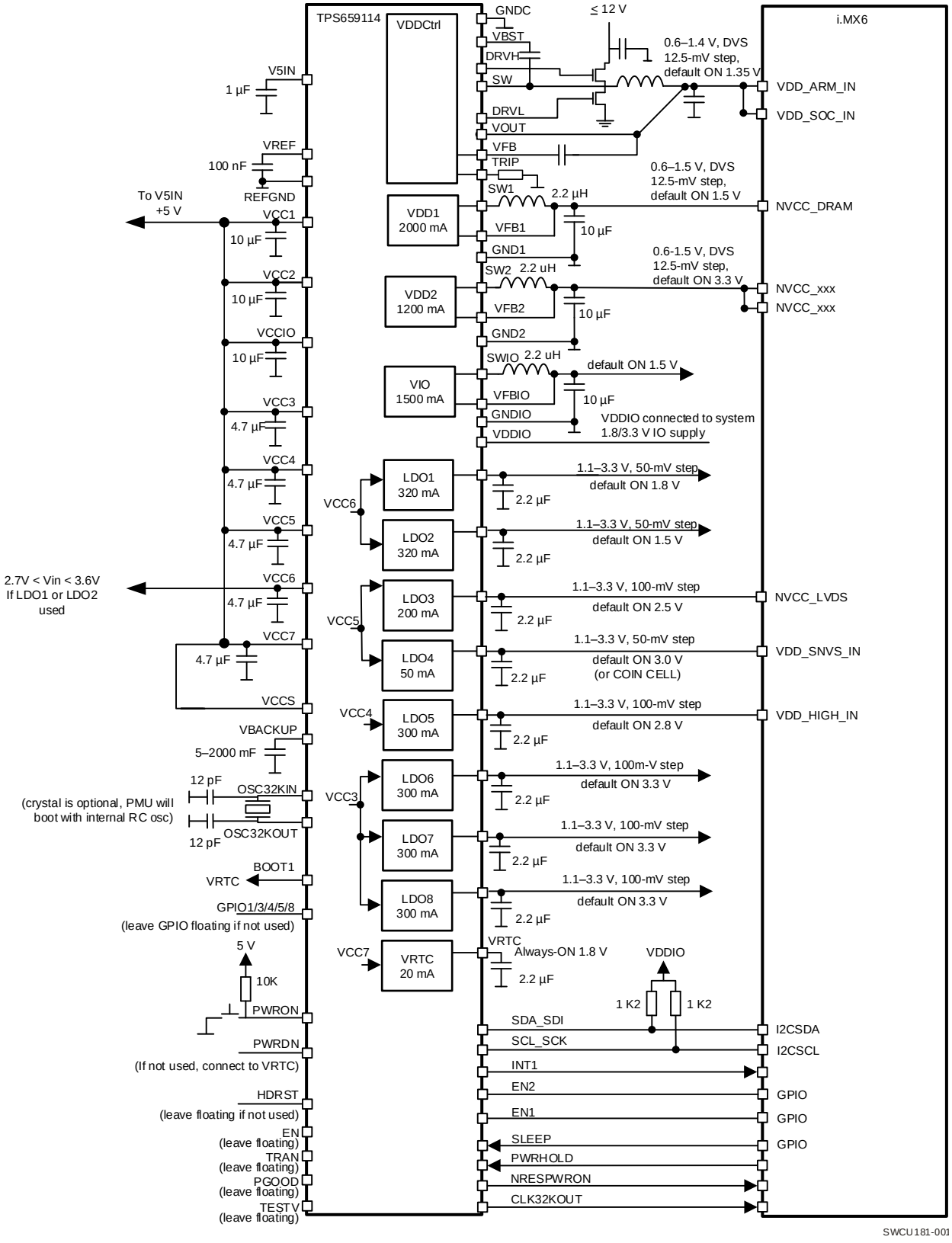



**Figure 1. Connecting TPS659114 to Freescale i.MX6**

## 3 EEPROM Setting

Table 1 describes the EEPROM configuration for the TPS659114 power-up sequence with BOOT1 = 1.

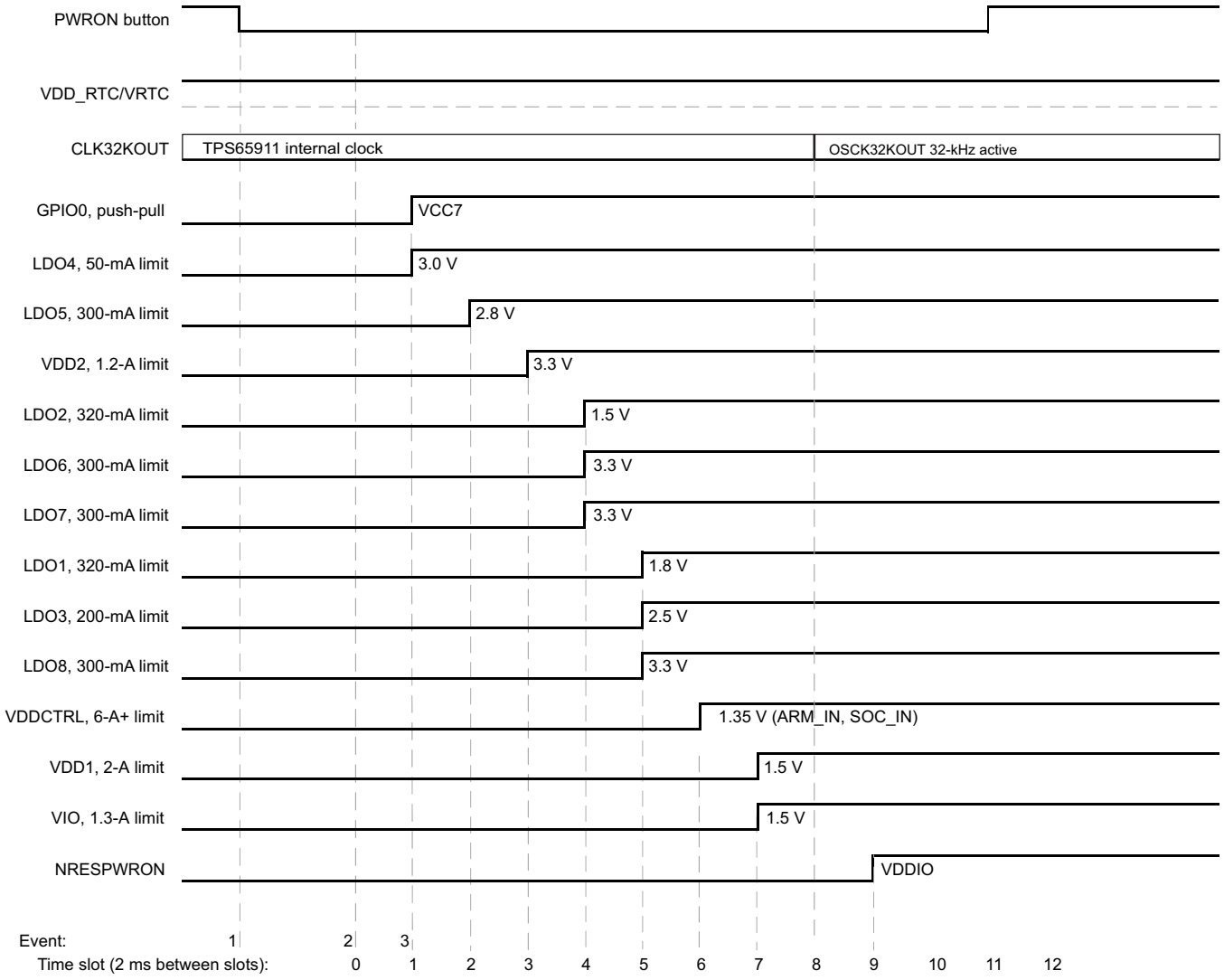
When a resource is associated to time slot 0, it means that the resource is OFF at power up.

**Table 1. EEPROM Configuration for TPS659114**

| REGISTER | BIT | DESCRIPTION | OPTION SELECTED |
|---|---|---|---|
| VDD1_OP_REG/ VDD1_SR_REG | SEL | VDD1 voltage level selection for boot. | 1.5 V |
| VDD1_REG | VGAIN_SEL | VDD1 gain selection, x1 or x2 | x1 |
| EEPROM | | VDD1 time slot selection | 7 |
| DCDCCTRL_REG | VDD1_PSKIP | VDD1 pulse skip mode enable | Skip enabled |
| VDD2_OP_REG/ VDD2_SR_REG | SEL | VDD2 voltage level selection for boot | 1.1 V |
| VDD2_REG | VGAIN_SEL | VDD2 gain selection, x1 or x3 | x3 |
| EEPROM | | VDD2 time slot selection | 3 |
| DCDCCTRL_REG | VDD2_PSKIP | VDD2 pulse skip mode enable | Skip enabled |
| VIO_REG | SEL[3:9] | VIO voltage selection | 1.5 V |
| EEPROM | | VIO time slot selection | 7 |
| DCDCCTRL_REG | VIO_PSKIP | VIO pulse skip mode enable | Skip enabled |
| VDDCtrl_OP_REG/ VDDCtrl_SR_REG | SEL | VDDCtrl voltage level selection for boot | 1.35 V |
| EEPROM | | VDDCtrl time slot | 6 |
| LDO1_REG | SEL[7:2] | LDO1 voltage selection | 1.8 V |
| EEPROM | | LDO1 time slot | 5 |
| LDO2_REG | SEL[7:2] | LDO2 voltage selection | 1.5 V |
| EEPROM | | LDO2 time slot | 4 |
| LDO3_REG | SEL[6:2] | LDO3 voltage selection | 2.5 V |
| EEPROM | | LDO3 time slot | 5 |
| LDO4_REG | SEL[7:2] | LDO4 voltage selection | 3.0 V |
| EEPROM | | LDO4 time slot | 1 |
| LDO5_REG | SEL[6:2] | LDO5 voltage selection | 2.8 V |
| EEPROM | | LDO5 time slot | 2 |
| LDO6_REG | SEL[6:2] | LDO6 voltage selection | 3.3 V |
| EEPROM | | LDO6 time slot | 4 |
| LDO7_REG | SEL[6:2] | LDO7 voltage selection | 3.3 V |
| EEPROM | | LDO7 time slot | 4 |
| LDO8_REG | SEL[6:2] | LDO8 voltage selection | 3.3 V |
| EEPROM | | LDO8 time slot | 5 |
| CLK32KOUT pin | | CLK32KOUT time slot | 8 |
| NRESPWRON, NRESPWRON2 pin | | NRESPWRON time slot | 9 |
| GPIO0 pin | | GPIO0 time slot | 1 |
| GPIO2 pin | | GPIO2 time slot | 0 |
| GPIO6 pin | | GPIO6 time slot | 0 |
| GPIO7 pin | | GPIO7 time slot | 0 |
| VRTC_REG | VRTC_OFFMASK | 0 = VRTC LDO will be in low-power mode during OFF state.<br>1 = VRC LDO will be in full-power mode during OFF state. | Full-power mode |
| DEVCTRL_REG | CK32K_CTRL | 0 = Clock source is crystal/external clock.<br>1 = Clock source is internal RC oscillator. | External |

**Table 1. EEPROM Configuration for TPS659114 (continued)**

| REGISTER | BIT | DESCRIPTION | OPTION SELECTED |
|---|---|---|---|
| DEVCTRL_REG | DEV_ON | 0 = No impact<br>1 = Will maintain device on, in ACTIVE or SLEEP state | 0 |
| DEVCTRL2_REG | TSLOT_LENGTH | Boot sequence time slot duration:<br>0 = 0.5 ms<br>1 = 2 ms | 2 ms |
| DEVCTRL2_REG | PWON_LP_OFF | 0 = Turn-off after PWRON long press not allowed.<br>1 = Turn-off after PWRON long press. | 1 |
| DEVCTRL2_REG | PWON_LP_RST | 0 = No impact<br>1 = Reset digital core when device is OFF. | 0 |
| DEVCTRL2_REG | IT_POL | 0 = INT1 signal will be active low.<br>1 = INT1 signal will be active high. | Active low |
| INT_MSK_REG | VMBHI_IT_MSK | 0 = Device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition.<br>1 = Start-up is reason required before switch-on. | 1 = Start-up requires activity on PWRHOLD or PWRON |
| INT_MSK3_REG | GPIO5_F_IT_MSK | 0 = GPIO5 falling edge detection interrupt not masked.<br>1 = GPIO5 falling edge detection interrupt masked. | Masked |
| INT_MSK3_REG | GPIO5_R_IT_MSK | 0 = GPIO5 rising edge detection interrupt not masked.<br>1 = GPIO5 rising edge detection interrupt masked. | Masked |
| INT_MSK3_REG | GPIO4_F_IT_MSK | 0 = GPIO4 falling edge detection interrupt not masked.<br>1 = GPIO4 falling edge detection interrupt masked. | Masked |
| INT_MSK3_REG | GPIO4_R_IT_MSK | 0 = GPIO4 rising edge detection interrupt not masked.<br>1 = GPIO4 rising edge detection interrupt masked. | Masked |
| GPIO0_REG | GPIO_ODEN | 0 = GPIO0 configured as push-pull output.<br>1 = GPIO0 configured as open-drain output. | Push-pull |
| WATCHDOG_REG | WATCHDOG_EN | 0 = Watchdog disabled<br>1 = Watchdog enabled, periodic operation with 100 s | Disabled |
| VMBCH_REG | VMBBUF_BYPASS | 0 = Enable input buffer for external resistive divider.<br>1 = In single-cell system, disable buffer for lower power consumption. | Enable buffer |
| VMBCH_REG | VMBCH_SEL[5:1] | Select threshold for boot gating comparator COMP1, 2.5–3.5 V. | 3.1 V |
| EEPROM | AUTODEV_ON | 0 = PWRHOLD pin is used as PWRHOLD feature.<br>1 = PWRHOLD pin is GPI. After power-on, DEV_ON is set high internally, no processor action needed to maintain supplies. | PWRHOLD feature implemented |
| EEPROM | PWRDN_POL | 0 = PWRDN signal is active low.<br>1 = PWRDN signal is active high. | Active low |




| Event Description | | |
|---|---|---|
| | 1 | PWRON button press falling edge |
| | 2 | Valid press after debounce |
| | 3 | First step of power up sequence available for DCDC, LDO activation. |

**Figure 2. Timing Diagram**

# 4 Getting Started With TPS659114

## 4.1 First Initialization

### 4.1.1 DCDC Maximum Current Capability

Upon reset, all buck converters initialize with ILMAX = 0, which may not allow proper regulation across all expected loads. In VIO_REG, VDD1_REG, and VDD2_REG, set the ILMAX bit according to the required maximum current.

### 4.1.2 I/O Polarity/Muxing Configuration

Voltage scaling for VDD1, VDD2, and VDDCtrl can be done either through the main $I^2C$ interface or through dedicated interface EN1/EN2. Refer to the processor documentation for information on which one is supported. To enable the dedicated voltage scaling interface, set the SR_CTL_I2C_SEL bit to 0 in the DEVCTRL_REG register.

If sleep mode is supported, program the SLEEPSIG_POL bit in the DEVCTRL2_REG register according to the GPIO from the processor. This can be set to active-low or active-high for SLEEP transitions. Software can configure specific power resources to enter the LOW-POWER or OFF state in sleep mode.

In the DEVCTRL_REG register, set the DEV_SLP bit to 1 to allow the SLEEP transition when requested through the SLEEP pin.

Update the GPIOx configuration (GPIOx_REG) based on the specification needs.

### 4.1.3 Define Wake Up/Interrupt Event (SLEEP or OFF)

Select the appropriate bits in the INT_MSK_REG, INT_MSK2_REG, and INT_MSK3_REG registers to activate an interrupt to the processor on the INT1 line.

### 4.1.4 Backup Battery Configuration

Backup Battery charging is disabled by default. To enable, set the BBCHEN bit to 1 in the BBCH_REG register. The maximum voltage can be set based on backup battery specifications by using the BBSEL bits in the BBCH_REG register.

### 4.1.5 Sleep Platform Configuration

Sleep mode is disabled by default. To use the sleep pin, sleep mode must first be enabled by setting DEV_SLP to 1 in the DEVCTRL_REG. Configure the state of the DC-DCs and LDOs when the SLEEP signal is used. By default, in sleep mode all resources maintain their output voltage and load capability, but response to transients (load change) is reduced. GPIO0 can follow sleep state.

Resources that must provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG and SLEEP_KEEP_RES_ON_REG registers.

Resources that can be set to off in the SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG and SLEEP_SET_RES_OFF_REG registers.

## 4.2 Event Management Through Interrupts

This section describes the TPS659114 interrupts.

### 4.2.1 INT_STS_REG.VMBHI_IT

The VMBHI_IT interrupt bit indicates that a supply (VBAT) is connected (PMIC leaving the BACKUP or NO SUPPLY state) and the system must be initialized (see Section 4.1, *First Initialization*).

### 4.2.2 INT_STS_REG.PWRON_IT

The PWRON_IT interrupt bit is triggered by pressing the PWRON button. If the device is in the OFF or SLEEP state, then this acts as a wake-up event and resources are reinitialized.

### 4.2.3 INT_STS_REG.PWRON_LP_IT

The PWRON_LP_IT interrupt bit is the PWRON long-press interrupt. This interrupt is generated when the PWRON button is pressed for 4 seconds. The application processor can make a decision to acknowledge the interrupt. If this interrupt is not acknowledged within the next second, the device interprets this as a power-down event.

### 4.2.4 INT_STS_REG.HOTDIE_IT

The HOTDIE_IT interrupt bit indicates that the temperature of the die is reaching the limit. The software must take action to decrease the power consumption before automatic shutdown.

### 4.2.5 INT_STS_REG.PWRHOLD_R/F_IT

The PWRHOLD_R/F_IT interrupt bit indicates a GPI interrupt event.

### 4.2.6 INT_STS_REG.RTC_ALARM_IT

The RTC_ALARM_IT interrupt bit is triggered when the RTC alarm set time is reached.

### 4.2.7 INT_STS2(3)_REG.GPIO_R/F_IT

The GPIOx_R/F_IT interrupt bit indicates a GPIO1, GPIO2 or GPIO3 interrupt event. It can be used to wake up the device from SLEEP state. This can be an interrupt coming from any peripheral device or alike.

### 4.2.8 INT_STS3_REG.PWRDN_IT

The PWRDN_IT interrupt bit is triggered when PWRDN reset is detected.

### 4.2.9 INT_STS3_REG.VMBDCH2_H/L_IT

The VMBDCH2_H_IT or VMBDCH2_L_IT interrupt bit is triggered when comparator 2 input (VCCS) is above or below the threshold, respectively.

### 4.2.10 INT_STS3_REG.WATCHDOG_IT

The WATCHDOG_IT interrupt bit is triggered from the watchdog (periodic or interrupt mode).

## 5 Ordering Information

**Table 2. Ordering Information**

| PART NUMBER | ORDERING INFORMATION | PROCESSOR |
|---|---|---|
| TPS659114 | TPS659114A2ZRC/R | Freescale i.MX6 |

# Revision History

**Changes from B Revision (August 2016) to C Revision** **Page**

- Changed document title from *TPS659114 User's Guide* : to *TPS659114 for Freescale i.MX6 Dual/Quad User's Guide* .. 1

**Changes from A Revision (January 2016) to B Revision** **Page**

- Changed VMBHI_IT_MSK Bit OPTION SELECTED in Table 1 ..... 4

**Changes from Original (January 2016) to A Revision** **Page**

- Updated Figure 1 ..... 2

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