NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P1P2V" represents connection to the +1.2V power plane.
2. The netname "P1P9V" represents connection to the +1.9V power plane.
3. The netname "P3P3V" represents connection to the +3.3V power plane.
4. The netname "P2P5V" represents connection to the +2.5V power plane.
5. The netname "P5V" represents connection to the +5.0V power plane.
6. The netname "P12V" represents connection to the +12.0V power plane.
7. The netname "GND" represents connection to the ground plane.
8. A "Z" suffix on a signal name indicates an active low signal.
9. All components with designators "U*", "Q*", and "D*" are electrostatic discharge sensitive.
10. All components with designators above 500 are mounted solder side of the board.
11. All resistor values are in ohms.
12. All capacitor values in microfarads unless otherwise specified.

COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2128668: Initial Release	12/06/2012	HPC
B	ECO 2134134: REV B	06/18/2013	HPC
C	ECO 2135374: REV C	08/15/2013	HPC
D		04/7/2016	
E		01/11/2017	

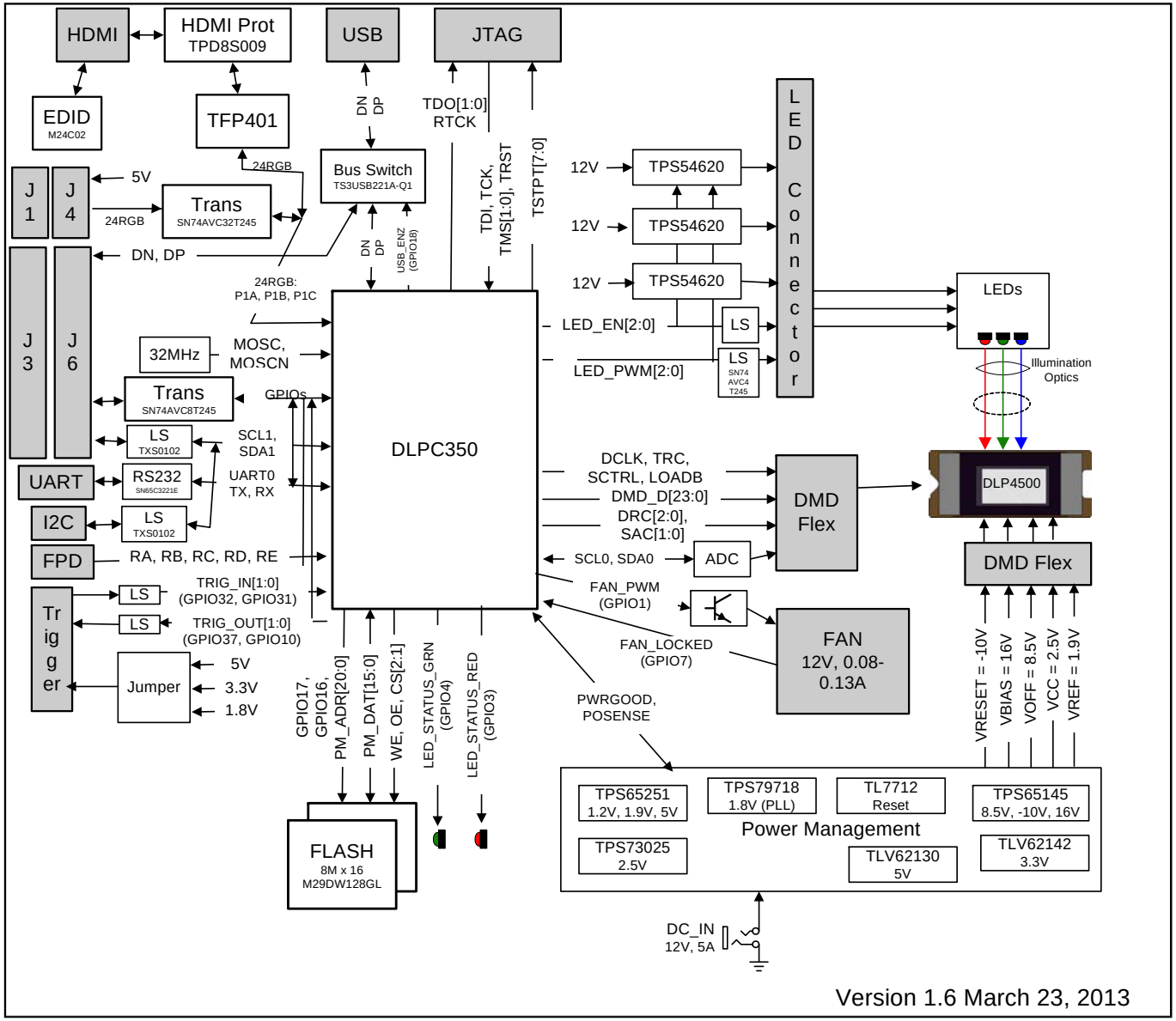
		DWN	DATE 08/15/2013
		ENGR	08/15/2013
		APVD	08/15/2013
		MFG	
N/A	0314PO	QA	
NEXT ASSY	USED ON		
APPLICATION		SW	Allegro Design Entry 16.5

TEXAS INSTRUMENTS

TITLE: ESD, LIGHTCRAFTER 4500

A3	DRAWING NO 2512909	REV E
SCALE	SHEET 1 of 29	

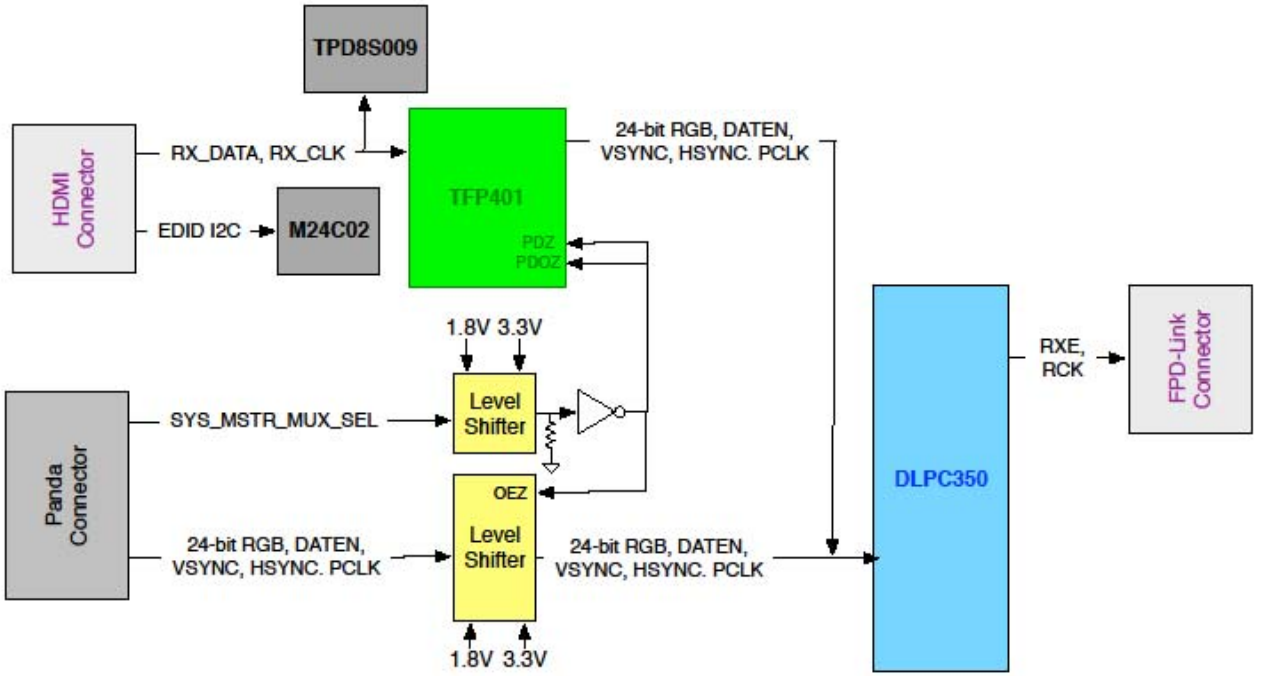
BLOCK DIAGRAM



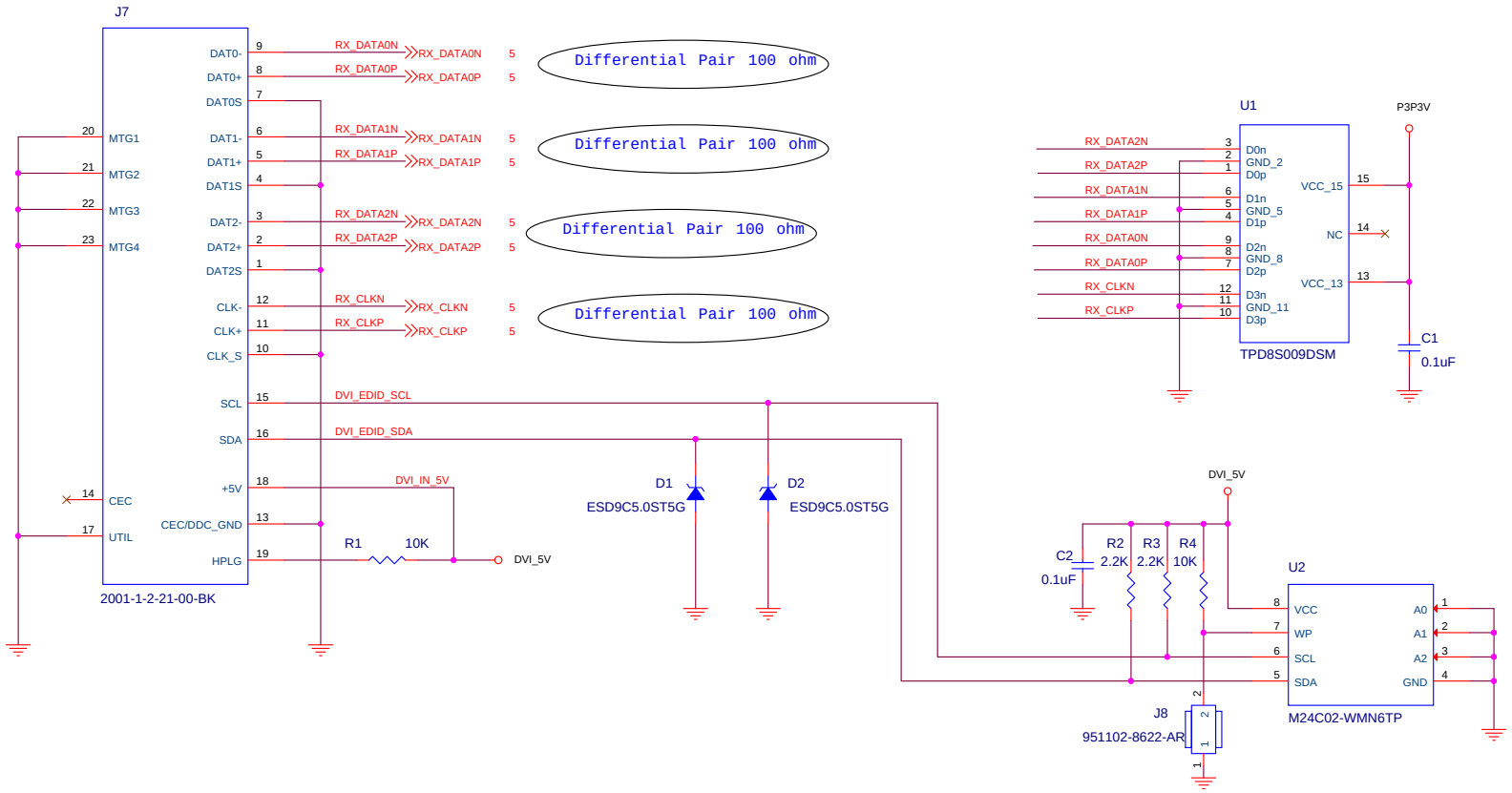
INDEX

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV E
	ISSUE DATE		SCALE	SHEET 2 OF 29

Video Input and Muxing



TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV E
	ISSUE DATE		SCALE	SHEET 3 OF 29	



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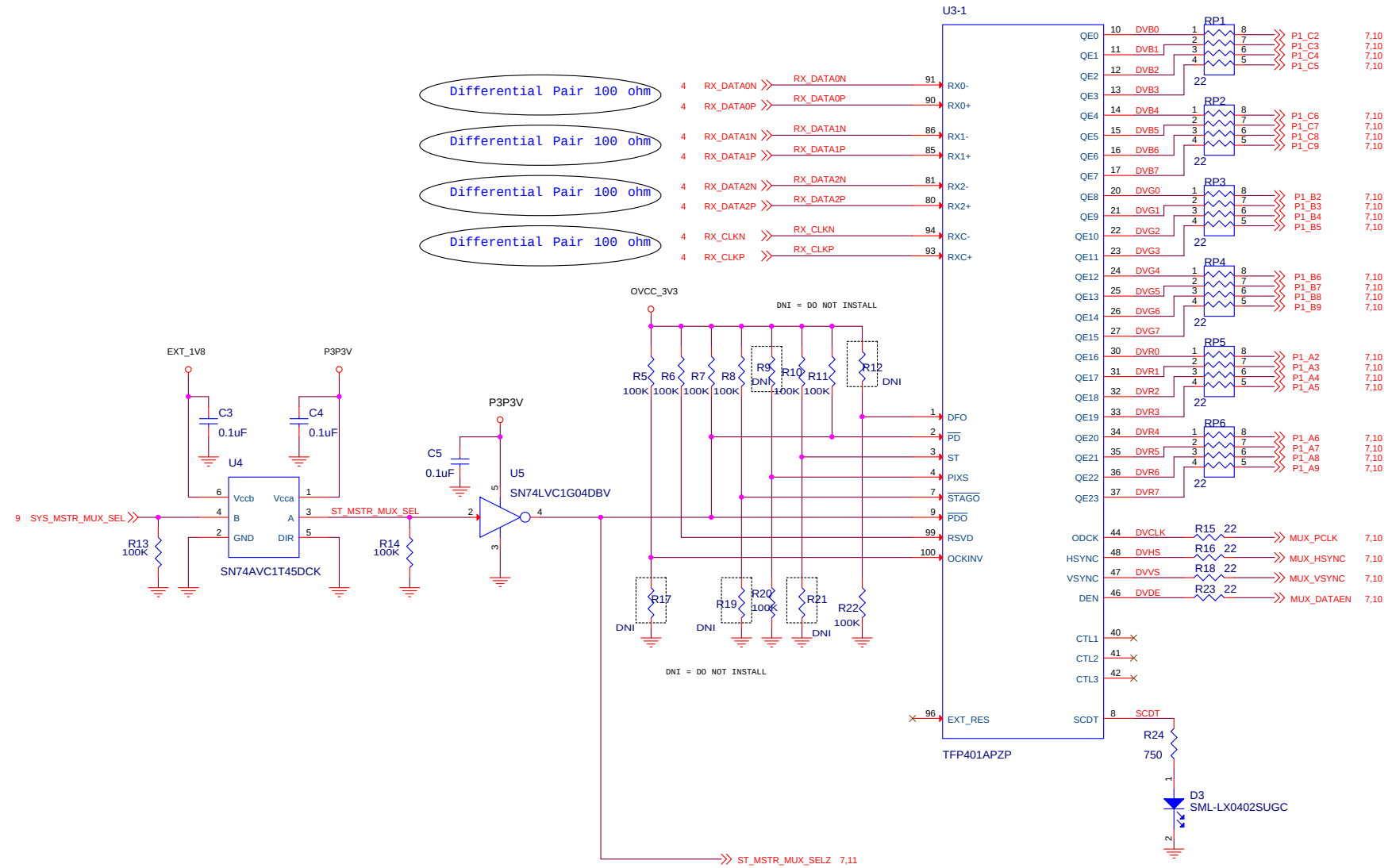
	ISSUE DATE		SCALE	SHEET 4 OF 29	



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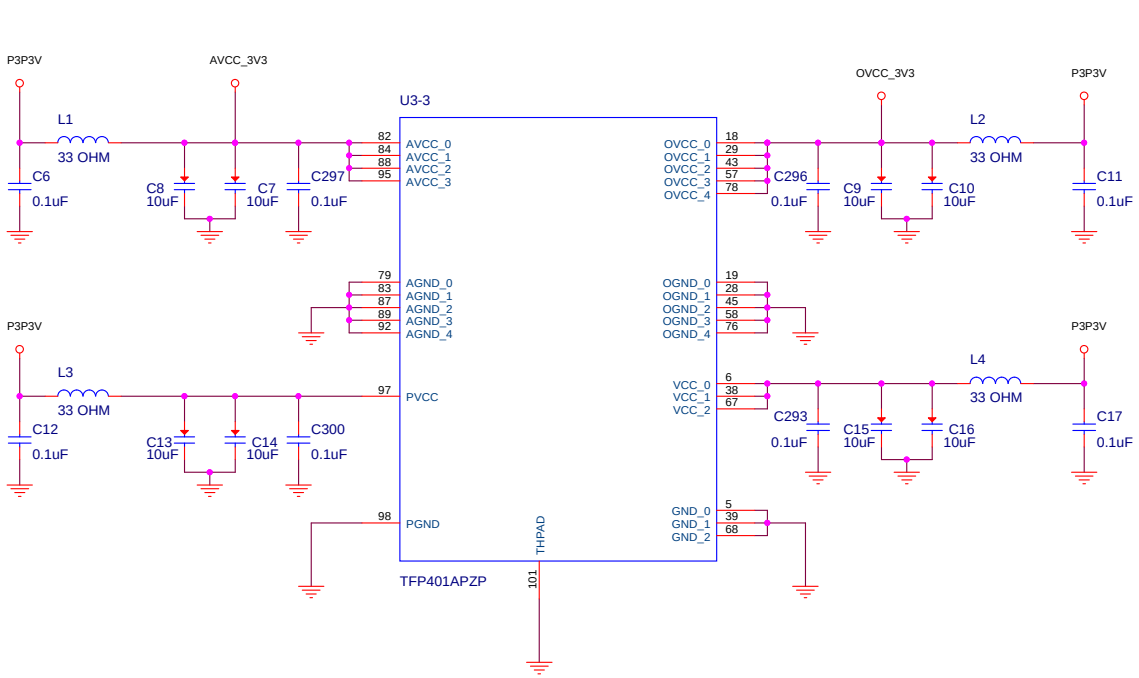
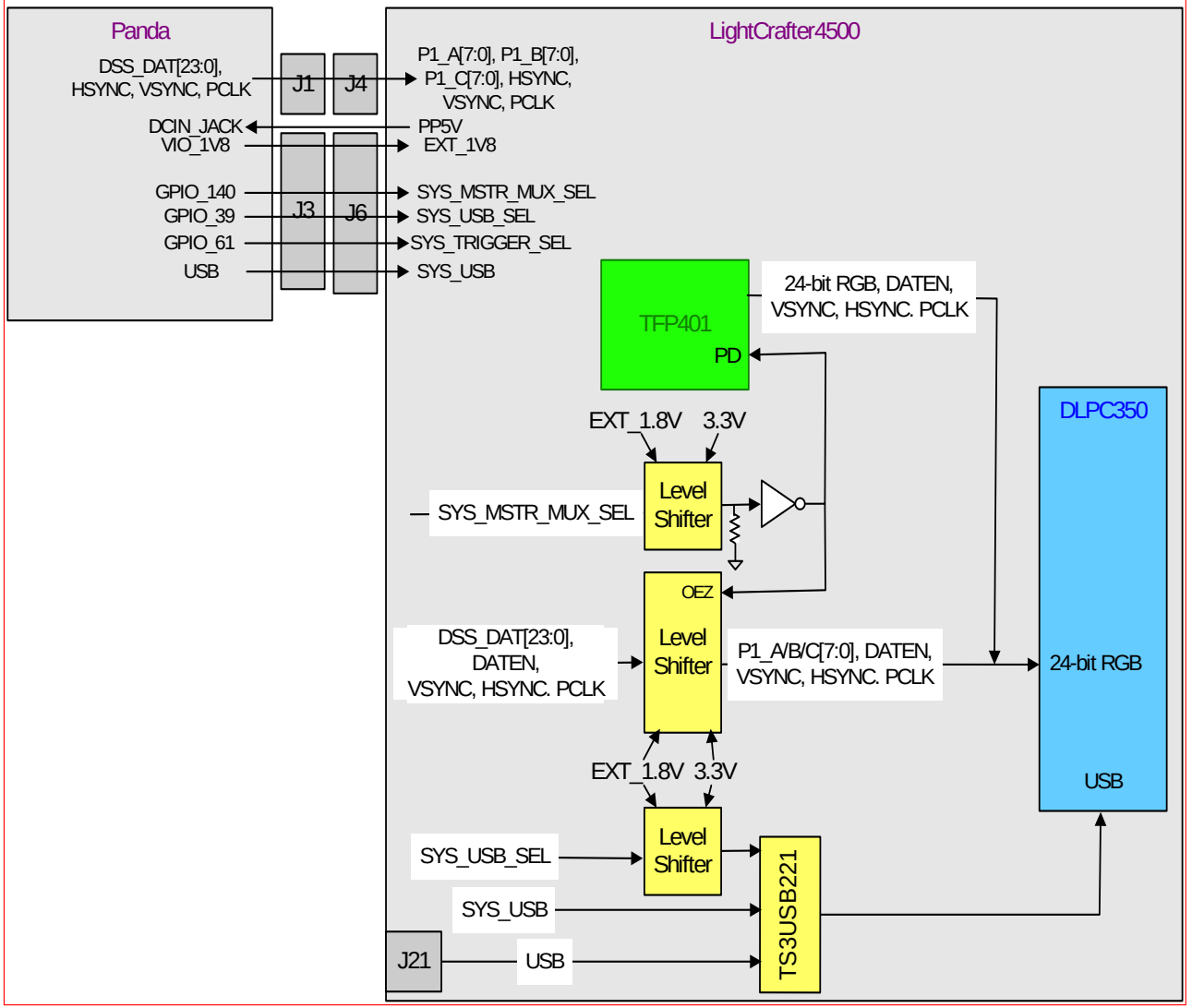
	ISSUE DATE		SCALE	SHEET 5 OF 29	



TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV E
	ISSUE DATE		SCALE	SHEET 6 OF 29	

Panda Connections



Panda to LightCrafter 4500 Connections

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV E
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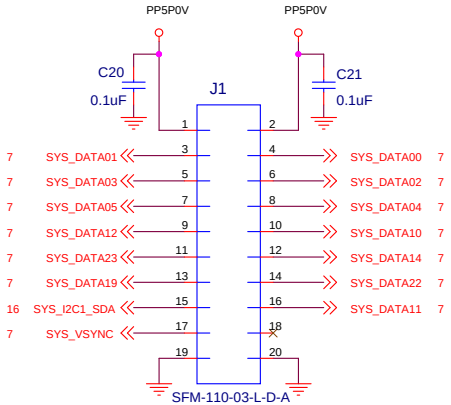
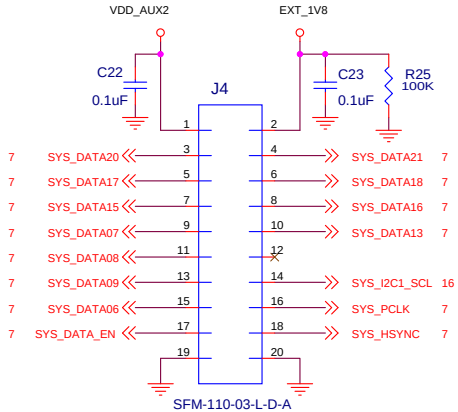
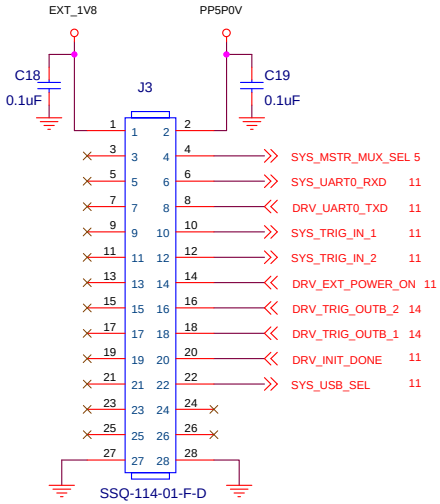
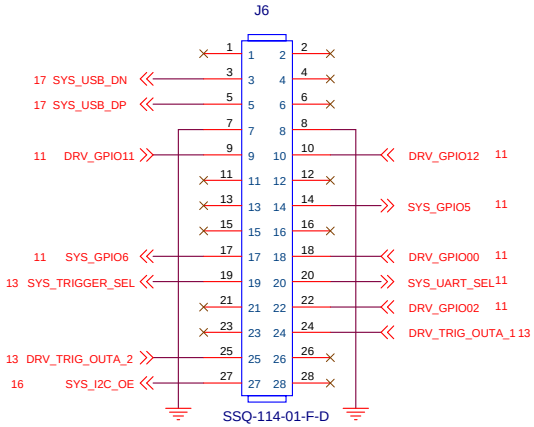




PANDA DATA PATH CONNECTORS



PANDA I/O CONNECTOR



PANDA I/O CONNECTOR

Processor Interface ConnectorS

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV E
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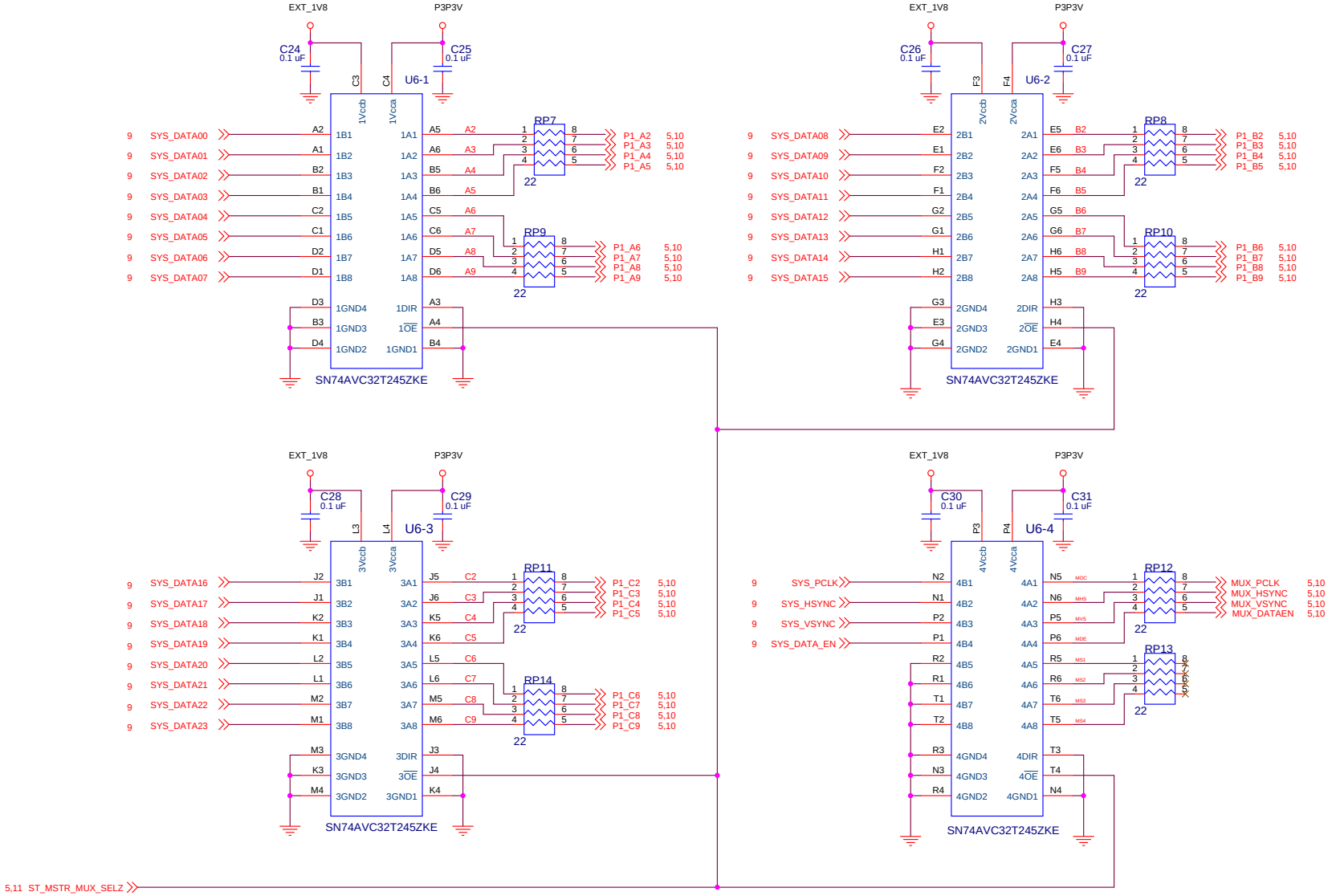

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV E
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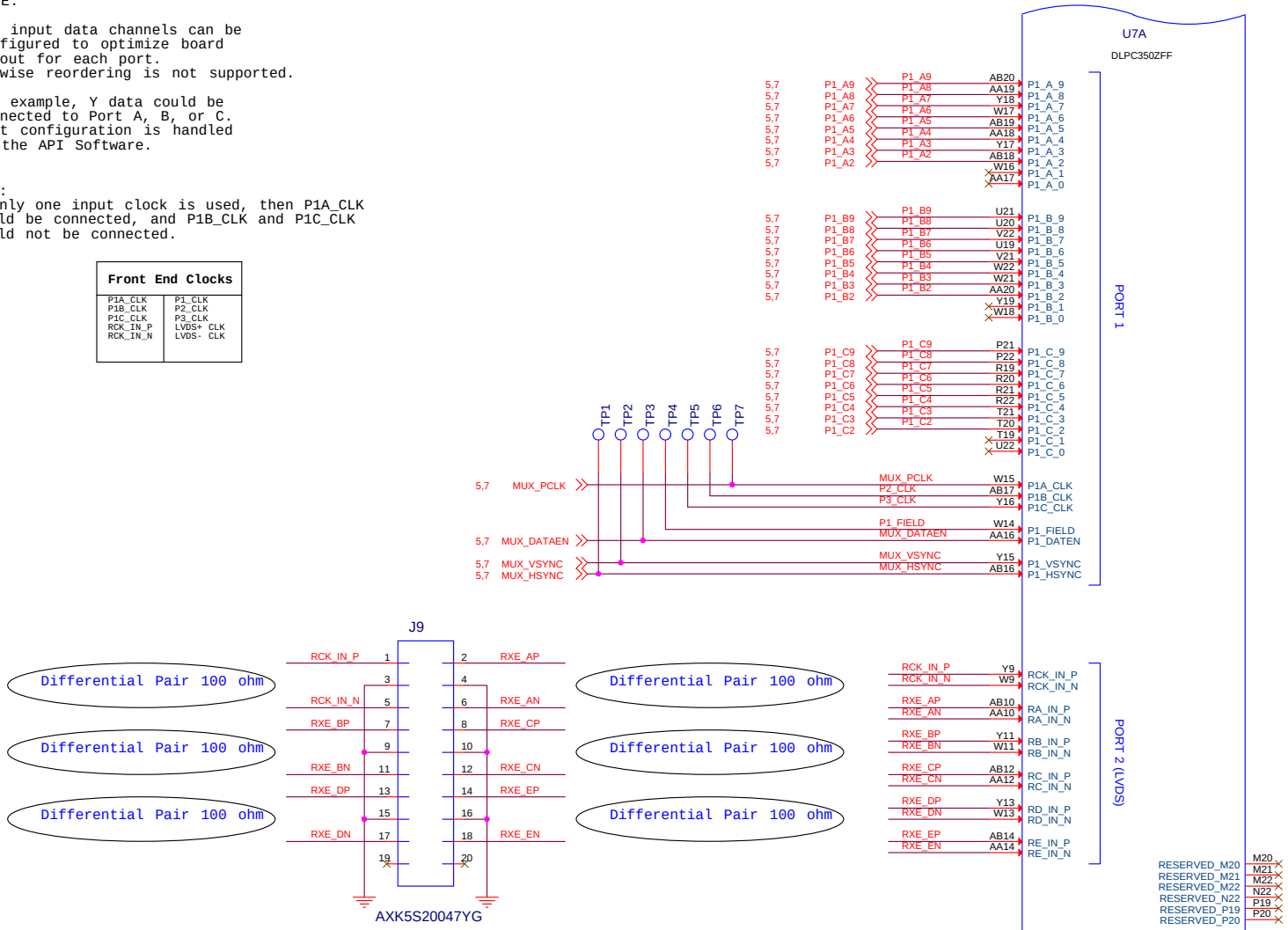
NOTE:

The input data channels can be configured to optimize board layout for each port. Bitwise reordering is not supported.

For example, Y data could be connected to Port A, B, or C. Port configuration is handled in the API Software.

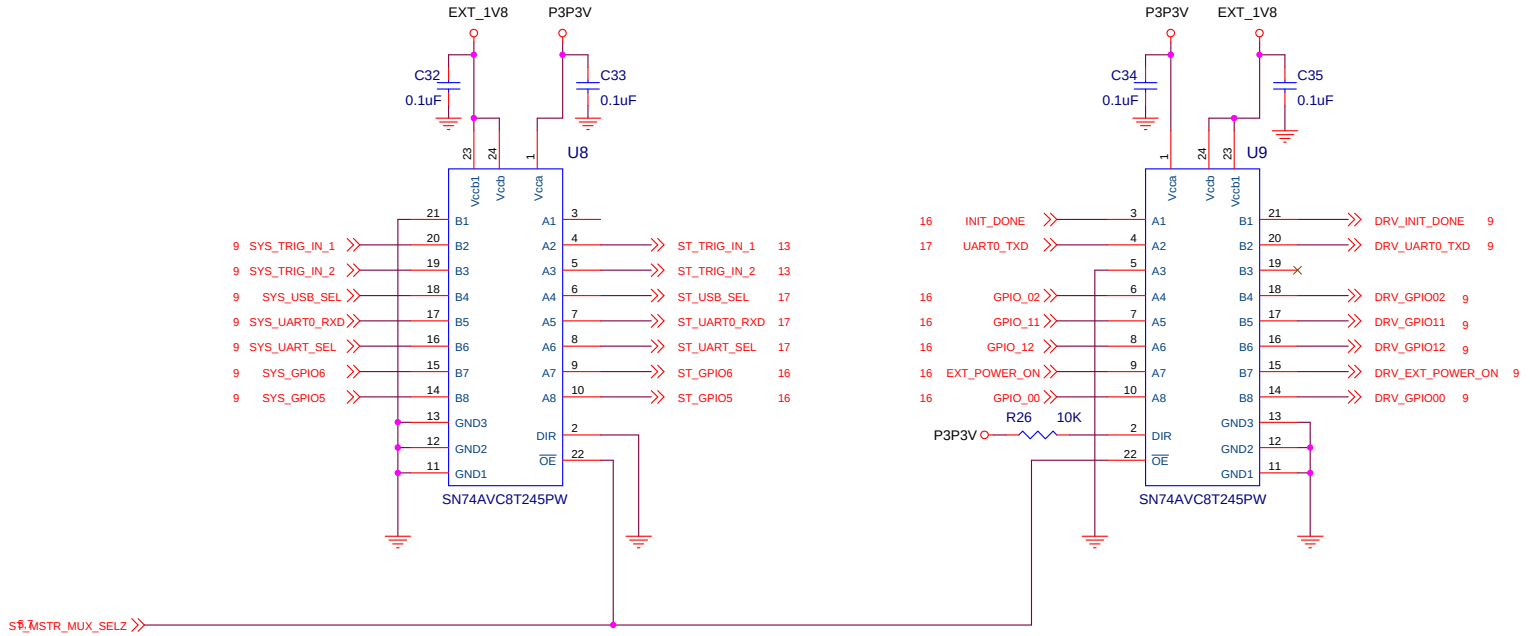
NOTE:
If only one input clock is used, then P1A_CLK should be connected, and P1B_CLK and P1C_CLK should not be connected.

Front End Clocks	
P1A_CLK	P1_CLK
P1B_CLK	P2_CLK
P1C_CLK	P3_CLK
RCK_IN_P	LVDS+ CLK
RCK_IN_N	LVDS- CLK



Front End Interface

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV E
	ISSUE DATE		SCALE	SHEET 10 OF 29



TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV E
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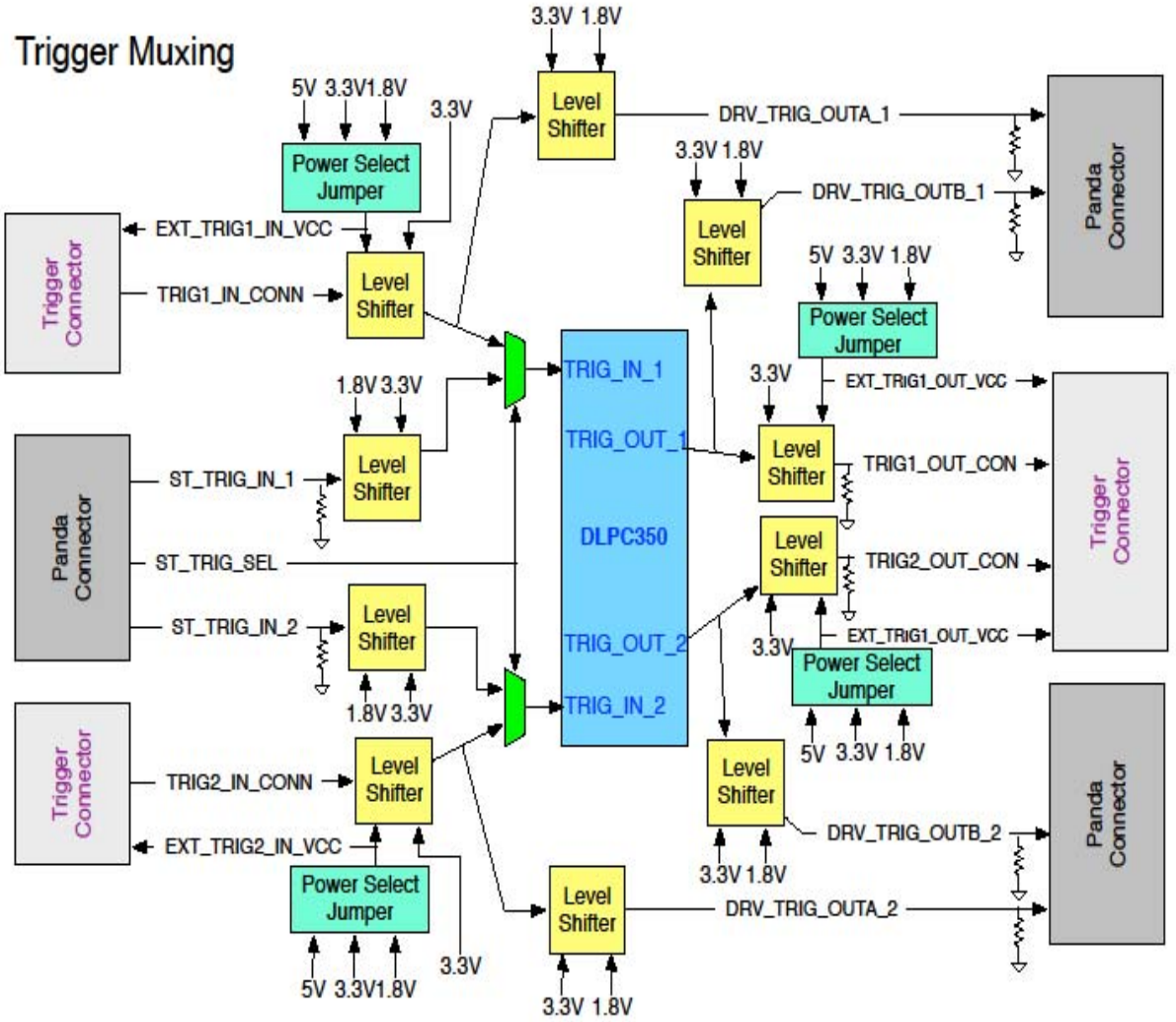
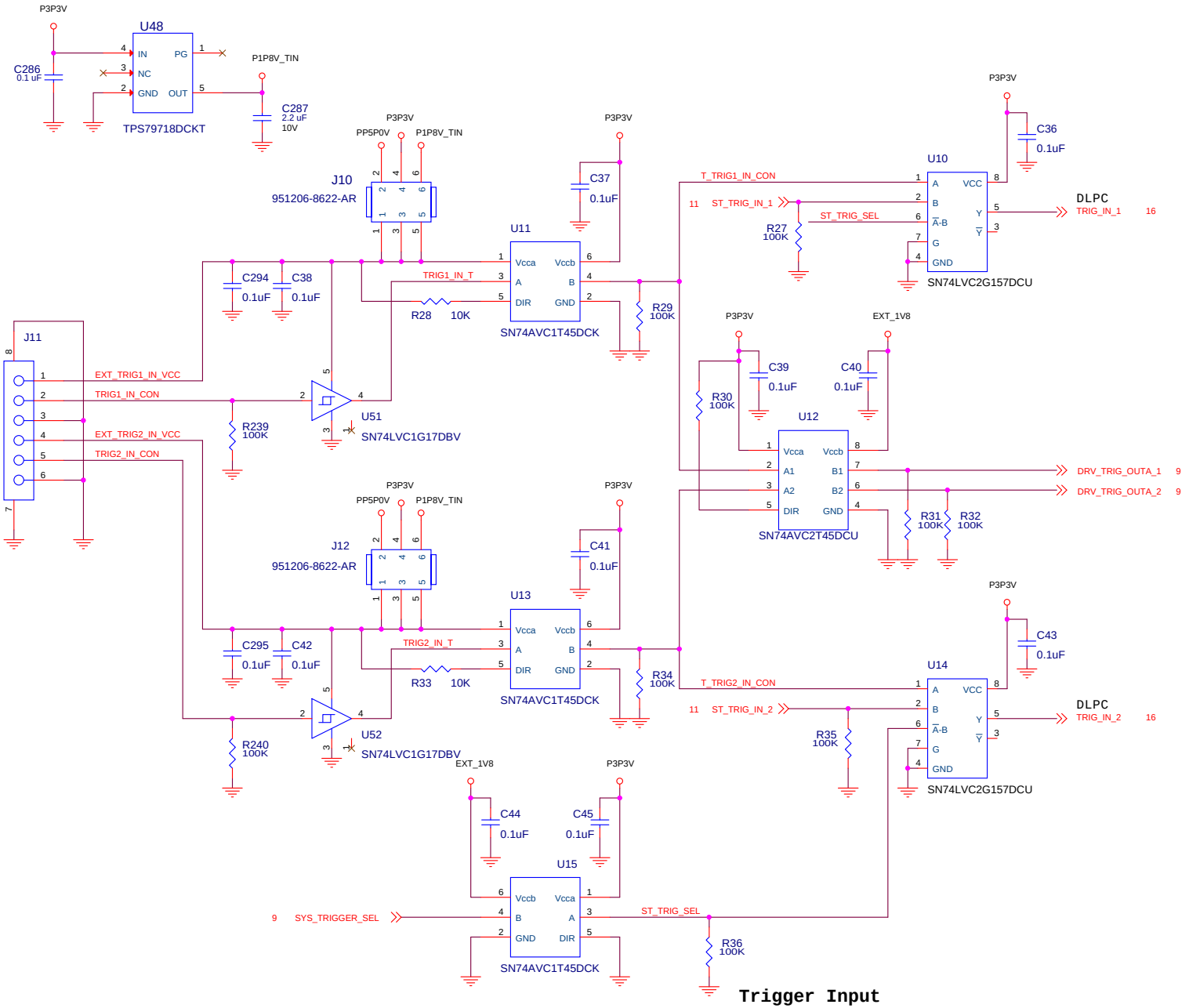
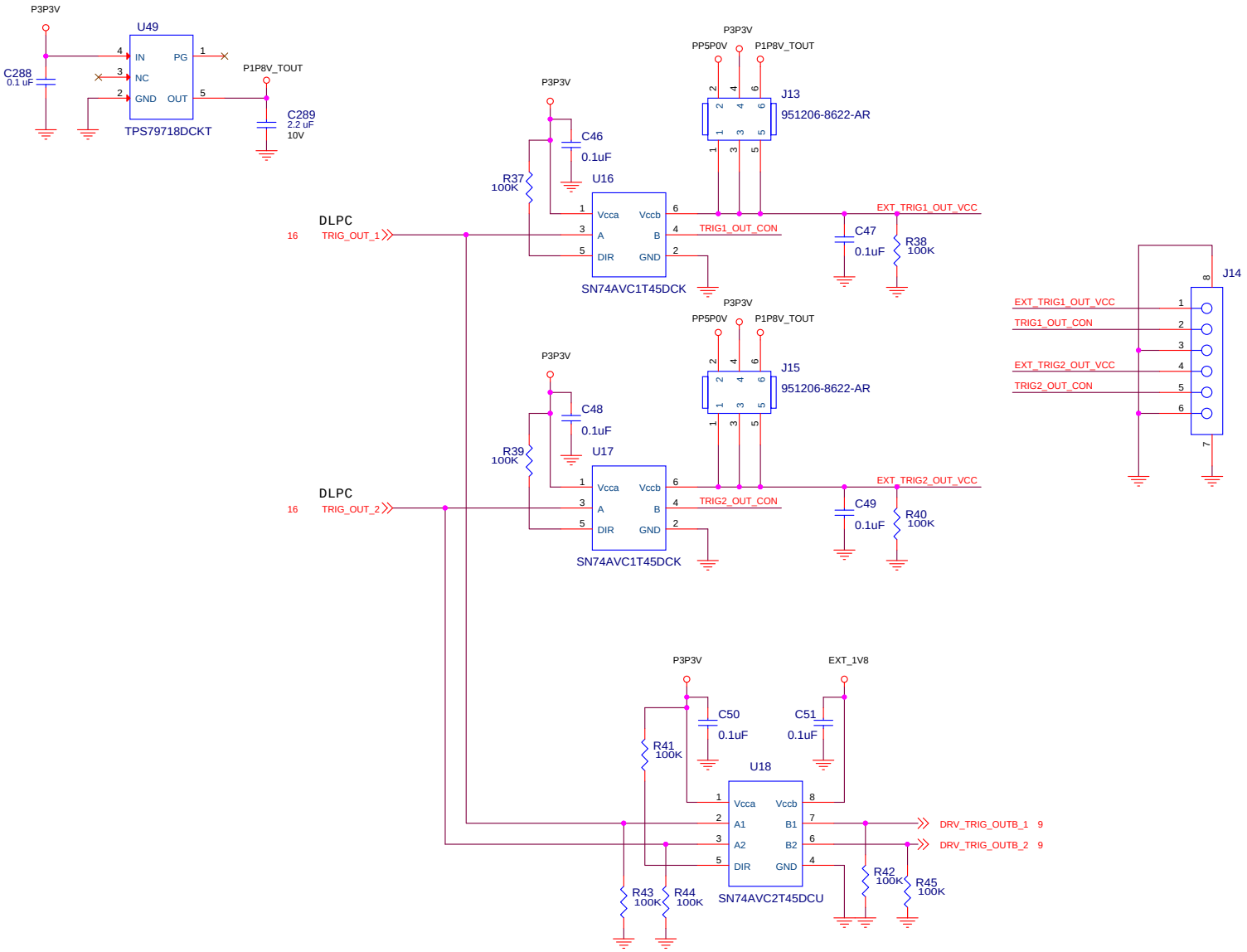


TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV E
	ISSUE DATE		SCALE	SHEET 12 OF 29	



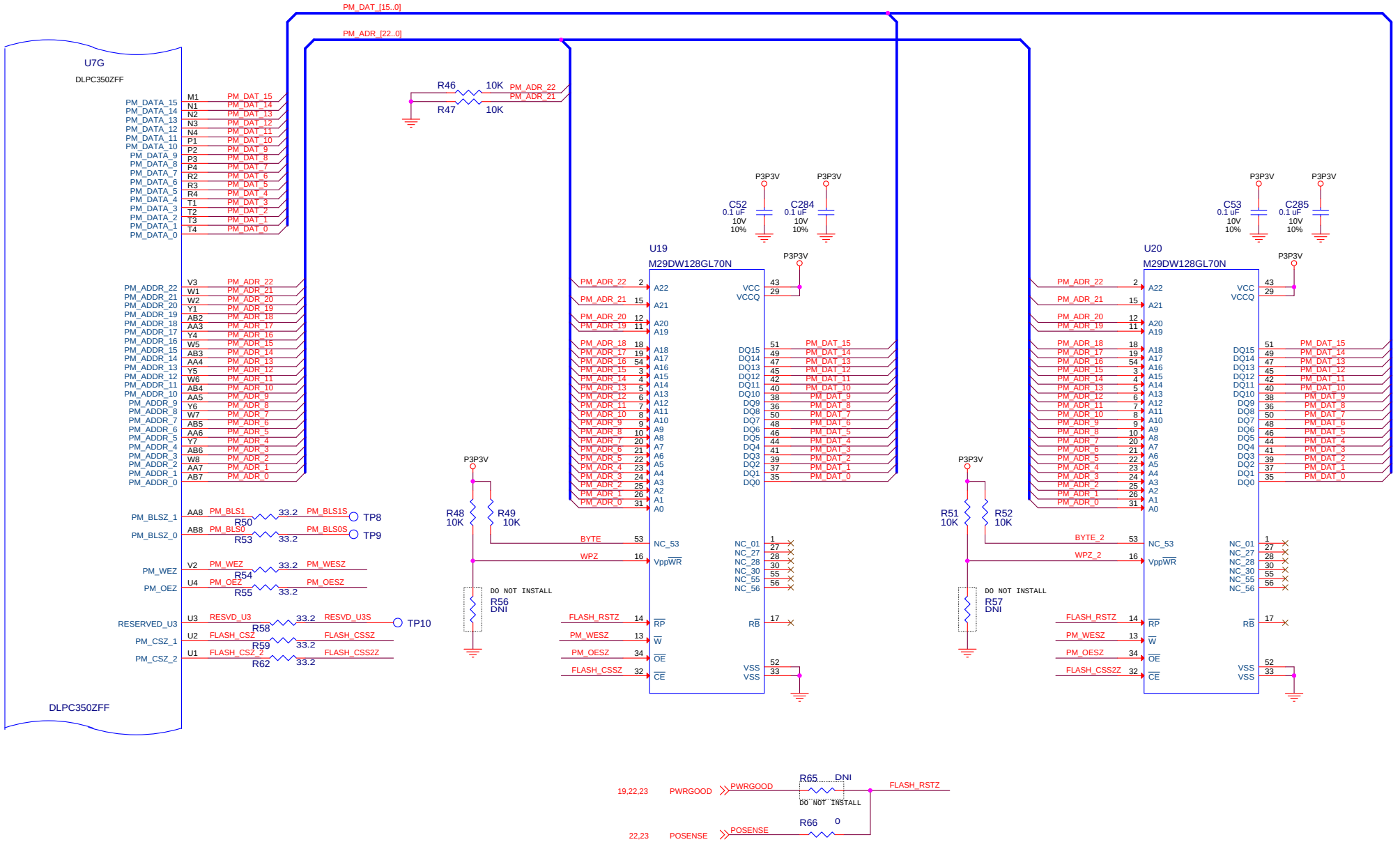
Trigger Input

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV E
	ISSUE DATE		SCALE	SHEET 13 OF 29	



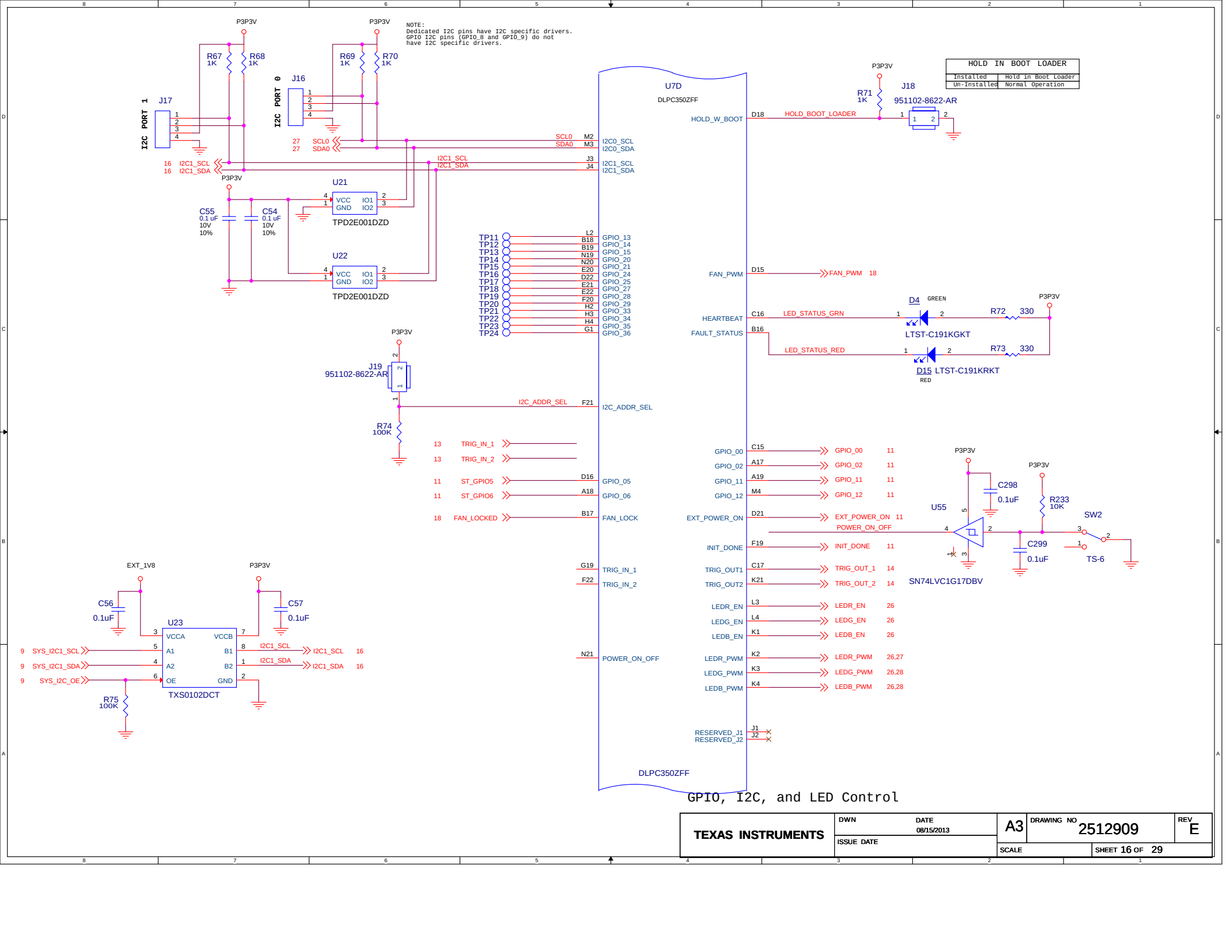
Trigger Output

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV E
	ISSUE DATE		SCALE	SHEET 14 OF 29	



Flash Memory Interface

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV E
	ISSUE DATE		SCALE	SHEET 15 OF 29


NOTE:
Dedicated I2C pins have I2C specific drivers.
GPIO I2C pins (GPIO_8 and GPIO_9) do not
have I2C specific drivers.
HOLD IN BOOT LOADER
Installed
Hold in Boot Loader
Un-Installed
Normal Operation
U7D
DLPC350ZFF
J17
I2C PORT 1
J16
I2C PORT 0
R67 1K
R68 1K
R69 1K
R70 1K
U21
U22
TPD2E001DZD
C55 0.1 uF 10V 10%
C54 0.1 uF 10V 10%
J18
951102-8622-AR
R71 1K
HOLD_W_BOOT
HOLD_BOOT_LOADER
J19
951102-8622-AR
R74 100K
I2C_ADDR_SEL
D4 GREEN
LTST-C191KGKT
D15 LTST-C191KRKT
RED
R72 330
R73 330
HEARTBEAT
FAULT_STATUS
LED_STATUS_GRN
LED_STATUS_RED
FAN_PWM
FAN_LOCKED
TRIG_IN_1
TRIG_IN_2
ST_GPIO5
ST_GPIO6
GPIO_05
GPIO_06
FAN_LOCK
POWER_ON_OFF
EXT_POWER_ON
INIT_DONE
TRIG_OUT1
TRIG_OUT2
LEDR_EN
LEDG_EN
LEDB_EN
LEDR_PWM
LEDG_PWM
LEDB_PWM
RESERVED_J1
RESERVED_J2
U55
SN74LVC1G17DBV
C298 0.1uF
C299 0.1uF
R233 10K
SW2
TS-6
EXT_1V8
C56 0.1uF
C57 0.1uF
U23
TXS0102DCT
R75 100K
SYS_I2C1_SCL
SYS_I2C1_SDA
SYS_I2C_OE
I2C1_SCL
I2C1_SDA
I2C0_SCL
I2C0_SDA
GPIO_00
GPIO_02
GPIO_11
GPIO_12
TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24
GPIO_13 GPIO_14 GPIO_15 GPIO_20 GPIO_21 GPIO_24 GPIO_25 GPIO_27 GPIO_28 GPIO_29 GPIO_33 GPIO_34 GPIO_35 GPIO_36
DLPC350ZFF
GPIO, I2C, and LED Control
TEXAS INSTRUMENTS
DWN
DATE 08/15/2013
ISSUE DATE
A3
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REV E
SCALE
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NOTE:
The RS232 interface is used for test interface and debug. It is not required for production designs.

RS-232 PORT 0

P3P3V
R76 0
U24
MAX3232CPWR
C58 0.1 uF 10V 10%
C59 0.1 uF 50V
C60 0.1 uF 50V
C61 0.1 uF 50V
C62 0.1 uF 50V
VCC GND V+ C1+ C1- V- C2+ C2-
SJ-2523-SMT
J20
0 R77
R78 DNI
R82 DNI
0 R83
0 R84
RS232_TX RS232_RX
T2OUT R1IN R2IN T1OUT
T2IN R1OUT R2OUT T1IN
UART0_TXD UART0_CTSZ UART0_RXD_DRV UART0_RTSZ

11 UART0_TXD
11 UART0_RXD

U7F
DLPC350ZFF
L19 UART0_TXD
L20 UART0_CTSZ
L21 UART0_RXD
M19 UART0_RTSZ
RESERVED_F4 RESERVED_F3 RESERVED_D1 RESERVED_C1 RESERVED_D2

P3P3V
R79 3.3K
R80 3.3K
R81 1K
F4 SSP0_CLK
F3 SSP0_TXD
D1 SSP0_RXD
C1 SSP0_CS21
D2 SSP0_CS20
TP25 TP26 TP27 TP28 TP29

P3P3V
C63 0.1uF
U25
SN74LVC2G157DCU
A B A-B G VCC Y Y GND
11 ST_UART0_RXD
11 ST_UART_SEL
R86 100K
R87 100K

NOTE:
The USB interface is used for test interface, debug and high-speed flash memory programming capability. It is not required for production designs where I2C is the primary communication bus.

J21
1734035-2
USB Type-Mini B Jack
USB_DAT_N
USB_DAT_P
R90 22 1/10W
R91 22 1/10W
USB_DAT_NS
USB_DAT_PS

Note: This buffer prevents the USB host from detecting the slave device before ARM processor initialization.

P3P3V
C65 0.1uF
U27
TS3USB221ARSER
1DN 1DP 2DP 2DN GND VCC DN DP SEL OEZ
DAT_N
DAT_P
C18 USB_ENZ
E3 USB_DAT_N
E2 USB_DAT_P
DLPC350ZFF

P3P3V
R88 100K
C64 0.1 uF 10V 10%
VBUS
U26
SN74LVC1G125DBVR
R85 3.3K
R89 1.5K
USB_ENZ

9 SYS_USB_DP
9 SYS_USB_DN

11 ST_USB_SEL
R92 100K

RS-232, Synchronous Serial Port, and USB

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV E
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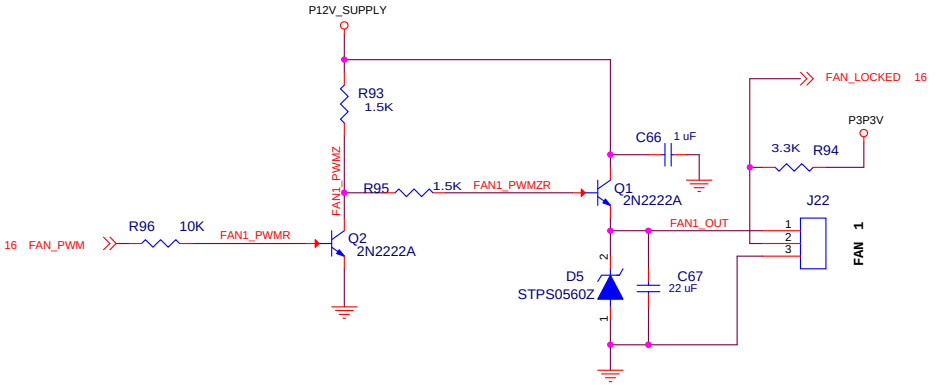

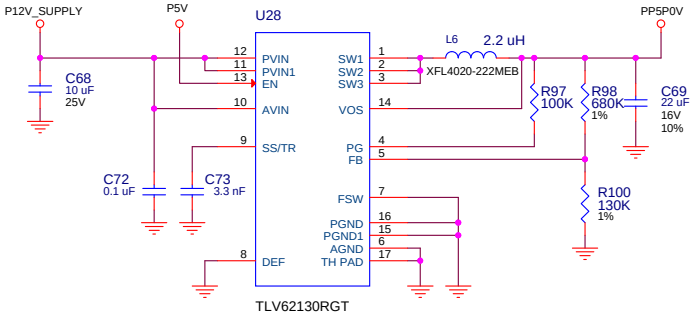

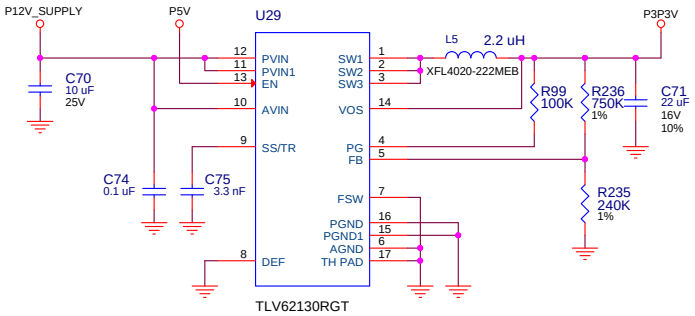

Fan, 3.3V & Panda 5.0V Power Supplies

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MULTI-ICE JTAG I/F

P3P3V

DO NOT INSTALL

R103 1K
R104 10K
R105 10K
R106 10K
R107 10K
R108 10K
R109 10K

J24

TRSTZ_IN
TDI
TMS2
TCK
RTCK
TDO2
ICE_RSTZ

P3P3V

R101 1K

NOTE:
TRSTZ should be pulled down for production designs.

U30
SN74LVC1G125DBVR

TRSTZ

R110 10K

P3P3V

R102 10K

J23
951102-8622-AR

MAN_RSTZ

MANUAL RESET JUMPER	
INSTALLED NOT INSTALLED	HOLD IN RESET NORMAL OPERATION (DEFAULT)

SW1
TL3305AF260

R111 100 1%

P3P3V

C76 0.1 uF 10V 10%

P3P3V

U31
TPS3838K33DBVT

VDD
MR
RESET
CT
GND

P3P3V

U32
SN74LVC1G07DBVR

PWRGOOD
PWRGOOD 15,22,23

P3P3V

C77 0.1 uF 10V 10%

JTAG BOUNDARY SCAN

J25

TRSTZ
TDI
TMS1
TDO1
TCK

53261-0671

NOTE:
JTAG I/F, ARM Trace and Testpoint connectors and signals are for board debug and test. They are not required for production designs.

U7E
DLPC350ZFF

TDO2 M18 RESERVED_M18
TDO1 L18 TDO1
TMS2 V16 RESERVED_V16
TMS1 V15 TMS1
TDI P18 TDI
TCK R18 TCK
TRSTZ V17 TRSTZ

RESERVED_K20 K20 TRACEPKT7R
RESERVED_K19 K19 TRACEPKT6R
RESERVED_J22 J22 TRACEPKT5R
RESERVED_J21 J21 TRACEPKT4R
RESERVED_J20 J20 TRACEPKT3R
RESERVED_J19 J19 TRACEPKT2R
RESERVED_H22 H22 TRACEPKT1R
RESERVED_H21 H21 TRACEPKT0R

RN1
33

TRACEPKT7 TP30
TRACEPKT6 TP31
TRACEPKT5 TP32
TRACEPKT4 TP33
TRACEPKT3 TP34
TRACEPKT2 TP35
TRACEPKT1 TP36
TRACEPKT0 TP37

TP38
TP39

RESERVED_F1 F1 TP40
RESERVED_G4 G4 TP41
RESERVED_G3 G3 TP42
RESERVED_F2 F2 TP43
RESERVED_G2 G2 TP44
RTCK G18

RTCKR R112 33 RTCK

ICTSEN_PD V6 ICTSEN
R113 4.7K
V7 HW_TEST_EN

SPARE E16 SEQ_SYNC
VPGM D17

DLPC350ZFF

R114 10K

Test Points, JTAG and Reset

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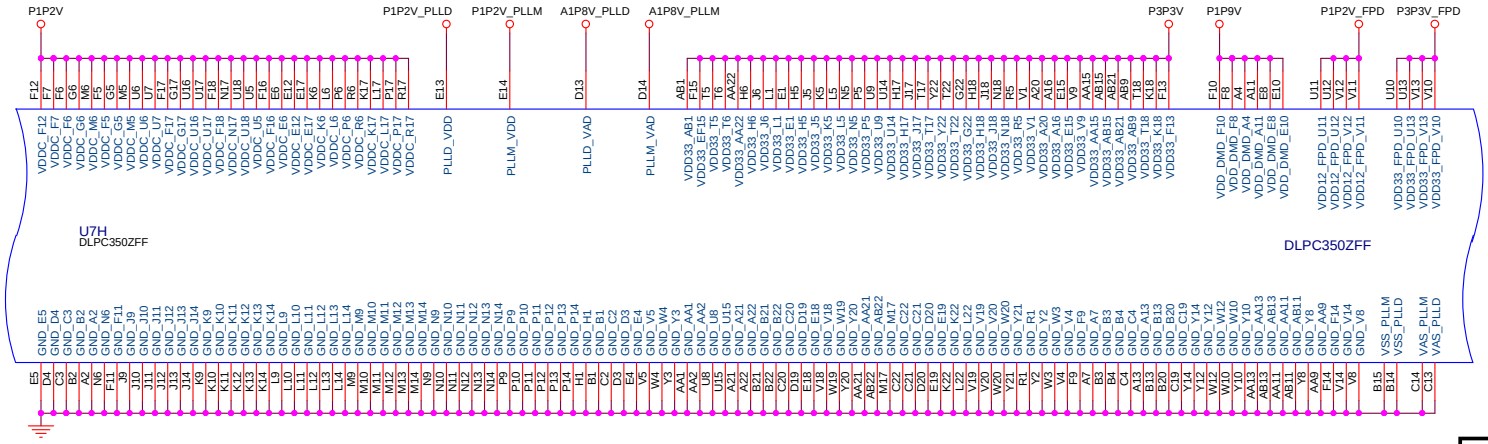

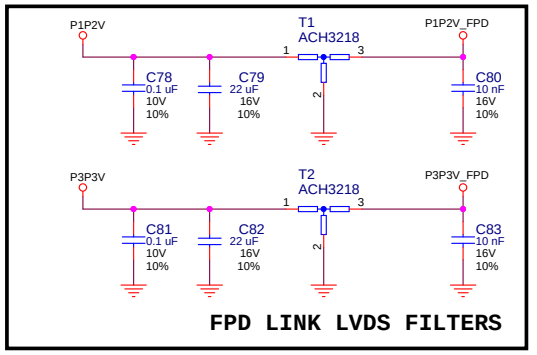

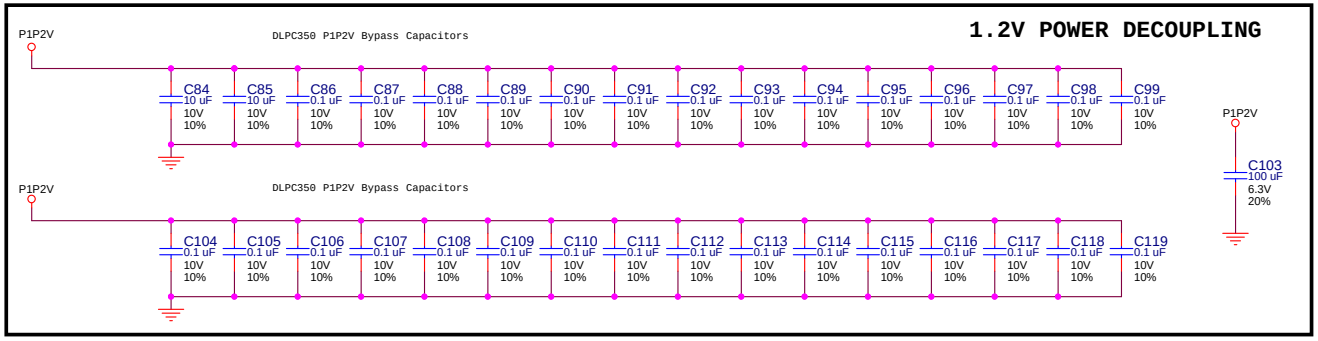

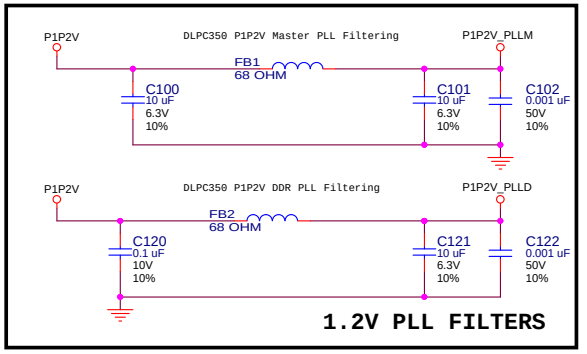

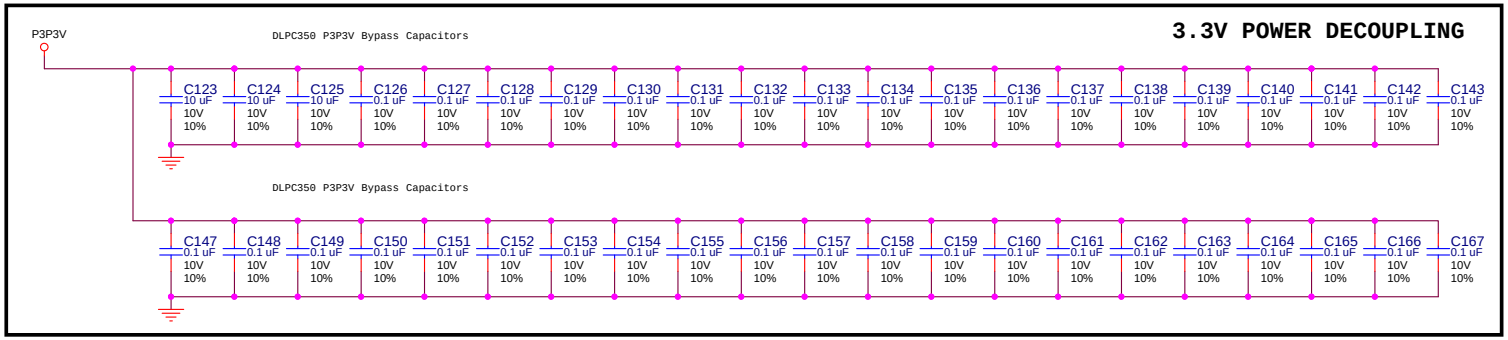

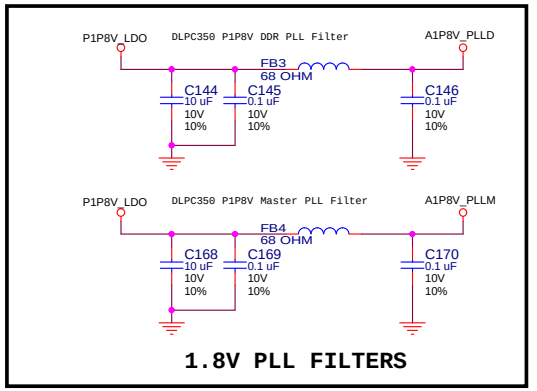

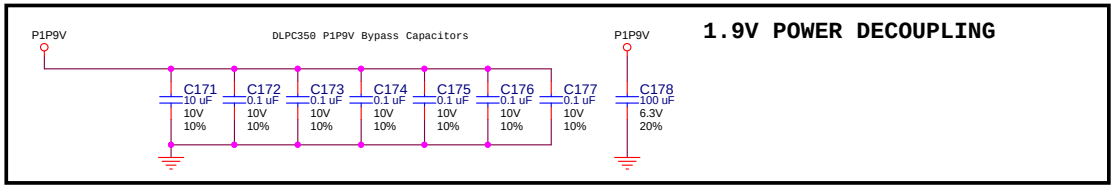

DLPC350 Power and Bypass Capacitors

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV E
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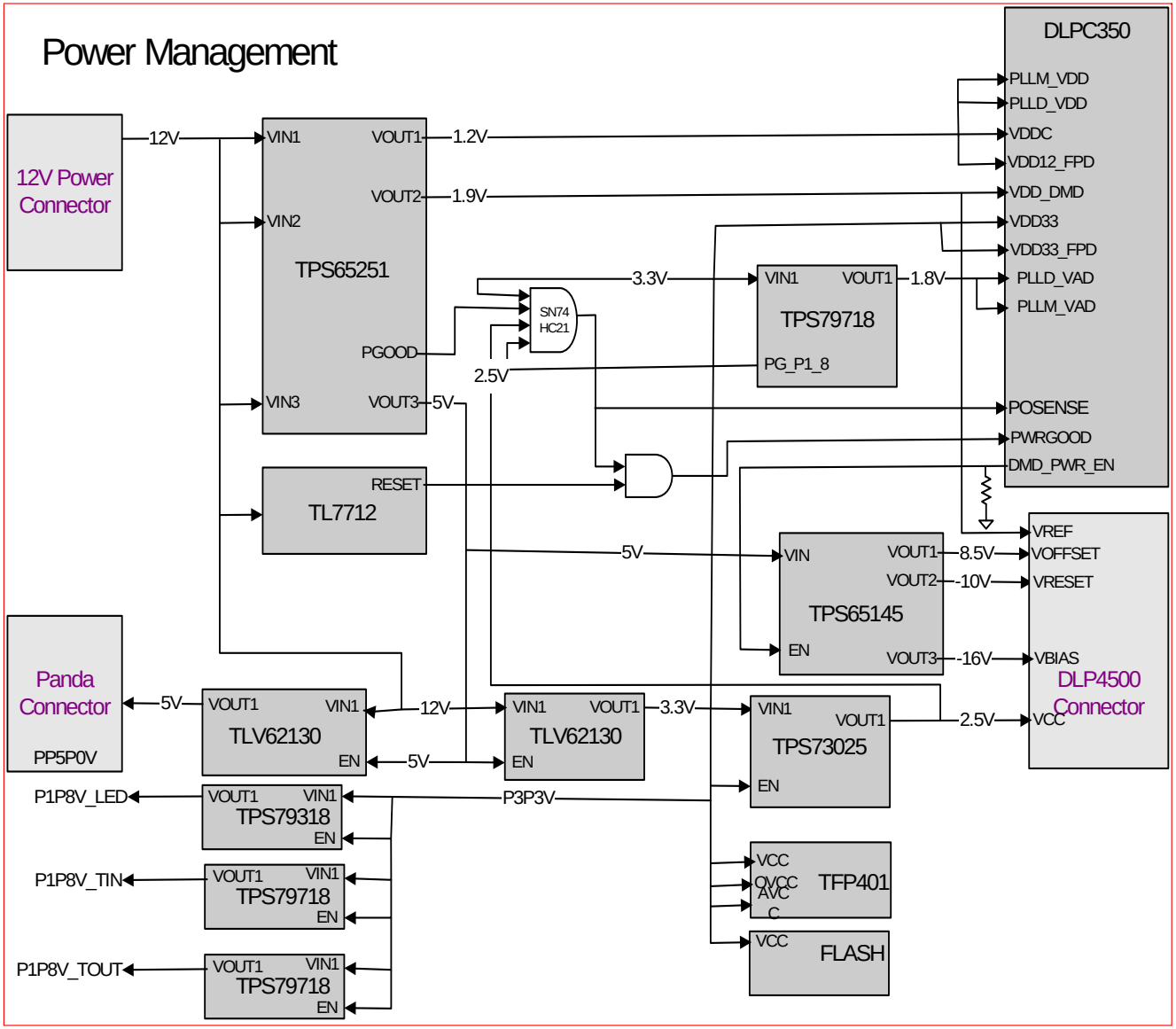

Power Management Block Diagram

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV E
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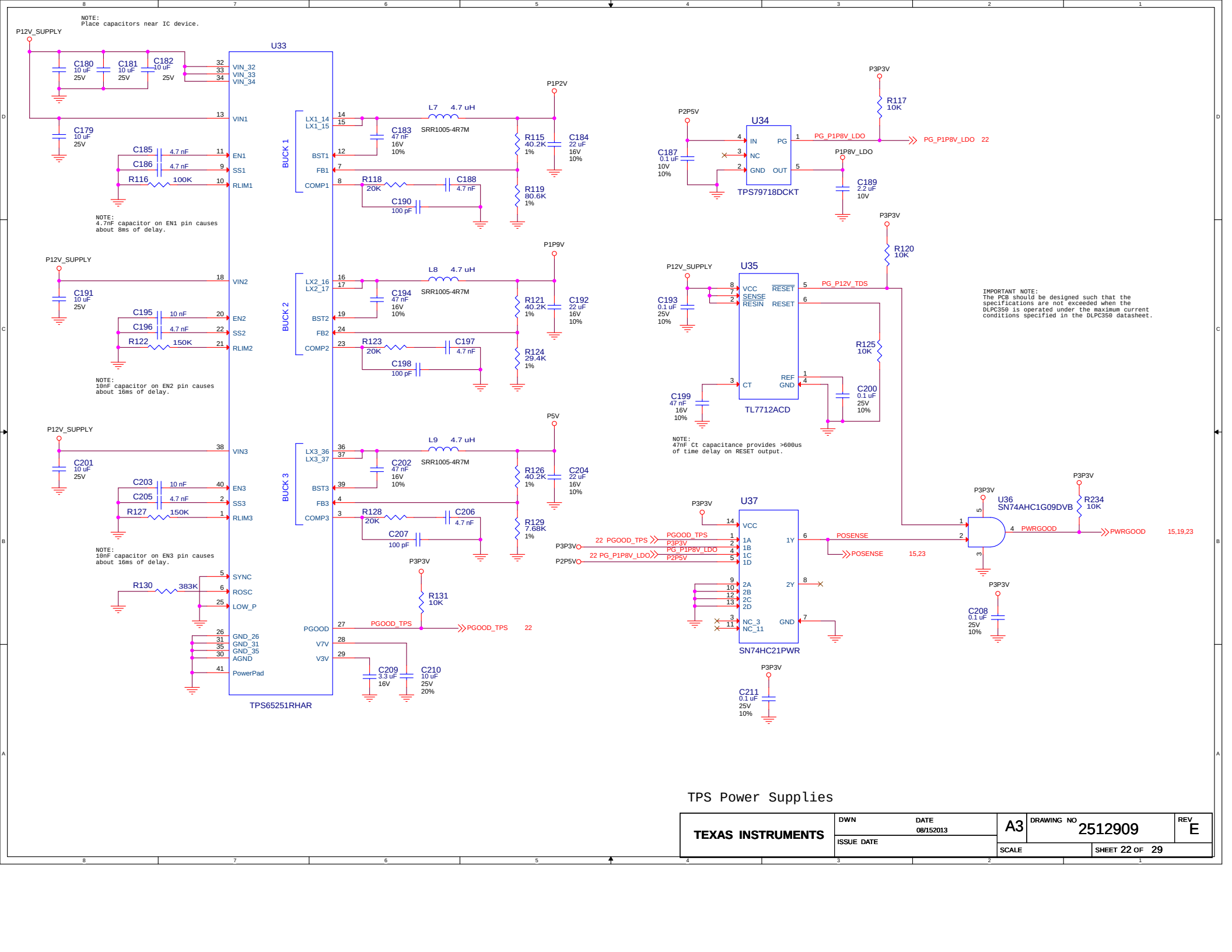
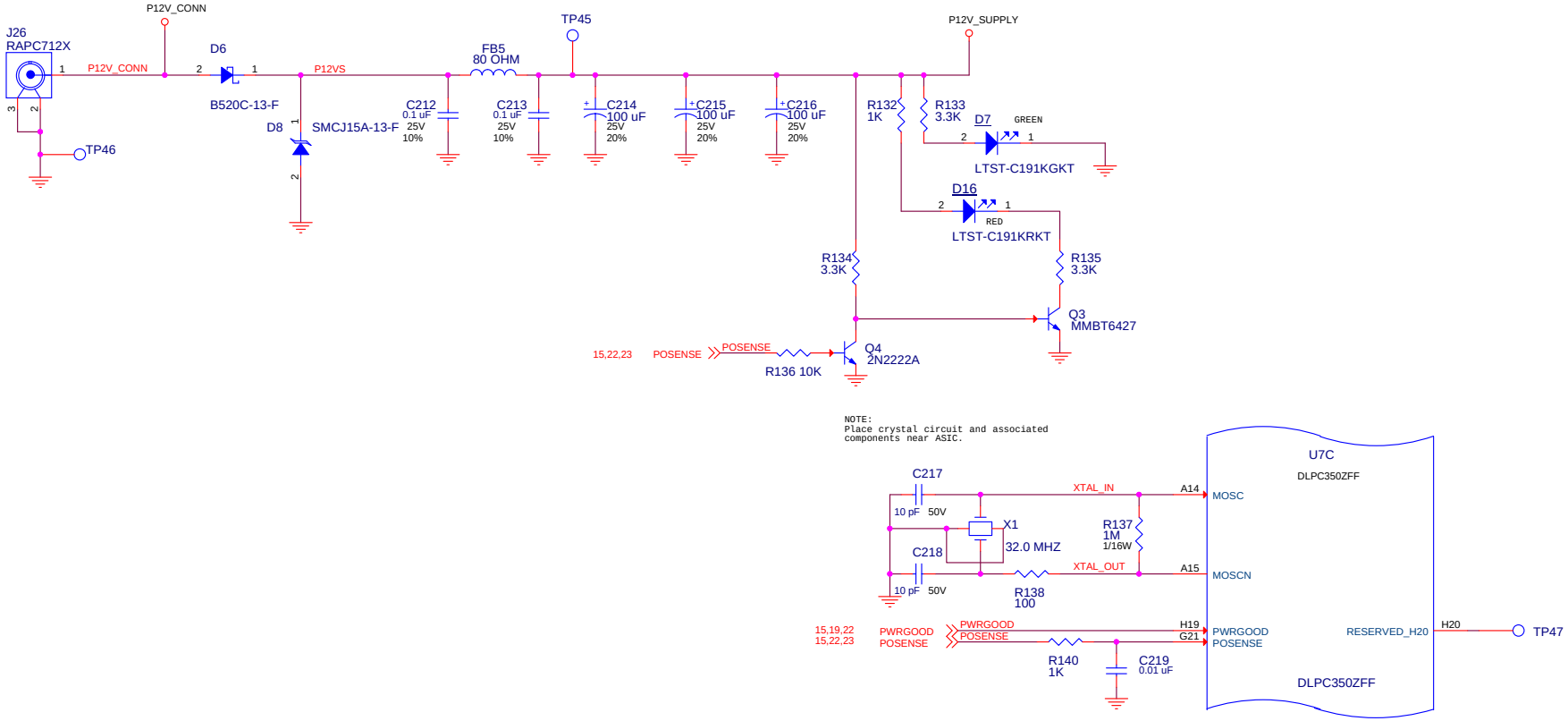


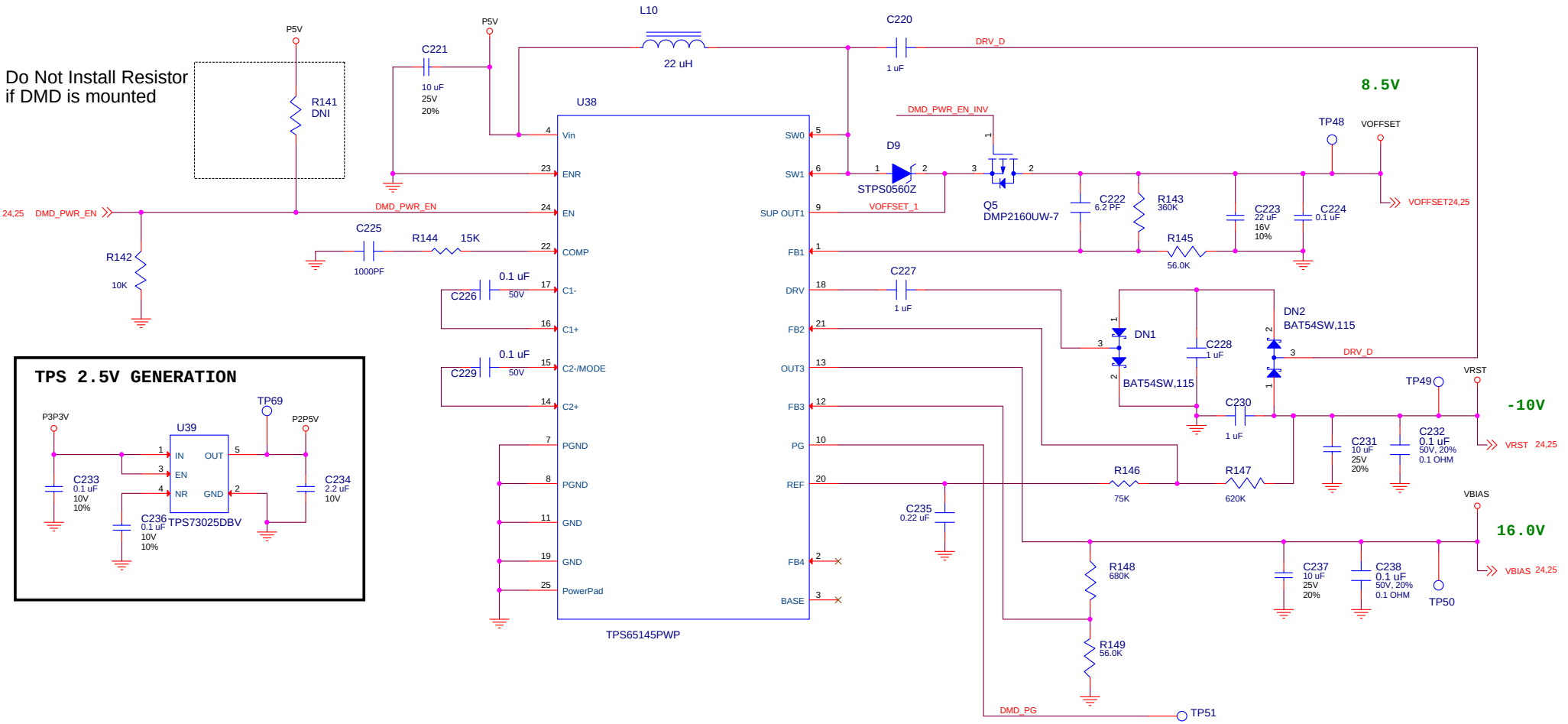
TPS Power Supplies

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV E
	ISSUE DATE		SCALE	SHEET 22 OF 29



Input Power and Oscillator Input

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV E
	ISSUE DATE		SCALE	SHEET 23 OF 29



DMD Power Supplies

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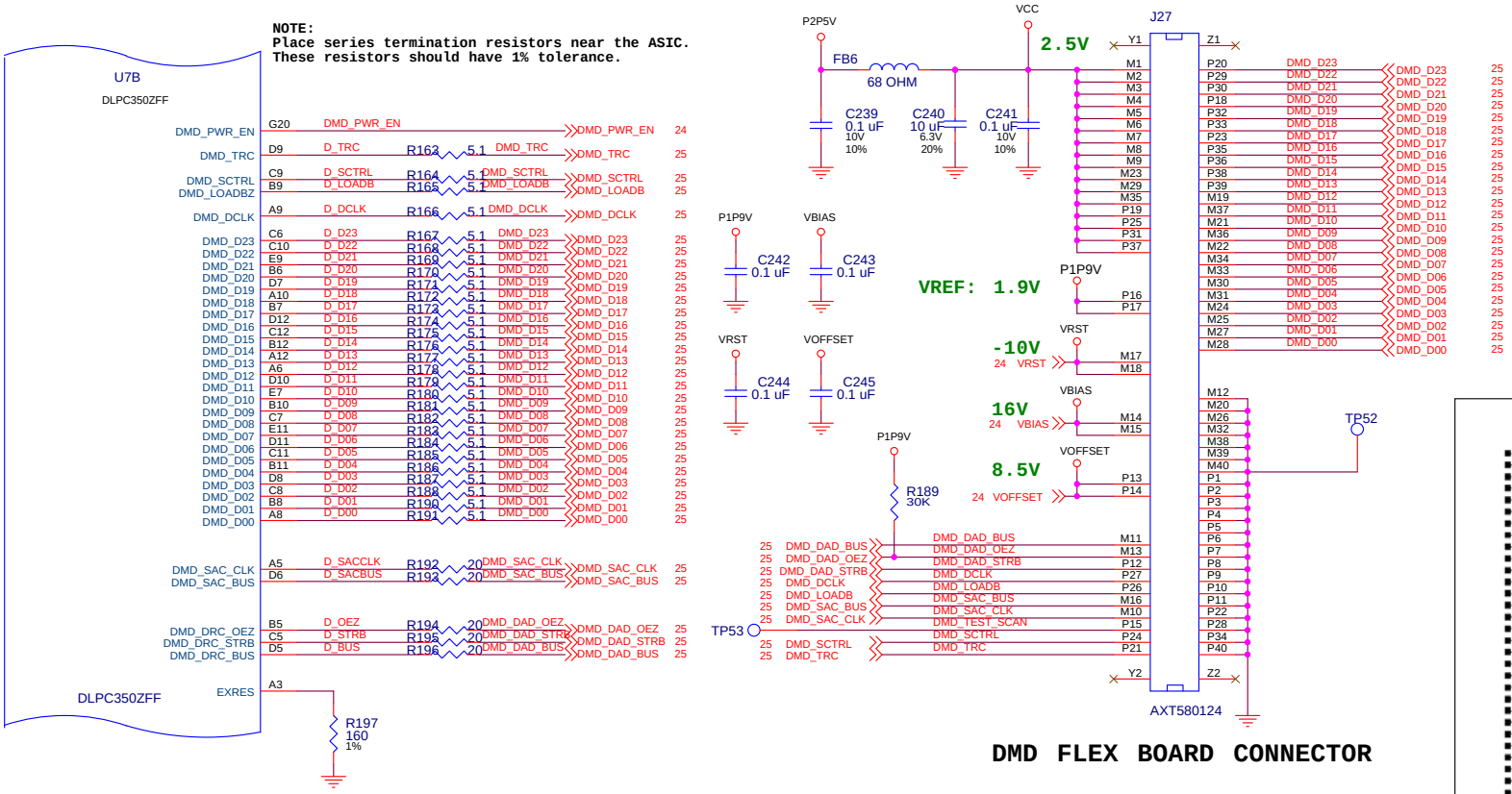
NOTE:
Place series termination resistors near the ASIC.
These resistors should have 1% tolerance.



DMD FLEX BOARD CONNECTOR

DMD FLEX BOARD CONNECTOR PINOUT

DMD Flex Interface

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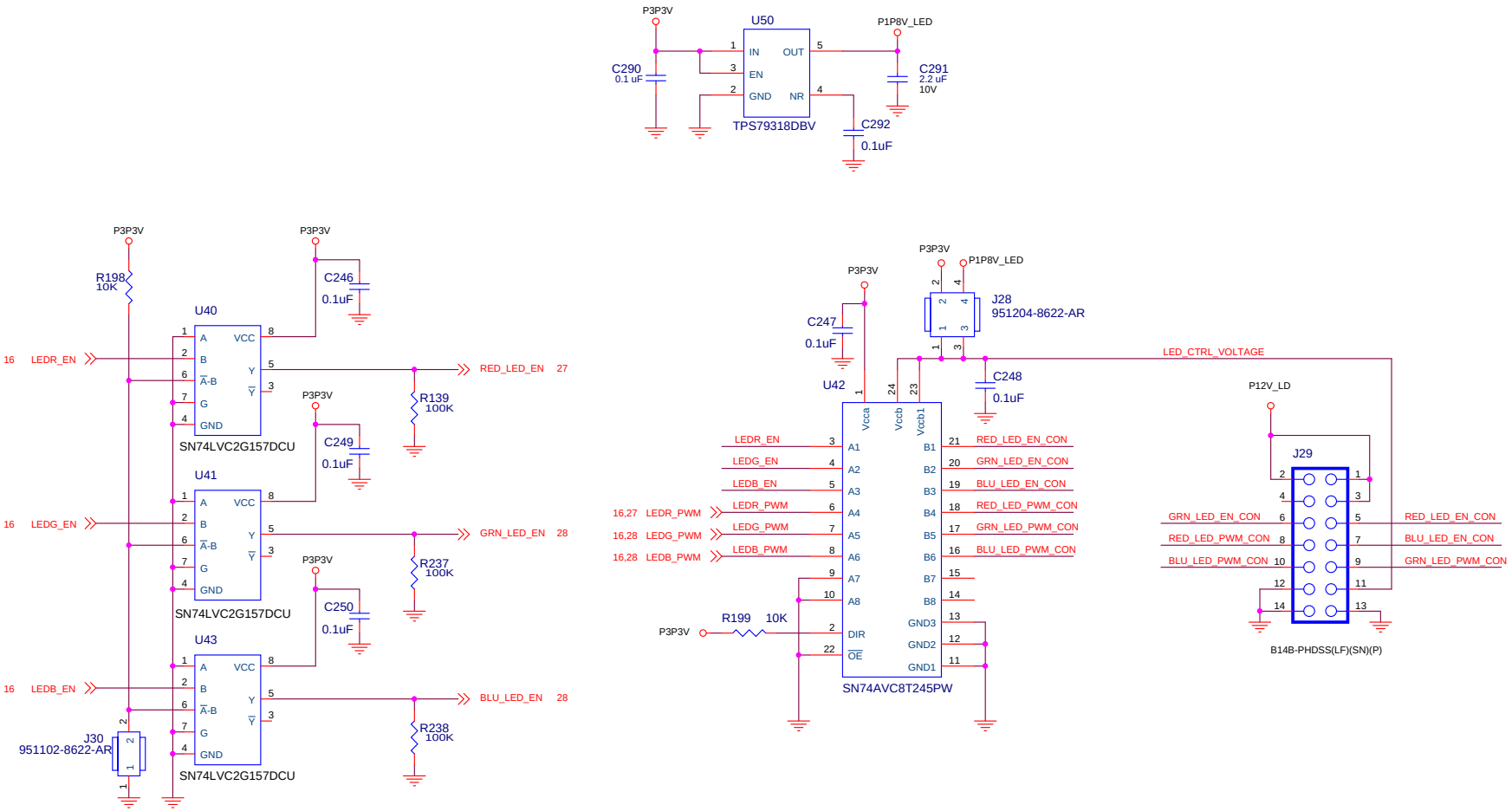
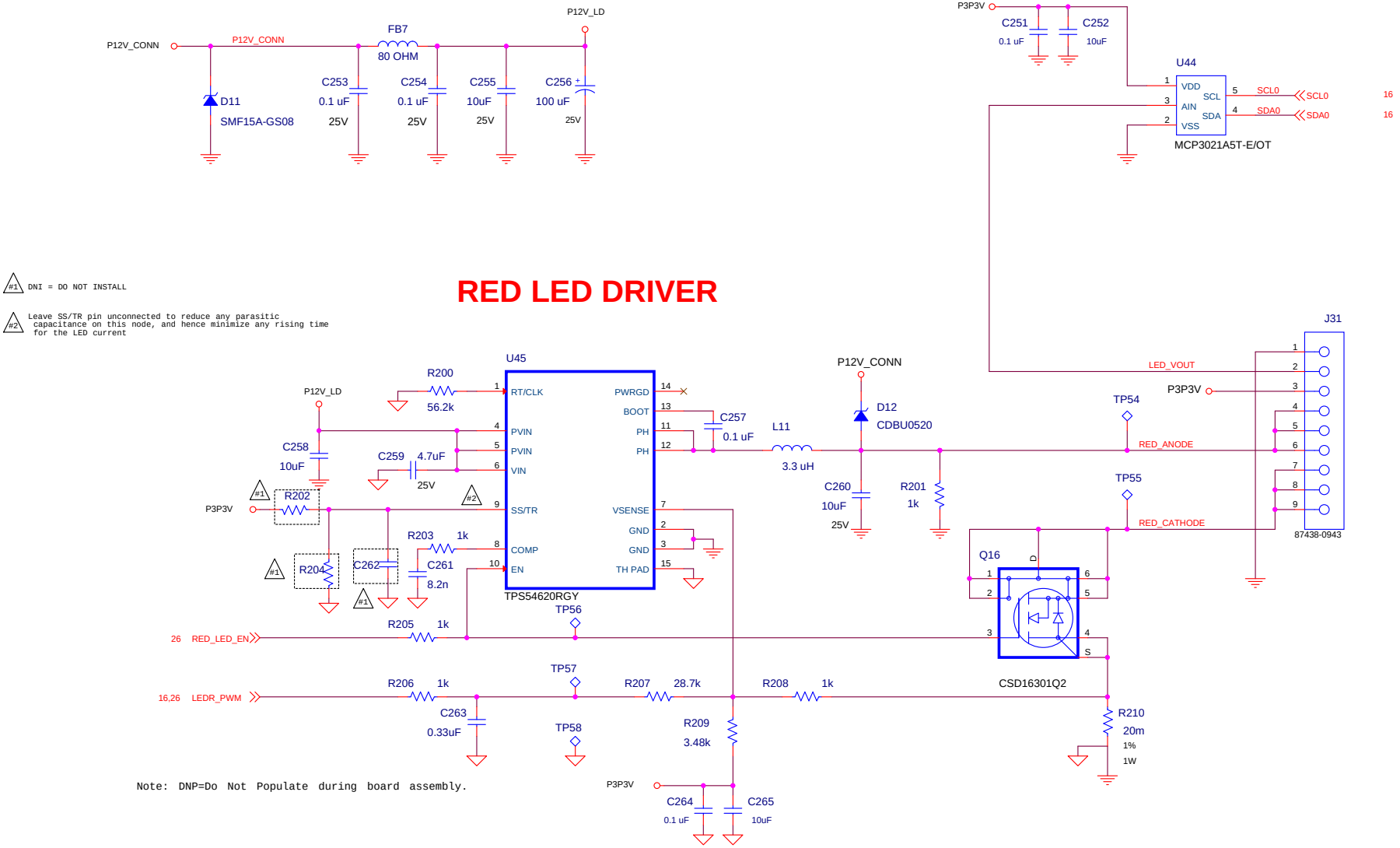
	ISSUE DATE			SCALE	SHEET 25 OF 29



TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV E
	ISSUE DATE		SCALE	SHEET 26 OF 29	



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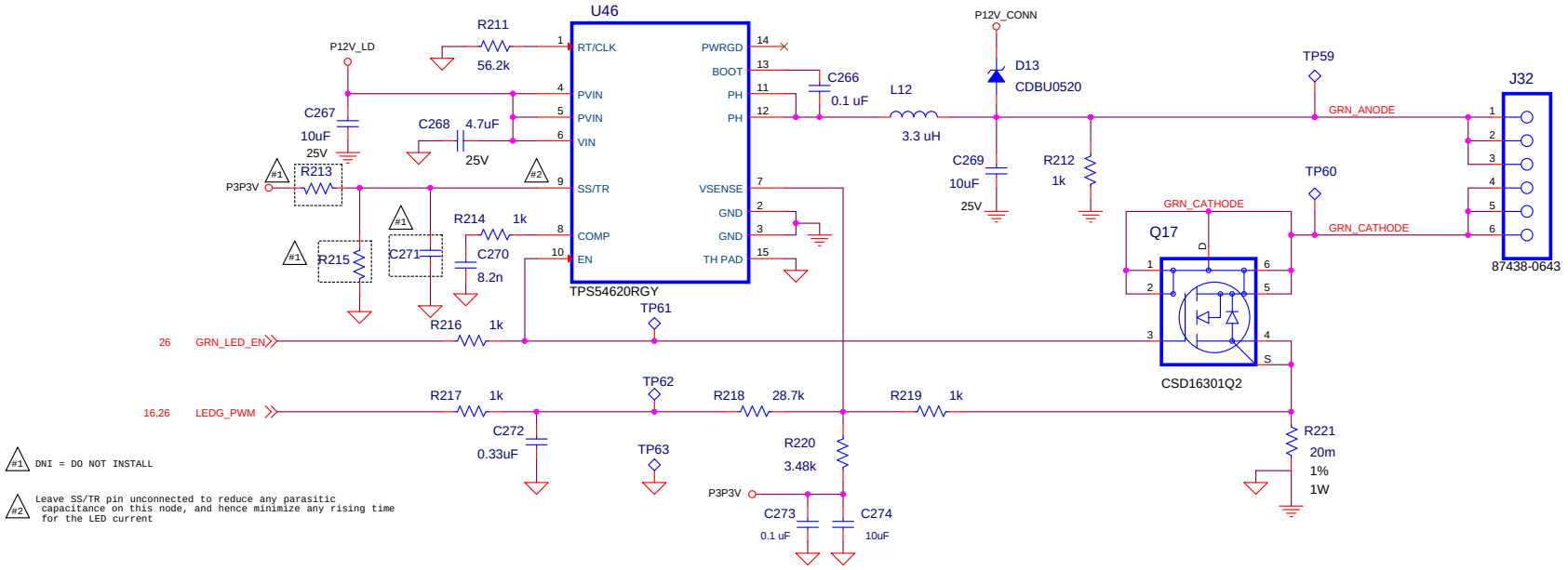
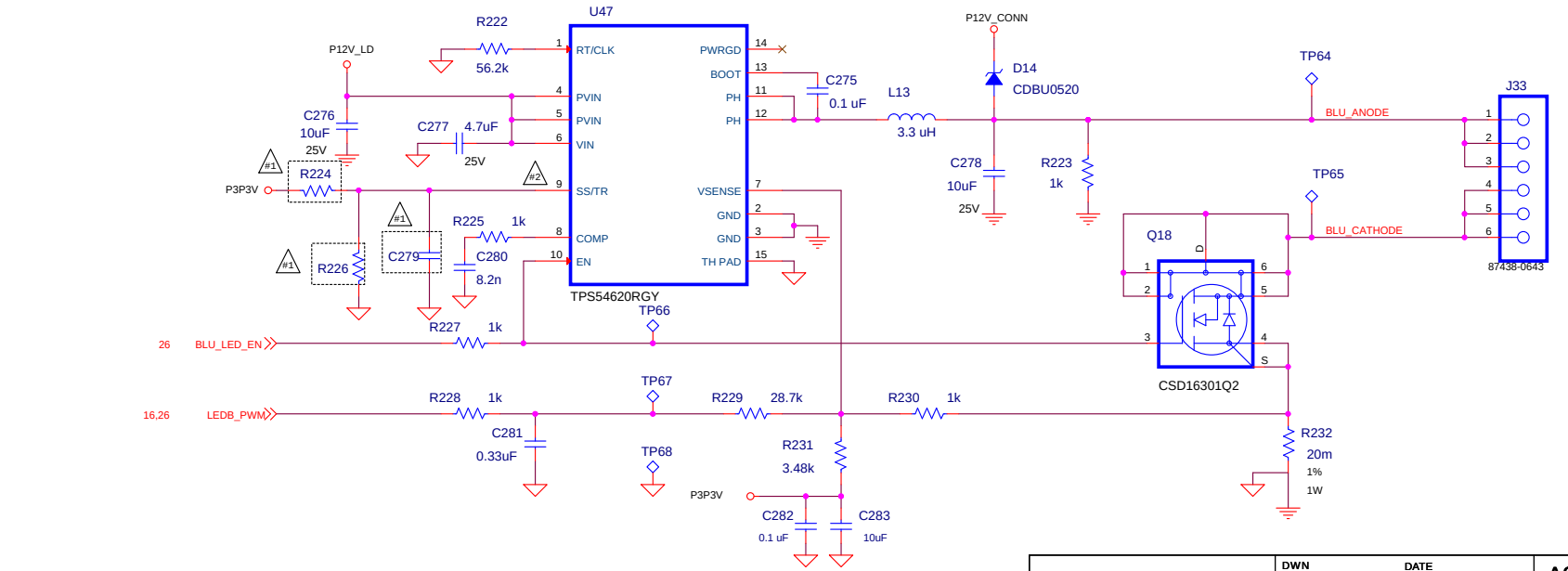
GREEN LED DRIVER



#1 DNI = DO NOT INSTALL

#2 Leave SS/TR pin unconnected to reduce any parasitic capacitance on this node, and hence minimize any rising time for the LED current

BLUE LED DRIVER



TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV E
	ISSUE DATE			SCALE	SHEET 28 OF 29

Revision History

Rev. A: Initial Release ~ 12/6/2012

Rev. B: Relelase ~ 06/18/2013

Rev. C: Relelase ~ 08/15/2013

All Sheets:
1) Cosmetic changes to reference designators, part values, and fonts
2) Remove unused Off Sheet Connectors
3) Add inter-sheet references
4) Replace obsolete parts in BOM

Sheet 7
1) Add Panda interface connection block diagram

Sheet 15
1) Correct SW2 part number

Sheet 18
1) Correct SW1 part number

Sheet 21
1) Up-date power management block diagram

Rev. D: Update ~ 04/7/2016

1) Changing C262, R202,R204, C279, R226, R224, C271, R215, R213, R78, R82, R19, R21, R9, R12, R17 to DNI (Do Not Install) MR 4/11/2016 .
2) Changing SW1 symbol type to push button and part# to TL3305AF260QG page 19. MR 4/11/2016.

Rev. E: Update ~ 01/11/2017

3) Original components used for D4 and D7 have been discontinued by manufacturer. A single diode solution is now in place for D4 and D7. New reference designators have been added D15, and D16. changes on page 16 and 23. MR 1/11/2017.
4) Original D10 part discontinued, Changed D10 from MAZ80330HL to DZ2J033M0L page 23. MR 1/11/2017.
5) Original J7 part discontinued, Changed J7 from MHDMI-19-02-H-TH-L-TR to 2001-1-2-21-00-BK page 4. MR 1/11/2017.

Schematic Revision History

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV E
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