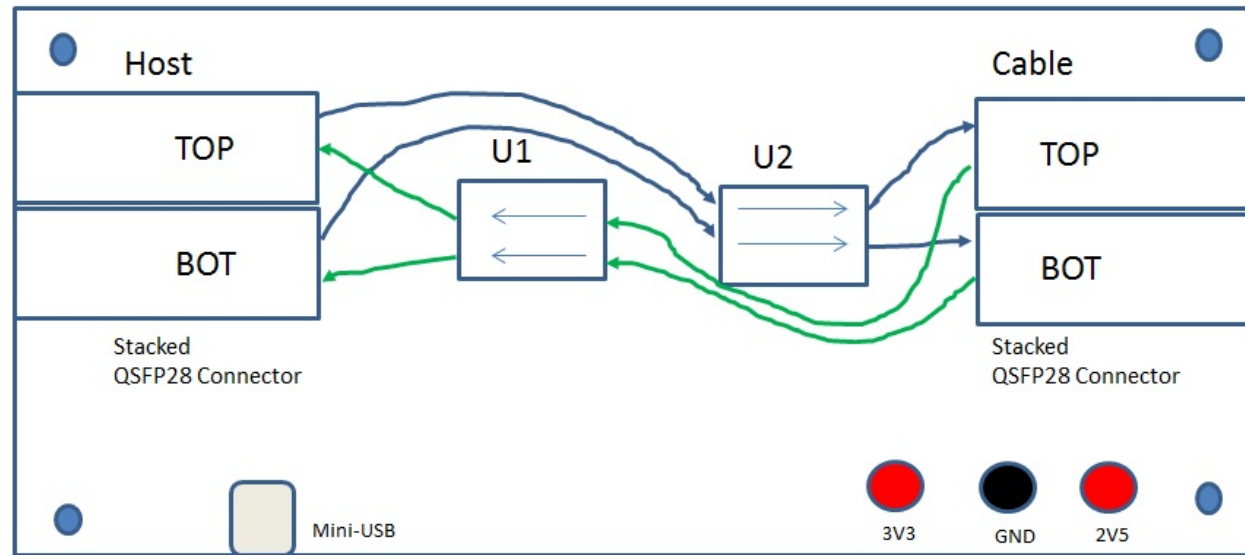


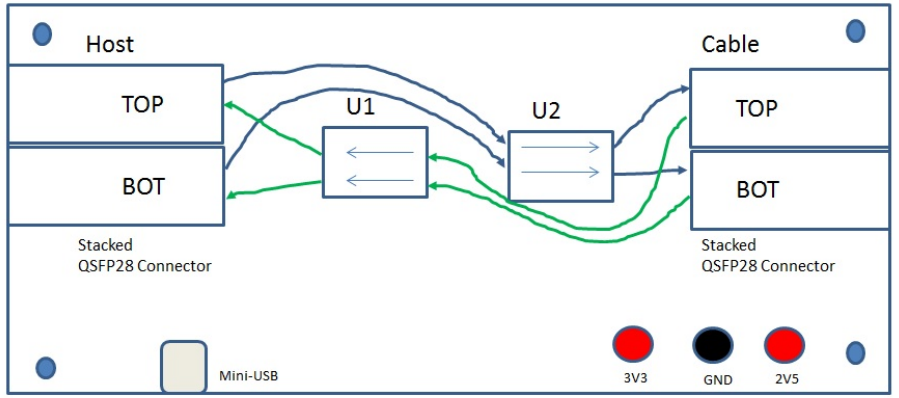
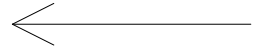
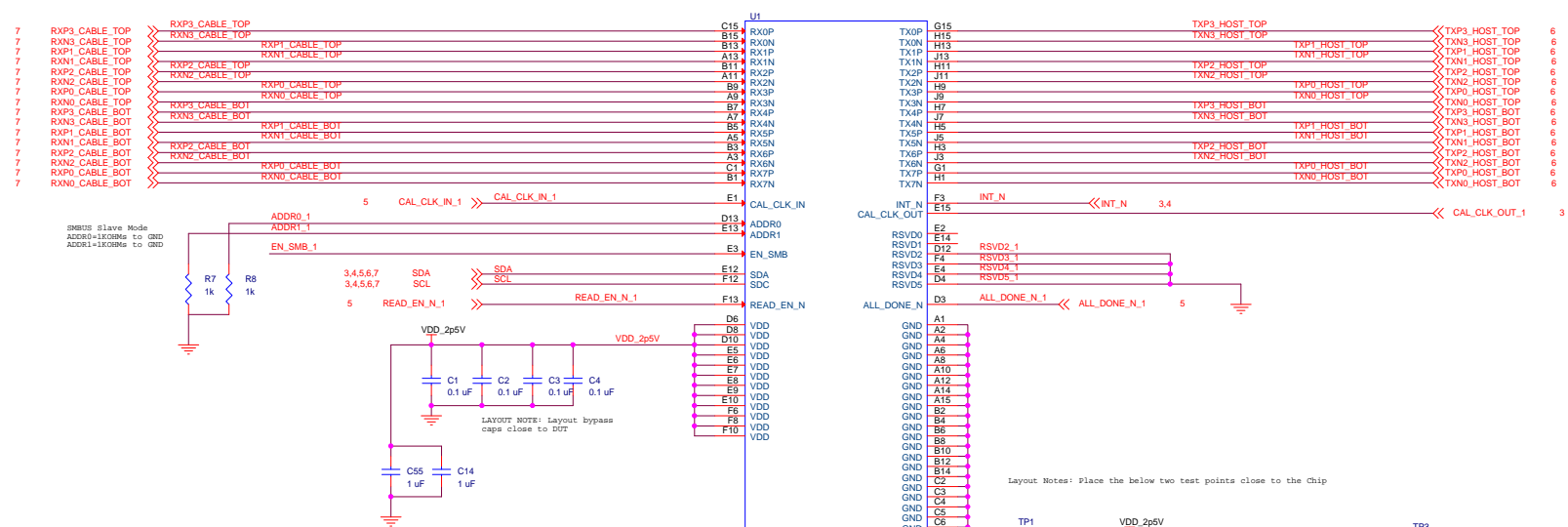
DS280BR810 QSFP Reference Design



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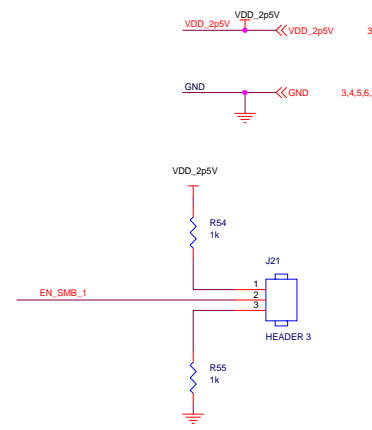
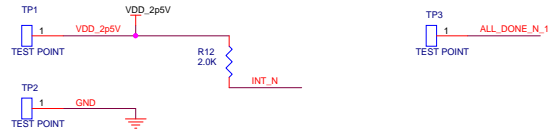
1st DS280BR810

Layout: All differential traces are to be routed with 100 ohm differential impedance



DS280BR8xx_DS280DF8xx

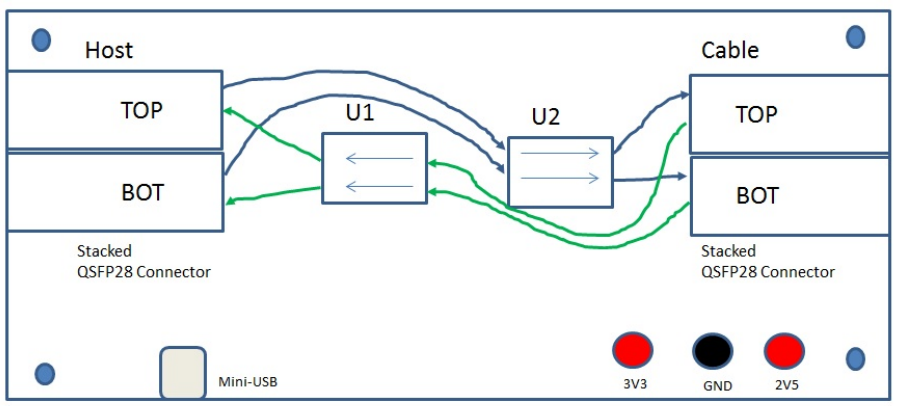
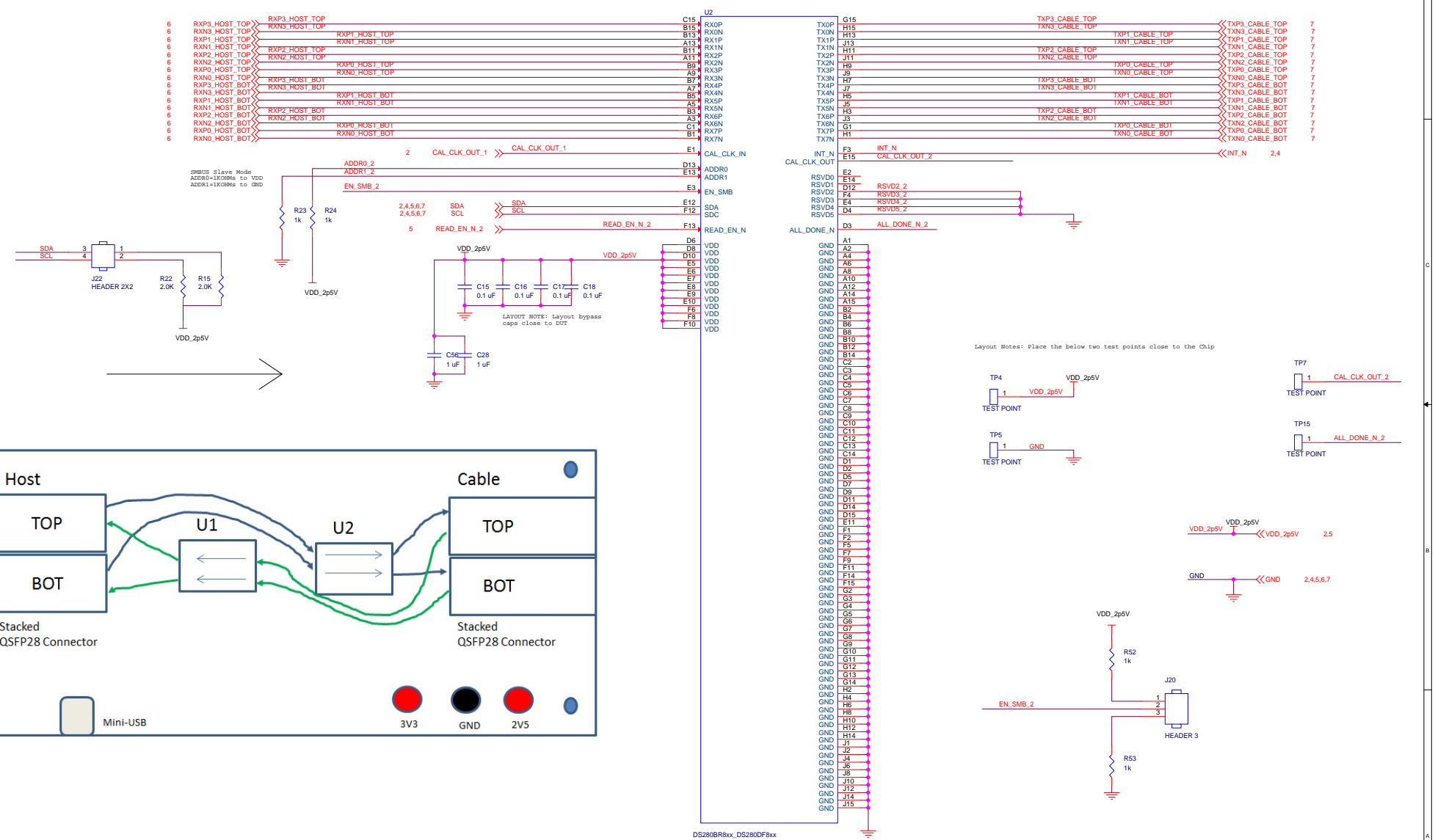
Layout Notes: Place the below two test points close to the Chip



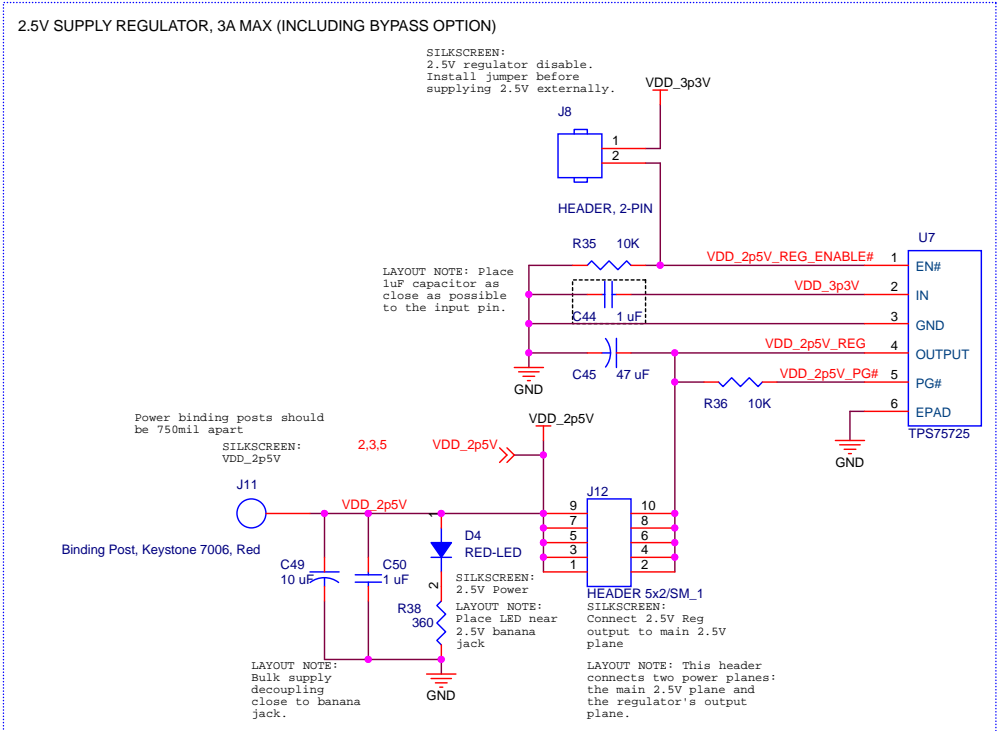
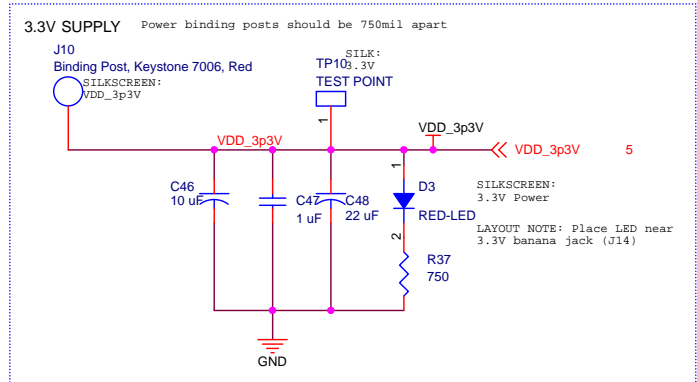
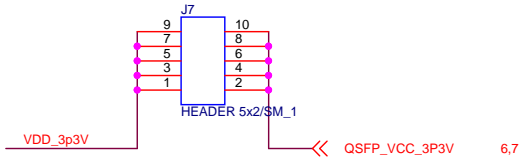
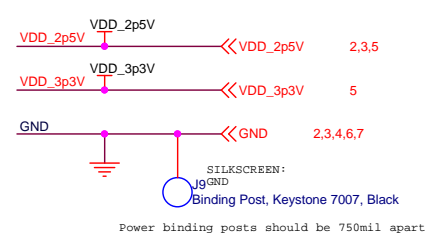
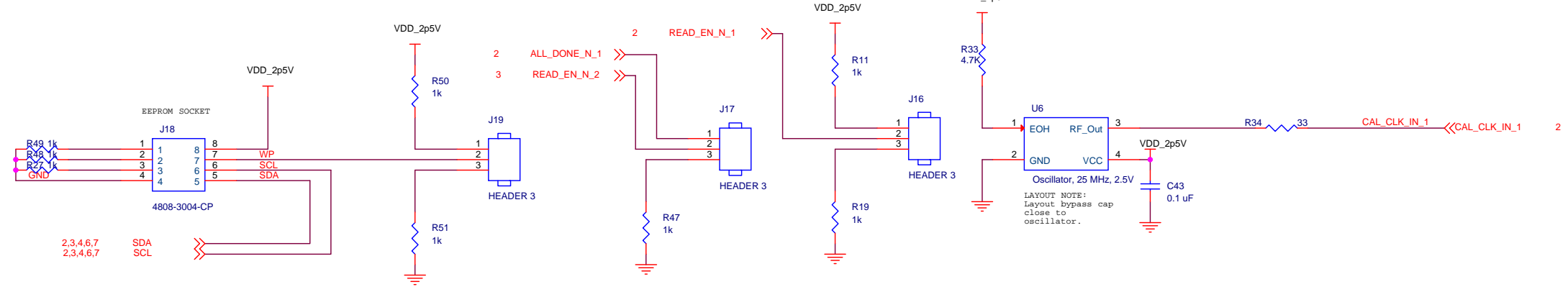
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2nd DS280BR810

Layout: All differential traces are to be routed with 100 ohm differential impedance

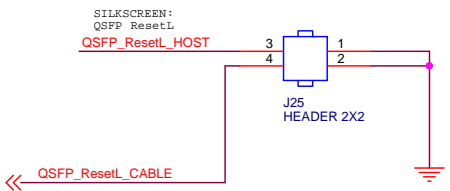
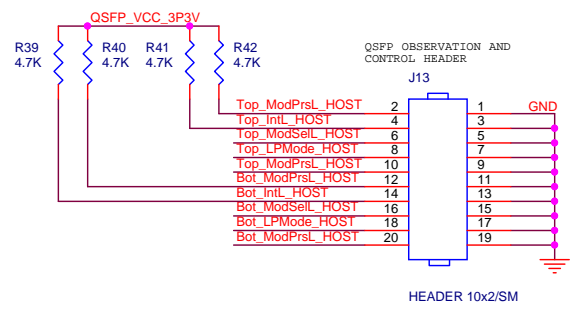
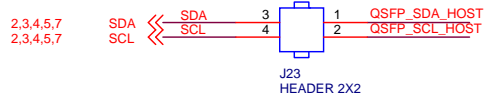
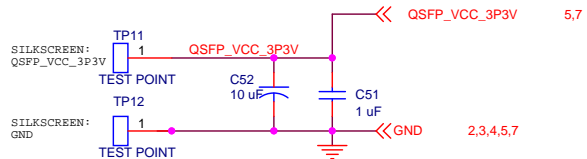


CLOCK AND POWER



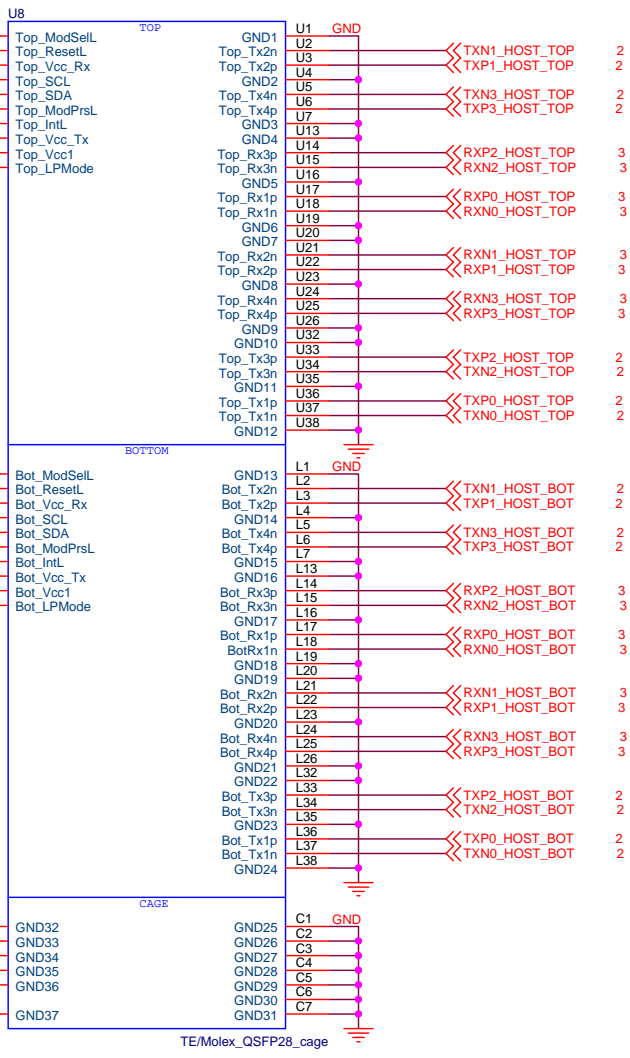
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QSFP28 HOST SIDE



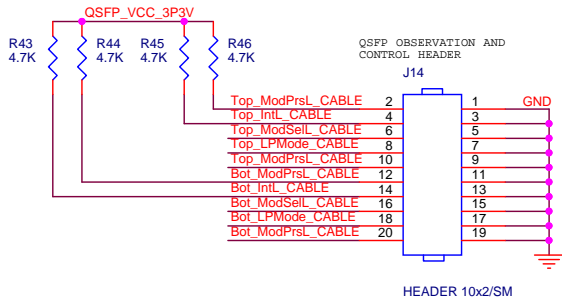
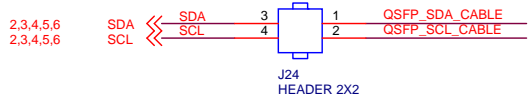
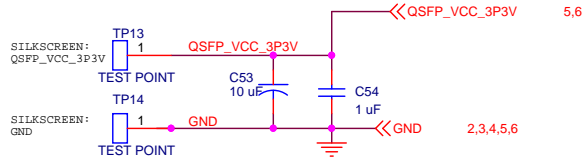
Top_ModSelL_HOST	U8
QSFP_ResetL_HOST	U9
QSFP_VCC_3P3V	U10
QSFP_SCL_HOST	U11
QSFP_SDA_HOST	U12
Top_ModPrsL_HOST	U27
Top_IntL_HOST	U28
QSFP_VCC_3P3V	U29
QSFP_VCC_3P3V	U30
Top_LPMoDe_HOST	U31

Bot_ModSelL_HOST	L8
QSFP_ResetL_HOST	L9
QSFP_VCC_3P3V	L10
QSFP_SCL_HOST	L11
QSFP_SDA_HOST	L12
Bot_ModPrsL_HOST	L27
Bot_IntL_HOST	L28
QSFP_VCC_3P3V	L29
QSFP_VCC_3P3V	L30
Bot_LPMoDe_HOST	L31



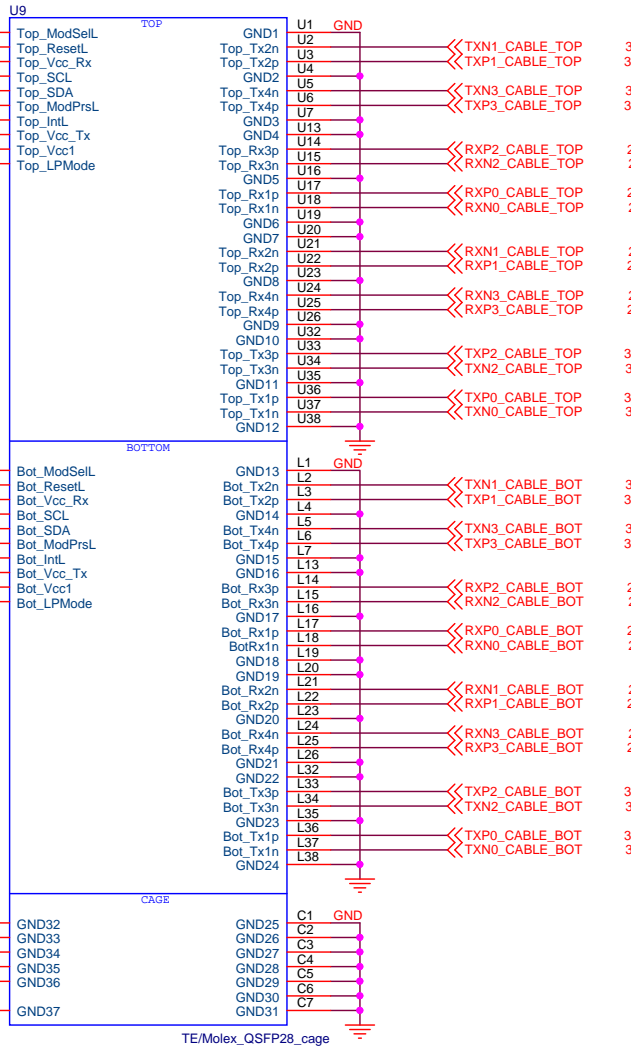
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QSFP28 Cable SIDE



Top_ModSelL_CABLE	U8
QSFP_ResetL_CABLE	U9
QSFP_VCC_3P3V	U10
QSFP_SCL_CABLE	U11
QSFP_SDA_CABLE	U12
Top_ModPrsL_CABLE	U27
Top_InIL_CABLE	U28
QSFP_VCC_3P3V	U29
QSFP_VCC_3P3V	U30
Top_LPMode_CABLE	U31

Bot_ModSelL_CABLE	L8
QSFP_ResetL_CABLE	L9
QSFP_VCC_3P3V	L10
QSFP_SCL_CABLE	L11
QSFP_SDA_CABLE	L12
Bot_ModPrsL_CABLE	L27
Bot_InIL_CABLE	L28
QSFP_VCC_3P3V	L29
QSFP_VCC_3P3V	L30
Bot_LPMode_CABLE	L31



6 QSFP_ResetL_CABLE

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