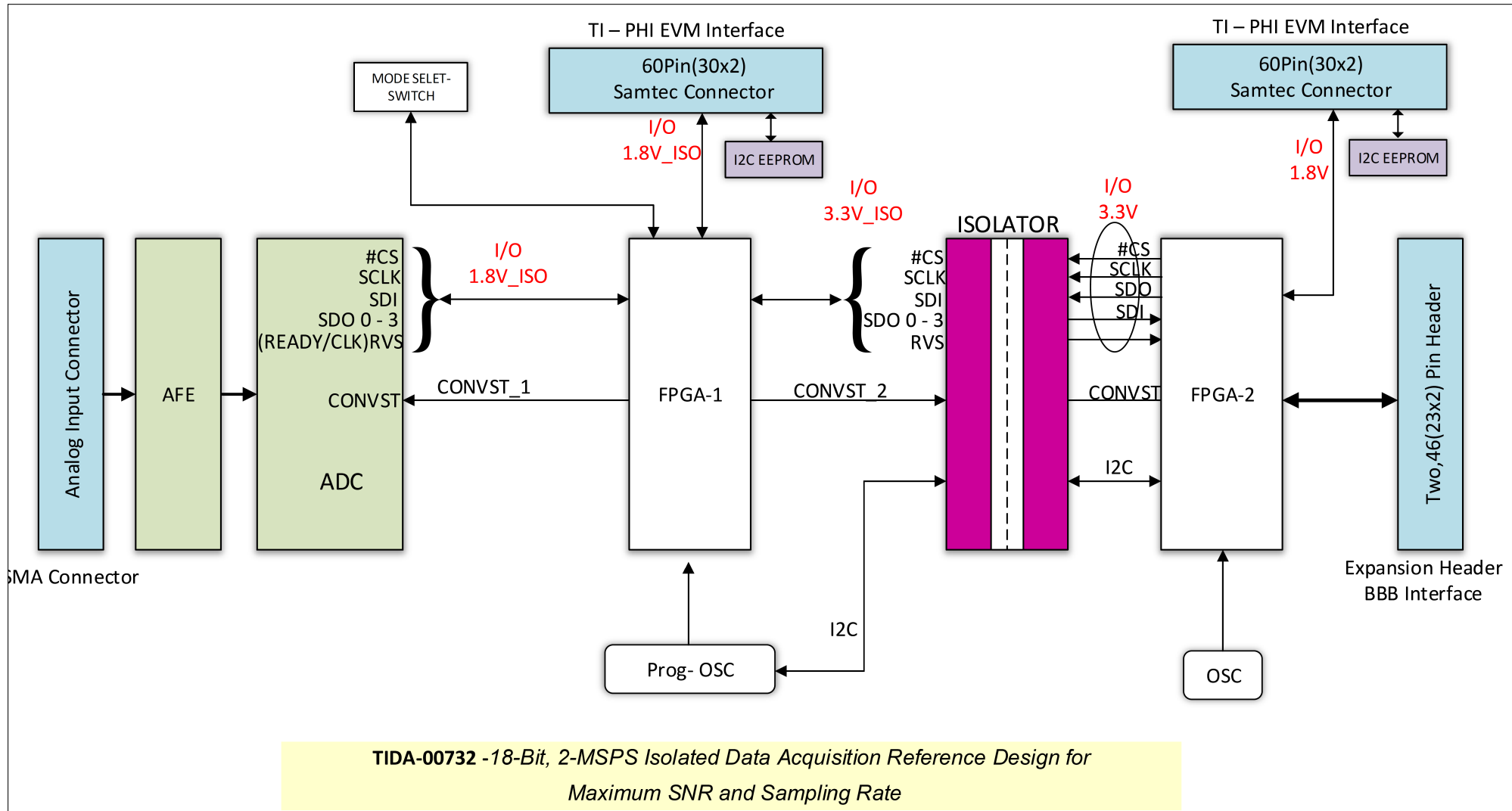


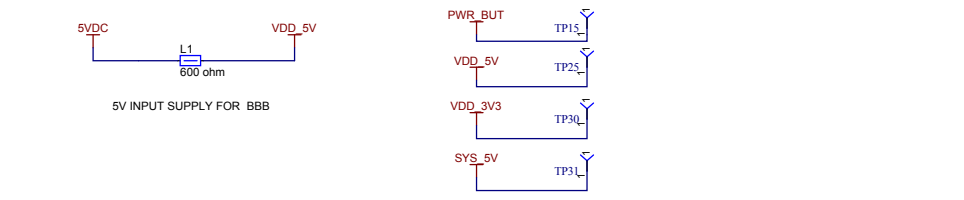
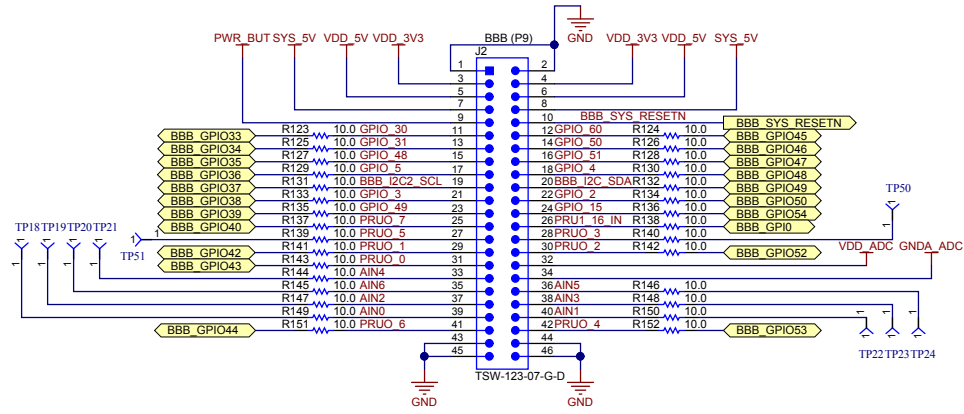
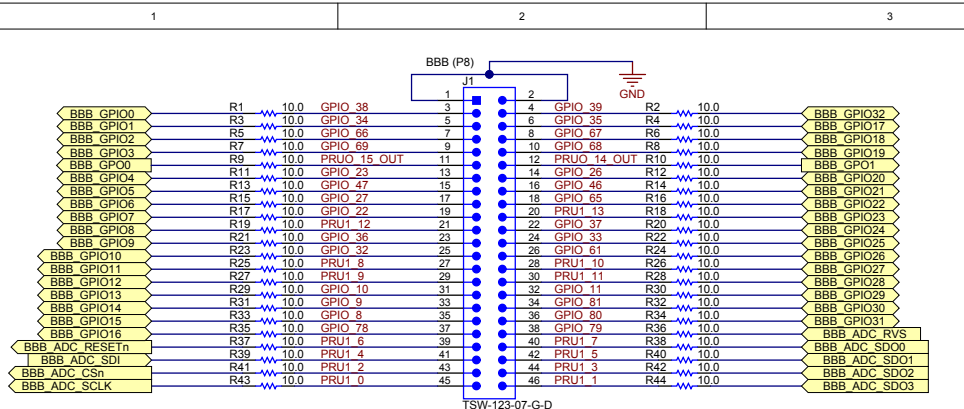
| Revision History |       |               |             |       |
|------------------|-------|---------------|-------------|-------|
| Rev              | ECN # | Approved Date | Approved by | Notes |
| N/A              | N/A   | N/A           | N/A         | N/A   |



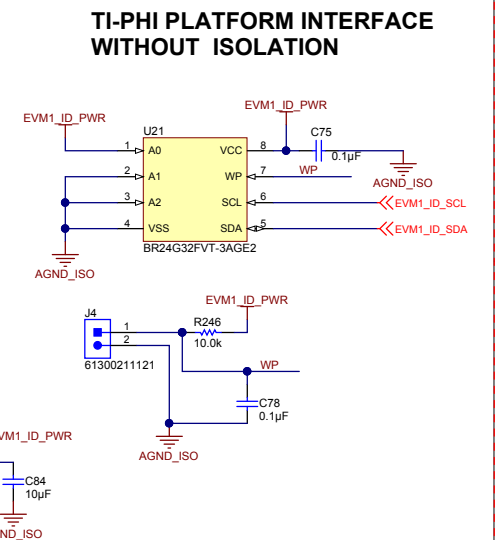
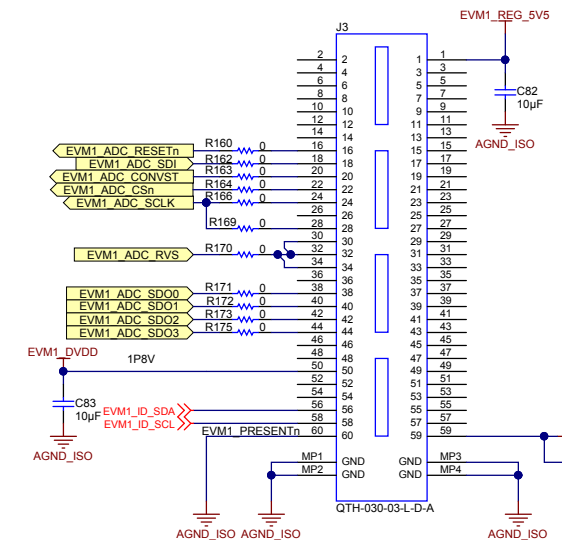
**TIDA-00732 -18-Bit, 2-MSPS Isolated Data Acquisition Reference Design for Maximum SNR and Sampling Rate**

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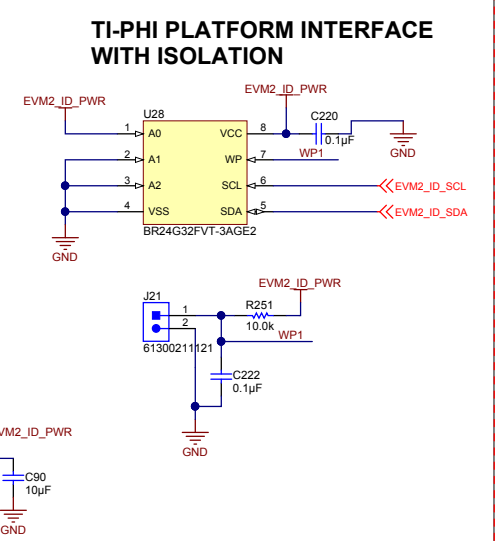
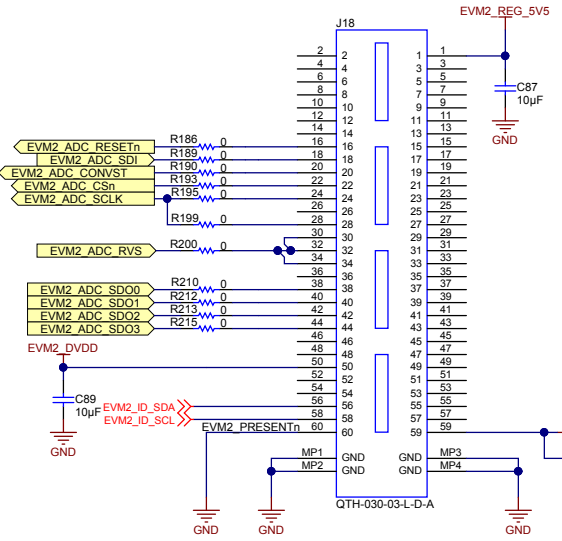
|                                   |  |                            |
|-----------------------------------|--|----------------------------|
| Orderable: N/A                    | Designed for: Public Release   | Mod. Date: 5/26/2016       |
| TID #: TID-00732                  | Project Title: Jitter minimizing techniques for digitally isolated high    |                            |
| Number: TIDA-00732                | Rev: E1  | Sheet Title: Block Diagram |
| SVN Rev: Version control disabled | Assembly Variant: ADS9110 w/REF5045  | Sheet: 1 of 10             |
| Drawn By: Anbu Mani               | File: TIDA-00732_CoverSheet_SchDoc   | Size: B                    |
| Engineer: Anbu Mani               | Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a> | © Texas Instruments, 2015  |

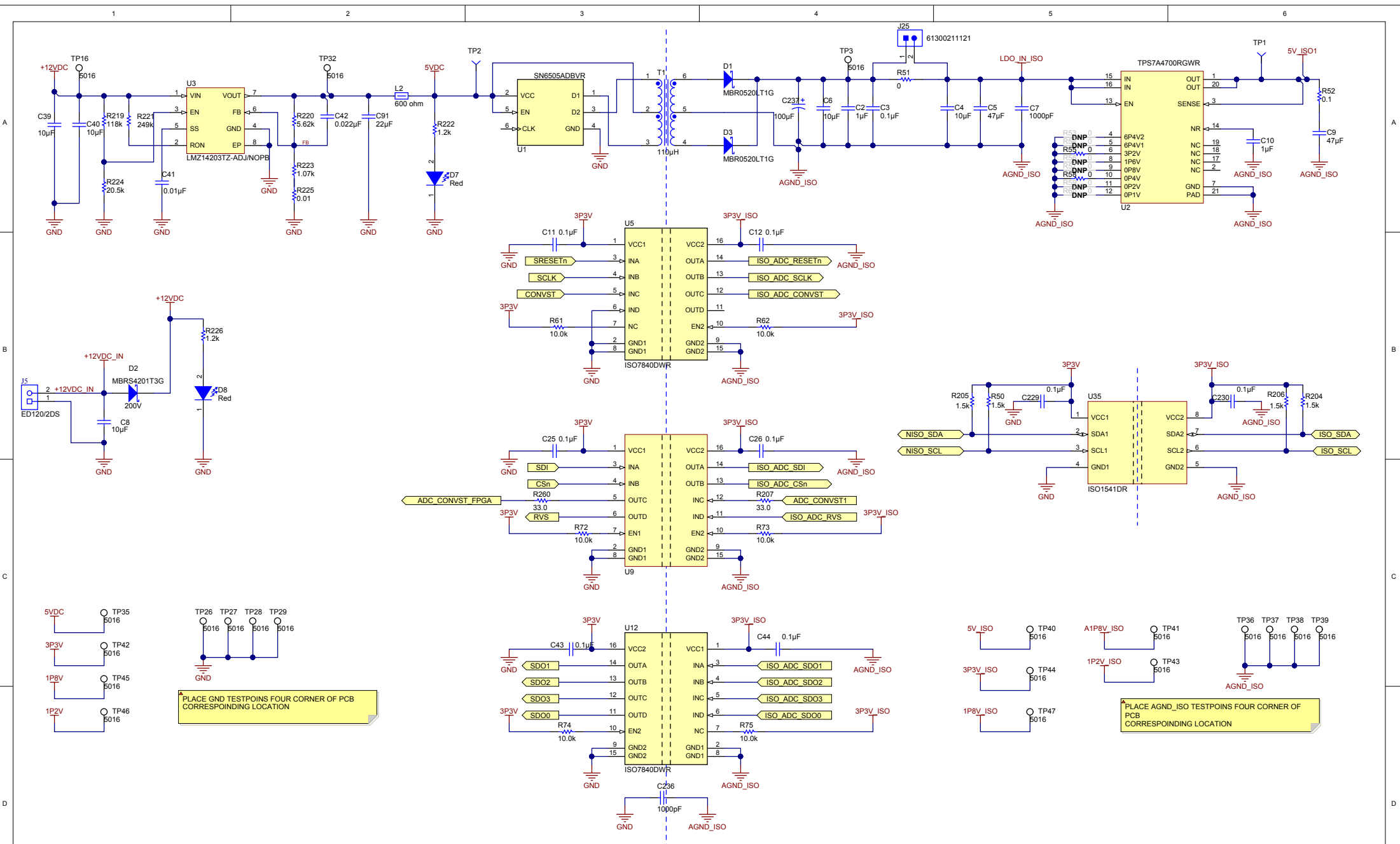


**BEAGLE BONE BLACK INTERFACE WITH ISOLATION**



**TI-PIHI PLATFORM INTERFACE WITH ISOLATION**





PLACE GND TESTPOINTS FOUR CORNER OF PCB CORRESPONDING LOCATION

PLACE AGND\_ISO TESTPOINTS FOUR CORNER OF PCB CORRESPONDING LOCATION

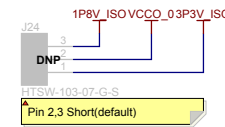
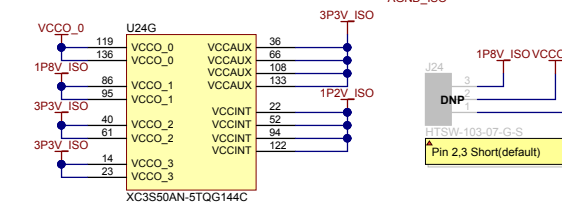
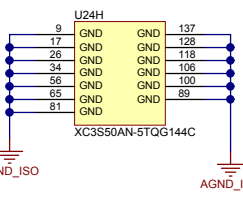
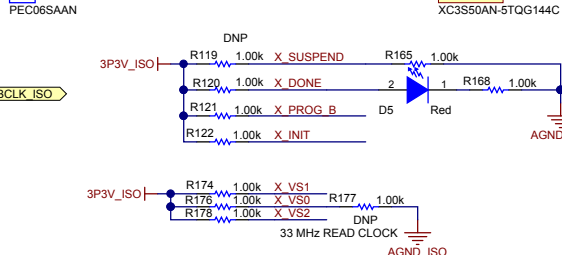
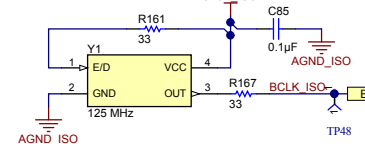
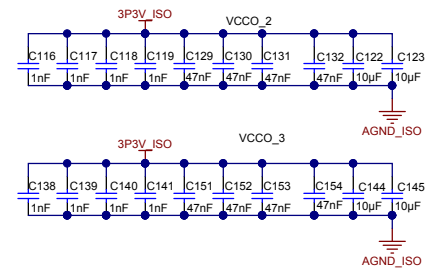
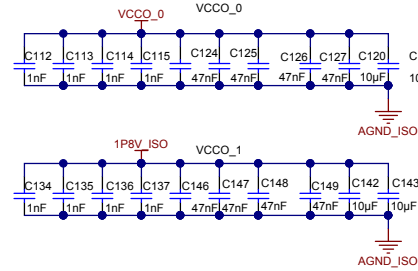
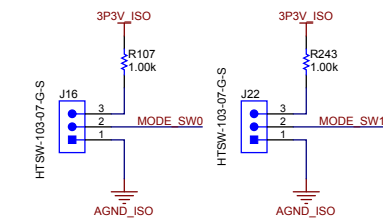
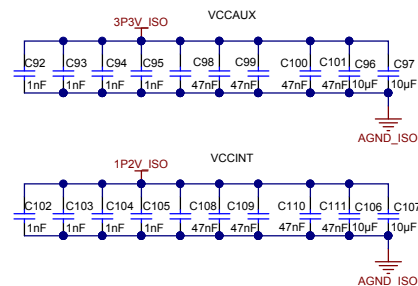
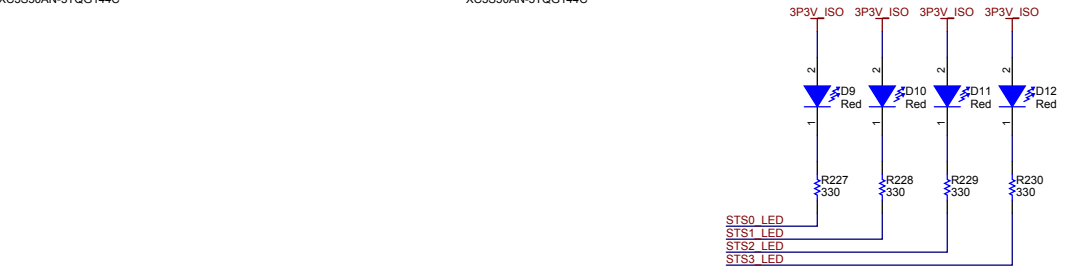
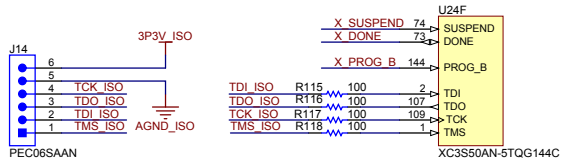
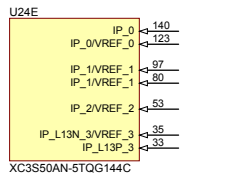
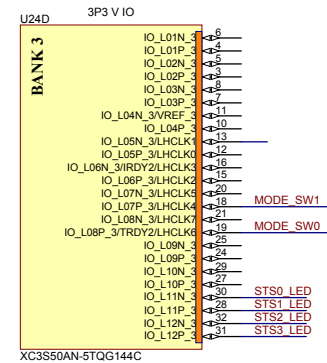
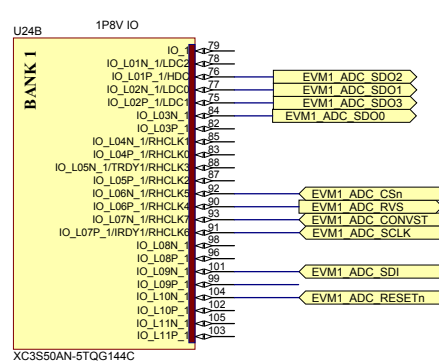
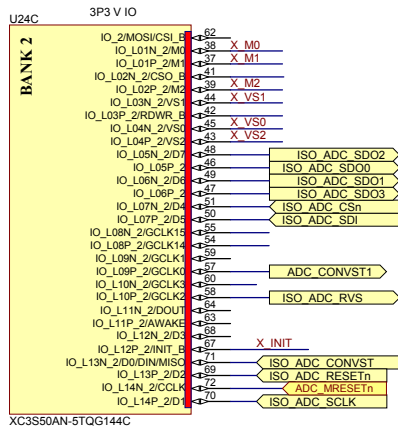
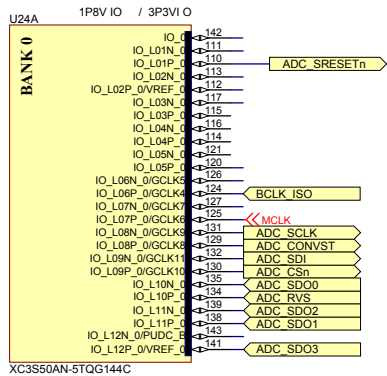
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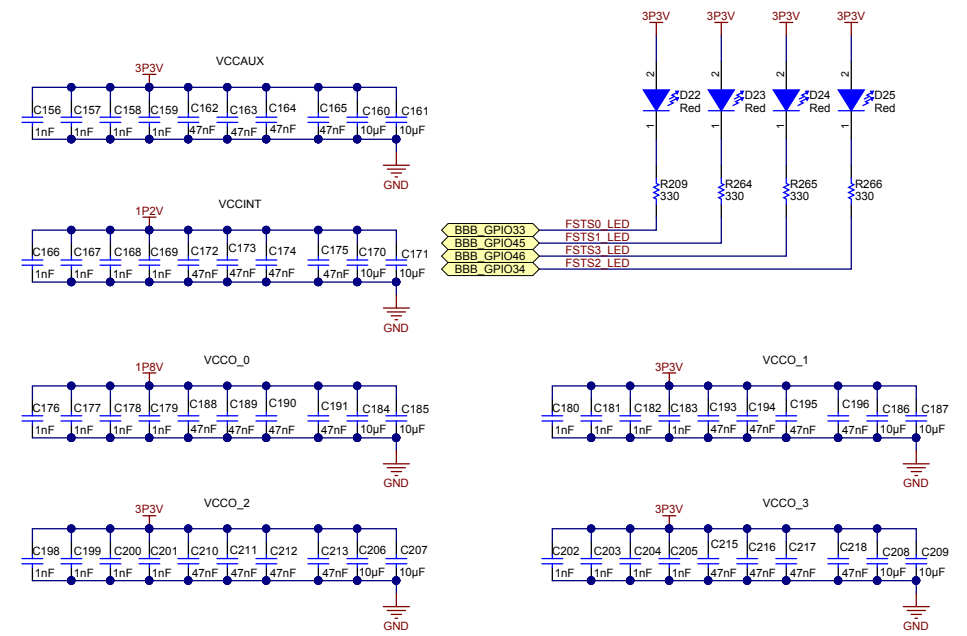
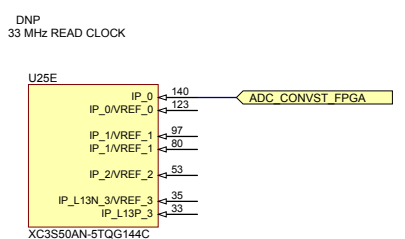
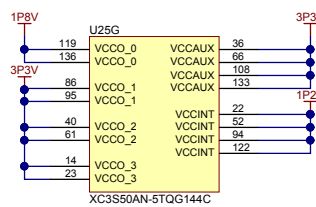
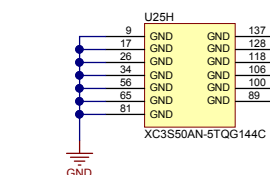
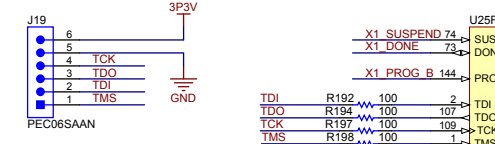
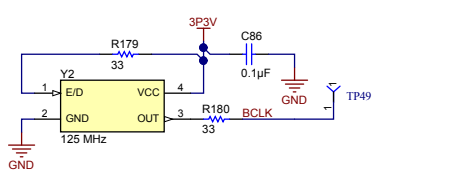
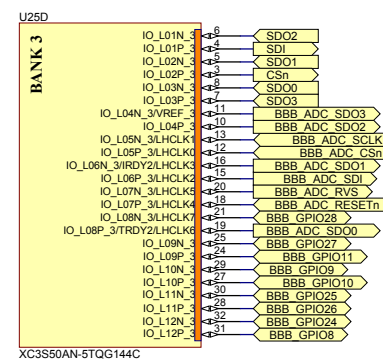
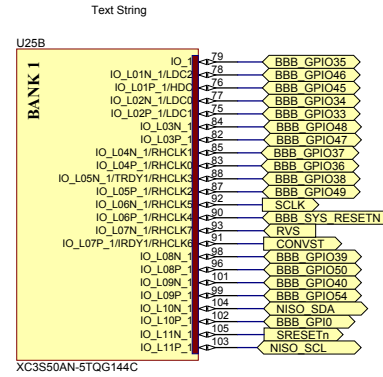
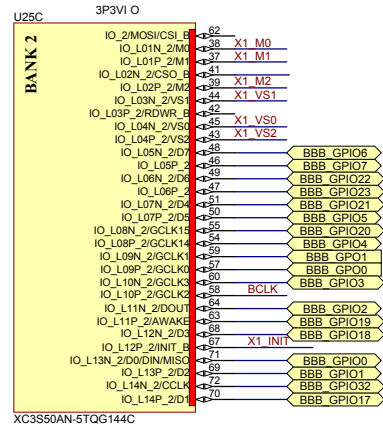
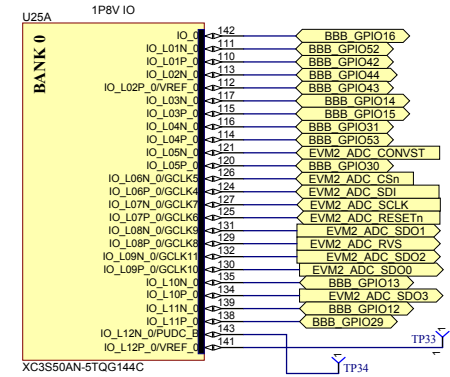
|                                   |  |                                |
|-----------------------------------|--|--------------------------------|
| Orderable: N/A                    | Designed for: Public Release   | Mod. Date: 2/27/2016           |
| TID #: TID-00732                  | Project Title: Jitter minimizing techniques for digitally isolated high    |                                |
| Number: TIDA-00732                | Rev: E1  | Sheet Title: Power & Isolators |
| SVN Rev: Version control disabled | Assembly Variant: ADS9110 w/REF5045  | Sheet: 3 of 10                 |
| Drawn By: Anbu Mani               | File: TIDA-00732_Isolator_SchDoc   | Size: B                        |
| Engineer: Anbu Mani               | Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a> |                                |





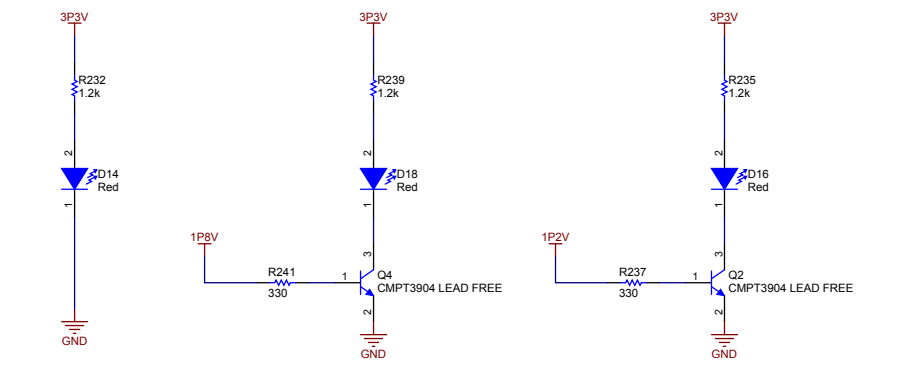
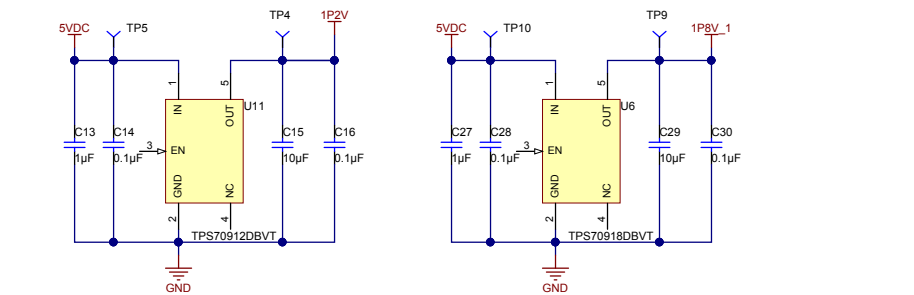
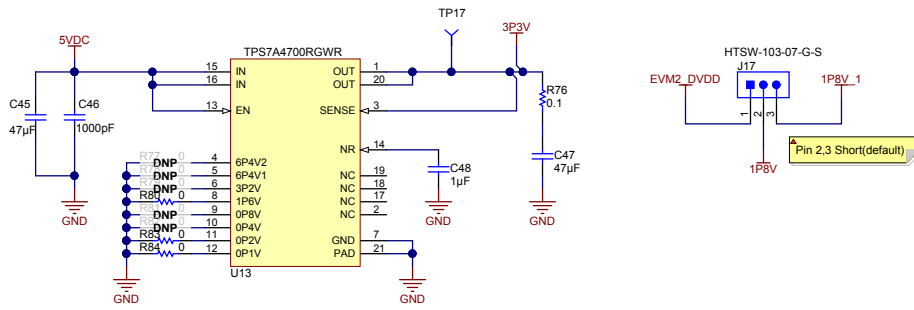


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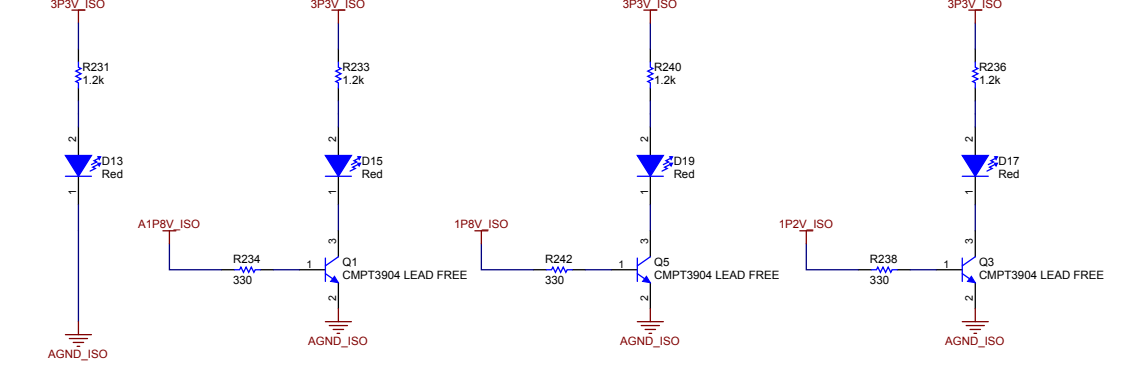
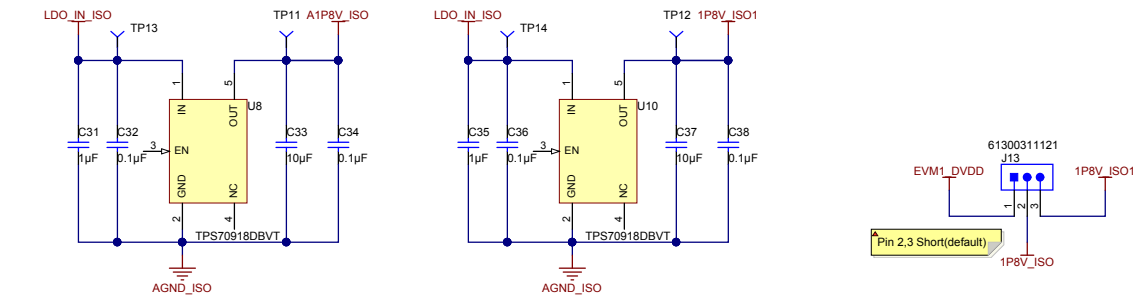
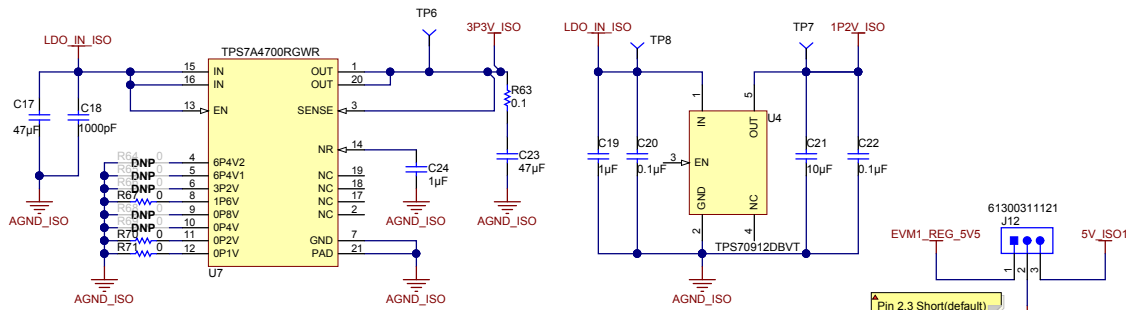


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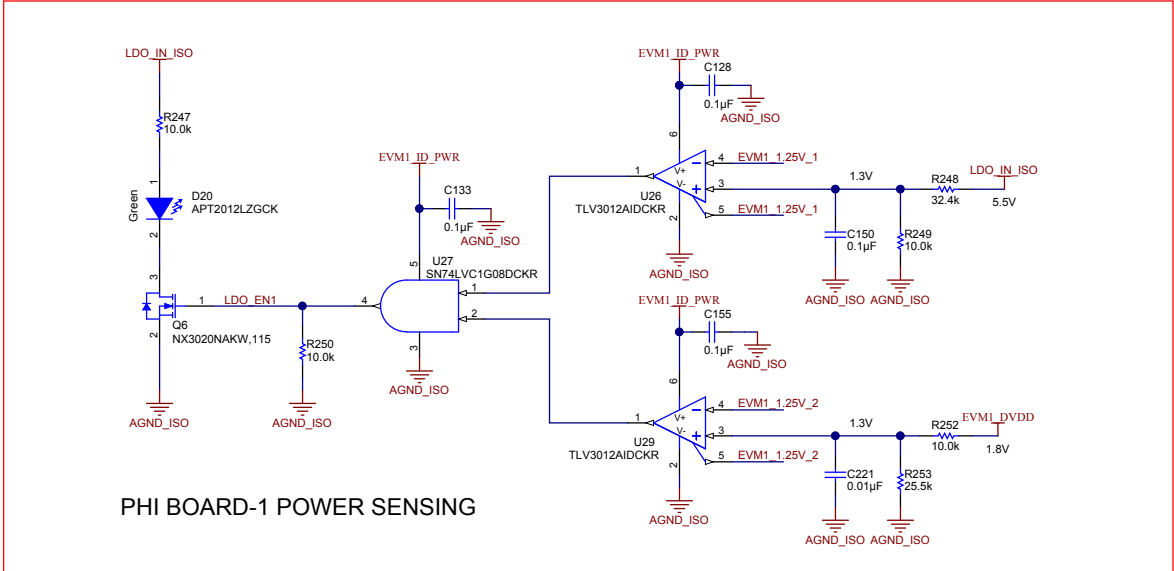
|                                   |  |                                       |
|-----------------------------------|--|---------------------------------------|
| Orderable: N/A                    | Designed for: Public Release   | Mod. Date: 2/26/2016                  |
| TID #: TID-00732                  | Project Title: Jitter minimizing techniques for digitally isolated high    |                                       |
| Number: TIDA-00732                | Rev: E1  | Sheet Title: FPGA 2, Non-Isolated End |
| SVN Rev: Version control disabled | Assembly Variant: ADS9110 w/REF5045  | Sheet: 6 of 10                        |
| Drawn By: Anbu Mani               | File: TIDA-00732_FPGA_2_SchDoc   | Size: B                               |
| Engineer: Anbu Mani               | Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a> | © Texas Instruments 2015              |



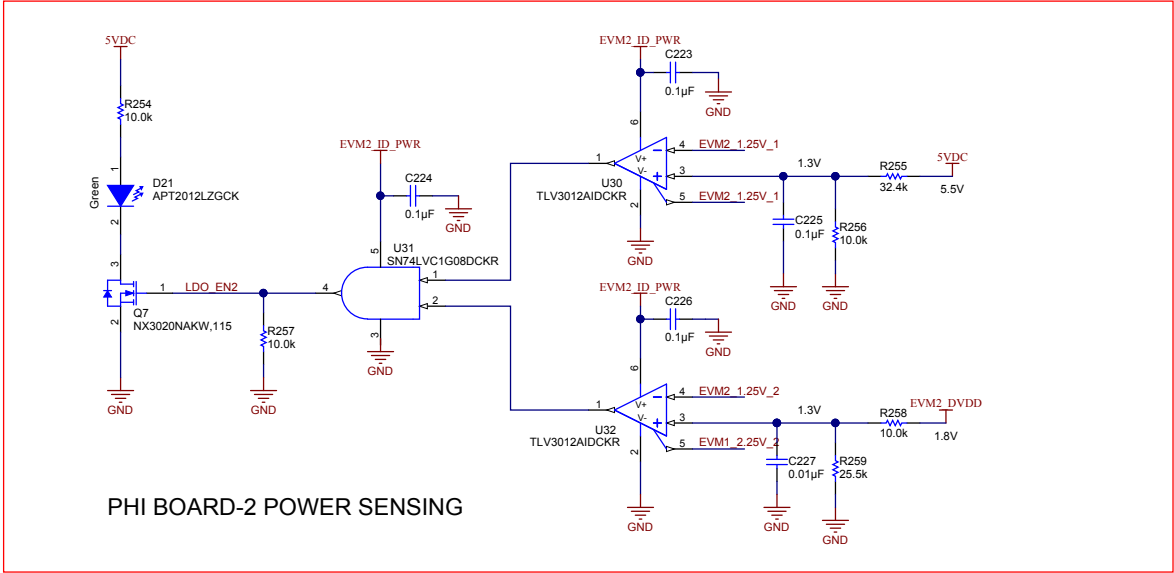
**NON-ISOLATED POWER RAIL**



**ISOLATED POWER RAIL**



PHI BOARD-1 POWER SENSING



PHI BOARD-2 POWER SENSING

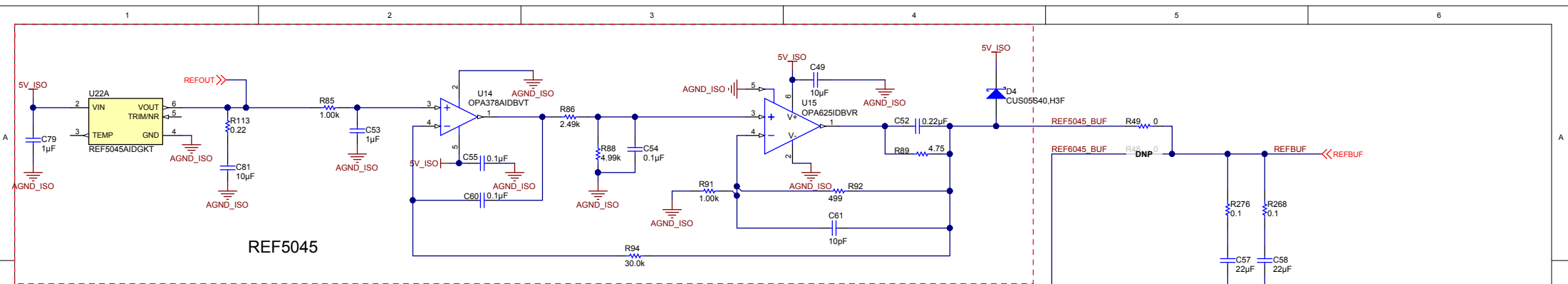
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|-----------------------------------|--|---|
| Orderable: N/A                    | Designed for: Public Release   | Mod. Date: 2/27/2016                              |
| TID #: TIDA-00732                 | Project Title: Jitter minimizing techniques for digitally isolated high    |   |
| Number: TIDA-00732                | Rev: E1  | Sheet Title: Power Sense - PH1 & PH2 Interface    |
| SVN Rev: Version control disabled | Assembly Variant: ADS9110 w/REF5045  | Sheet: 8 of 10                                    |
| Drawn By: Anbu Mani               | File: TIDA-00732_Pwr_Sense_SchDoc  | Size: B   |
| Engineer: Anbu Mani               | Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a> | <a href="http://www.ti.com">http://www.ti.com</a> |

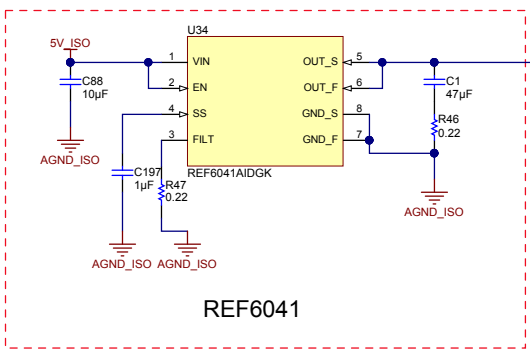


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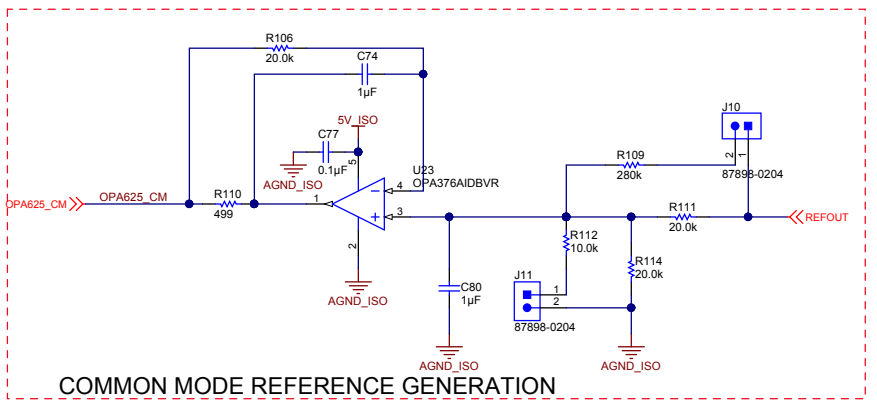




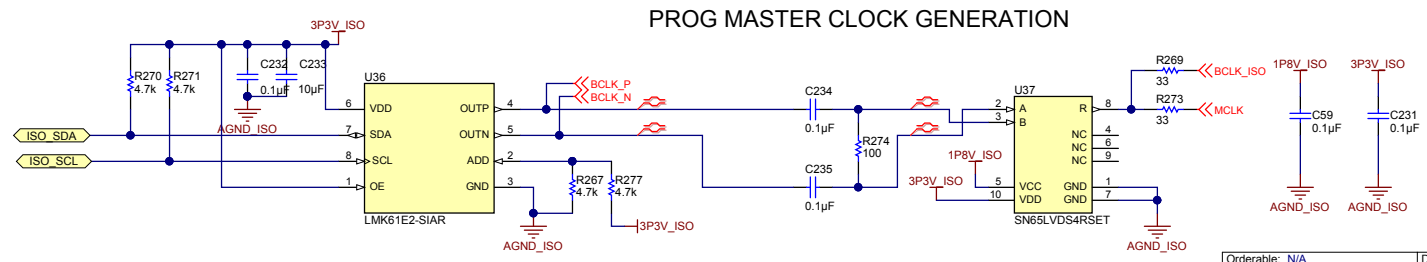
REF5045



REF6041



COMMON MODE REFERENCE GENERATION



PROG MASTER CLOCK GENERATION

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|                                   |  |                                      |
|-----------------------------------|--|--------------------------------------|
| Orderable: N/A                    | Designed for: Public Release   | Mod. Date: 2/27/2016                 |
| TID #: TIDA-00732                 | Project Title: Jitter minimizing techniques for digitally isolated high    |                                      |
| Number: TIDA-00732                | Rev: E1  | Sheet Title: ADC Reference Selection |
| SVN Rev: Version control disabled | Assembly Variant: ADS9110 w/REF5045  | Sheet: 9 of 10                       |
| Drawn By: Anbu Mani               | File: TIDA-00732_ADC_Ref_Select.SchDoc                                     | Size: B                              |
| Engineer: Anbu Mani               | Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a> |                                      |

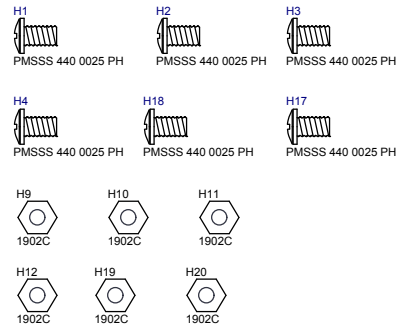




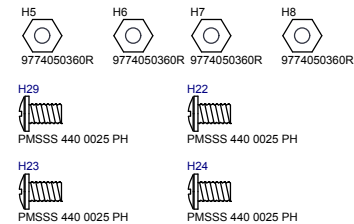
PCB Number: TIDA-00732  
PCB Rev: E1



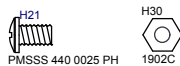
### For Corner Mounting



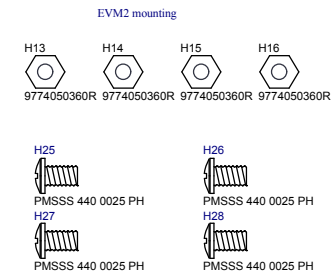
### For PH11 Mounting



### For Beagle Bone Block Mounting



### For PH12 Mounting



| Label Table |            |
|-------------|------------|
| Variant     | Label Text |
|             |            |
|             |            |
|             |            |
|             |            |
|             |            |
|             |            |
|             |            |
|             |            |
|             |            |
|             |            |

LBL1  
PCB Label  
Size: 0.65" x 0.20"

ZZ1  
Label Assembly Note  
This Assembly Note is for PCB labels only

ZZ2  
Assembly Note  
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3  
Assembly Note  
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4  
Assembly Note  
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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|-----------------------------------|--|------------------------|
| Orderable: N/A                    | Designed for: Public Release   | Mod. Date: 2/27/2016   |
| TID #: TID-00732                  | Project Title: Jitter minimizing techniques for digitally isolated high    |                        |
| Number: TIDA-00732                | Rev: E1  | Sheet Title: Fasteners |
| SVN Rev: Version control disabled | Assembly Variant: ADS9110 w/REF5045  | Sheet: 10 of 10        |
| Drawn By: Anbu Mani               | File: TIDA-00732_TID_Hardware.SchDoc                                       | Size: B                |
| Engineer: Anbu Mani               | Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a> |                        |



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