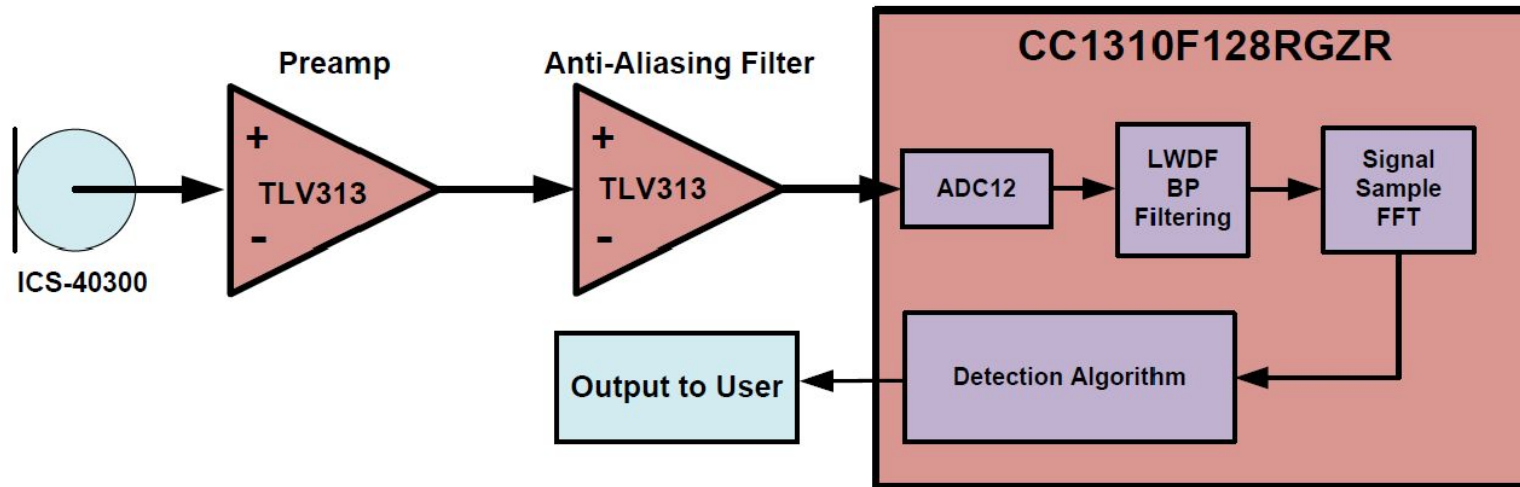
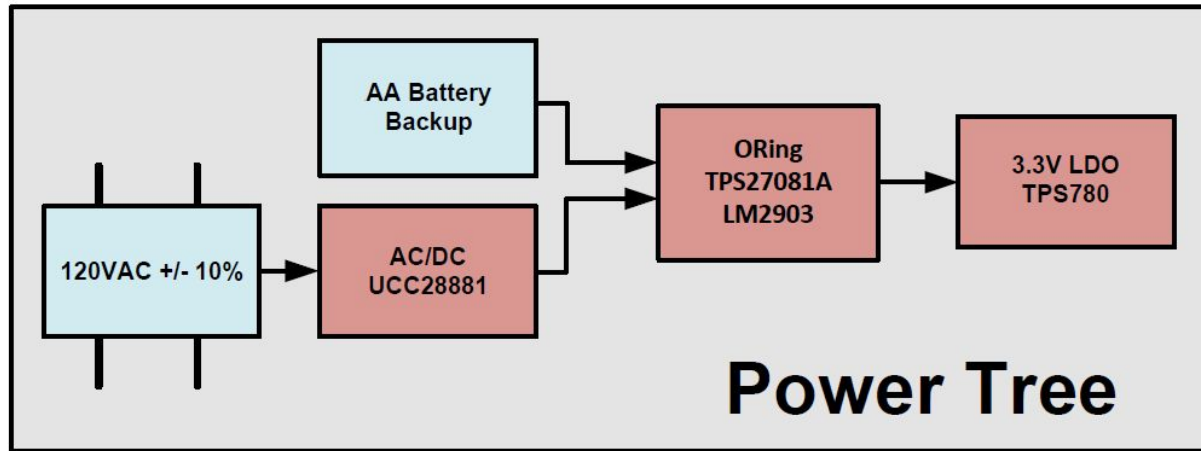


Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A



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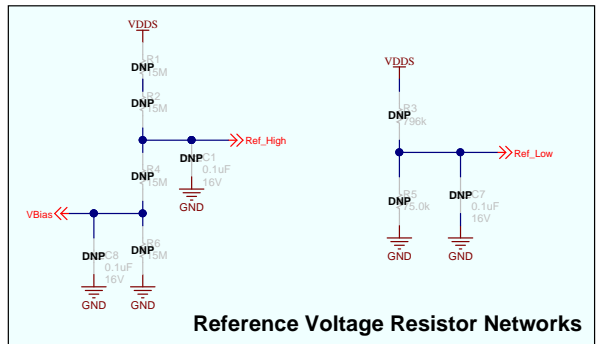
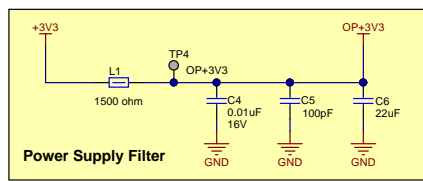
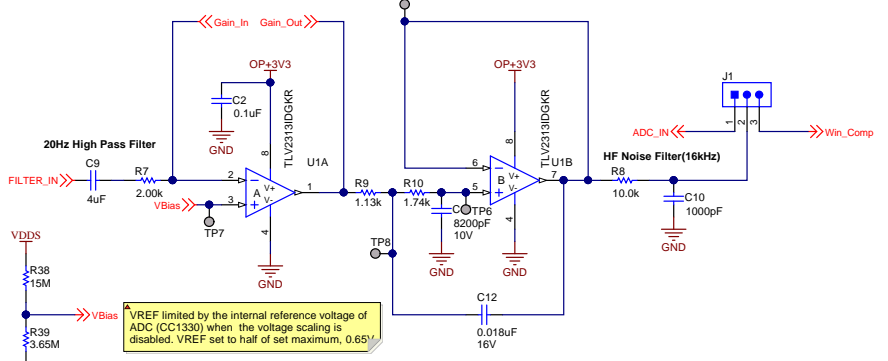
Orderable: Default build	Designed for: Public Release	Mod. Date: 10/9/2017
TID #: 01519	Project Title: Alarm detector	
Number: TIDA-01519 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 5
Drawn By:	File: TIDA-01519_CoverSheet_SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	http://www.ti.com



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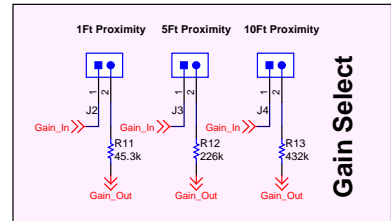
Variable Gain Stage

Anti-Aliasing Filter (8.5kHz Cutoff)

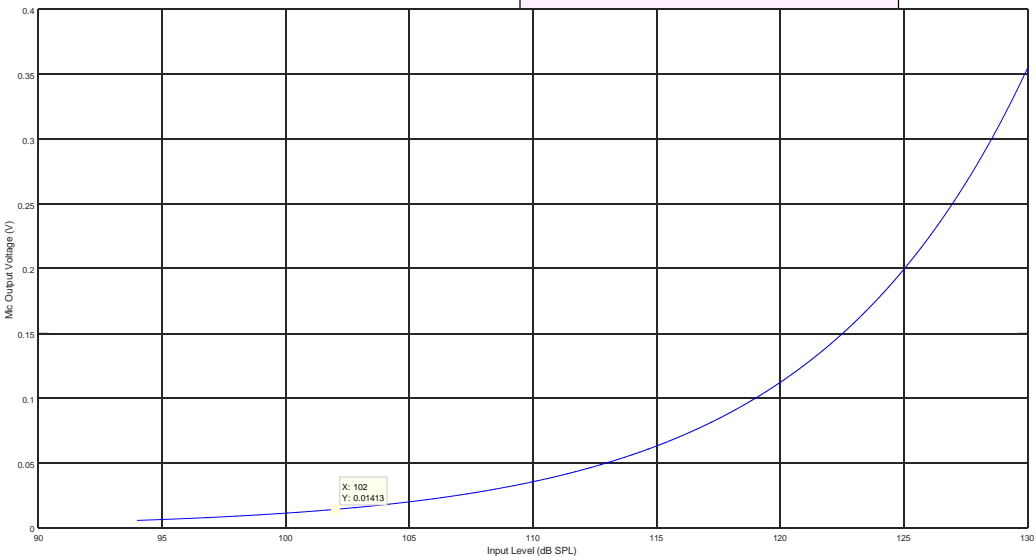
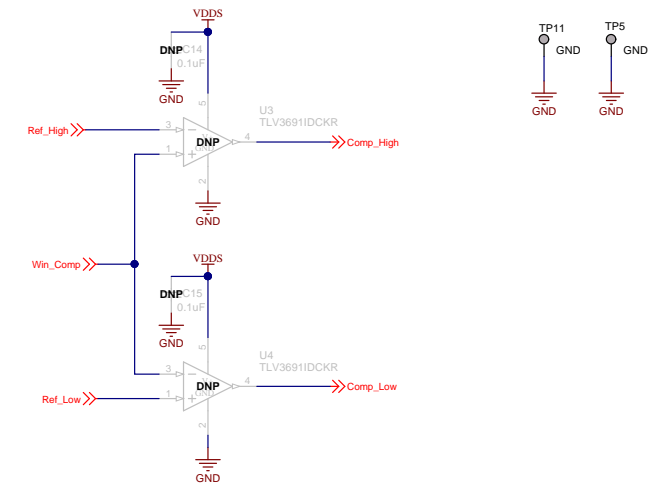
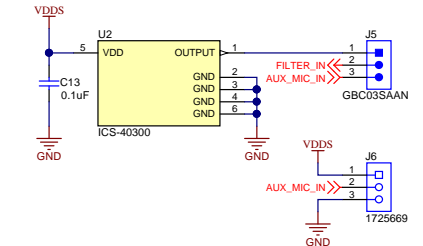


Reference Voltage Resistor Networks

Min dB Level at 10' = 85dB => 2.1mV RMS
 Min dB Level at 5' = 91.02dB => 4mV RMS
 Min dB Level at 1' = 105dB => 20mV RMS
 * Voltages based on 10th degree polyfit prediction



Gain Select

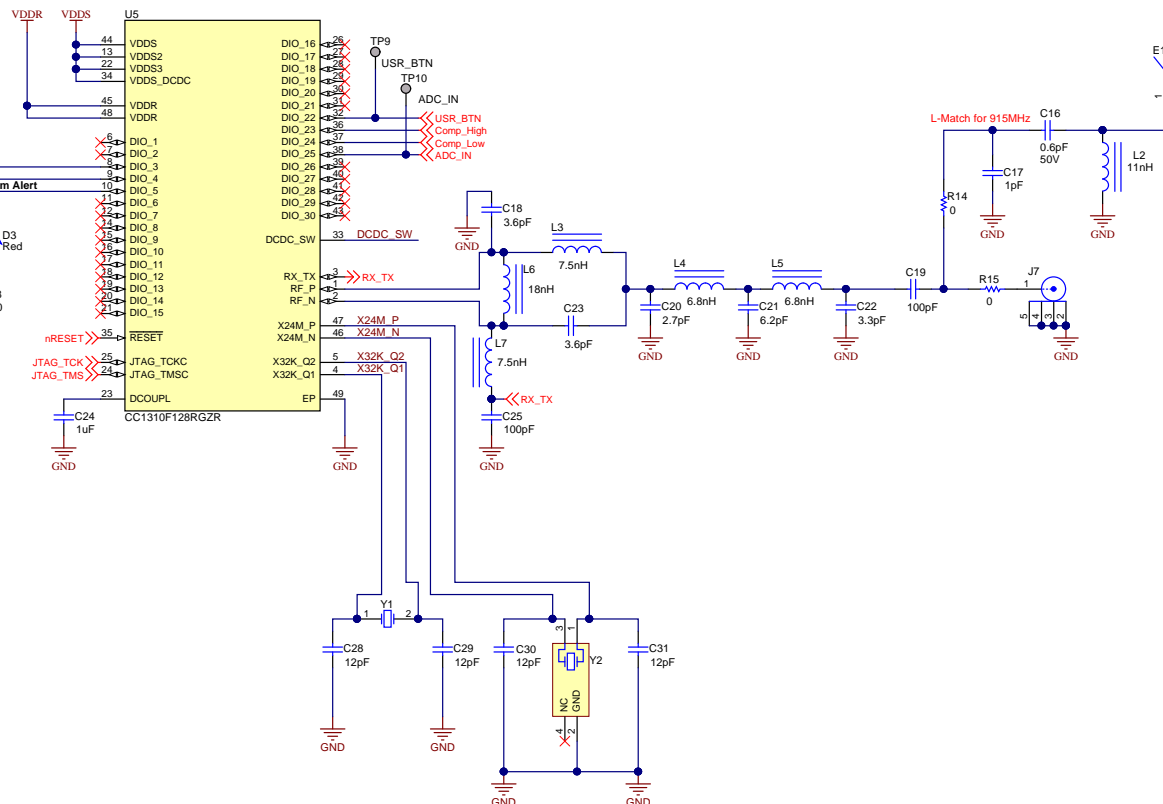


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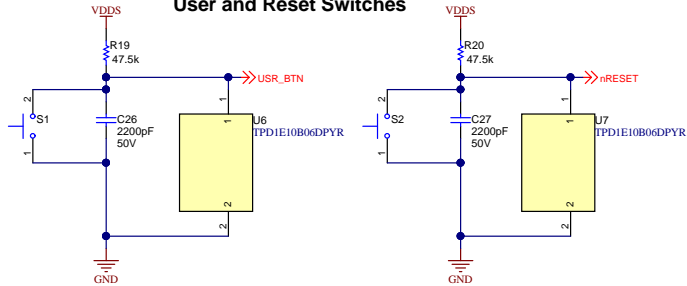
Orderable: Default build	Designed for: Public Release	Mod. Date: 9/7/2017
TID #: 01519	Project Title: Alarm detector	
Number: TIDA-01519 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 2 of 5
Drawn By:	File: TIDA-01519 Analog_FE_SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	



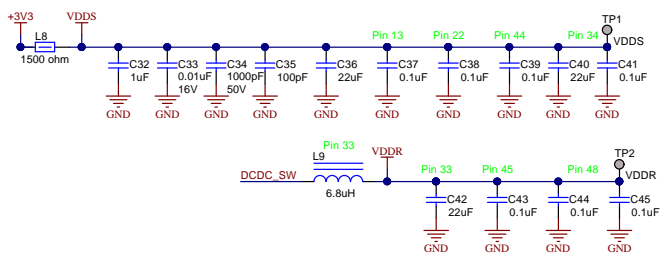
Wireless MCU



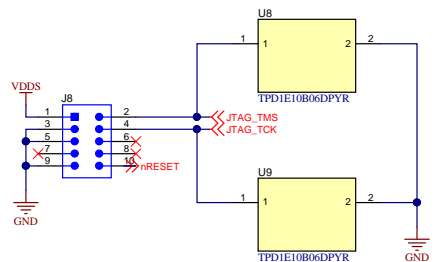
User and Reset Switches



Wireless MCU Bypass Capacitors & DC-DC Passives



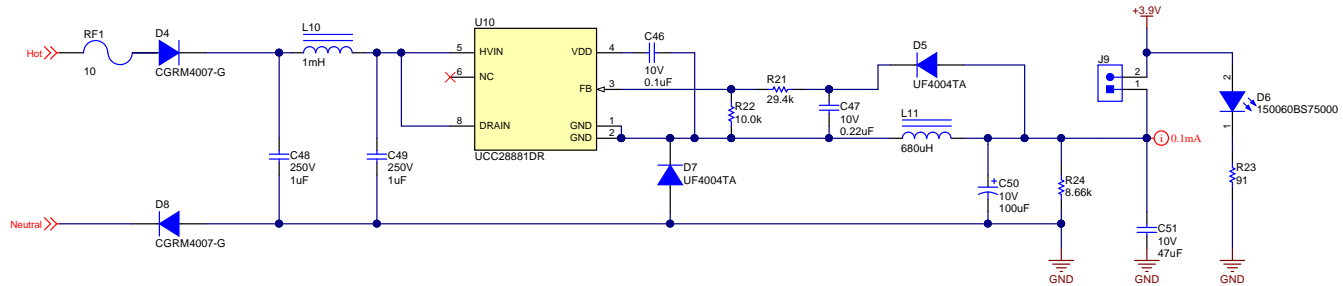
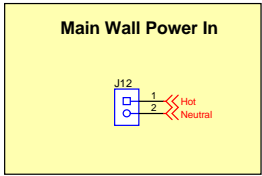
JTAG Programming Interface



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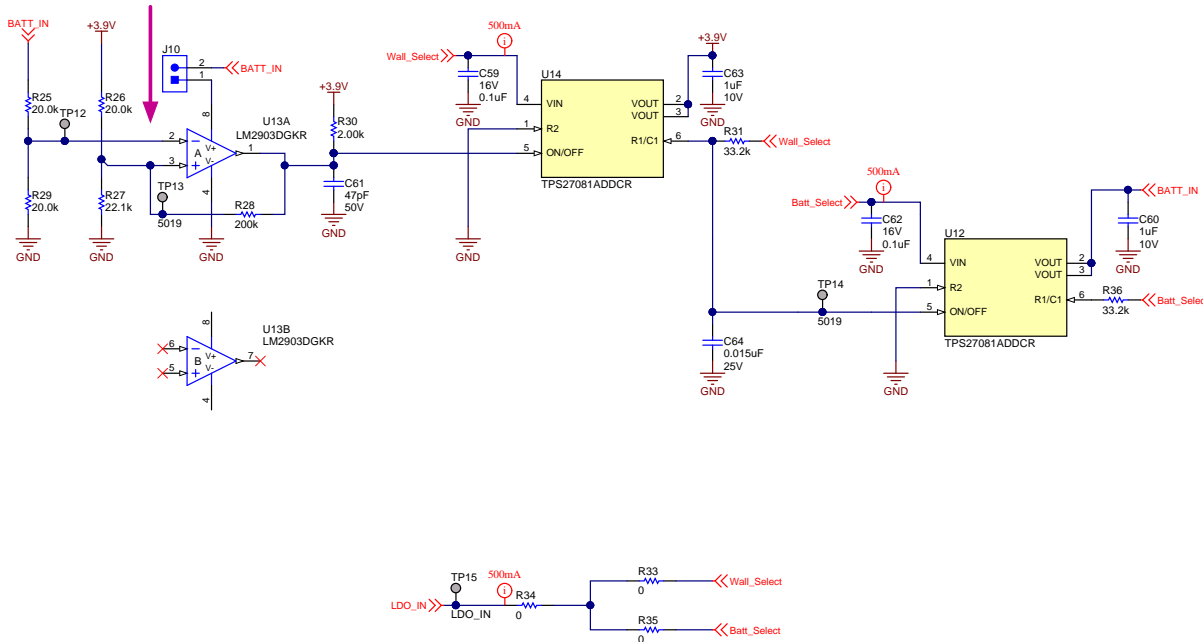
Orderable: Default build	Designed for: Public Release	Mod. Date: 9/7/2017
TID #: 01519	Project Title: Alarm detector	
Number: TIDA-01519 Rev: E1	Sheet Title:	
SVN Rev. Version control disabled	Assembly Variant: 001	Sheet: 3 of 5
Drawn By:	File: TIDA-01519_Power-MCU_SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	

Wall Power Supply Rectification & Smoothing

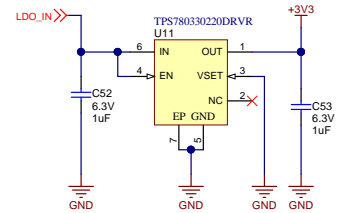


2.14V Required on Inverting Input to Switch from Wall to Batt. This is equivalent to 4.28V from the battery. This ensures that the battery is only used once the wall supply is absent.

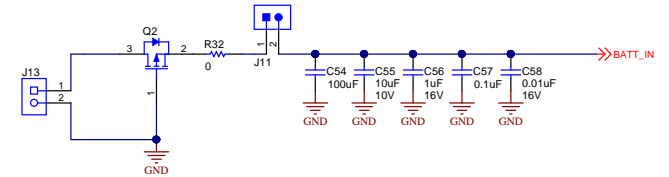
Power Supply ORing



Main Power Supply 3.3V LDO



Battery & Reservoir Capacitors



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Orderable: Default build	Designed for: Public Release	Mod. Date: 8/31/2017
TID #: 01519	Project Title: Alarm detector	
Number: TIDA-01519 Rev: E1	Sheet Title:	
SVN Rev. Version control disabled	Assembly Variant: 001	Sheet: 4 of 5
Drawn By:	File: TIDA-01519_WallPowerV2p0_SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	http://www.ti.com



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H1 SJ-5003 (BLACK) H2 SJ-5003 (BLACK) H3 SJ-5003 (BLACK) H4 SJ-5003 (BLACK)

DNP FID1 DNP FID2 DNP FID3 DNP FID4 DNP FID5 DNP FID6

PCB LOGO Pb-Free Symbol PCB LOGO FCC disclaimer

SH-J1 SH-J2 SH-J3 SH-J4 SH-J5 SH-J9 SH-J10 SH-J11

Variant	Label Text
001	Default Build
002	Minimum BOM

LBL1 PCB Label THT-14-423-10

ZZ1 Label Assembly Note This Assembly Note is for PCB labels only

ZZ2 Assembly Note These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 Assembly Note These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 Assembly Note These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5 Assembly Note Microphone U2 requires special precautions for mounting and board cleaning. See datasheet for full details.

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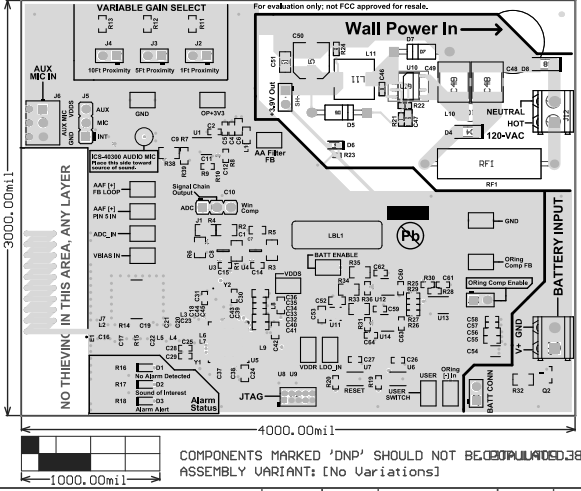
Orderable: Default build	Designed for: Public Release	Mod. Date: 9/5/2017
TID #: 01519	Project Title: Alarm detector	
Number: TIDA-01519 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 5 of 5
Drawn By:	File: TIDA-01519_Hardware.SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4 High TG	9.00mil	4.2	
5	Signal Layer 1	Copper	1.42mil		
6	Dielectric 2	FR-4 High TG	9.00mil	4.2	
7	Signal Layer 2	Copper	1.42mil		
8	Dielectric 3	FR-4 High TG	9.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

Top Layer contains 50 ohm single-ended using 18 mil trace.

- Z21 ■ Install Label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
- Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
- Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.
- Z25 ■ Microphone U2 requires special precautions for mounting and board cleaning. See datasheet for full details.



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 6 MIL
 MIN. VIA PAD SIZE: 18 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 31 MIL (0.8mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER **Purple**
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL:
 CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER



PROJECT TITLE: Alarm detector
 DESIGNED FOR: Public Release
 FILE NAME: TIDA-01519.PcbDoc

ADP-1519-001	TOP	13	BOARD # 1710A-01519	DATE: 01/10/10	DESIGNER: E1	SUN 3:28:10	INSTRUMENTS
LAYER NAME = TOP	TOP		TID #: 01519	DATE: 01/10/10	DESIGNER: E1	TIME: 3:28:10	INSTRUMENTS
PLOTTED BY: E1	TOP		GENERATED BY: 10/27/10	DATE: 01/10/10	DESIGNER: E1	TIME: 3:28:10	INSTRUMENTS

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ENGINEER: Brian Dempsey
 LAYOUT BY: Krypton Solutions/RS
 SCALE: 1.00
 ALTUM DESIGNER VERSION: 17.1.5.472

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