

TIDEP-01002

REV A TO A1 CHANGE SUMMARY:

- Sheet 01: Bump schematic version to Rev A1.
- Sheet 02: Add note for LP8860 EEPROM defaults.
- Sheet 10: Add DS9xx note to terminate unused lvds with 100 ohm.
- Sheet 14: Change R608 from 3.32K to 1K for lower default level.
- Sheet 16: Change LP87xx nRST to VSYS_3V3 so PMIC will power up.
- Sheet 16: Change C608 to no-pop to speed up the VIO_3V3 ramp.
- Sheet 17: Add pull-ups to SD card interface that got inadvertently dropped from LCARD.

REV A1 TO B CHANGE SUMMARY:

- Sheet 01: Bump schematic version to Rev B.
- Sheet 10: Terminate unused lvds with 100 ohm.
- Sheet 10: Fix inversion of OXA_2:0 -/+
- Sheet 17: Update SD card connector, non-EOL part

REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	07/17/2018	JAC
A1	PROTOTYPE UPDATE	10/05/2018	JAC
B	BETA UPDATE	10/09/2018	JAC

- SH01 - TITLE PAGE
- SH02 - NOTES
- SH03 - J6E MEM VIP CAM DIS SYS
- SH04 - J6E CNTVY
- SH05 - J6E DDR
- SH06 - J6E ANA PWR
- SH07 - J6E DIG PWR
- SH08 - DDR3 MEMORY BANK 1
- SH09 - MEM eMMC
- SH10 - DISPLAY/CSI2
- SH11 - ENET/CAN/CLASS-D
- SH12 - USB-UART/JTAG
- SH13 - HDMI
- SH14 - POWER INPUT/DISPLAY
- SH15 - POWER LM5141
- SH16 - PMIC
- SH17 - LDCP SUPPORT

REVISION STATUS OF SHEETS

REV	SH	1	2	3	4	5	6	7	8	9	10	DATE	BY	DESCRIPTION
												07/17/2018	J.A.C.	DWN
												07/17/2018	T.W.K.	CHR
												07/17/2018	J.A.C.	ENGR
												07/17/2018	J.A.C.	ENGR-MGR
												07/17/2018	J.A.C.	DR
												07/17/2018	C.M.D.	DR
												07/17/2018	J.A.C.	MFG
												07/17/2018	J.A.C.	RLSE
												07/17/2018	J.A.C.	APPLICATION

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Preliminary Information - Subject to change			
Title: DRA71x DCARD CPU Board			
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INDEX	BALL	SIGNAL	GPIO	RAIL	IPU/IPD	SCHEMATIC NET	XPU/XPD	
1	L3	GPMC_A11	GPIO2_1	VDDSHV10	PD	H_DS90C189_RSTn	PD-10K	1.8V GPIO
2	A18	MCASP1_AXR8	GPIO5_10	VDDSHV3	PD	H_DCAN1_STB	PD-10K	
3	B17	MCASP1_AXR9	GPIO5_11	VDDSHV3	PD	H_DCAN1_EN	PD-10K	
4	B16	MCASP1_AXR10	GPIO5_12	VDDSHV3	PD	H_DCAN1_nFAULT	PU-10K	
5	A15	MCASP1_AXR4	GPIO5_6	VDDSHV3	PD	ENET_EN	PU-3.32K	*
6	A14	MCASP1_AXR5	GPIO5_7	VDDSHV3	PD	ENET_WAKE	PU-3.32K	*
7	A17	MCASP1_AXR6	GPIO5_8	VDDSHV3	PD	ENET_INH	PU-3.32K	*
8	A16	MCASP1_AXR7	GPIO5_9	VDDSHV3	PD	ENET_INTSn	PU-3.32K	*
9	AA1	MMC3_DAT5	GPIO1_23	VDDSHV7	PU	HDMI_HPD	IPU-10K	
10	AB1	MMC3_DAT7	GPIO1_25	VDDSHV7	PU	HDMI_CEC_A	IPU-10K	
11	Y2	MMC3_CLK	GPIO6_29	VDDSHV7	PU	MMC_PWR_ON	PU-10K	
12	Y1	MMC3_CMD	GPIO6_30	VDDSHV7	PU	EN_SDIO_3V3	PU-10K	
13	Y4	MMC3_DAT0	GPIO6_31	VDDSHV7	PU	H_DISPLAY_RSTn	PD-3.32K	*
14	F24	SPI2_CS0	GPIO7_17	VDDSHV3	PU	H_TAS2505_RSTn	PD-3.32K	*
15	W2	MMC3_DAT3	GPIO7_2	VDDSHV7	PU	GPIO_7_2	PD-3.32K	*
16	Y3	MMC3_DAT4	GPIO1_22	VDDSHV7	PU	GPIO1_22/EHRPWM3A	PU-10K	
17	Y5	GPIO6_10	GPIO6_10	VDDSHV7	PU	GP6_10/EHRPWM2A	PU-10K	
18	Y6	GPIO6_11	GPIO6_11	VDDSHV7	PU	GP6_11/EHRPWM2B	PU-10K	

Device	I2C1	I2C2
CPU ID EEPROM	0x50	
CPU TAS25051R	0x18	
CPU LP87523-Q1	0x60	
CPU LP8860-Q1	0x2D	
CPU HDMI EEDID		0x50

POWER RAILS	VOLTAGE
VDDSHV1	3.3V
VDDSHV3	3.3V
VDDSHV4	3.3V
VDDSHV7	3.3V
VDDSHV8	3.3V/1.8V
VDDSHV9	3.3V
VDDSHV10	1.8V
VDDSHV11	1.8V

```
uint8_t lp8860_eeprom[] = {
0xED, //60
0xDC, //61
0xDC, //62
0xF8, //63
0xDD, //64
0xE5, //65
0xFA, //66 F8 PWM, FA BRT_REG
0x77, //67
0x77, //68
0x71, //69
0x3F, //6A
0xB7, //6B
0x17, //6C
0xEF, //6D
0xB0, //6E
0x8B, //6F
0xCE, //70
0xCA, //71
0xE5, //72
0xE4, //73
0x35, //74
0x06, //75
0xDA, //76
0xFF, //77
0x3E}; //78
```

HS1



APF19-19-10CB/A01

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DRA71x / DRA79x / TDA2E-17 / AM570x

Data Manual: SPRS960A_July2016
 Package: CBD, 17x17mm, 538 PPGA, 0.65mm Pitch
 PCB Footprint: J6Entry_DRA71x_PDN_v4
 SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

HDMI

VDDA_HDMI

GPMC/GPIO

VDDSHV10

GPIO

VDDSHV3

GPMC/MMC2

VDDSHV11

SYSTEM

GPMC/GPIO

VDDSHV10

CLOCKING

VDDA_OSC

MEMORY-Nonvolatile

MMC1

VDDSHV8

CONTROL

VDDSHV3

Video Inputs

VIN2

VDDSHV1

I2C

VDDSHV3

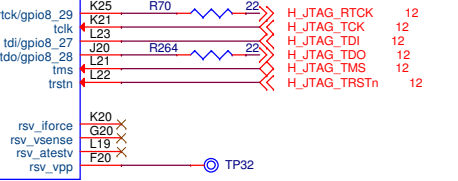
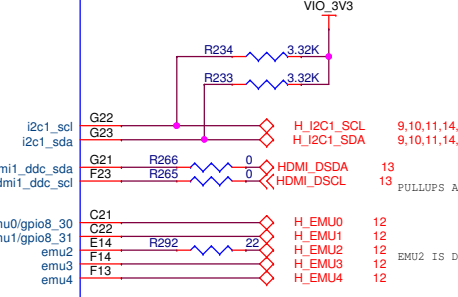
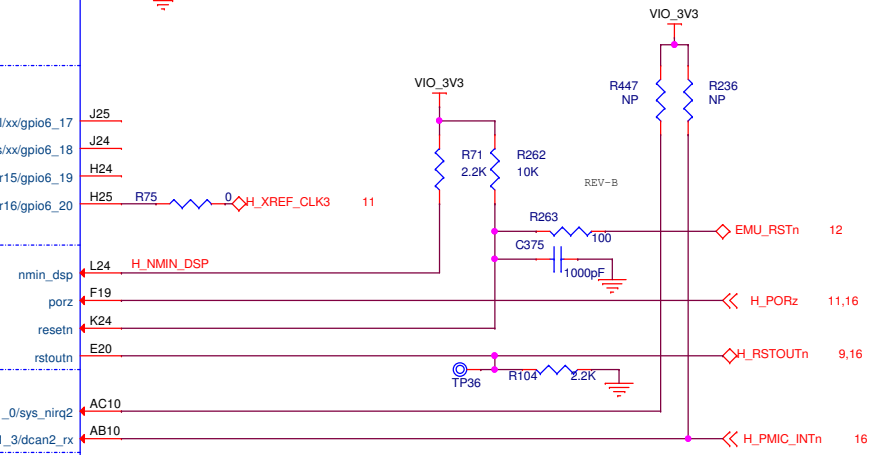
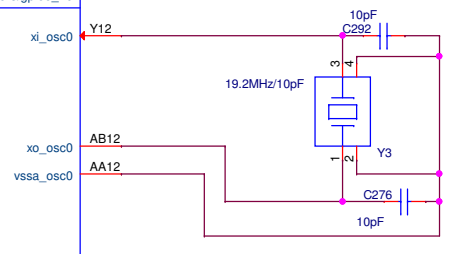
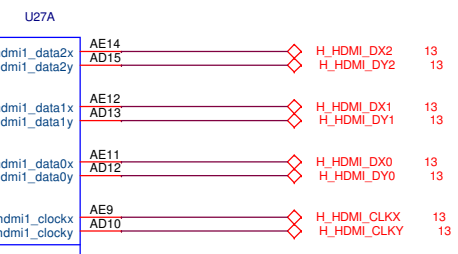
Debug

VDDSHV3

CSI

VDDA_CSI

Si Test



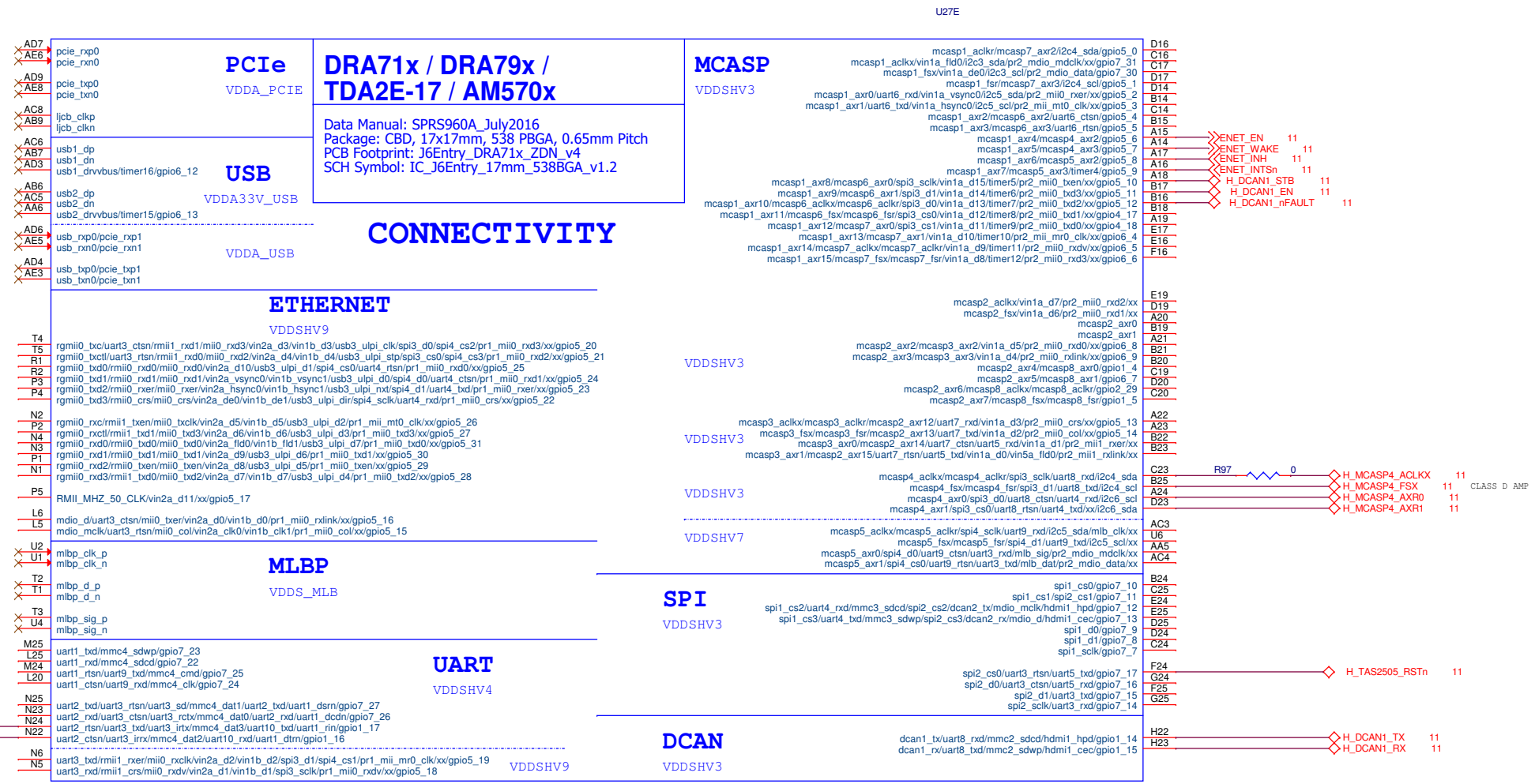
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Title: DRA71x DCARD CPU Board

Page Contents: J6E MEM VIP CAM DIS SYS

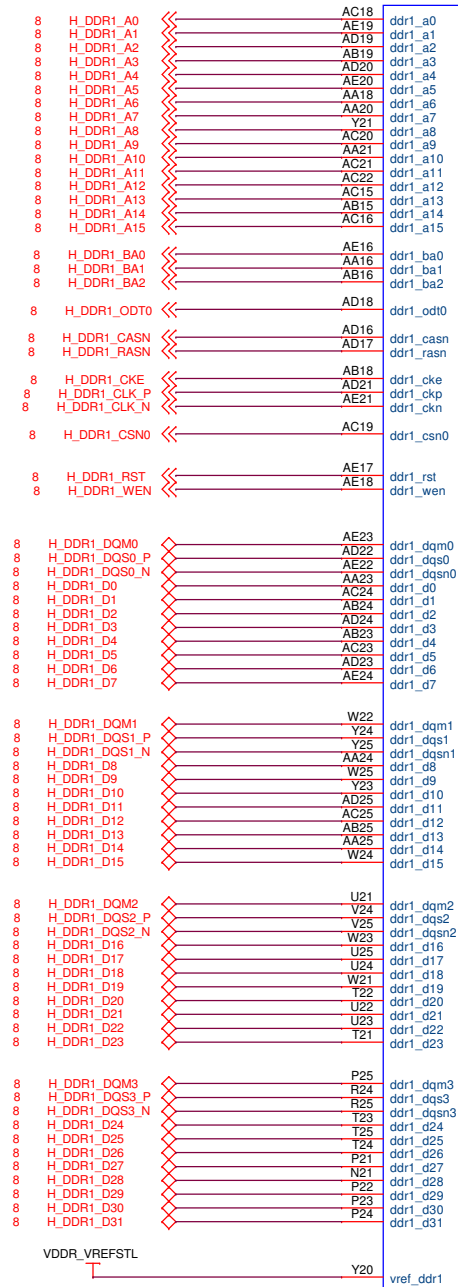
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DRA71x

X777AJG CBD

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**DRA71x / DRA79x /
TDA2E-17 / AM570x**

Data Manual: SPRS960A_July2016
 Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
 PCB Footprint: J6Entry_DRA71x_ZDN_v4
 SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

**MEMORY-
Volatile, DDR3
EMIF1**

VDDS_DDR1

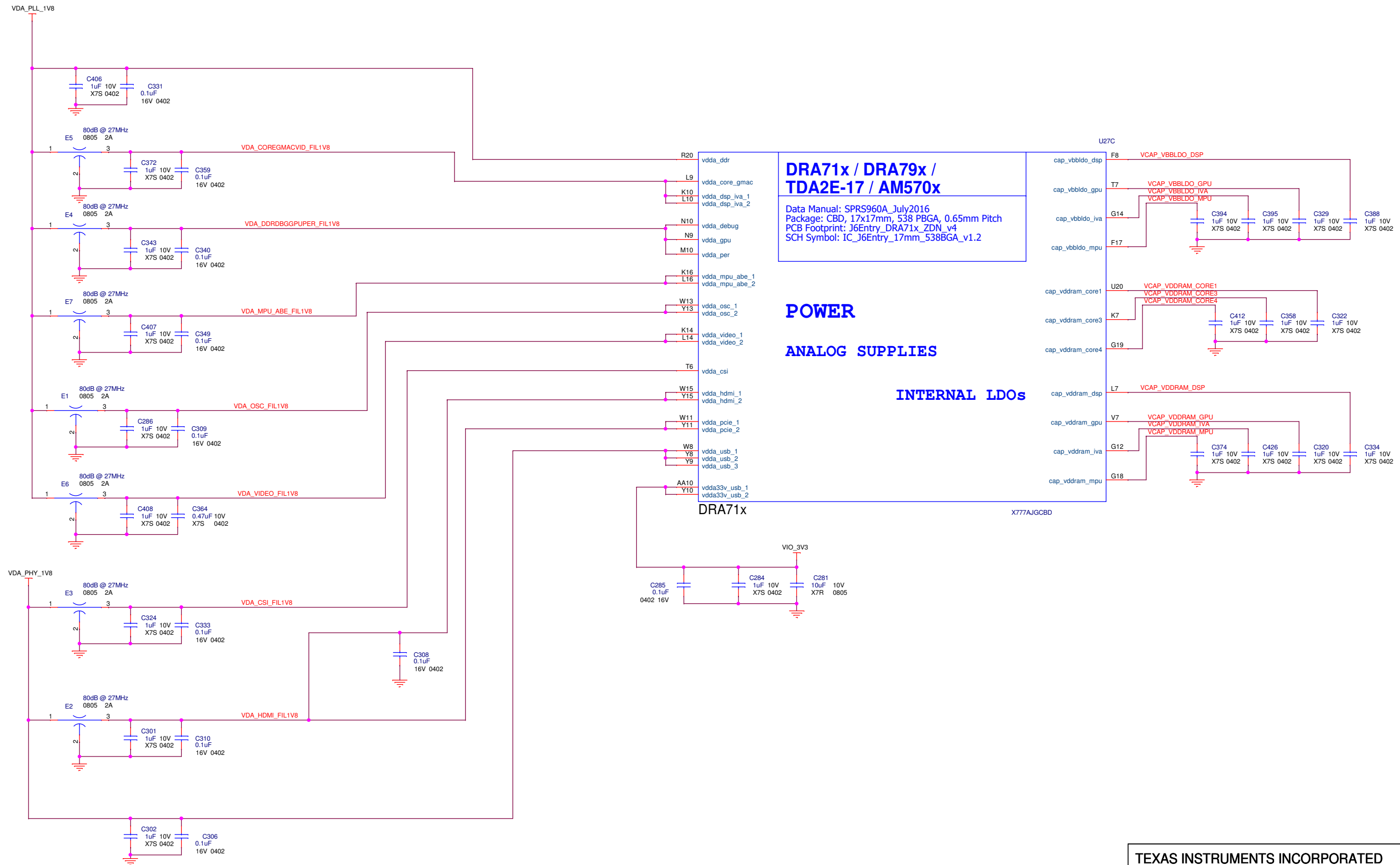
DRA71x

X777AJGCB

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DRA71x / DRA79x / TDA2E-17 / AM570x
 Data Manual: SPRS960A_July2016
 Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
 PCB Footprint: J6Entry_DRA71x_ZDN_v4
 SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

POWER ANALOG SUPPLIES

INTERNAL LDOs

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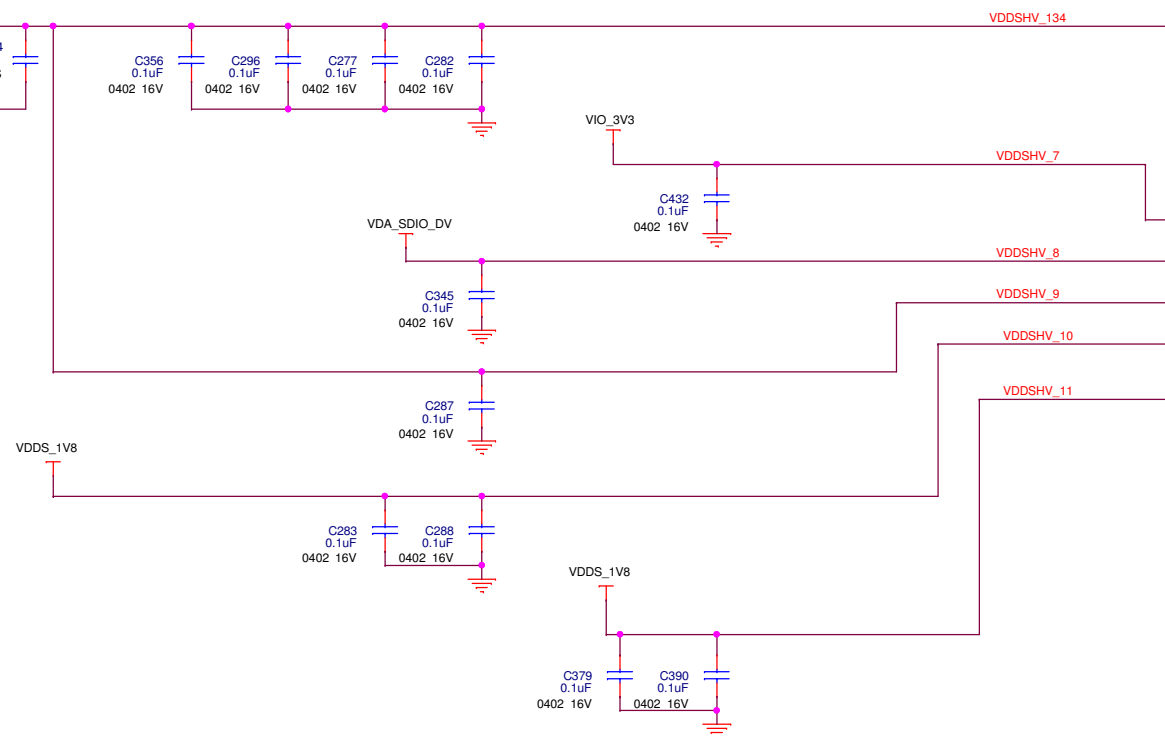
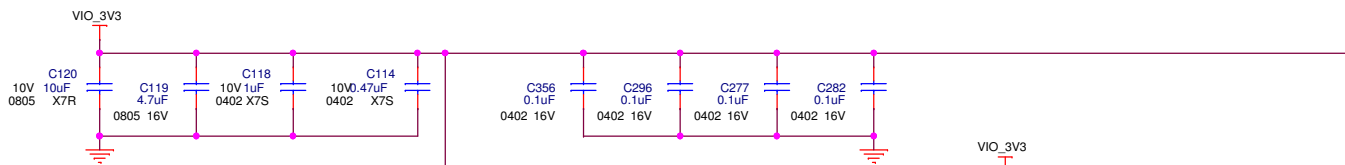
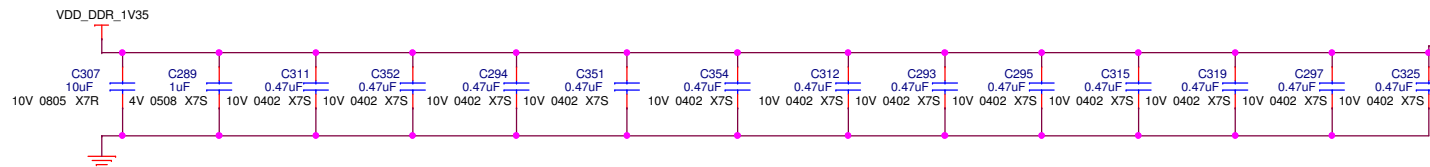
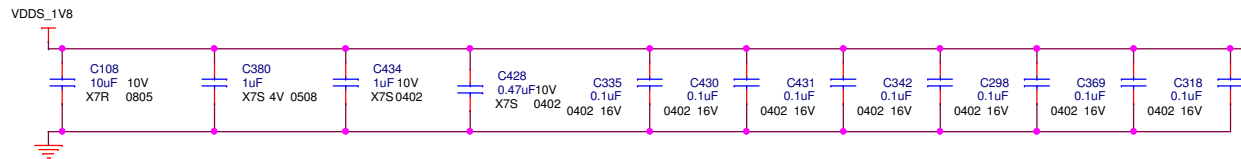
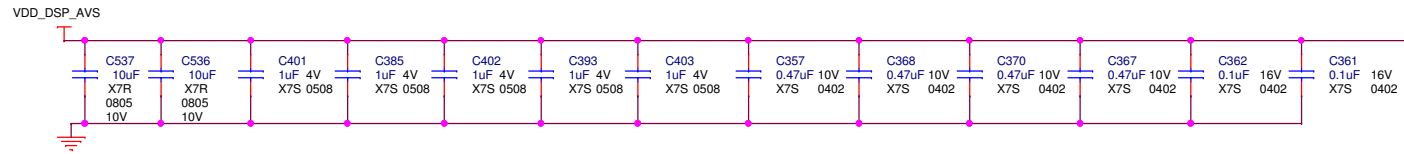
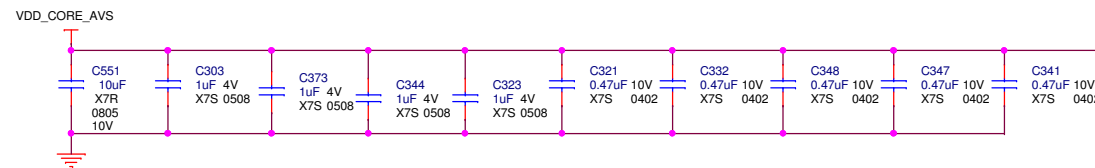
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Title: DRA71x DCARD CPU Board

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- J15 vdd_1
- J16 vdd_2
- J18 vdd_3
- K12 vdd_4
- K18 vdd_5
- L12 vdd_6
- L17 vdd_7
- M11 vdd_8
- M13 vdd_9
- M15 vdd_10
- M17 vdd_11
- N11 vdd_12
- N13 vdd_13
- N15 vdd_14
- N18 vdd_15
- P10 vdd_16
- P12 vdd_17
- P14 vdd_18
- P16 vdd_19
- P18 vdd_20
- R10 vdd_21
- R12 vdd_22
- R14 vdd_23
- R16 vdd_24
- R17 vdd_25
- T9 vdd_26
- T11 vdd_27
- T13 vdd_28
- T15 vdd_29
- T17 vdd_30
- U9 vdd_31
- U11 vdd_32
- U13 vdd_33
- U15 vdd_34
- U18 vdd_35
- V10 vdd_36
- V12 vdd_37
- V14 vdd_38
- V16 vdd_39
- V18 vdd_40
- W10 vdd_41
- W12 vdd_42
- W14 vdd_43
- W16 vdd_44

- H9 vdd_dsp_1
- H11 vdd_dsp_2
- H13 vdd_dsp_3
- J9 vdd_dsp_4
- J11 vdd_dsp_5
- J13 vdd_dsp_6

- G11 vdds18v_1
- H20 vdds18v_2
- W7 vdds18v_3
- Y18 vdds18v_4

- P7 vdds_mlb_1
- R7 vdds_mlb_2

- P20 vdds18v_ddr1_1
- Y19 vdds18v_ddr1_2
- AA19 vdds18v_ddr1_3

- T19 vdds_ddr1_1
- T20 vdds_ddr1_2
- W20 vdds_ddr1_3
- W17 vdds_ddr1_4
- W18 vdds_ddr1_5
- W20 vdds_ddr1_6

- G9 vddshv1_1
- G10 vddshv1_2

- G15 vddshv3_1
- G17 vddshv3_2
- H15 vddshv3_3
- H17 vddshv3_4
- J19 vddshv3_5
- K19 vddshv3_6

- M19 vddshv4_1
- N19 vddshv4_2

- U7 vddshv7_1
- U8 vddshv7_2

- N8 vddshv8_1
- P8 vddshv8_2

- M7 vddshv9_1
- N7 vddshv9_2

- J7 vddshv10_1
- J8 vddshv10_2
- K8 vddshv10_3

- F7 vddshv11_1
- G7 vddshv11_2
- H7 vddshv11_3

DRA71x / DRA79x / TDA2E-17 / AM570x
 Data Manual: SPRS960A_July2016
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 PCB Footprint: J6Entry_DRA71x_ZDN_v4
 SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

POWER
DIGITAL SUPPLIES & GNDS

- vss_1 A1
- vss_2 A25
- vss_3 G8
- vss_4 G13
- vss_5 G16
- vss_6 H8
- vss_7 H10
- vss_8 H12
- vss_9 H14
- vss_10 H16
- vss_11 H18
- vss_12 H19
- vss_13 J10
- vss_14 J12
- vss_15 J14
- vss_16 J17
- vss_17 K9
- vss_18 K11
- vss_19 K13
- vss_20 K15
- vss_21 K17
- vss_22 L8
- vss_23 L11
- vss_24 L13
- vss_25 L15
- vss_26 L18
- vss_27 AA13
- vss_28 M8
- vss_29 M9
- vss_30 M12
- vss_31 M14
- vss_32 M16
- vss_33 M18
- vss_34 M20
- vss_35 N12
- vss_36 N14
- vss_37 N16
- vss_38 N17
- vss_39 N20
- vss_40 P9
- vss_41 P11
- vss_42 P13
- vss_43 P15
- vss_44 P17
- vss_45 P19
- vss_46 R8
- vss_47 R9
- vss_48 R11
- vss_49 R13
- vss_50 R15
- vss_51 R18
- vss_52 T8
- vss_53 T10
- vss_54 T12
- vss_55 T14
- vss_56 T16
- vss_57 T18
- vss_58 U10
- vss_59 U12
- vss_60 U14
- vss_61 U16
- vss_62 U17
- vss_63 U19
- vss_64 V8
- vss_65 V9
- vss_66 V11
- vss_67 V13
- vss_68 V15
- vss_69 V17
- vss_70 V19
- vss_71 W9
- vss_72 W19
- vss_73 Y7
- vss_74 Y14
- vss_75 Y16
- vss_76 Y17
- vss_77 AA7
- vss_78 AA8
- vss_79 AA9
- vss_80 ABB
- vss_81 AC13
- vss_82 AE1
- vss_83 AE15
- vss_84 AE25
- vss_85 AA15
- vss_86

DRA71x

X777AJGCBD

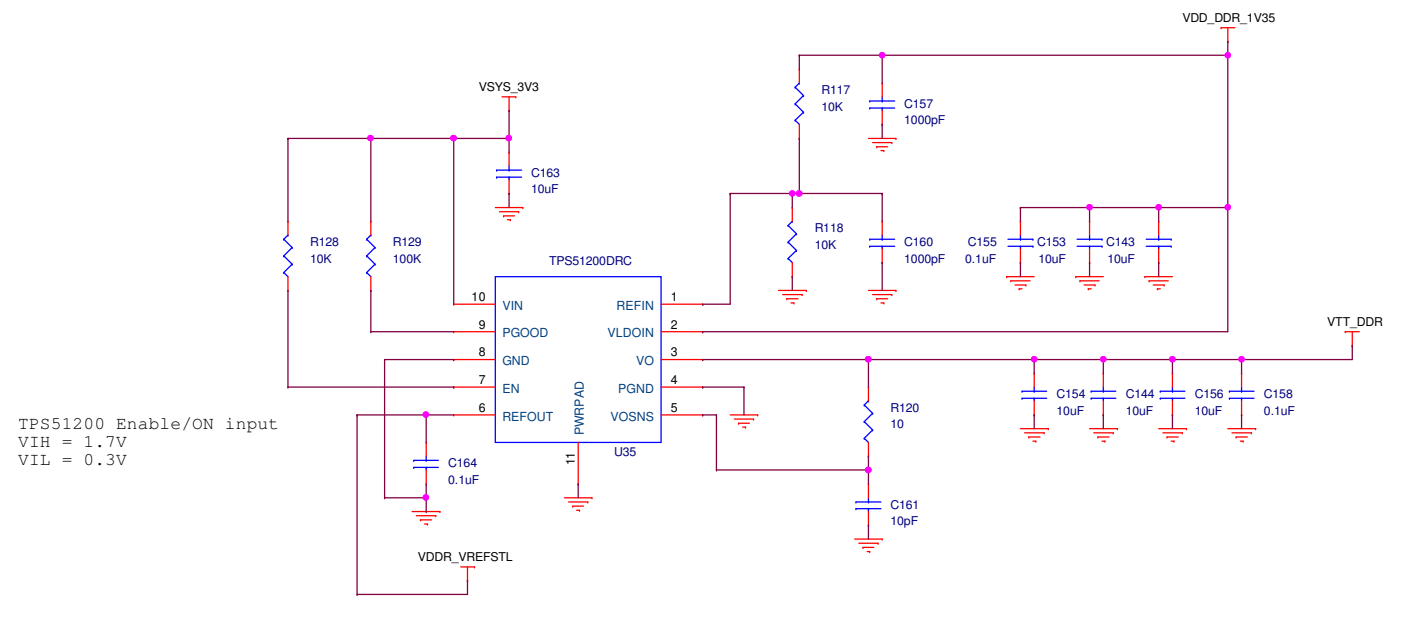
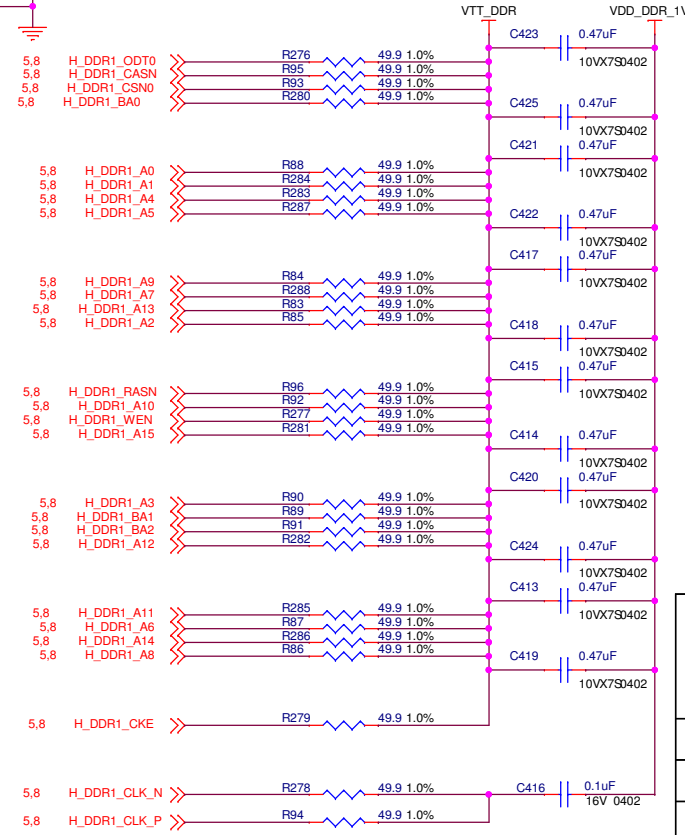
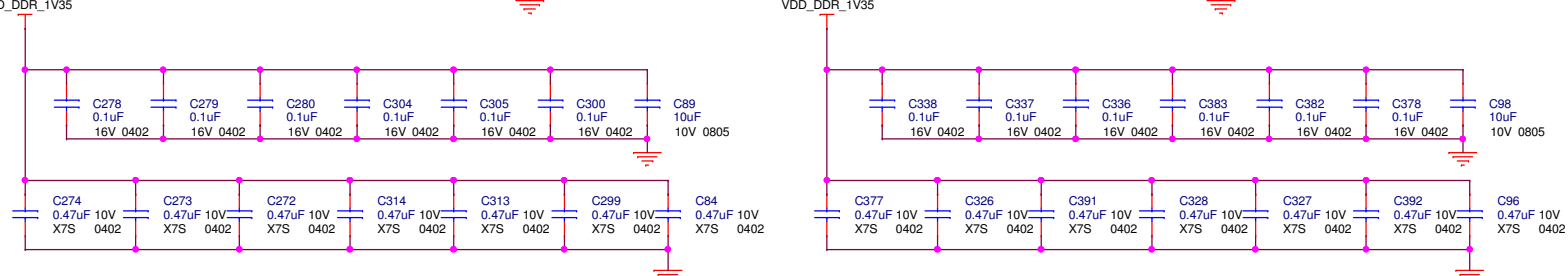
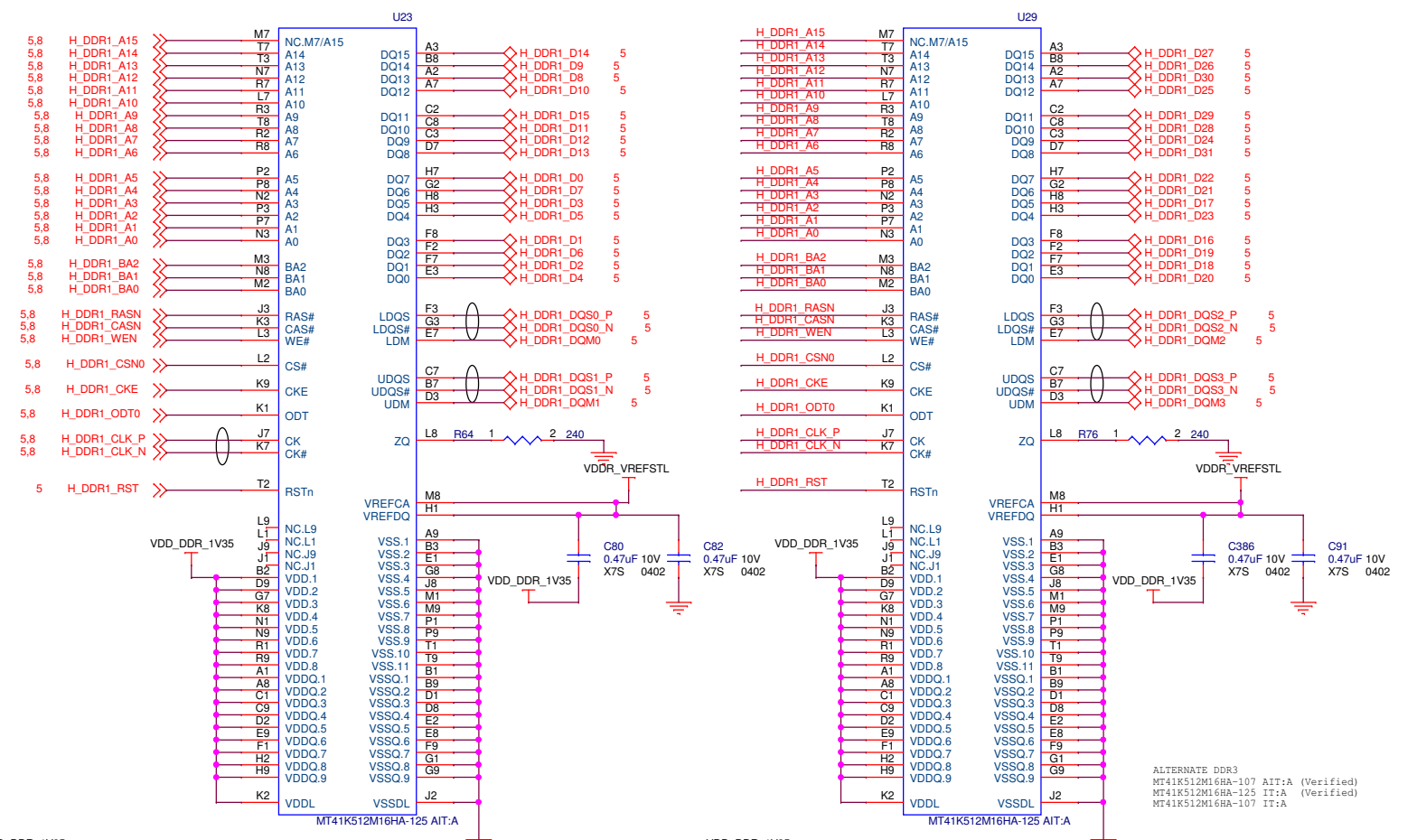
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Preliminary Information - Subject to change

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Page Contents: J6E DIG PWR

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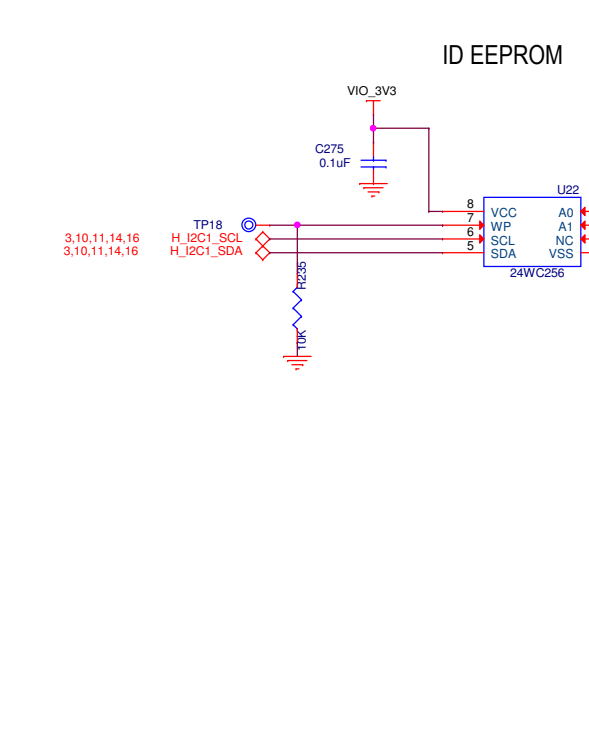
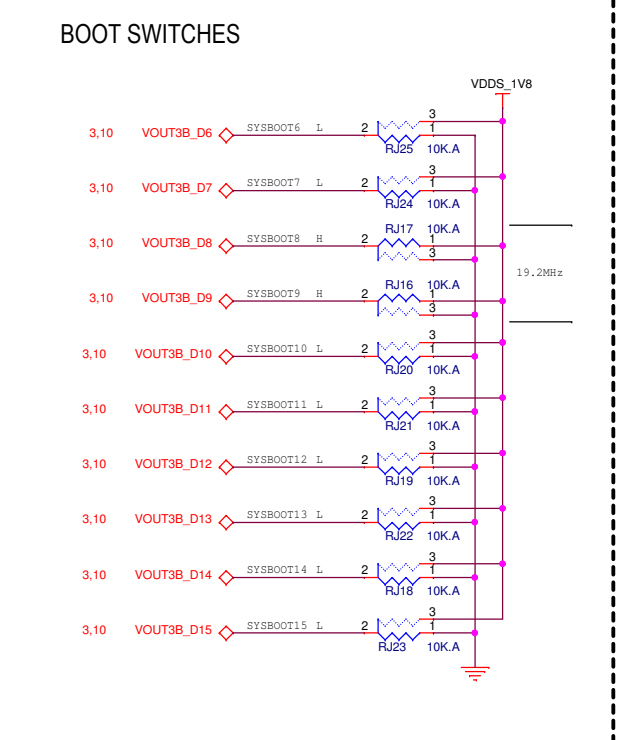
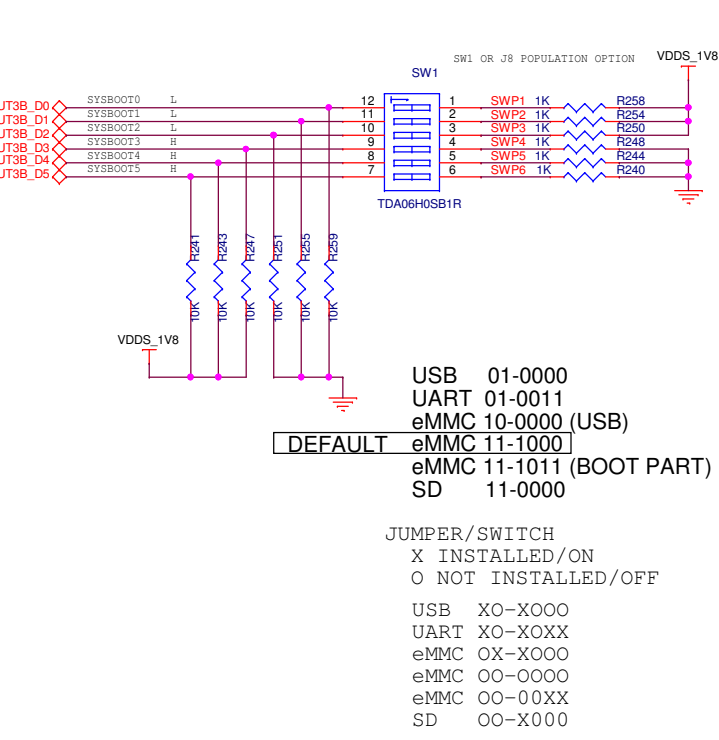
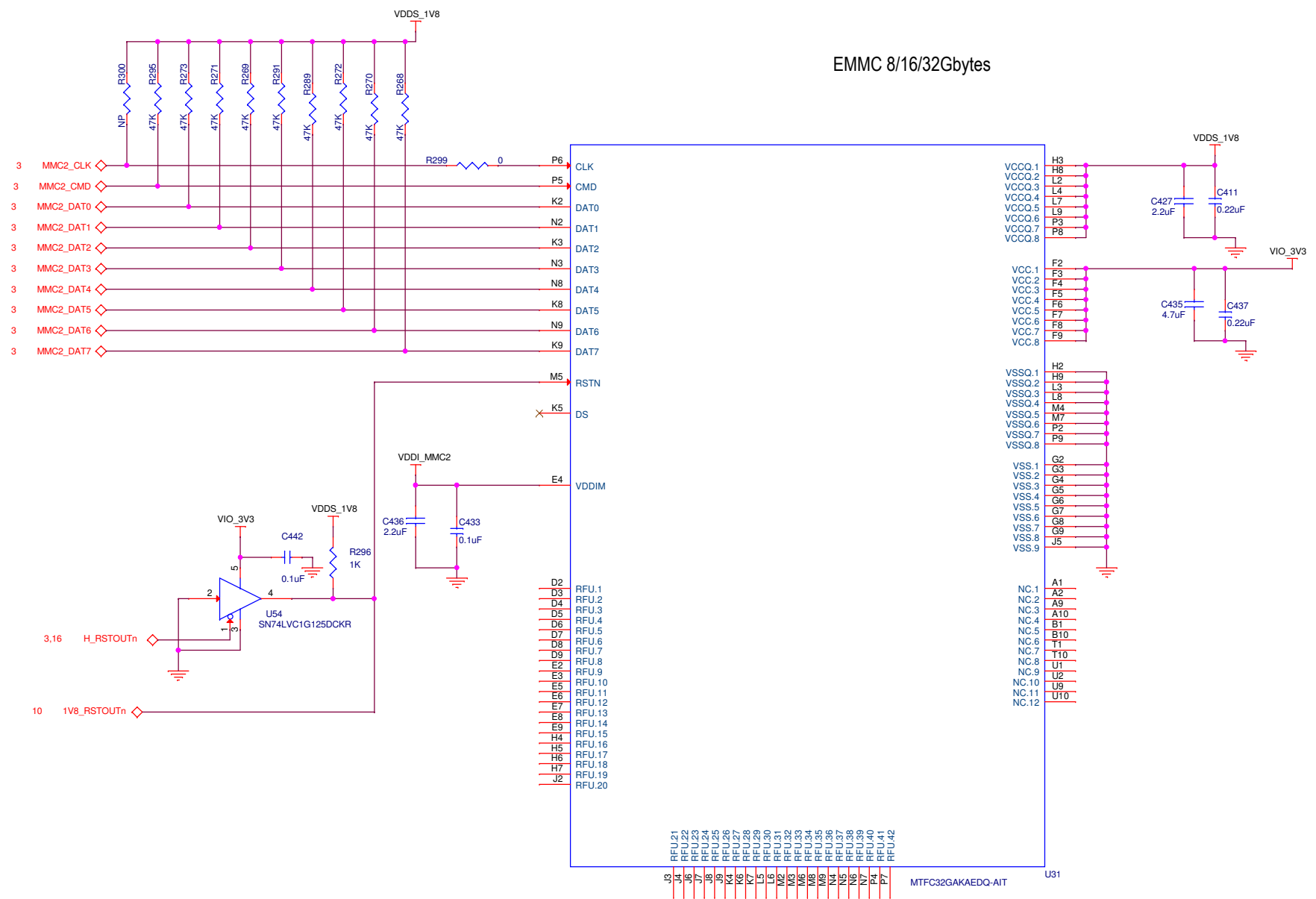
Preliminary Information - Subject to change

Title: DRA71x DCARD CPU Board

Page Contents: DDR3 MEMORY BANK 1

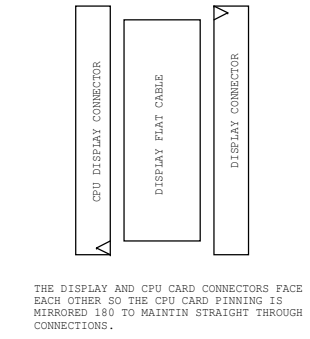
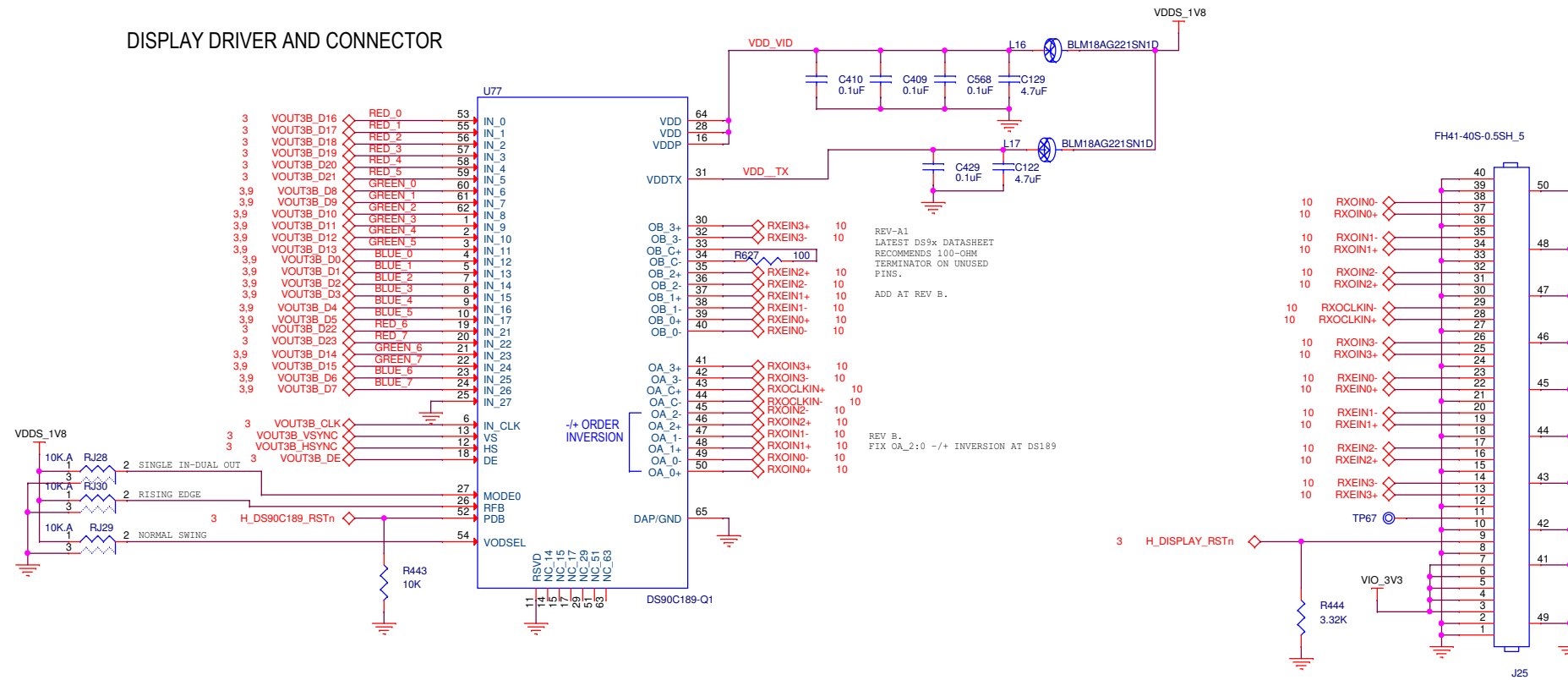
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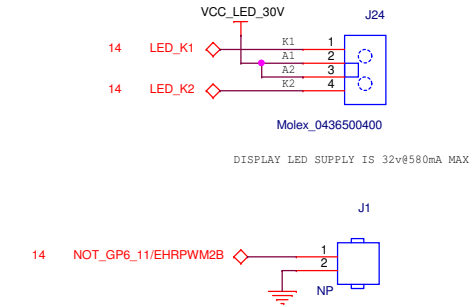
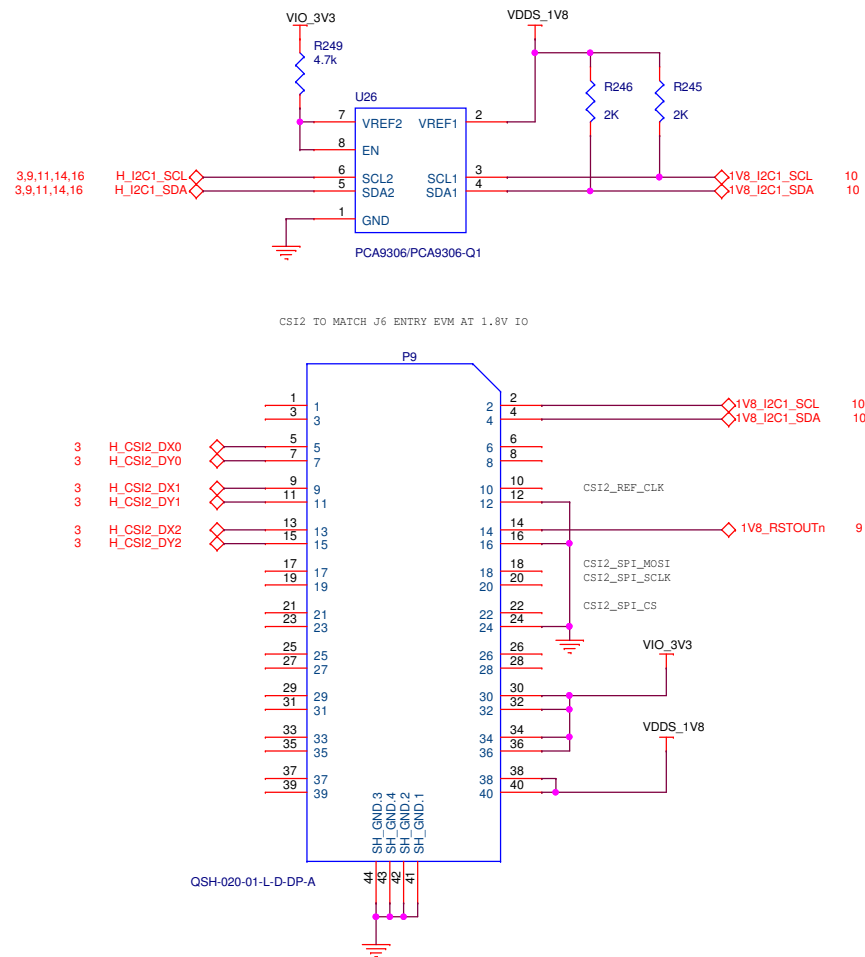


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DISPLAY DRIVER AND CONNECTOR



CSI2 EXPANSION



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Preliminary Information - Subject to change

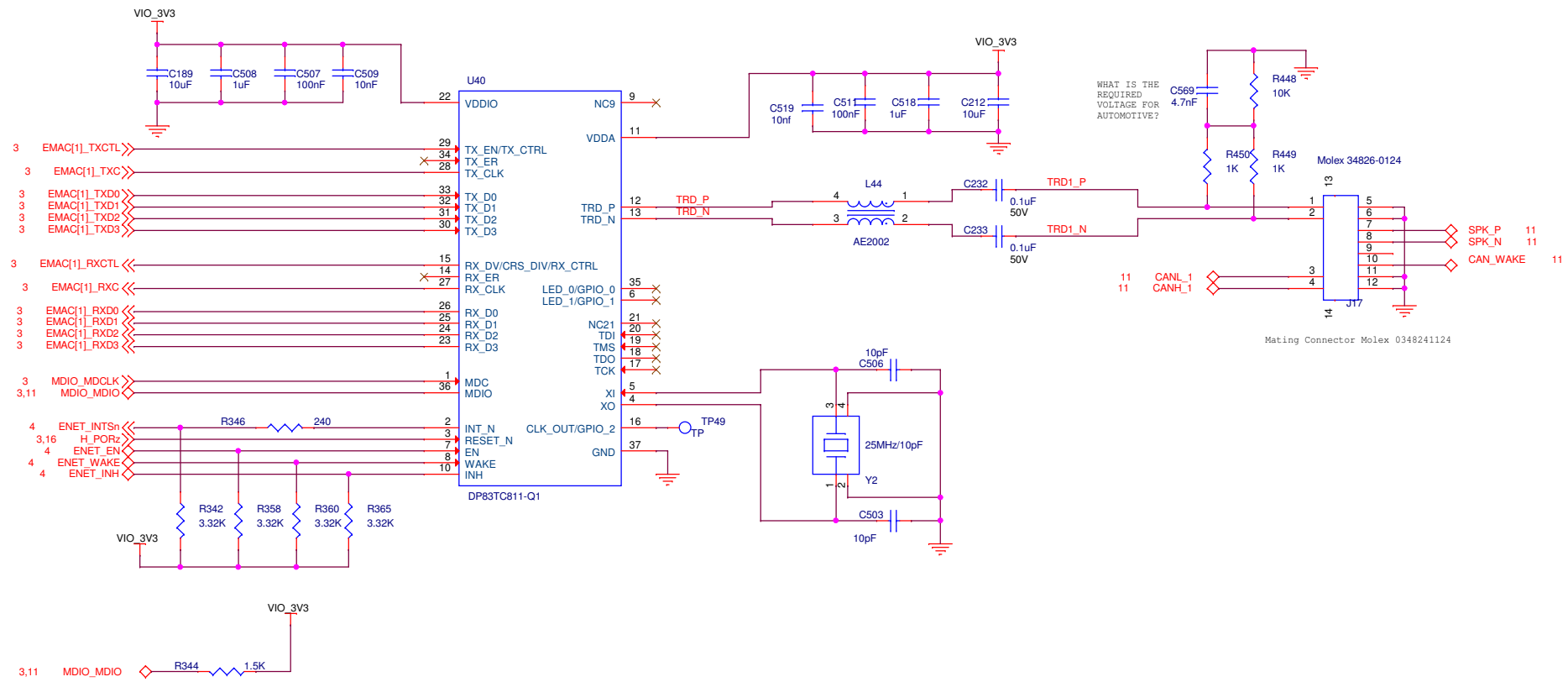
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Page Contents: DISPLAY/CSI2

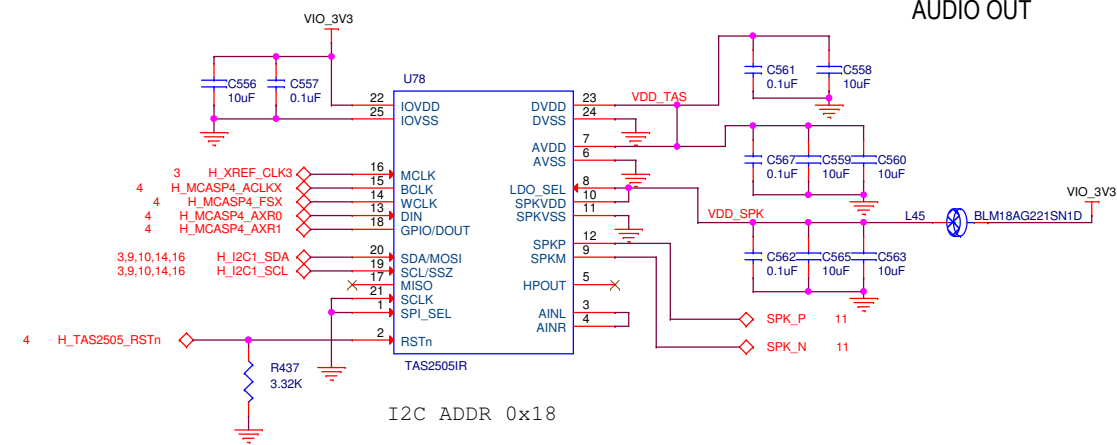
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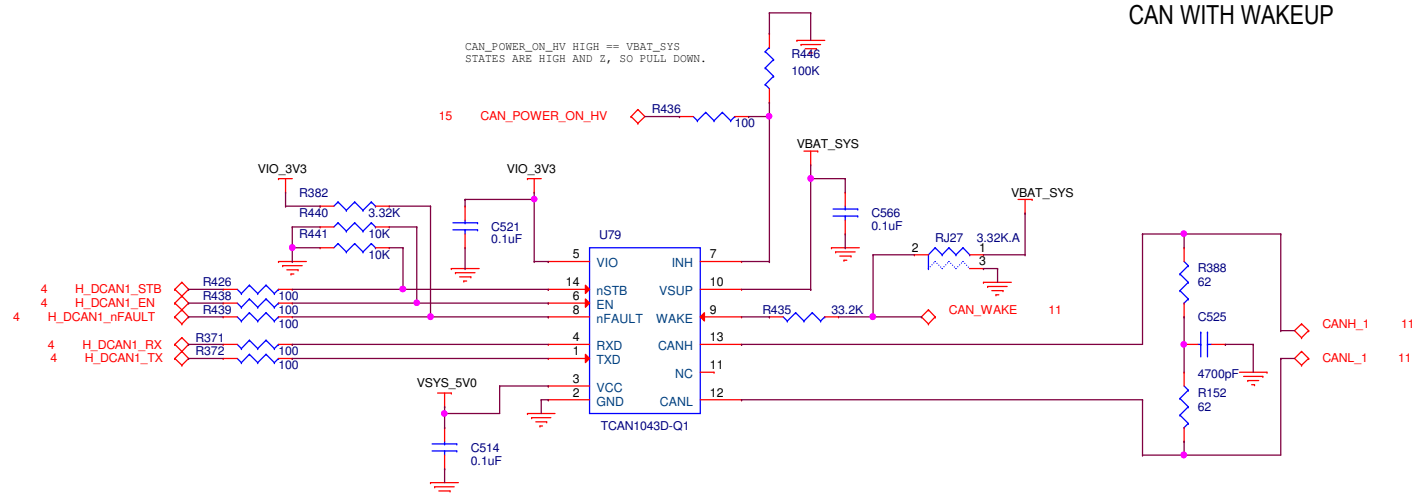
ENET



AUDIO OUT



CAN WITH WAKEUP



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Preliminary Information - Subject to change

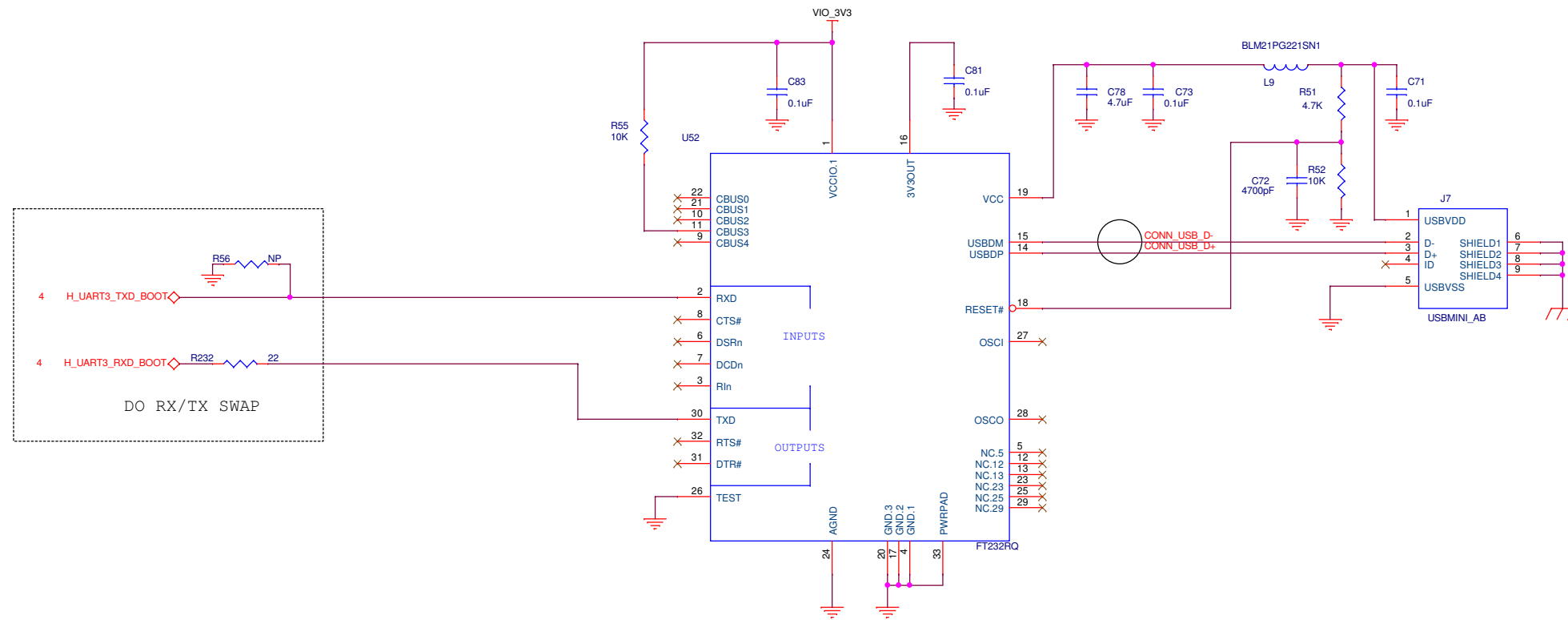
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Page Contents: ENET/CAN/CLASS-D

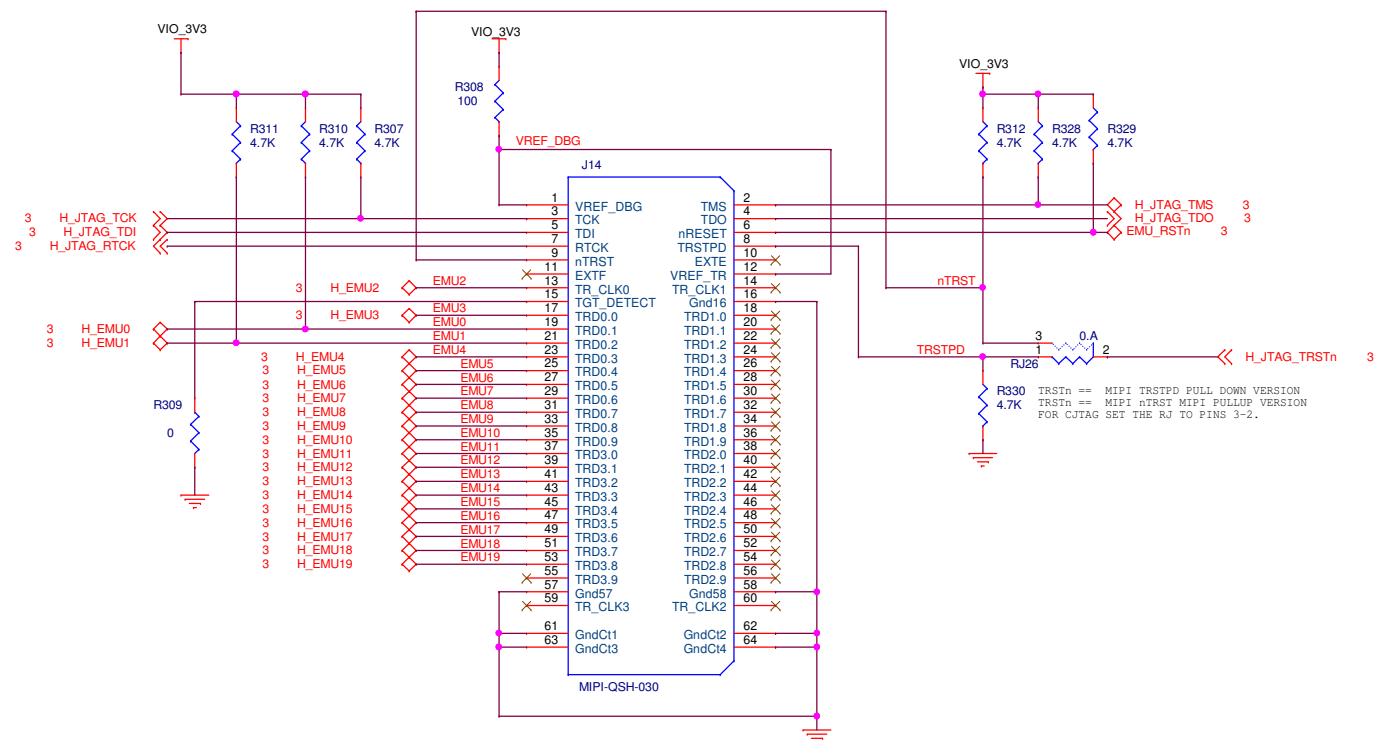
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TERMINAL/UART-BOOT



JTAG/DEBUG



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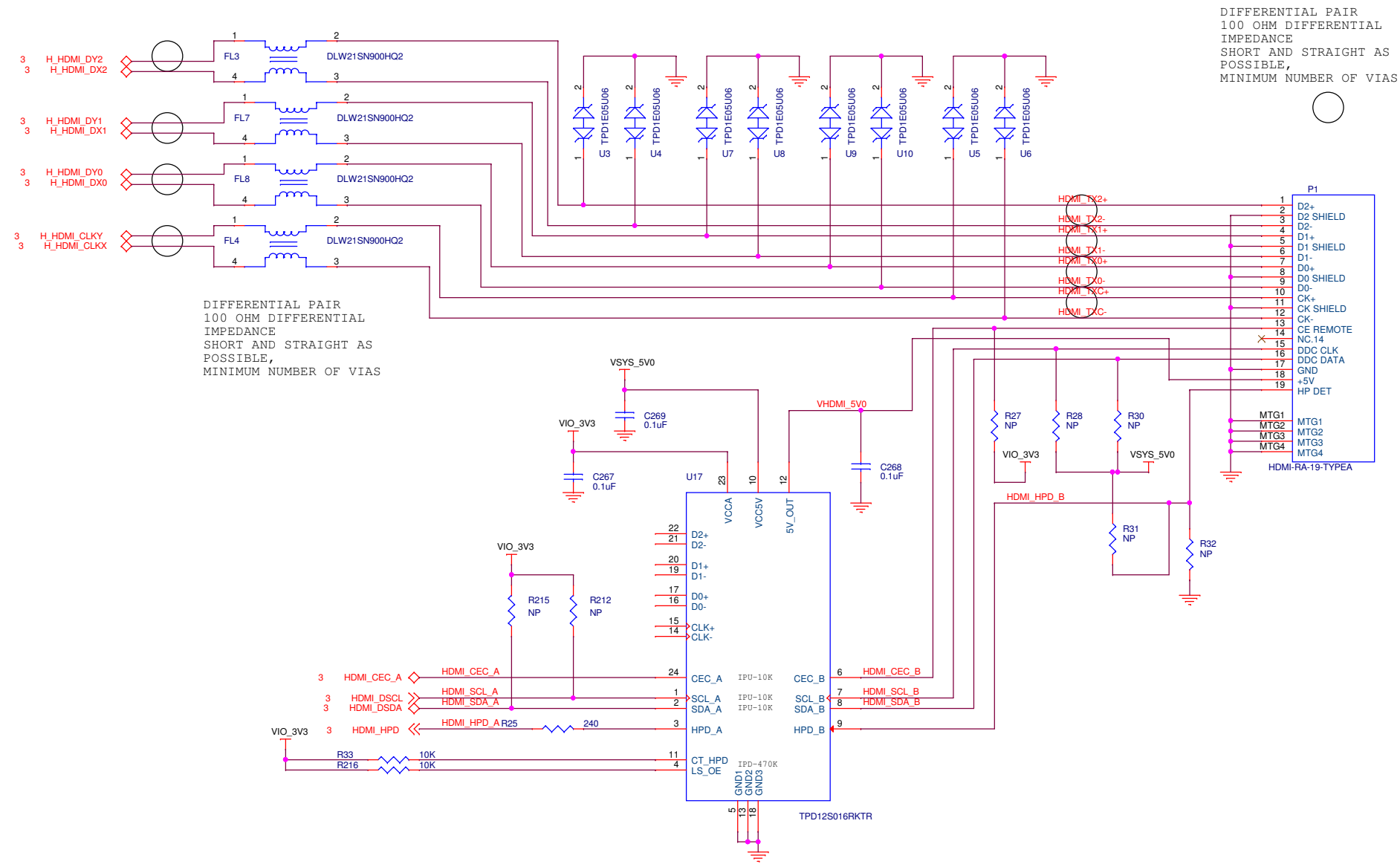
Preliminary Information - Subject to change

Title: DRA71x DCARD CPU Board

Page Contents: USB-UART/JTAG

Size: C DOC NO: 518872 REV: A

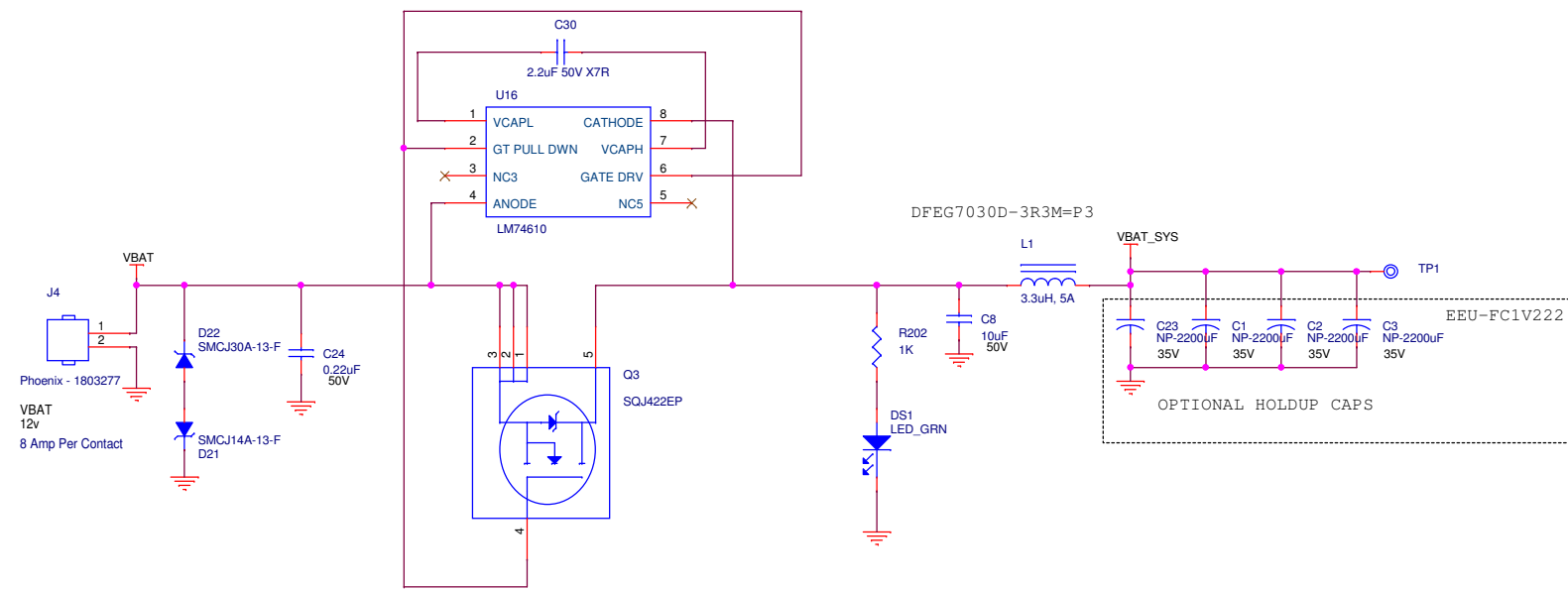
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DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

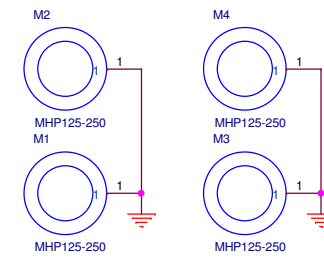
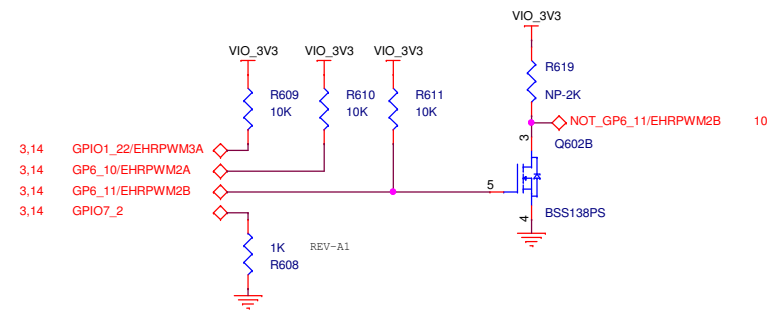
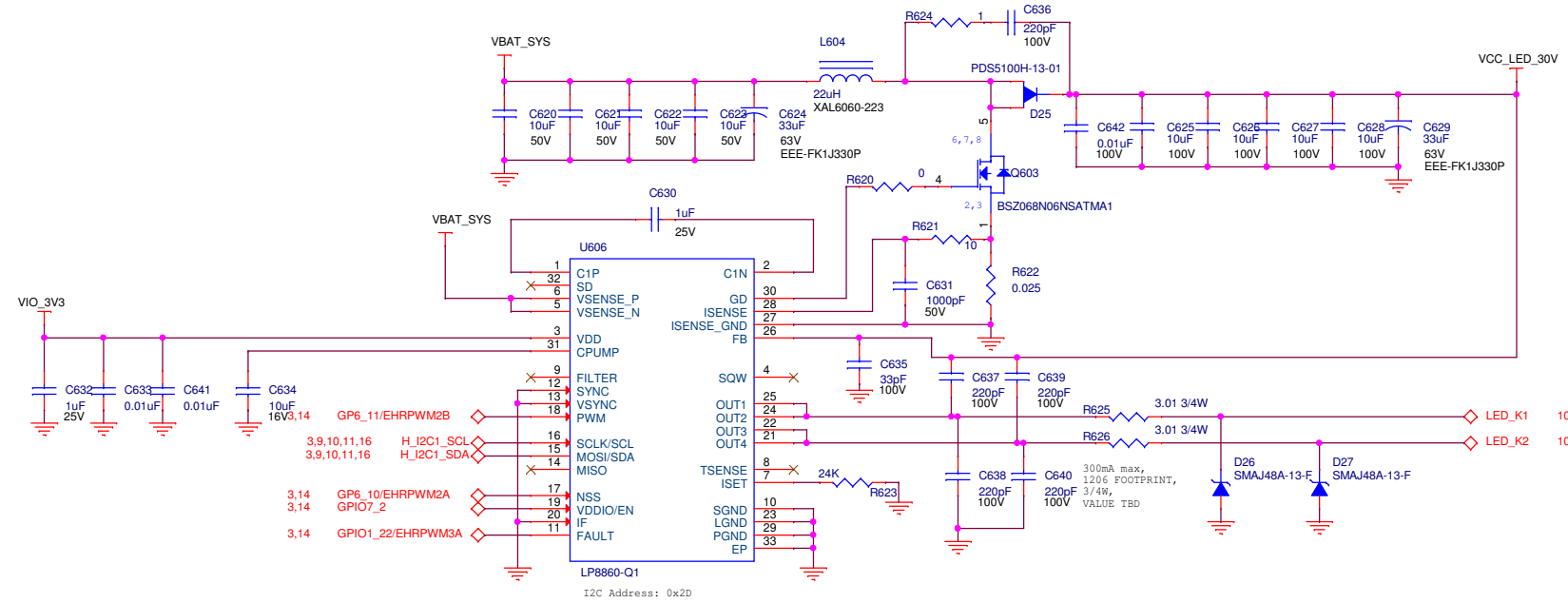
DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

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POWER INPUT AND PROTECTION

30V DISPLAY LED POWER



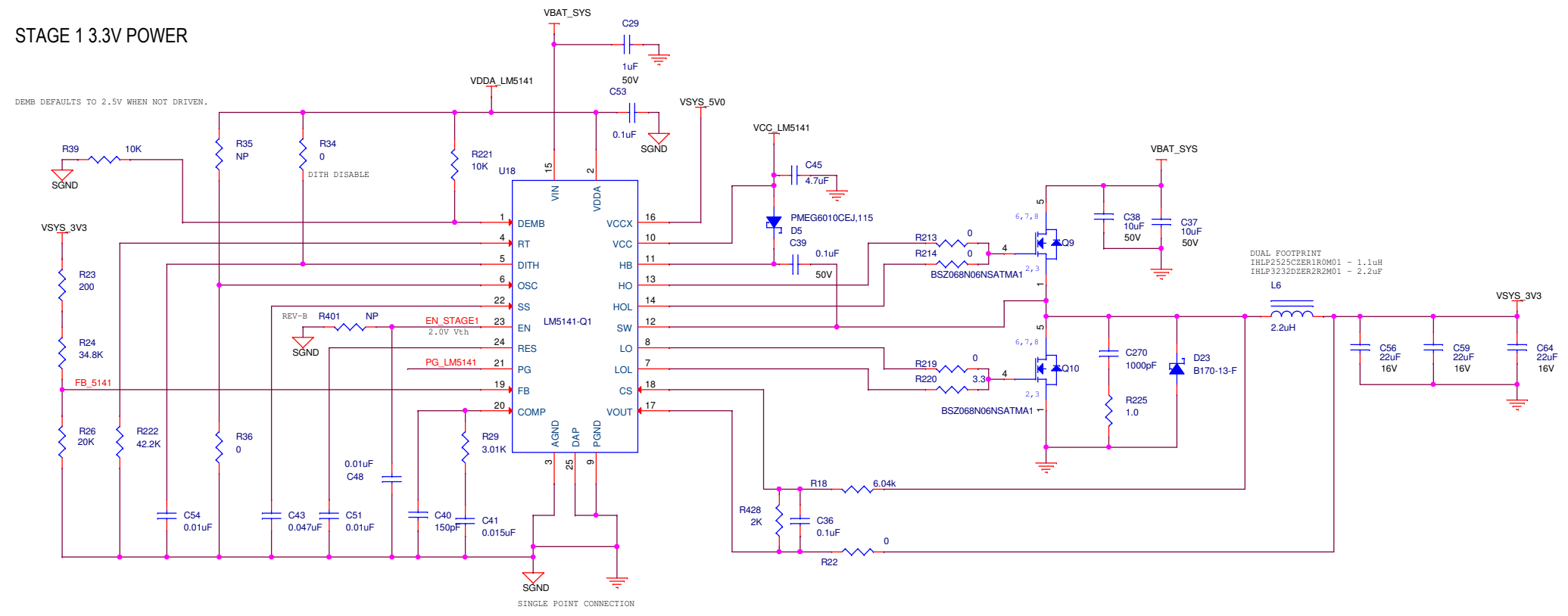
TEXAS INSTRUMENTS INCORPORATED

Preliminary Information - Subject to change

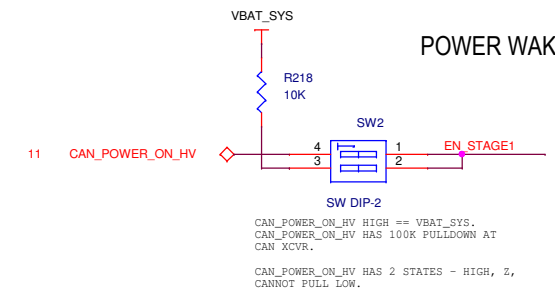
Title: DRA71x DCARD CPU Board		
Page Contents: INPUT/DISPLAY POWER		
Size: C	DOC NO: 518872	REV: A1
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STAGE 1 3.3V POWER

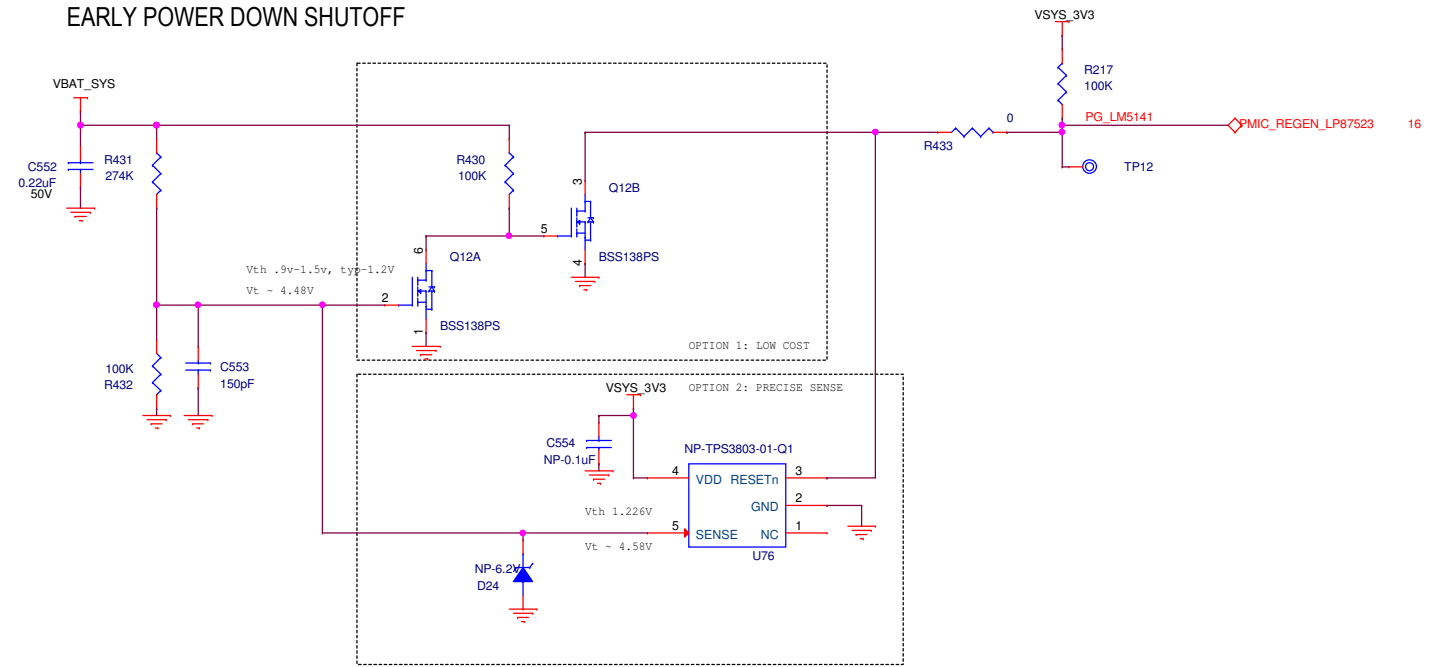
DEMB DEFAULTS TO 2.5V WHEN NOT DRIVEN.



POWER WAKEUP BYPASS

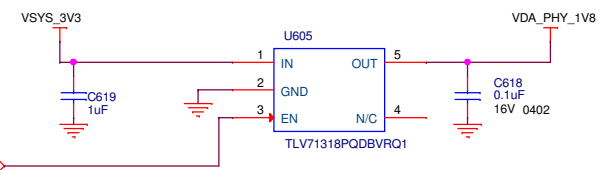
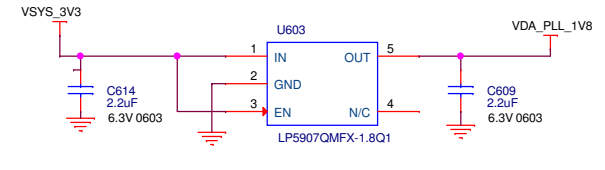
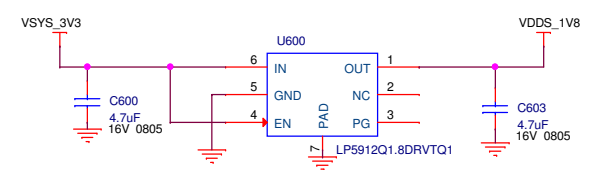
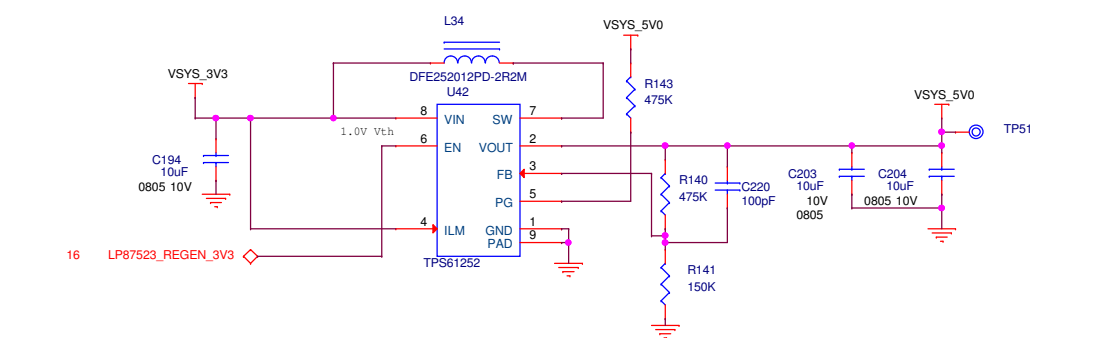
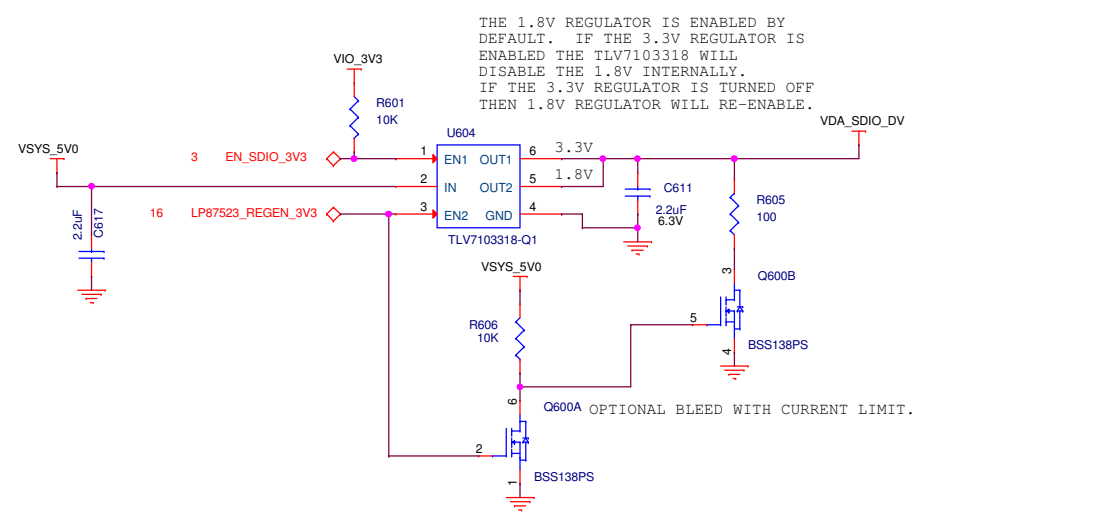
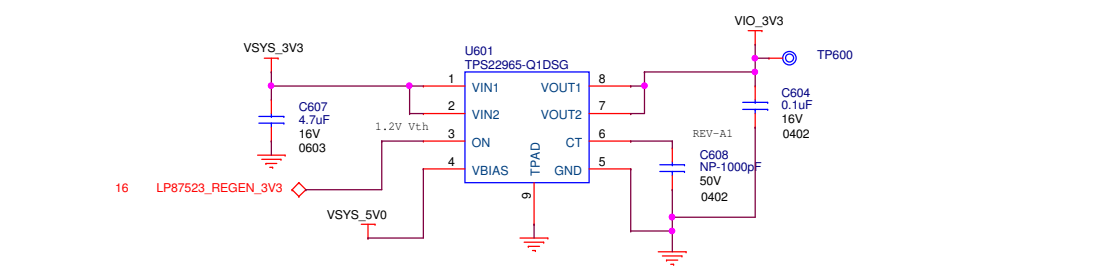
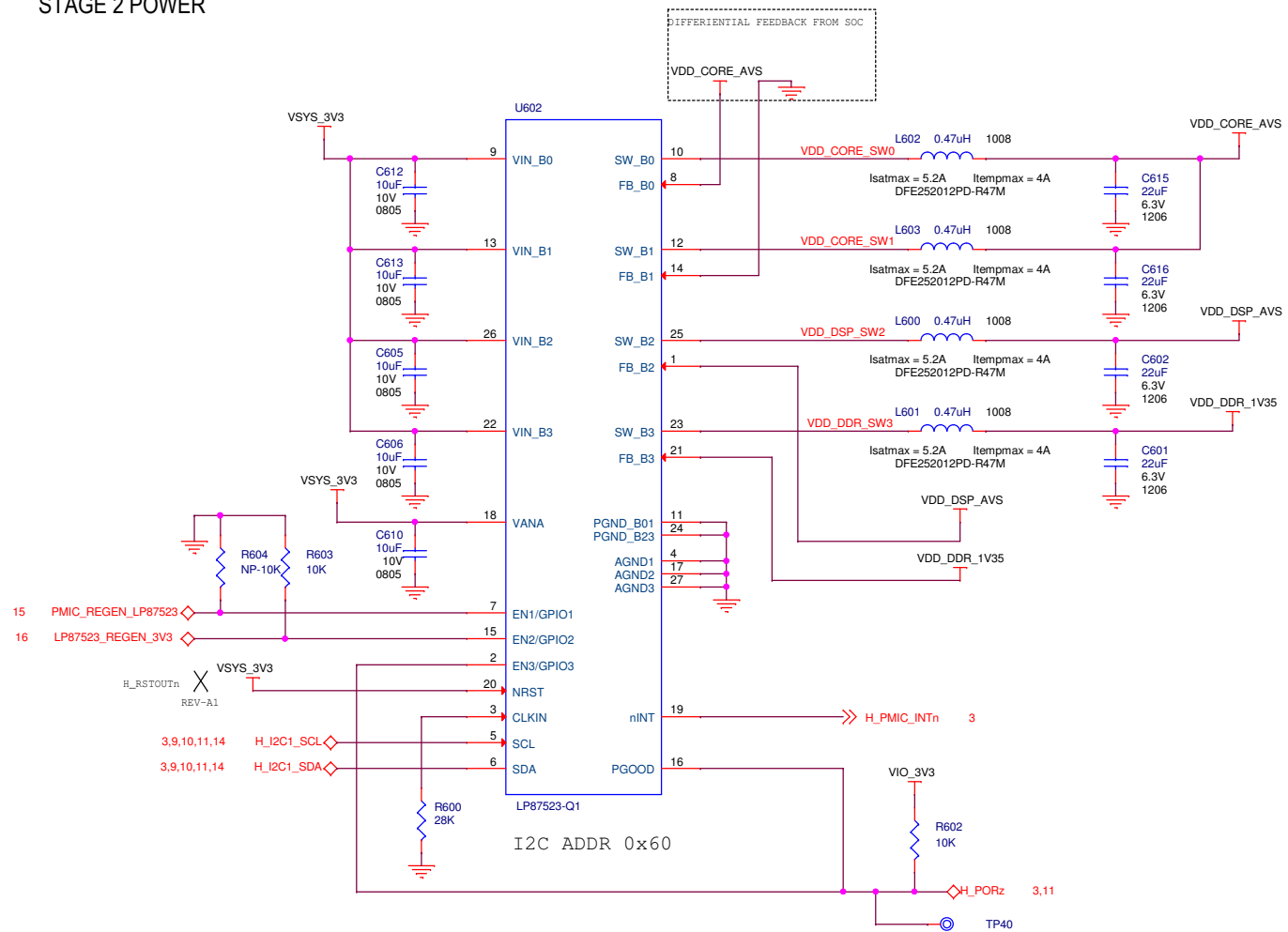


EARLY POWER DOWN SHUTOFF



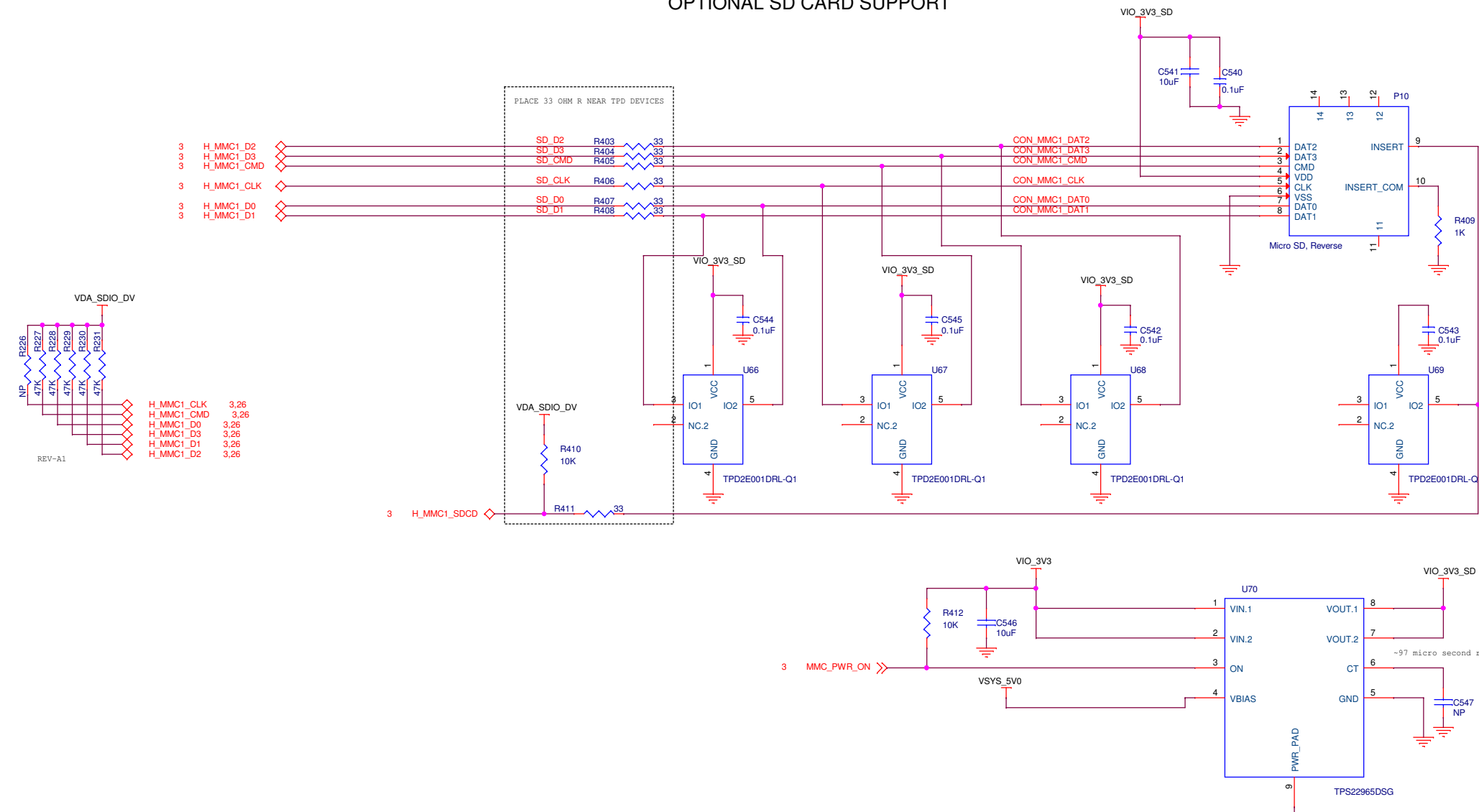
TEXAS INSTRUMENTS INCORPORATED		
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STAGE 2 POWER



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OPTIONAL SD CARD SUPPORT



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