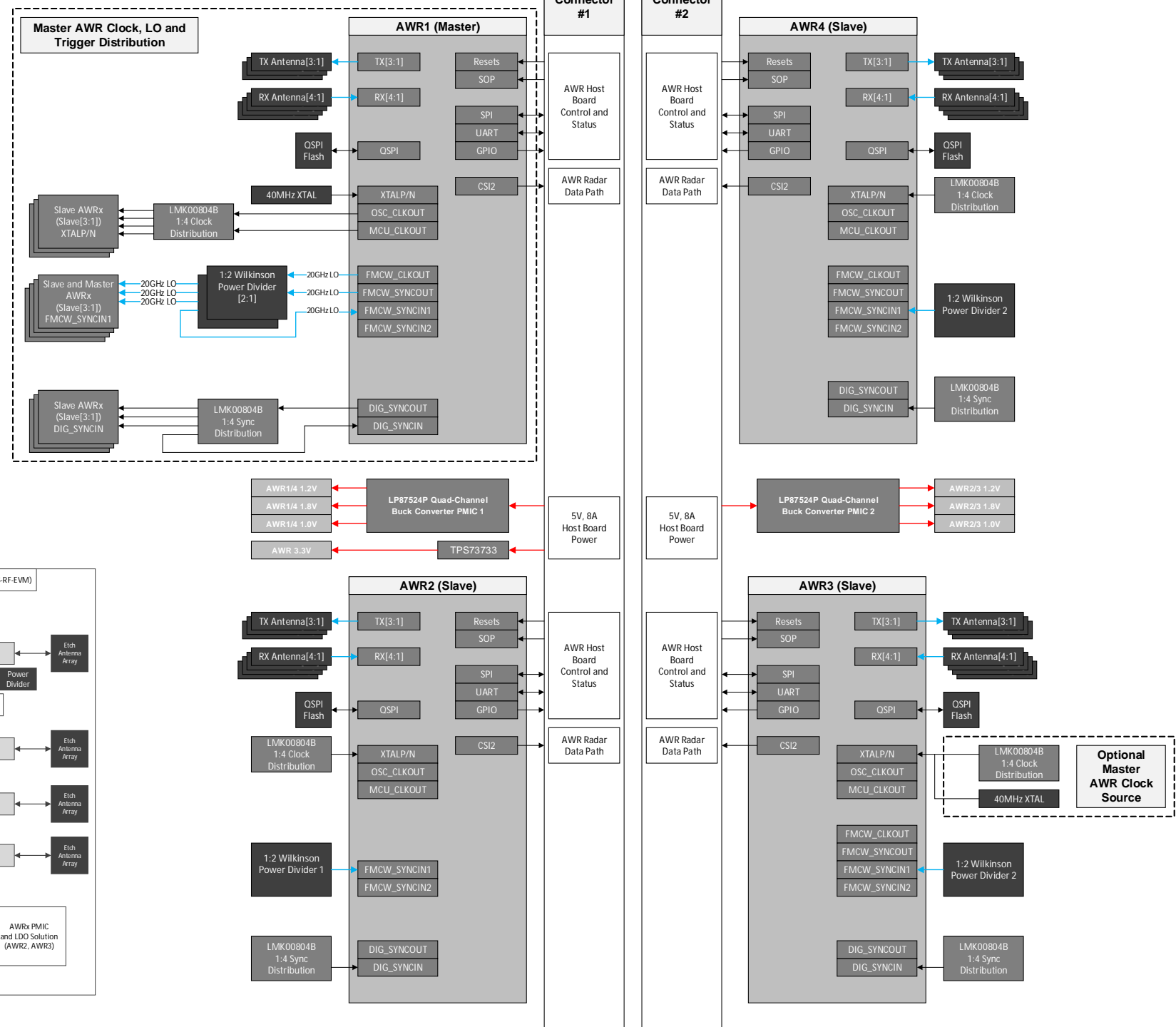


mmWave Cascade Radar RF Board (MMWCAS-RF-EVM)

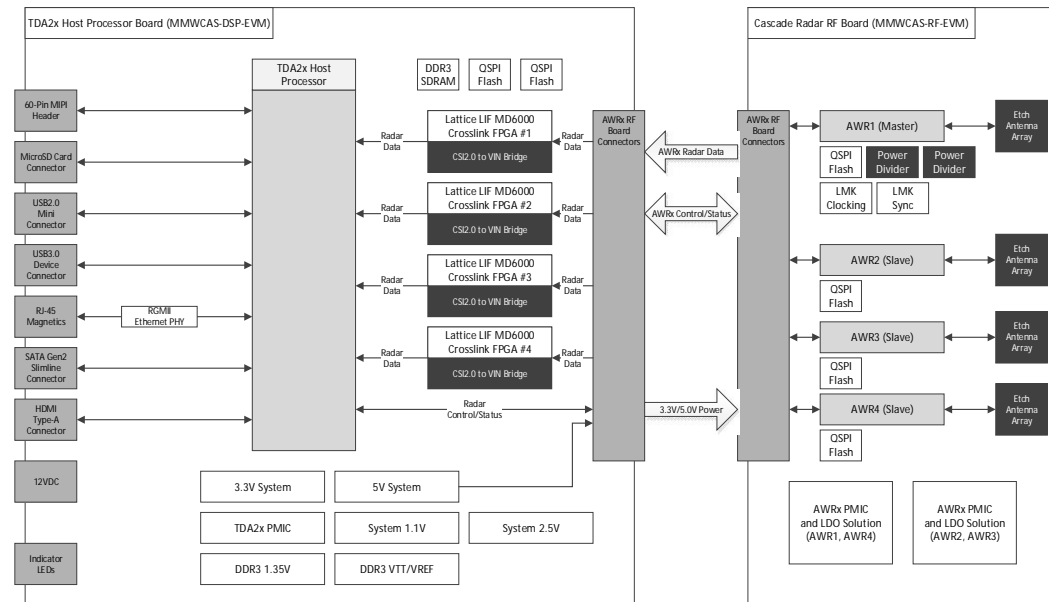
System Description

Cascade Radar RF Board	
4x AWRx 76-81GHz Radar SoC	Integrated VCO, LO distribution, PA, LNA, ADC, 3 TX and 4 RX ARM MCU R4 Controller
AWR RF Peripherals	
12x TX, 16x RX Antennas	12 total transmitters across all 4 AWRx devices 16 total receivers across all 4 AWRx devices
Embedded Antenna	4-element series-fed patch antenna
20 GHz LO Star Distribution	2x Wilkinson Power dividers fed by the Master AWRx device LO output to Slave AWRx devices
AWR Digital Peripherals	
CSI2.0 4-lane	600Mbps/Lane for 2.4Gbps ADC IF data per device
QSPI Flash	16Mbit QSPI flash for AWR firmware updates
Serial Peripherals	SPI, I2C, UART, GPIO
System Temperature	TMP112 I2C Temperature Sensors
Power	
Radar Power Management IC (PMIC) Solution	2x LP87524P Quad-Channel, Integrated FET, Buck Converters and LC filtering solution

Cascade Radar RF System Diagram



Cascade Radar Evaluation Kit Diagram



CASCADE RF BOARD	EVM HARDWARE	REVISION HISTORY
PROC054E_System_Top.SchDoc	PROC054E_EVM_Hardware.SchDoc	PROC054E_Revision_History.SchDoc

Cascade Radar RF Board - Top Level Schematic

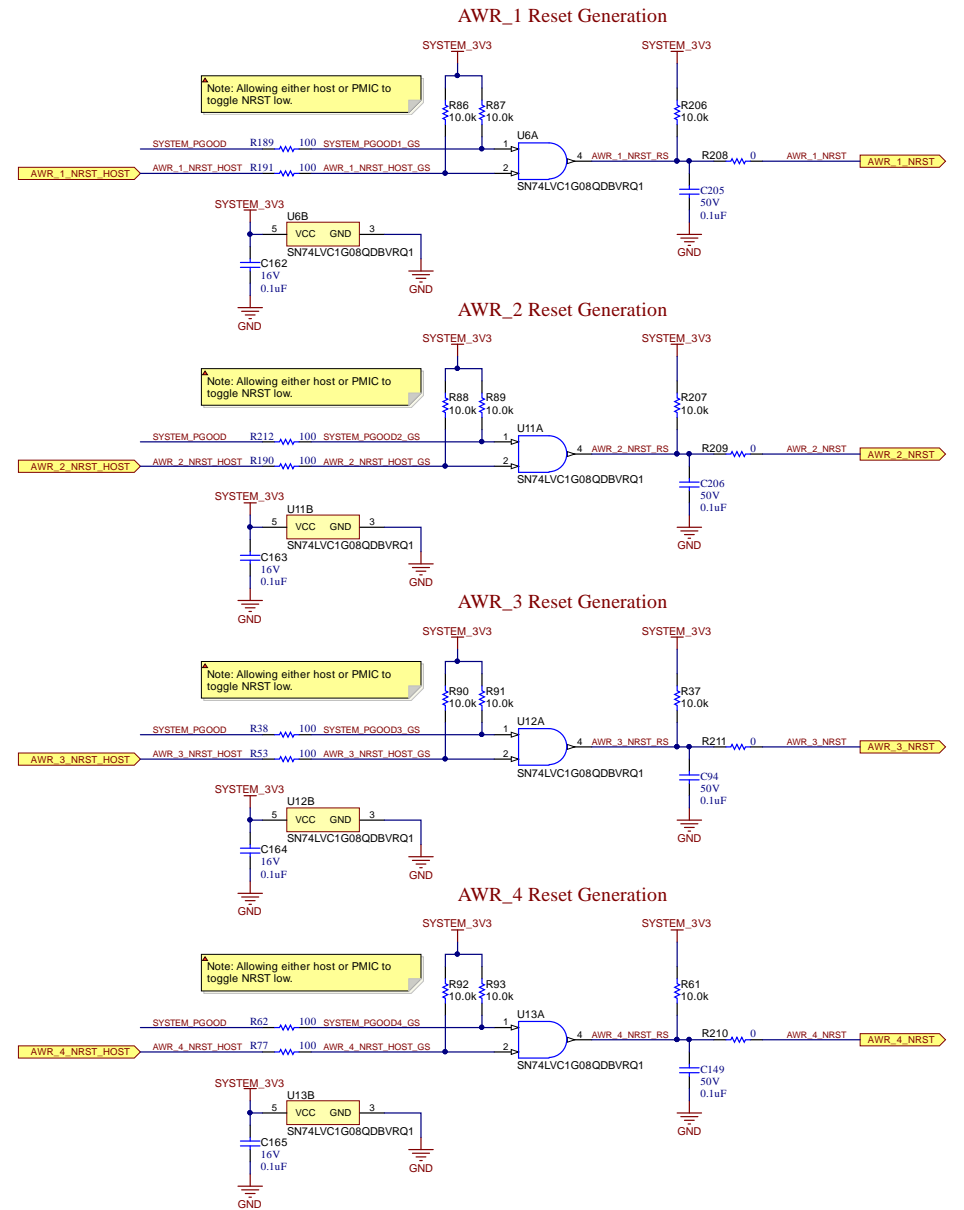
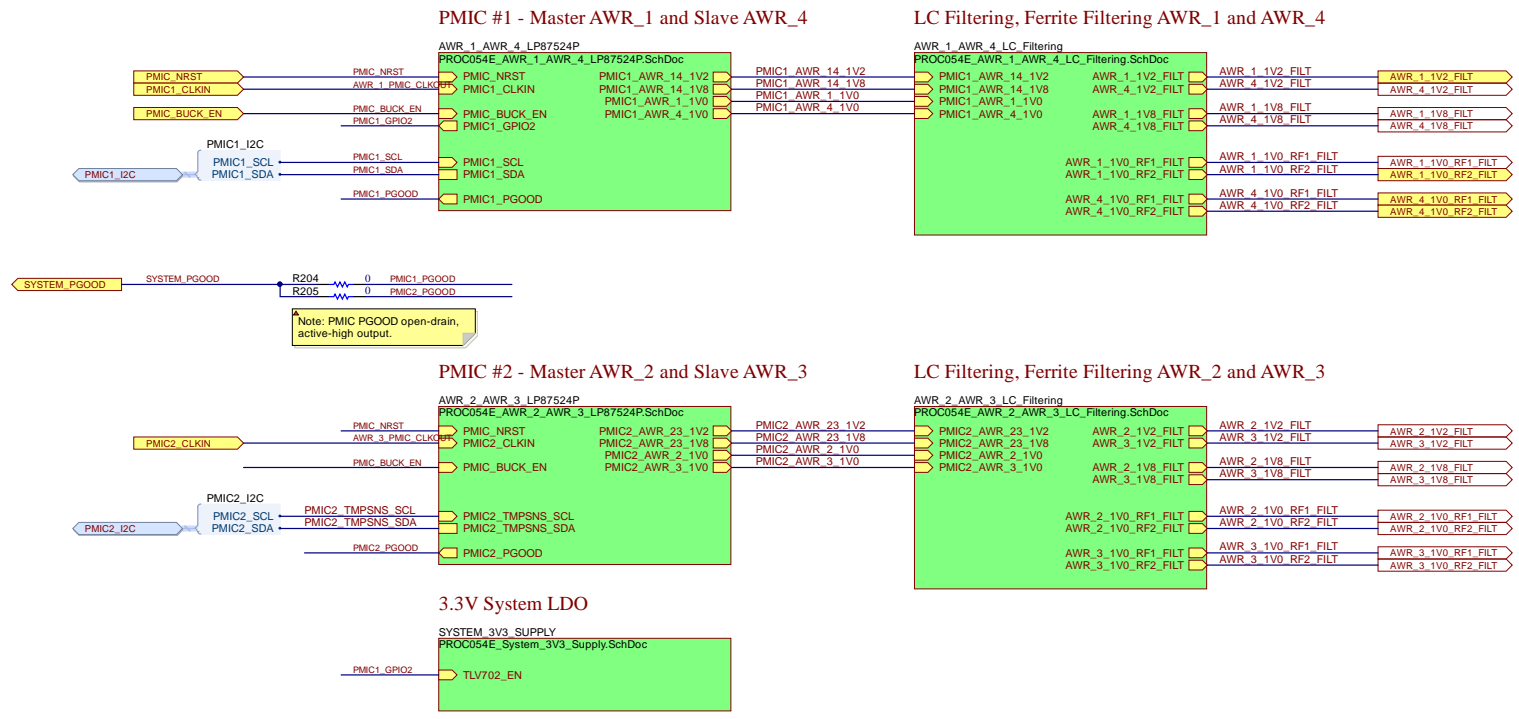


Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

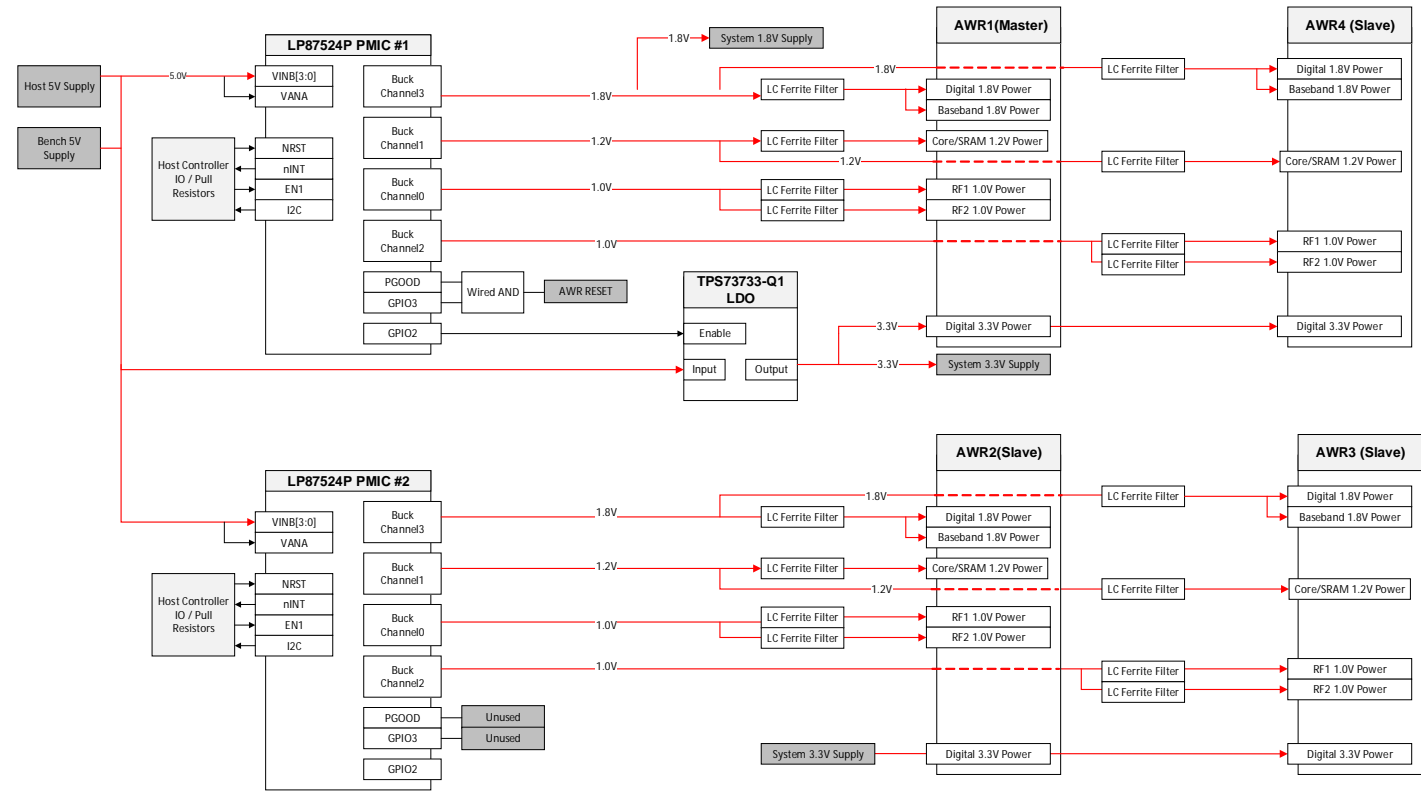
References

4-A+ 2.5-A - Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
 LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
 XWR1xxx Power Management Optimizations - Low Cost LC Filter Solution

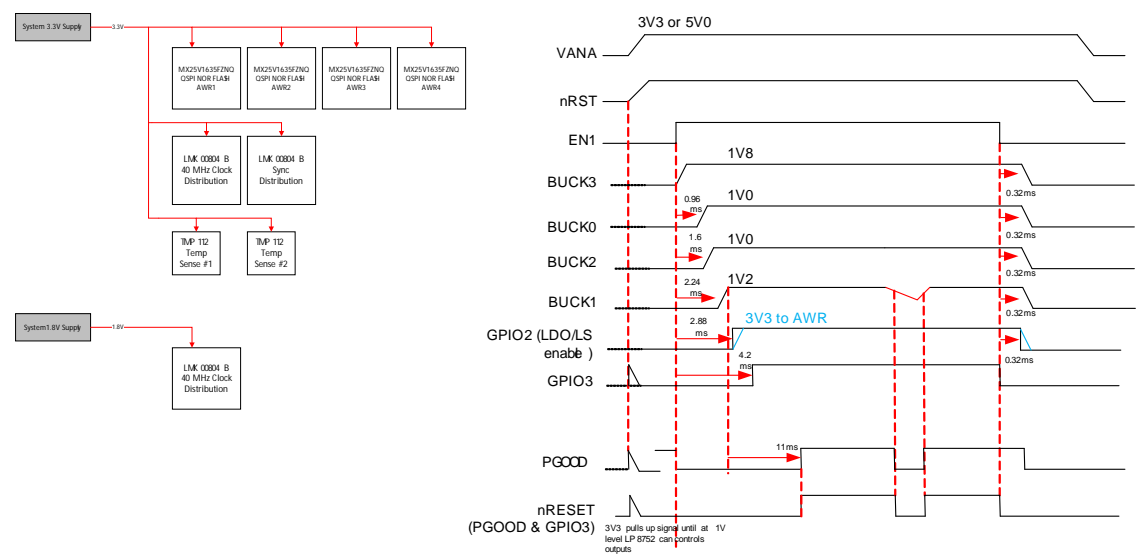
Cascade RF System Power



System Power Diagram



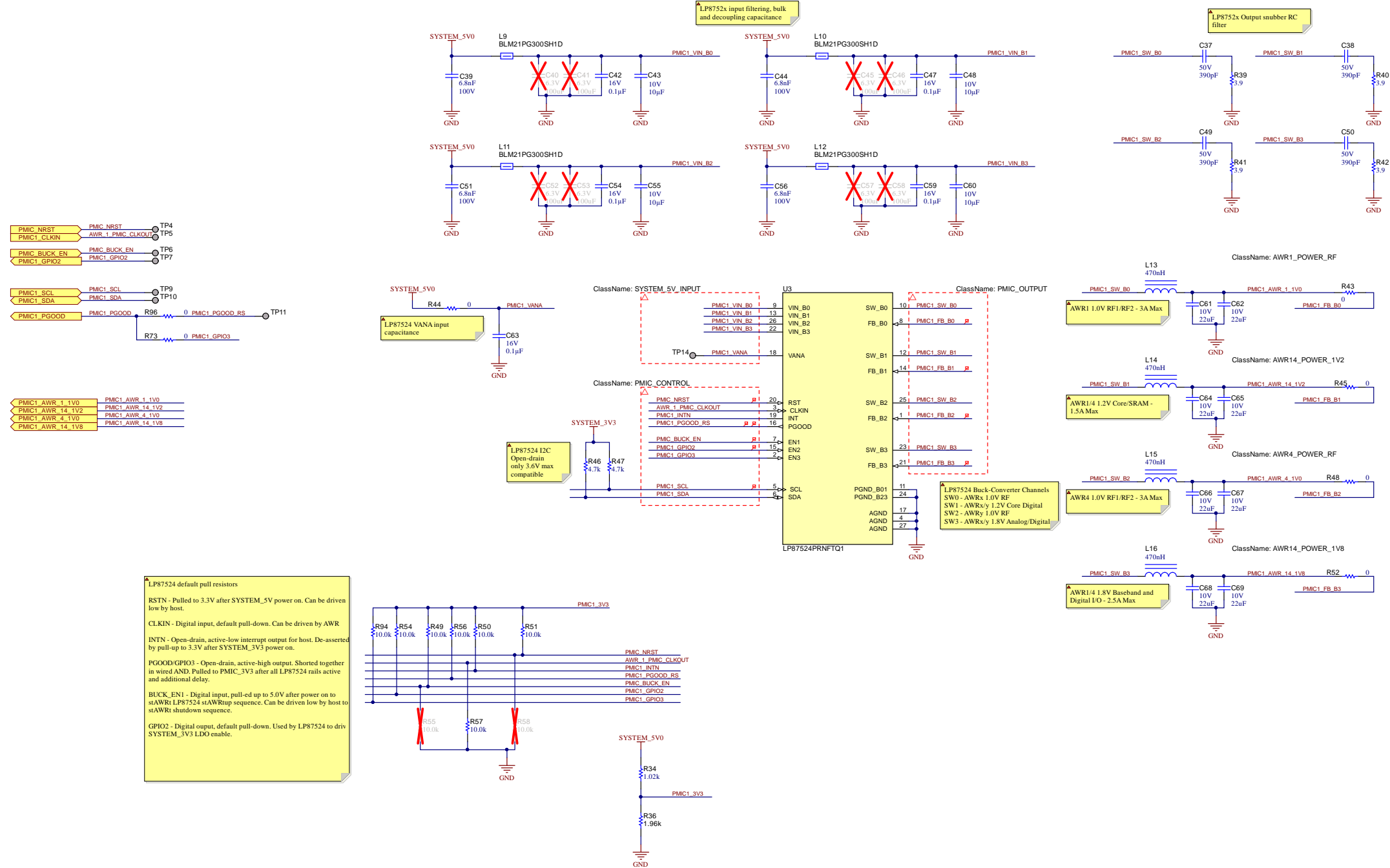
System Power Sequence Diagram



LP87524P Quad-Channel Synchronous Buck PMIC - Master AWR_1 and Slave AWR_4

References

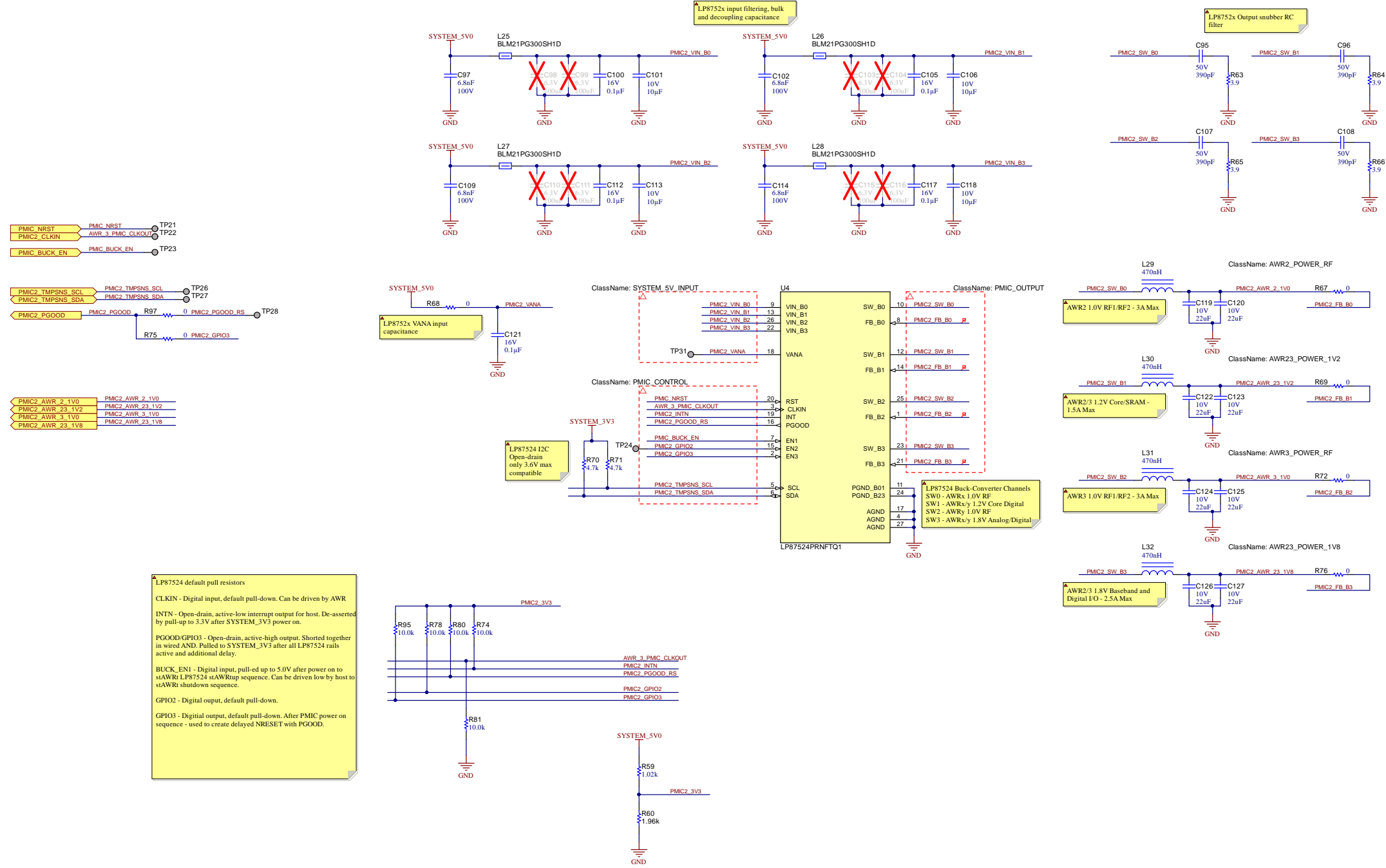
4-A+ 2-5-A - Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
 LP87524-Q1 Quad-Output, Single-Phase Buck Converter Evaluation Module
 XWR1xxx Power Management Optimizations - Low Cost LC Filter Solution



LP87524P Quad-Channel Synchronous Buck PMIC - Slave AWR_2 and Slave AWR_3

References

4-A+ 2-5-A - Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
 LP87524-Q1 Quad-Output, Single-Phase Buck Converter Evaluation Module
 XWR1xxx Power Management Optimizations - Low Cost LC Filter Solution



LP87524 default pull resistors

CLKIN - Digital input, default pull-down. Can be driven by AWR

INTN - Open-drain, active-low interrupt output for host. De-asserted by pull-up to 3.3V after SYSTEM_3V3 power on.

PGOOD/GPIO3 - Open-drain, active-high output. Shorted together in wired AND. Pulled to SYSTEM_3V3 after all LP87524 rails active and additional delay.

BUCK_EN1 - Digital input, pull-up to 5.0V after power on to stAWR1 LP87524 stAWR1up sequence. Can be driven low by host to stAWR1 shutdown sequence.

GPIO2 - Digital output, default pull-down.

GPIO3 - Digital output, default pull-down. After PMIC power on sequence - used to create delayed NRESET with PGOOD.

References

4-A+ 2.5-A - Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
 LP27524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
 XWR1xxx Power Management Optimizations - Low Cost LC Filter Solution

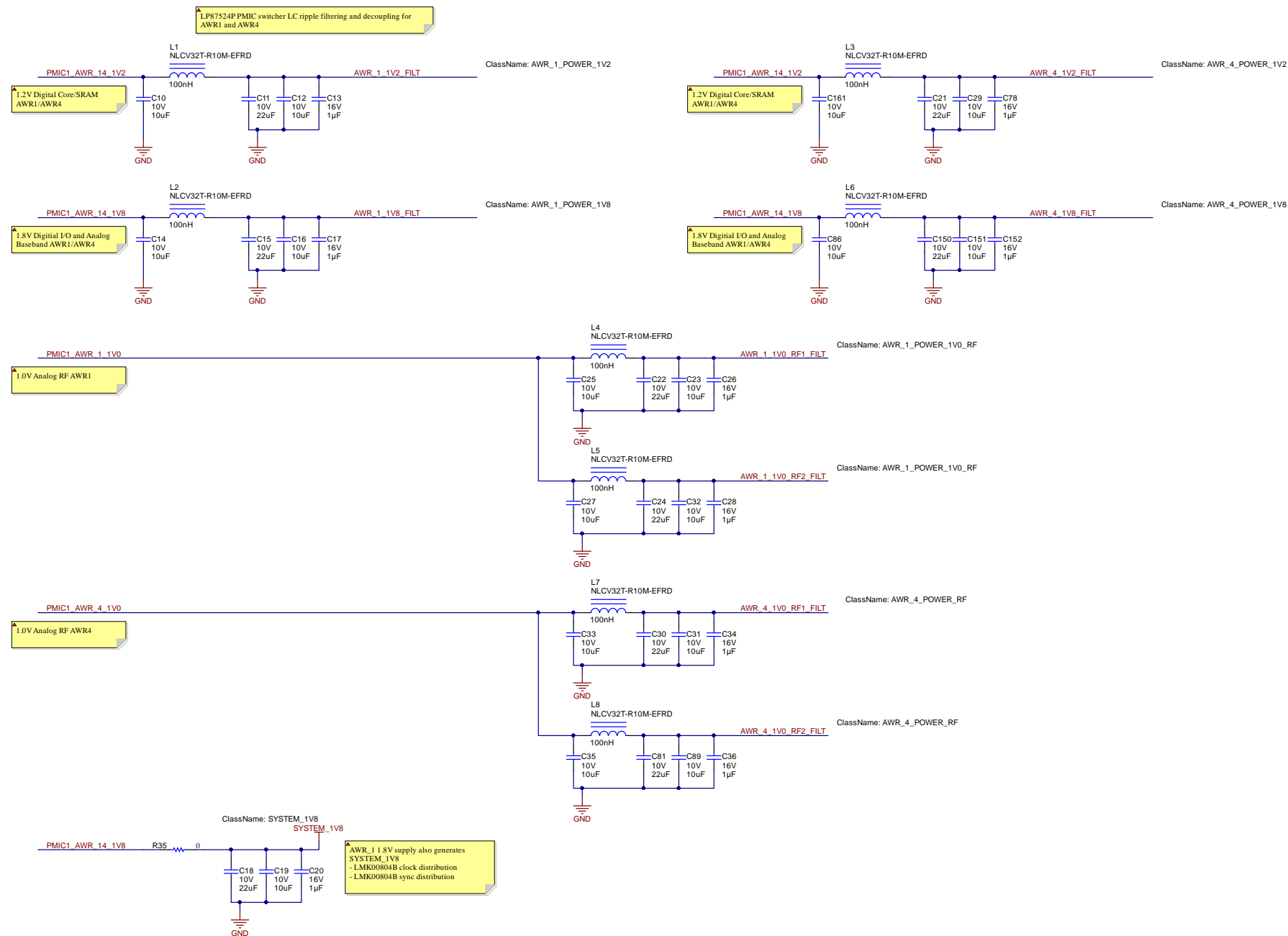
AWR Power Filtering and Decoupling - Master AWR_1 and Slave AWR_4

PMIC1_AWR_14_1V2	PMIC1_AWR_14_1V2
PMIC1_AWR_14_1V8	PMIC1_AWR_14_1V8
PMIC1_AWR_1_1V0	PMIC1_AWR_1_1V0
PMIC1_AWR_4_1V0	PMIC1_AWR_4_1V0

AWR_1_1V2_FILT	AWR_1_1V2_FILT
AWR_4_1V2_FILT	AWR_4_1V2_FILT

AWR_1_1V8_FILT	AWR_1_1V8_FILT
AWR_4_1V8_FILT	AWR_4_1V8_FILT

AWR_1_1V0_RF1_FILT	AWR_1_1V0_RF1_FILT
AWR_1_1V0_RF2_FILT	AWR_1_1V0_RF2_FILT
AWR_4_1V0_RF1_FILT	AWR_4_1V0_RF1_FILT
AWR_4_1V0_RF2_FILT	AWR_4_1V0_RF2_FILT



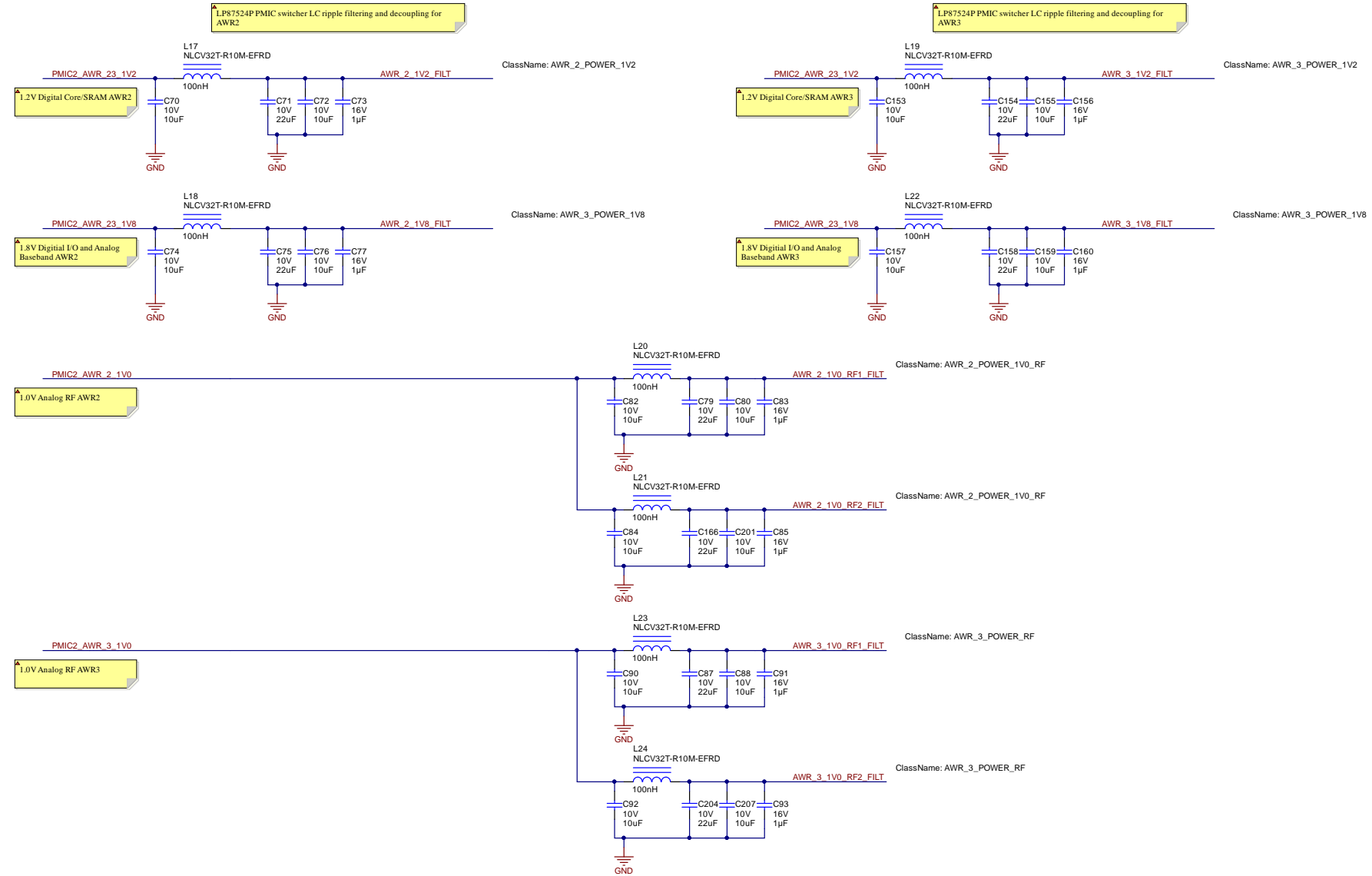
AWR1243 Power Filtering and Decoupling - Master AWR_2 and Slave AWR_3

References

4-A+ 2.5-A - Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
 LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
 XWR1xxx Power Management Optimizations - Low Cost LC Filter Solution

PMIC2_AWR_23_1V2 PMIC2_AWR_23_1V2
 PMIC2_AWR_23_1V8 PMIC2_AWR_23_1V8
 PMIC2_AWR_2_1V0 PMIC2_AWR_2_1V0
 PMIC2_AWR_3_1V0 PMIC2_AWR_3_1V0

AWR_2_1V2_FILT AWR_2_1V2_FILT
 AWR_3_1V2_FILT AWR_3_1V2_FILT
 AWR_2_1V8_FILT AWR_2_1V8_FILT
 AWR_3_1V8_FILT AWR_3_1V8_FILT
 AWR_2_1V0_RF1_FILT AWR_2_1V0_RF1_FILT
 AWR_2_1V0_RF2_FILT AWR_2_1V0_RF2_FILT
 AWR_3_1V0_RF1_FILT AWR_3_1V0_RF1_FILT
 AWR_3_1V0_RF2_FILT AWR_3_1V0_RF2_FILT

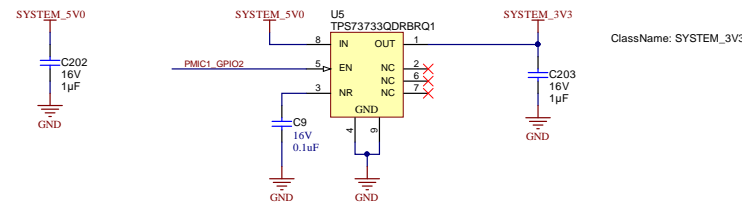


System 3.3V Supply

References

TLV7028EVM-463 Evaluation Module
 TPS22965 Evaluation Module

TPS73733-Q1 5.0V to 3.3V LDO - System 3.3V Power



TLV702_EN PMIC1_GPIO2

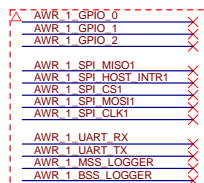
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system.

Orderable: MMW_CAS_RF_EVM	Designed for: Public Release	Mod. Date: 8/14/2020
TID #: N/A	Project Title: MMW_CAS_RF_EVM	
Number: PROC054	Rev: E	Sheet Title: System_3V3_Supply
Rev: Not in version control	Assembly VAWRiant:	Sheet: 8 of 19
Drawn By: a0271760	File: PROC054E_System_3V3_SupplySchDoc	Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave	http://www.ti.com

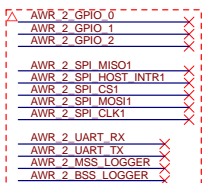


Host to RF Board Connectors

ClassName: AWR_1_GENERAL



ClassName: AWR_2_GENERAL

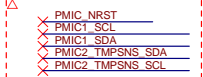


EXT DIG SYNC
EXT 40MHZ CLK 1V8

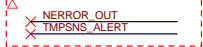
ClassName: AWR_SYNC

ClassName: AWR_CLOCK

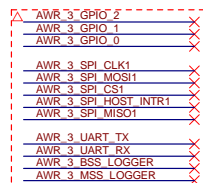
ClassName: PMIC_CONTROL



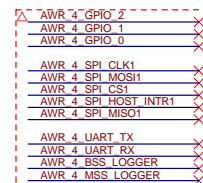
ClassName: AWR_SAFETY



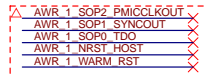
ClassName: AWR_3_GENERAL



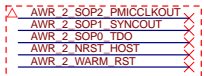
ClassName: AWR_4_GENERAL



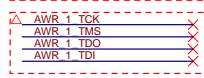
ClassName: AWR_1_SOP_RESET



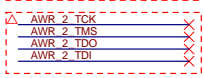
ClassName: AWR2_SOP_RESET



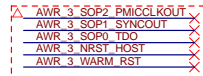
ClassName: AWR_1_JTAG



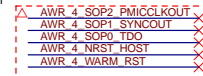
ClassName: AWR_2_JTAG



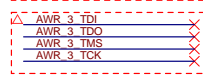
ClassName: AWR_3_SOP_RESET



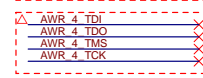
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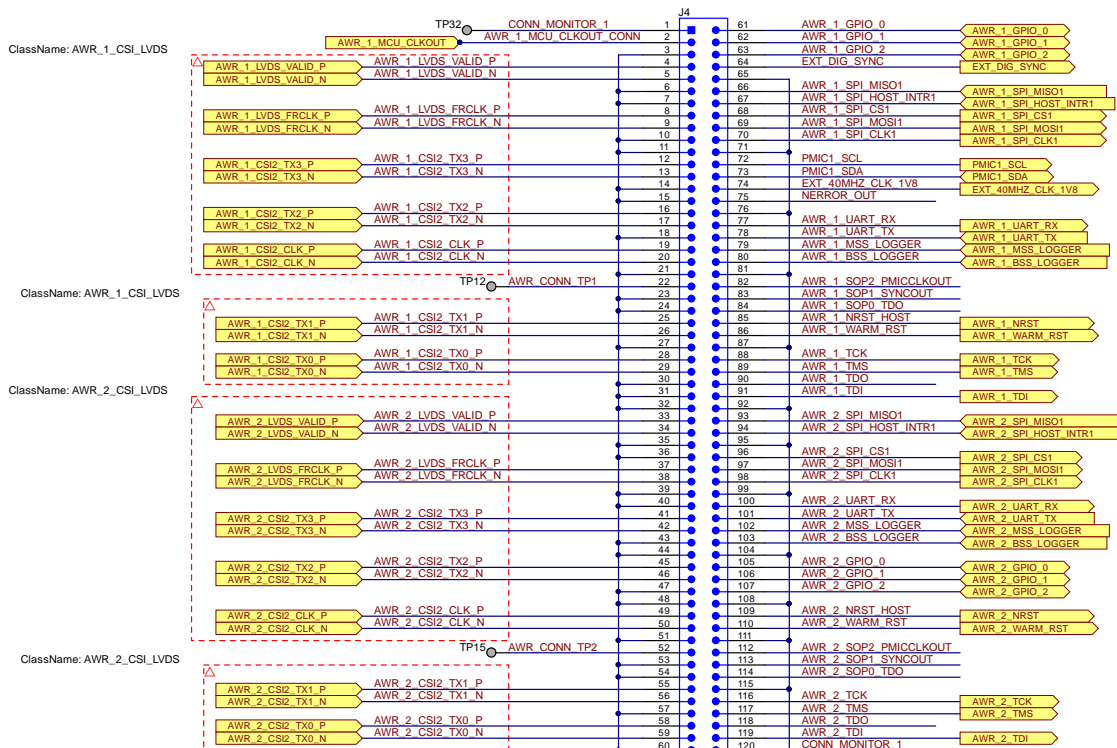
ClassName: AWR_3_JTAG



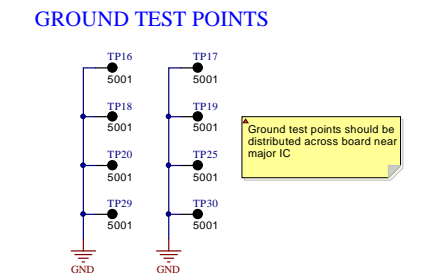
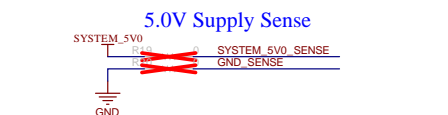
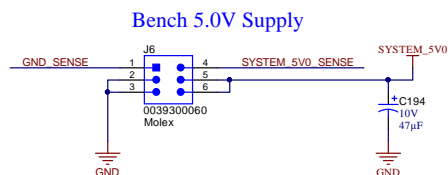
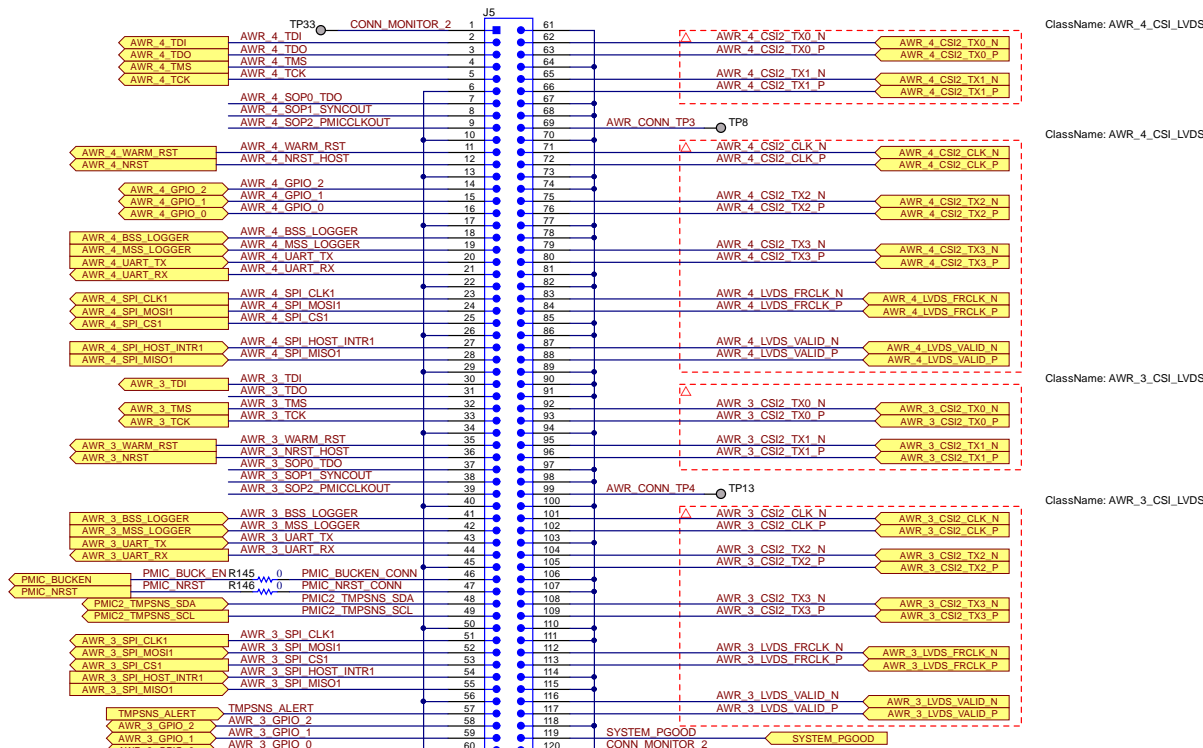
ClassName: AWR_4_JTAG



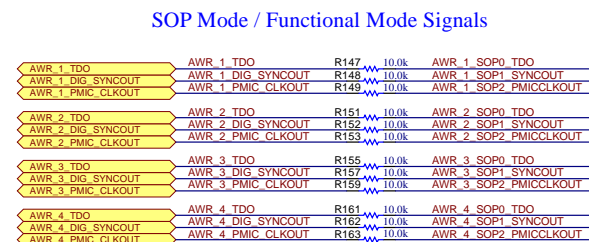
Host Board Connector 1



Host Board Connector 2

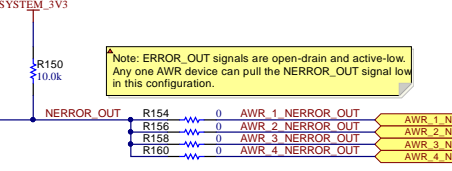


Ground test points should be distributed across board near major IC

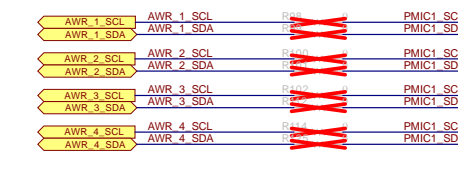


Note: Both functional mode and SOP modes of TDO signals are provided at the RF Host Interface connector. Host device should not simultaneously drive the SOP mode pin and functional pin.

Safety Error Signals



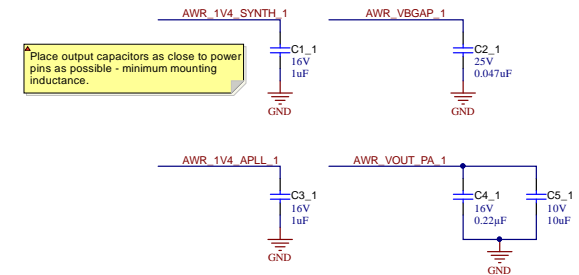
AWR and PMIC I2C Signals



AWR Radar SoC - Interfaces

References
<http://www.ti.com/product/AWR2243>

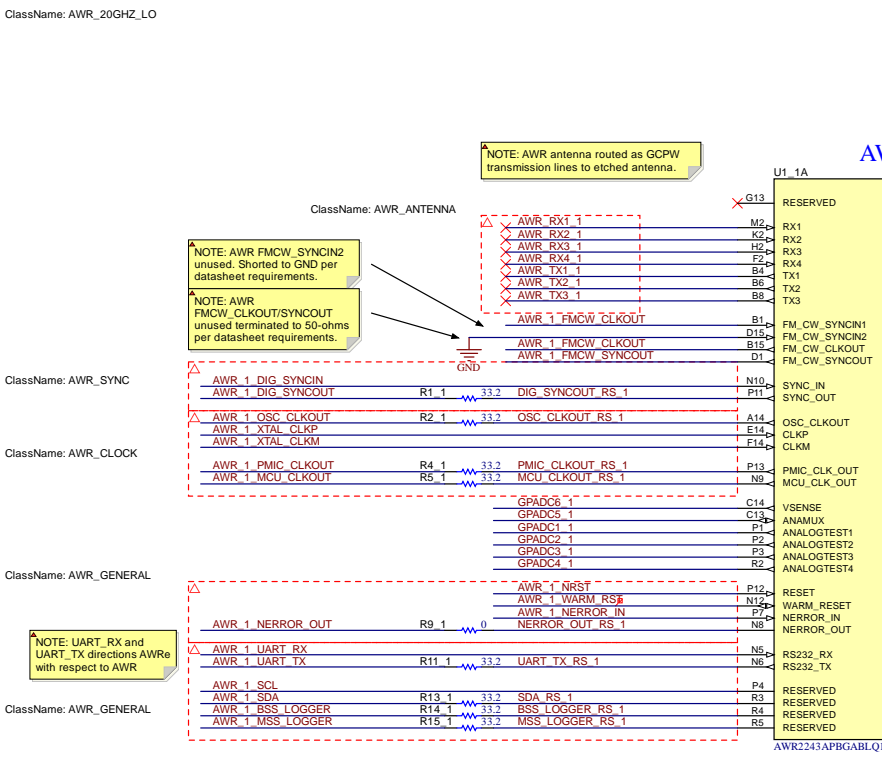
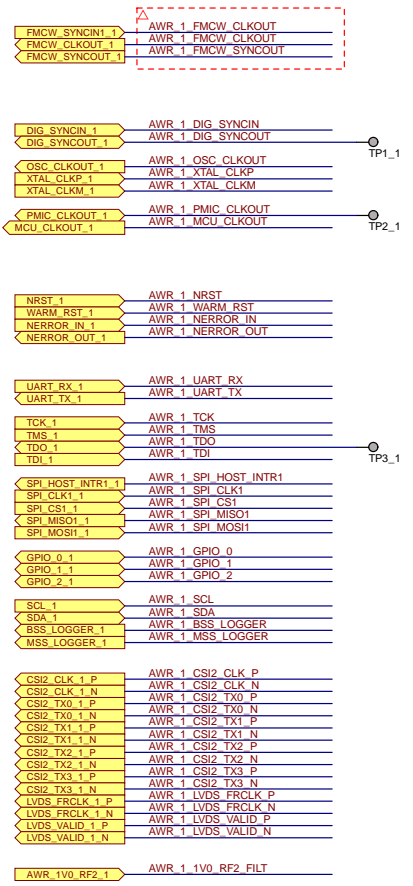
AWR LDO and Bandgap Output Capacitors



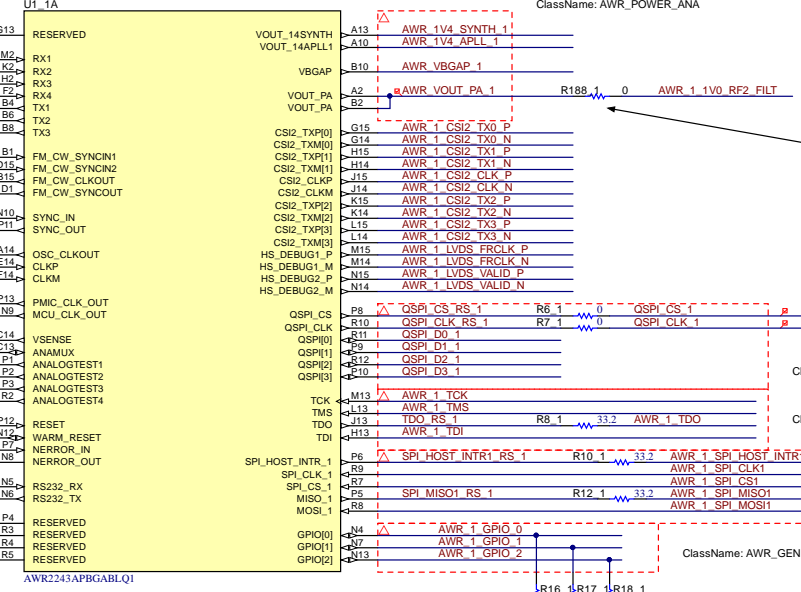
Place R188 as close as possible to VOUT_PA/RF2 pins

Note: AWR_1V0_RF2 optionally shorted to AWR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.
 R188 installed - shorts AWR_VOUT_PA to AWR_1V0_RF2 (default)
 R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

Place termination and pull-up resistors close to QSPI controller - minimize stubs.



AWR Interfaces

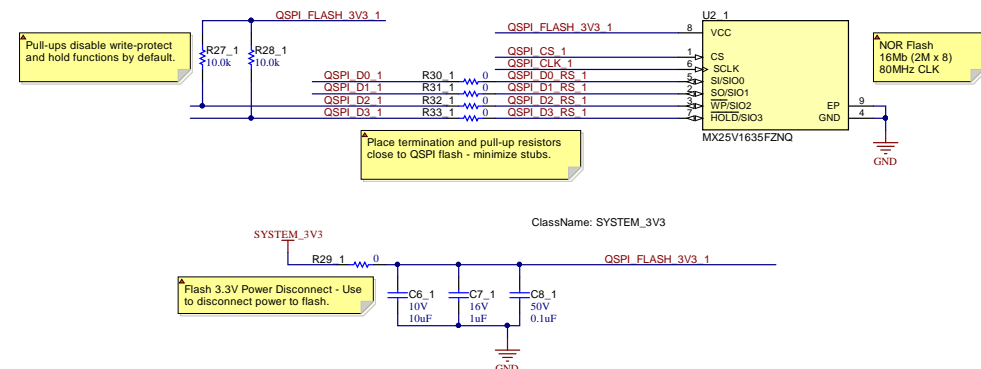


SOP[2:0] Pins

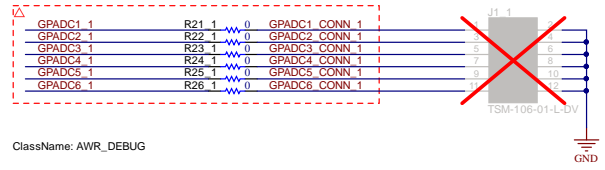
NOTE: SOP (start on power) Pins
 SOP[2]/PMIC_CLK_OUT
 SOP[1]/SYNC_OUT
 SOP[0]/TDO

SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
 SOP[2:0] = 0b001 -> SOP_MODE4 "Functional"
 SOP[2:0] = 0b101 -> SOP_MODE5 "QSPI Flashing"

NOR QSPI FLASH (For Development Purposes)

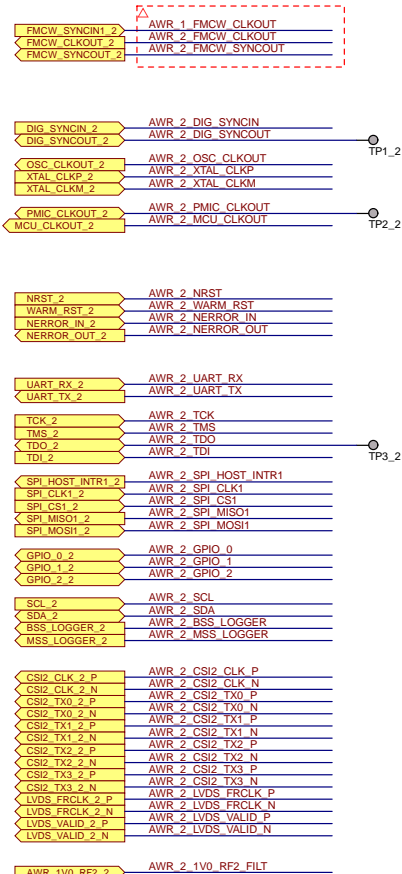


Debug Test Header (For Development Purposes)



AWR Radar SoC - Interfaces

References
<http://www.ti.com/product/AWR2243>



ClassName: AWR_20GHZ_LO

ClassName: AWR_SYNC

ClassName: AWR_CLOCK

ClassName: AWR_GENERAL

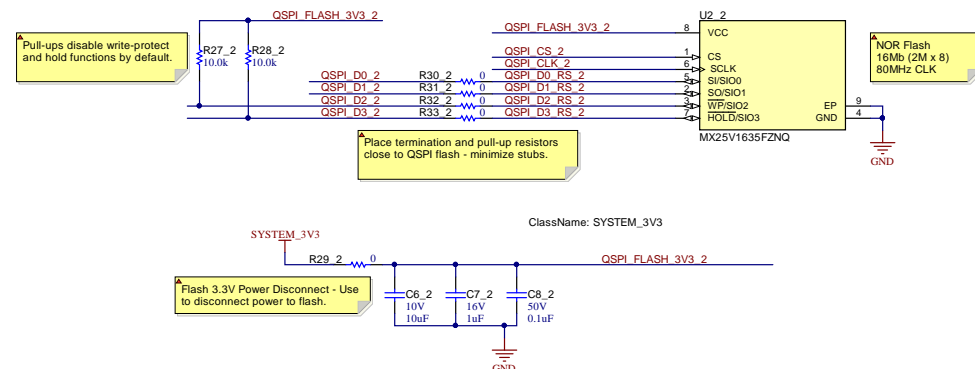
ClassName: AWR_GENERAL

SOP[2:0] Pins

NOTE: SOP (start on power) Pins
 SOP[2]/PMIC_CLK_OUT
 SOP[1]/SYNC_OUT
 SOP[0]/TDO

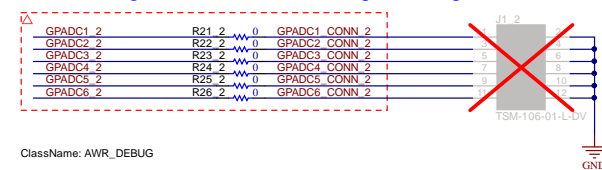
SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
 SOP[2:0] = 0b001 -> SOP_MODE4 "Functional"
 SOP[2:0] = 0b101 -> SOP_MODE5 "QSPI Flashing"

NOR QSPI FLASH (For Development Purposes)



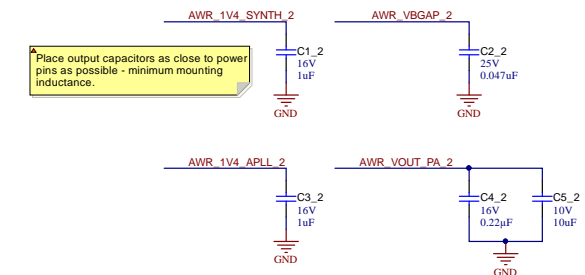
ClassName: SYSTEM_3V3

Debug Test Header (For Development Purposes)



ClassName: AWR_DEBUG

AWR LDO and Bandgap Output Capacitors



Place output capacitors as close to power pins as possible - minimum mounting inductance.

Place R188 as close as possible to VOUT_PA/RF2 pins

Note: AWR_1V0_RF2 optionally shorted to AWR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.

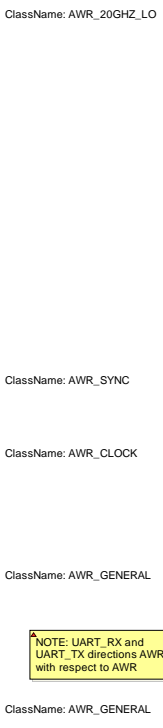
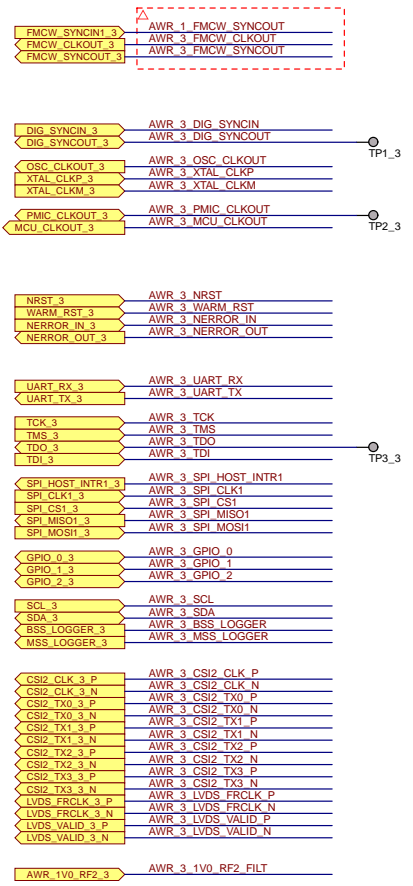
R188 installed - shorts AWR_VOUT_PA to AWR_1V0_RF2 (default)

R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

Place termination and pull-up resistors close to QSPI controller - minimize stubs.

AWR Radar SoC - Interfaces

References
<http://www.ti.com/product/AWR2243>

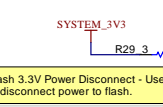
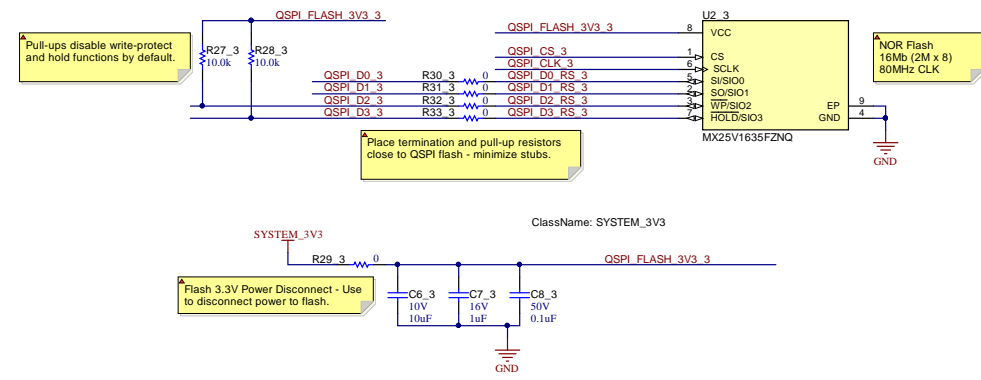


SOP[2:0] Pins

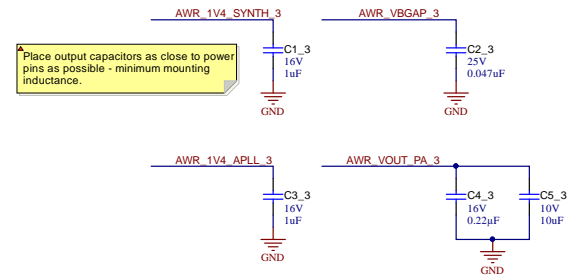
NOTE: SOP (start on power) Pins
 SOP[2]/PMIC_CLK_OUT
 SOP[1]/SYNC_OUT
 SOP[0]/TDO

SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
 SOP[2:0] = 0b001 -> SOP_MODE4 "Functional"
 SOP[2:0] = 0b101 -> SOP_MODE5 "QSPI Flashing"

NOR QSPI FLASH (For Development Purposes)



AWR LDO and Bandgap Output Capacitors



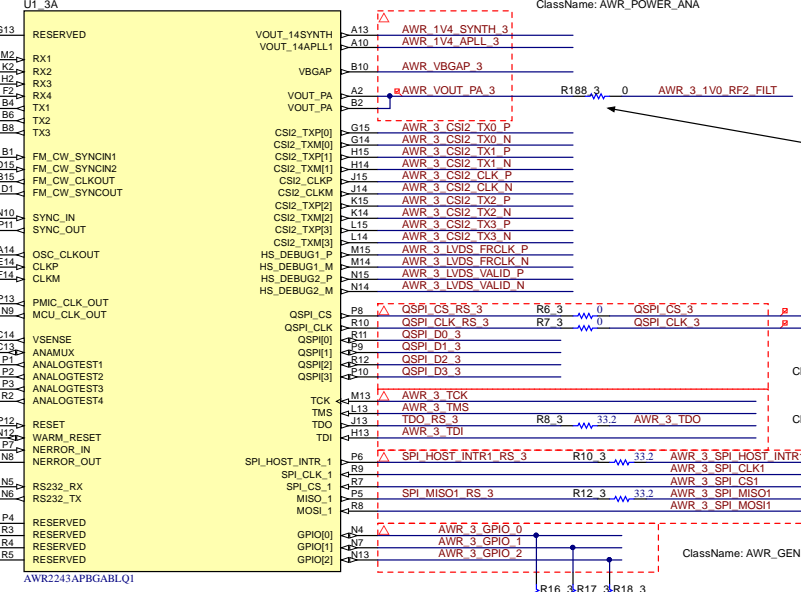
Place output capacitors as close to power pins as possible - minimum mounting inductance.

Place R188 as close as possible to VOUT_PA/RF2 pins

Note: AWR_1V0_RF2 optionally shorted to AWR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.
 R188 installed - shorts AWR_VOUT_PA to AWR_1V0_RF2 (default)
 R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

Place termination and pull-up resistors close to QSPI controller - minimize stubs.

AWR Interfaces



ClassName: AWR_POWER_ANA

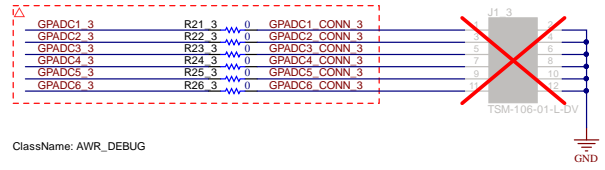
ClassName: AWR_QSPI

ClassName: AWR_JTAG

ClassName: AWR_GENERAL

ClassName: AWR_GENERAL

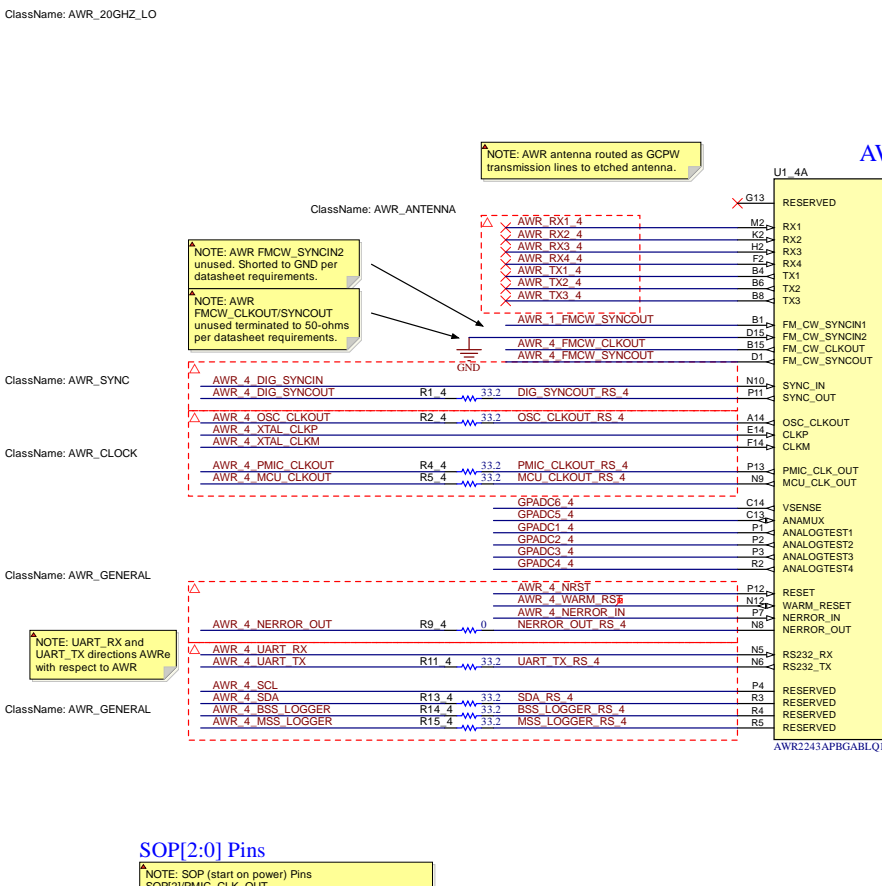
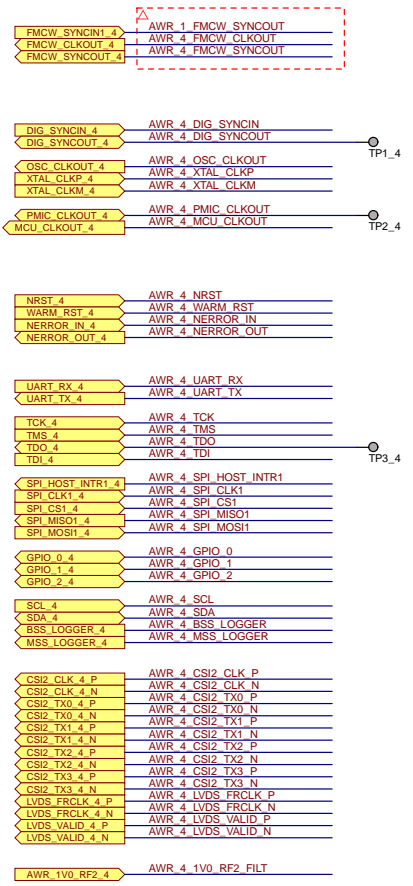
Debug Test Header (For Development Purposes)



ClassName: AWR_DEBUG

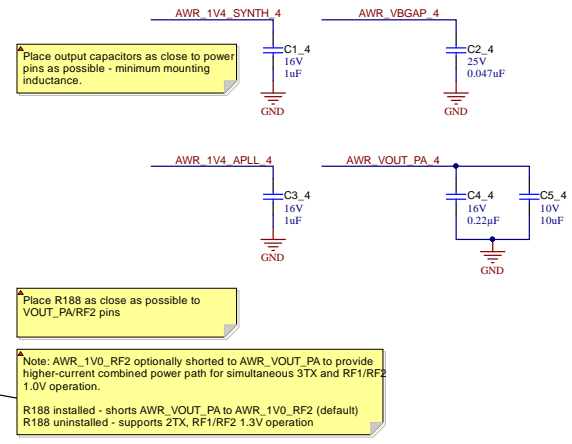
AWR Radar SoC - Interfaces

References
<http://www.ti.com/product/AWR2243>



SOP[2:0] Pins
 NOTE: SOP (start on power) Pins
 SOP[2]/PMIC_CLK_OUT
 SOP[1]/SYNC_OUT
 SOP[0]/TDO
 SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
 SOP[2:0] = 0b001 -> SOP_MODE4 "Functional"
 SOP[2:0] = 0b101 -> SOP_MODE5 "QSPI Flashing"

AWR LDO and Bandgap Output Capacitors



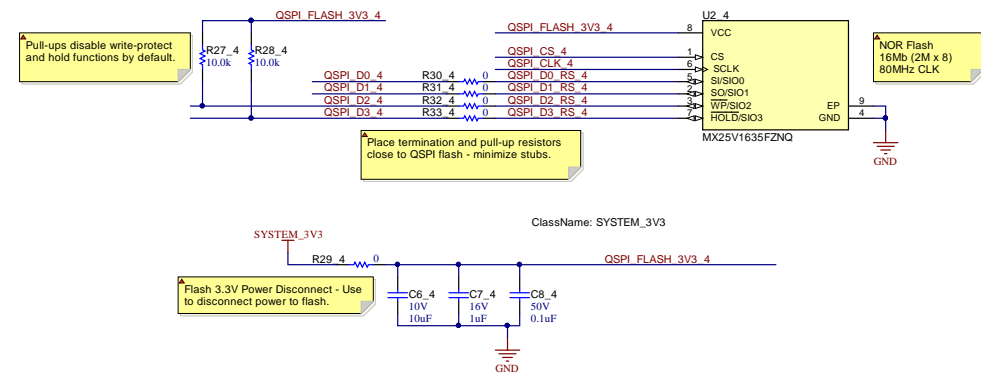
Place output capacitors as close to power pins as possible - minimum mounting inductance.

Place R188 as close as possible to VOUT_PA/RF2 pins

Note: AWR_1V0_RF2 optionally shorted to AWR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.
 R188 installed - shorts AWR_VOUT_PA to AWR_1V0_RF2 (default)
 R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

Place termination and pull-up resistors close to QSPI controller - minimize stubs.

NOR QSPI FLASH (For Development Purposes)

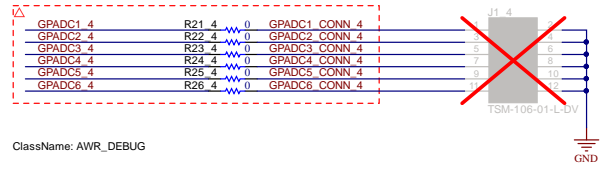


Pull-ups disable write-protect and hold functions by default.

Place termination and pull-up resistors close to QSPI flash - minimize stubs.

Flash 3.3V Power Disconnect - Use to disconnect power to flash.

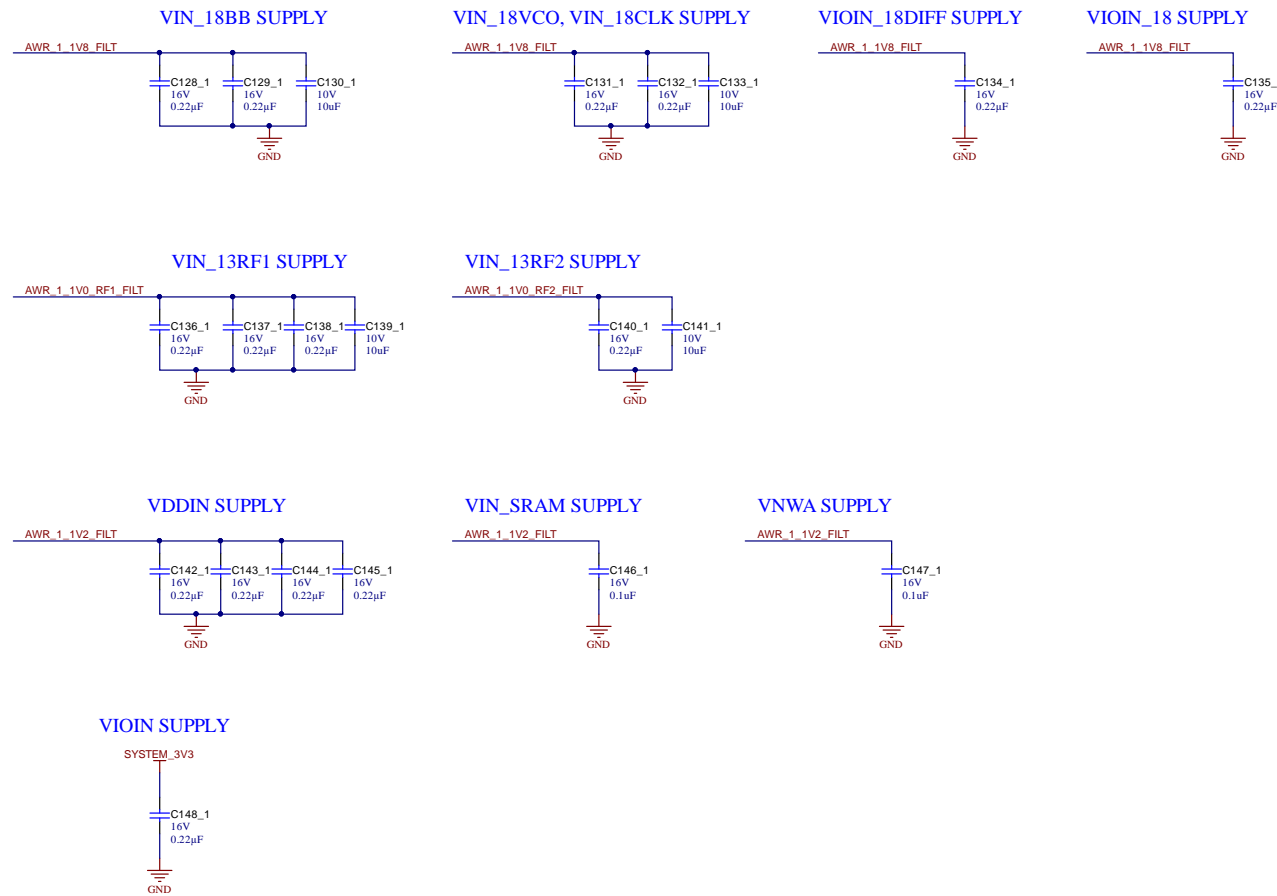
Debug Test Header (For Development Purposes)



ClassName: AWR_DEBUG

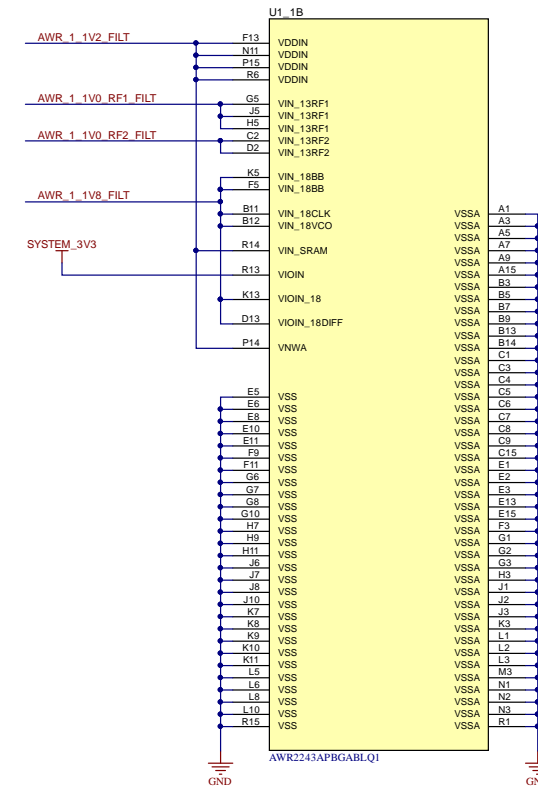
AWR Radar SoC - Power and Decoupling

AWR Power - BGA Decoupling



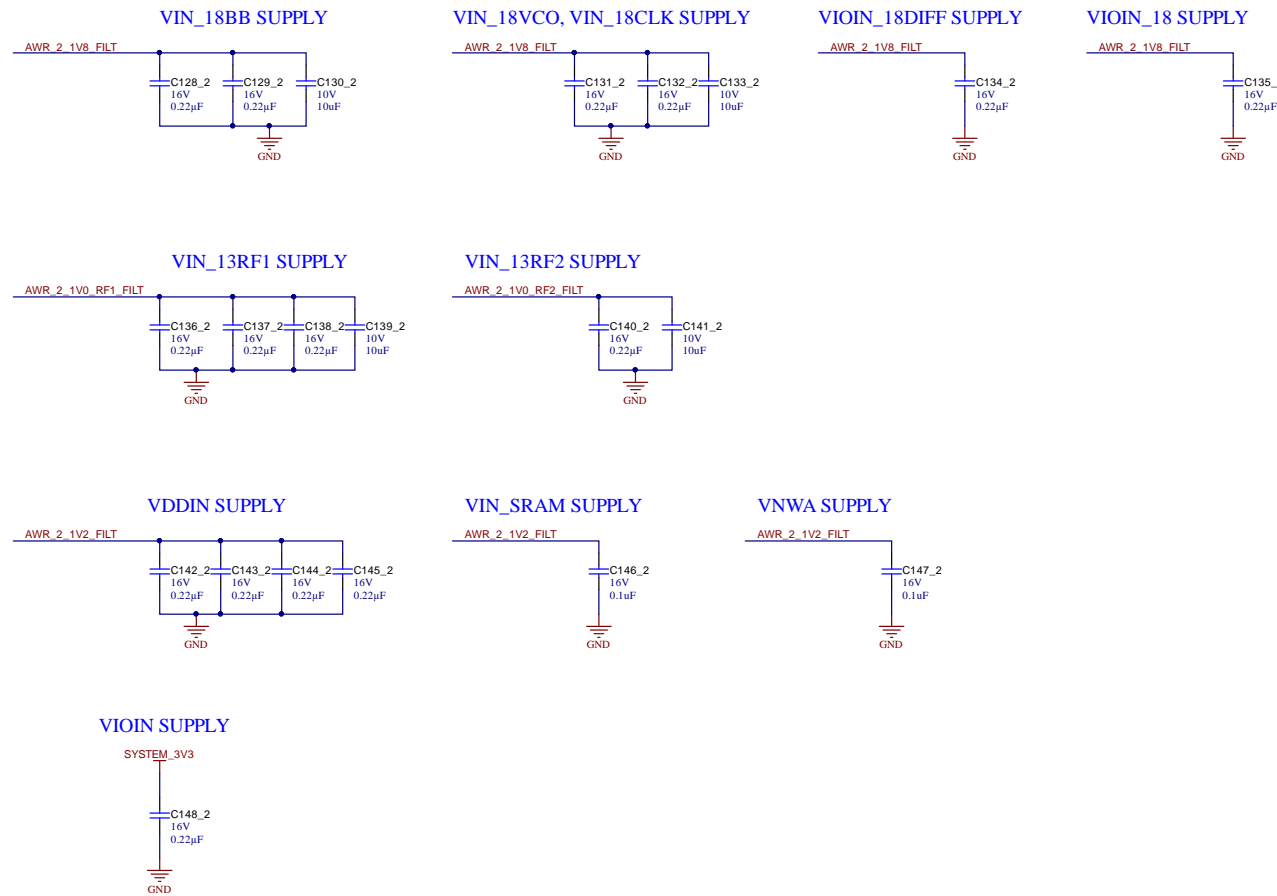
AWR_1V2_1	AWR_1_1V2_FILT
AWR_1V8_1	AWR_1_1V8_FILT
AWR_1V0_RF1_1	AWR_1_1V0_RF1_FILT
AWR_1V0_RF2_1	AWR_1_1V0_RF2_FILT

AWR Power



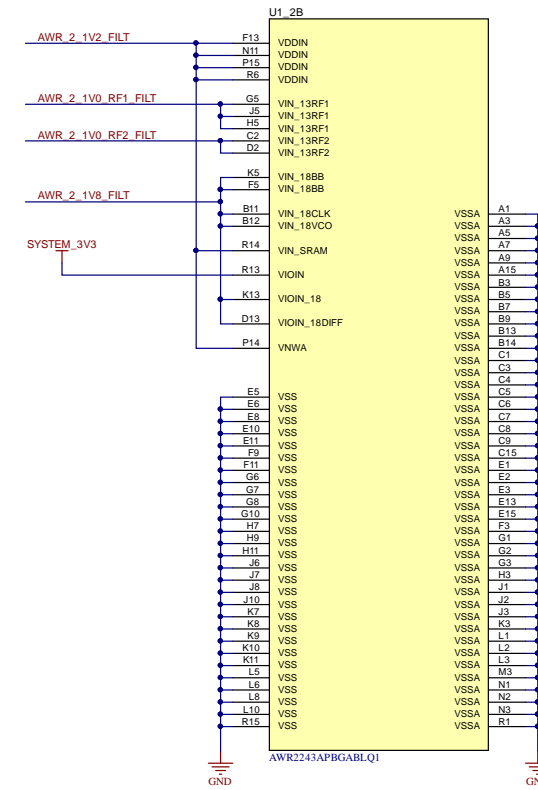
AWR Radar SoC - Power and Decoupling

AWR Power - BGA Decoupling



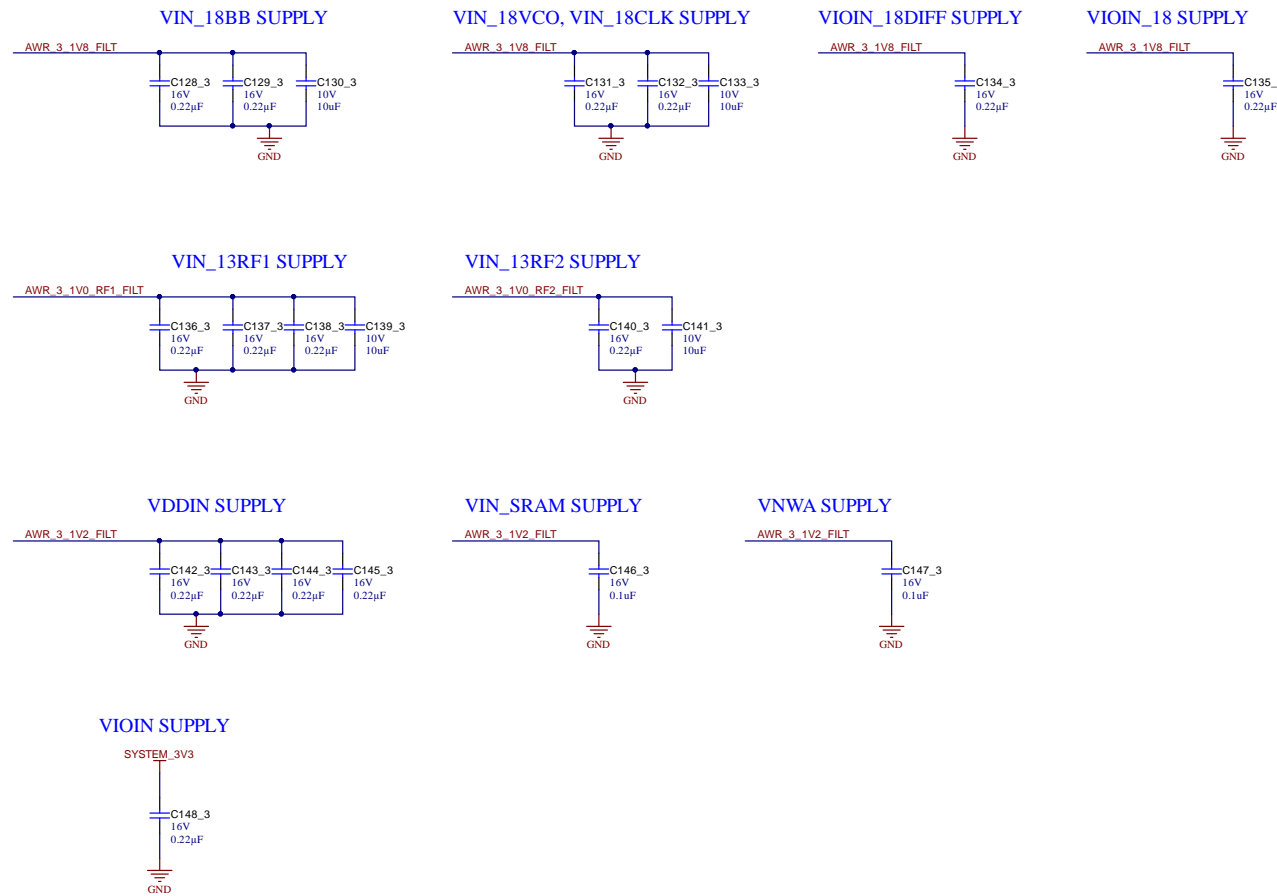
AWR_1V2_2	AWR_2_1V2_FILT
AWR_1V8_2	AWR_2_1V8_FILT
AWR_1V0_RF1_2	AWR_2_1V0_RF1_FILT
AWR_1V0_RF2_2	AWR_2_1V0_RF2_FILT

AWR Power



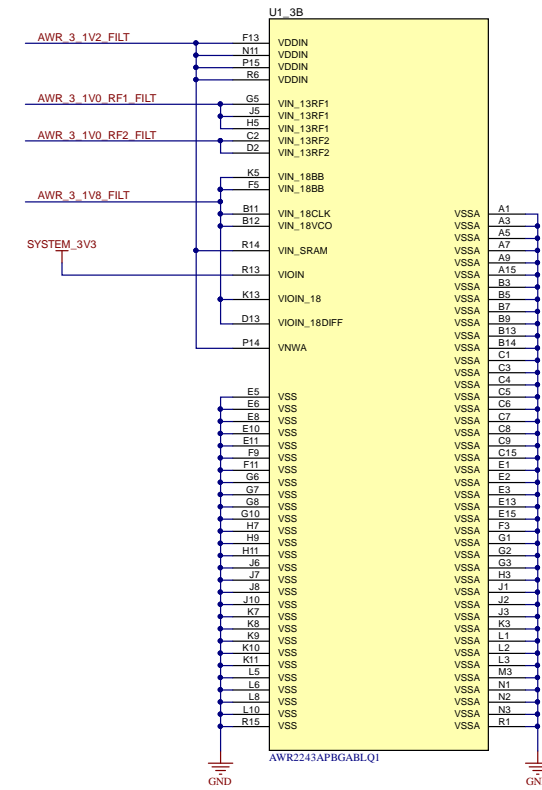
AWR Radar SoC - Power and Decoupling

AWR Power - BGA Decoupling



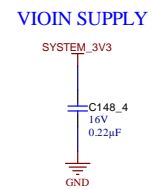
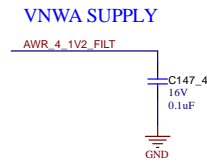
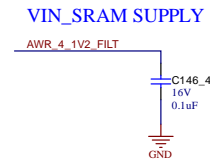
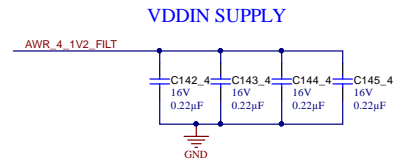
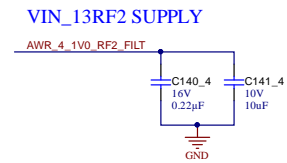
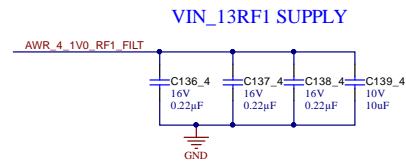
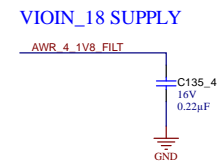
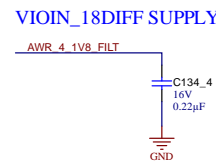
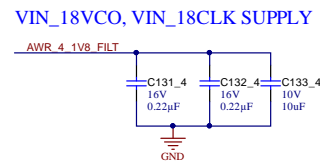
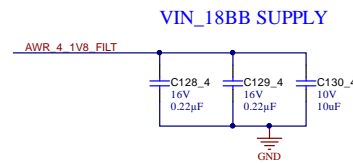
AWR_1V2_3	AWR_3_1V2_FILT
AWR_1V8_3	AWR_3_1V8_FILT
AWR_1V0_RF1_3	AWR_3_1V0_RF1_FILT
AWR_1V0_RF2_3	AWR_3_1V0_RF2_FILT

AWR Power



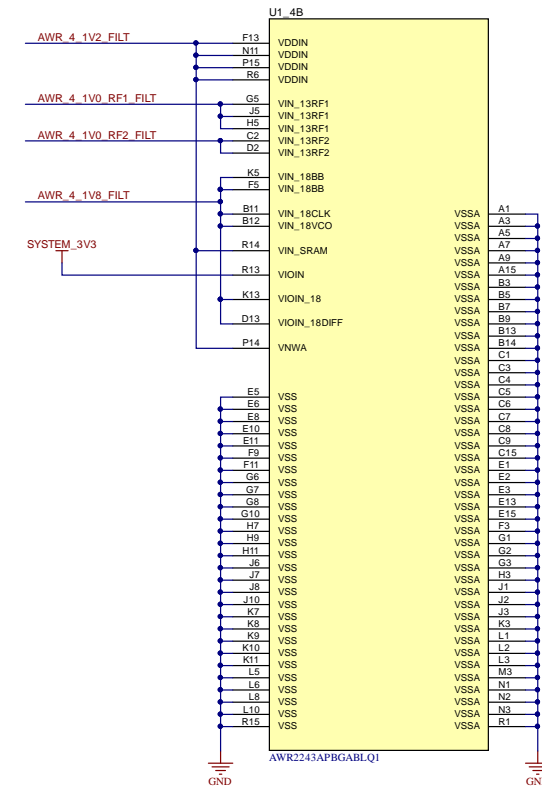
AWR Radar SoC - Power and Decoupling

AWR Power - BGA Decoupling



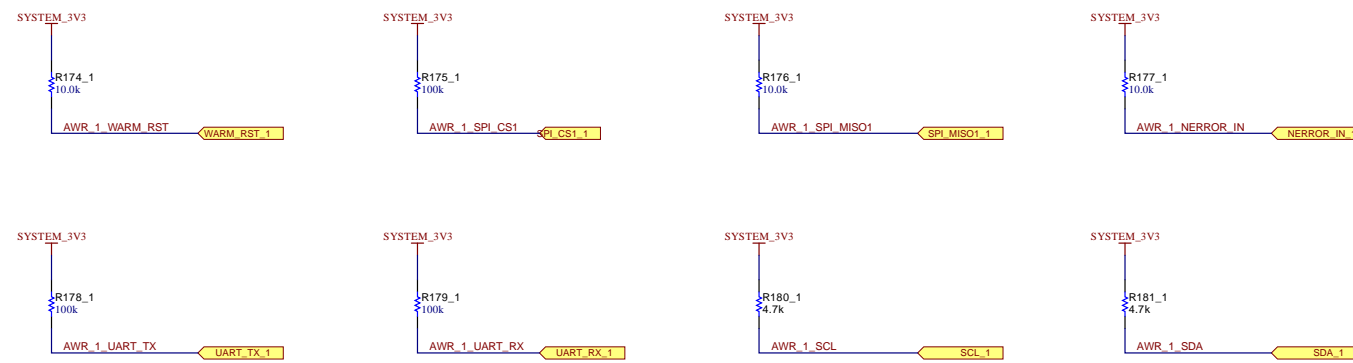
AWR_1V2_4	AWR_4_1V2_FILT
AWR_1V8_4	AWR_4_1V8_FILT
AWR_1V0_RF1_4	AWR_4_1V0_RF1_FILT
AWR_1V0_RF2_4	AWR_4_1V0_RF2_FILT

AWR Power

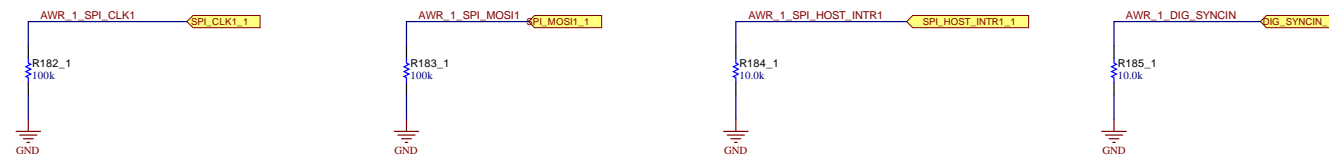


AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS

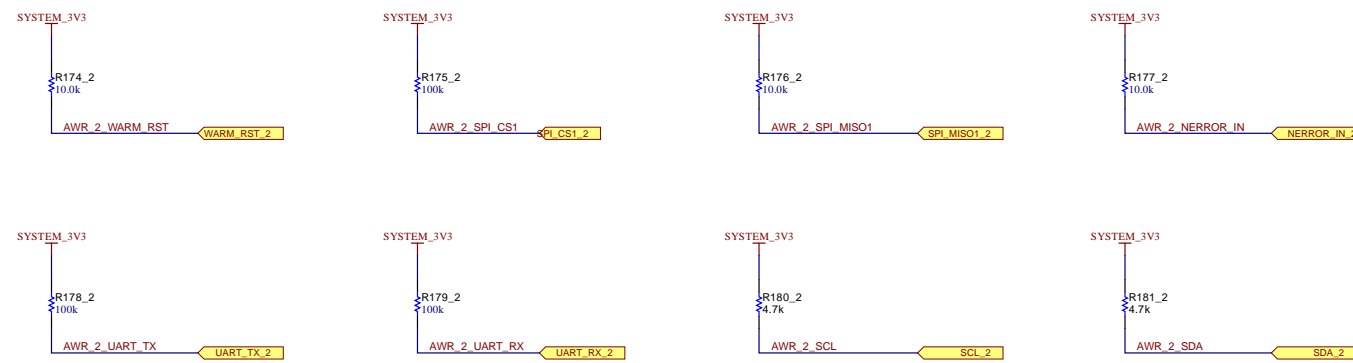


PULL DOWN OPTIONS

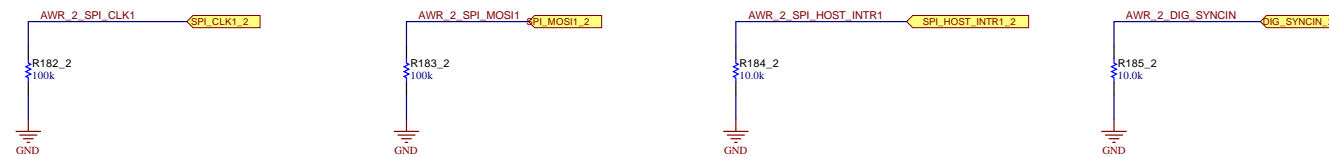


AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS

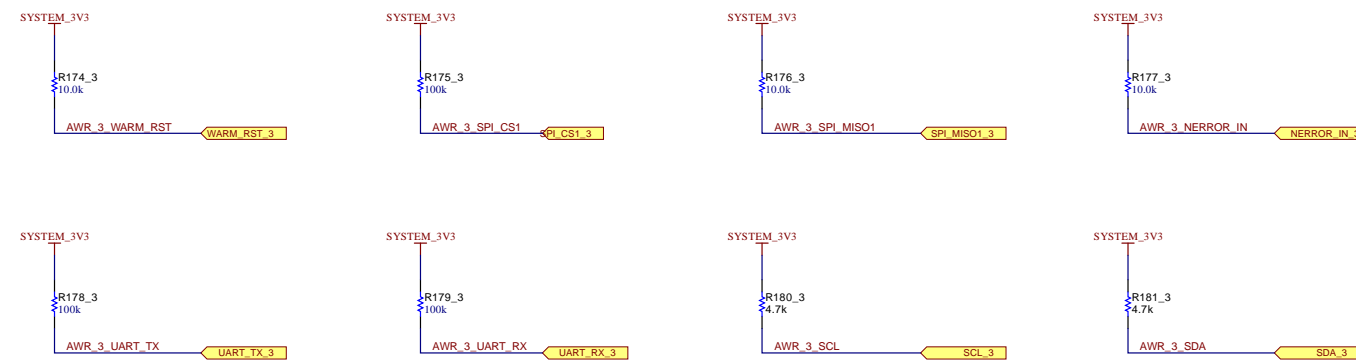


PULL DOWN OPTIONS

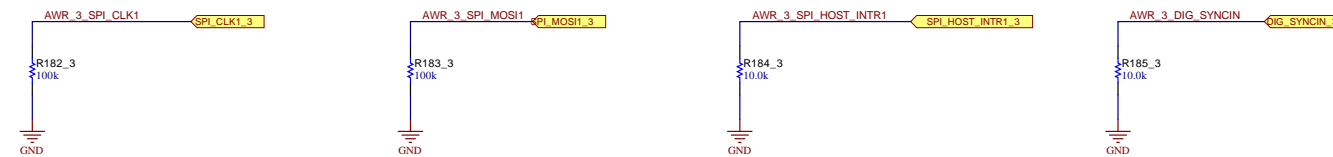


AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS

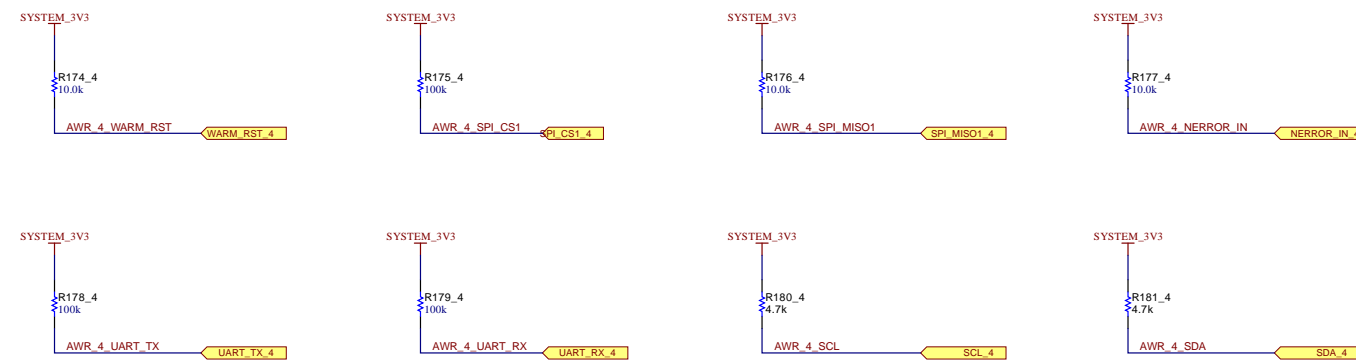


PULL DOWN OPTIONS

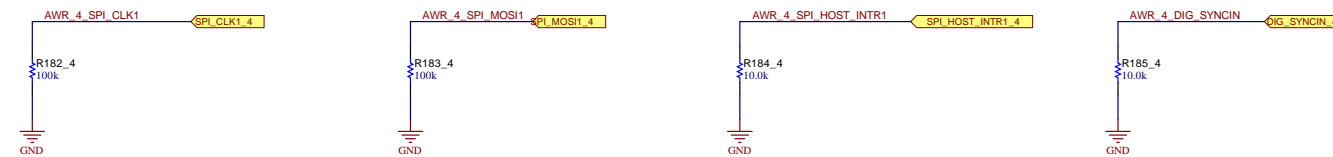


AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



PULL DOWN OPTIONS

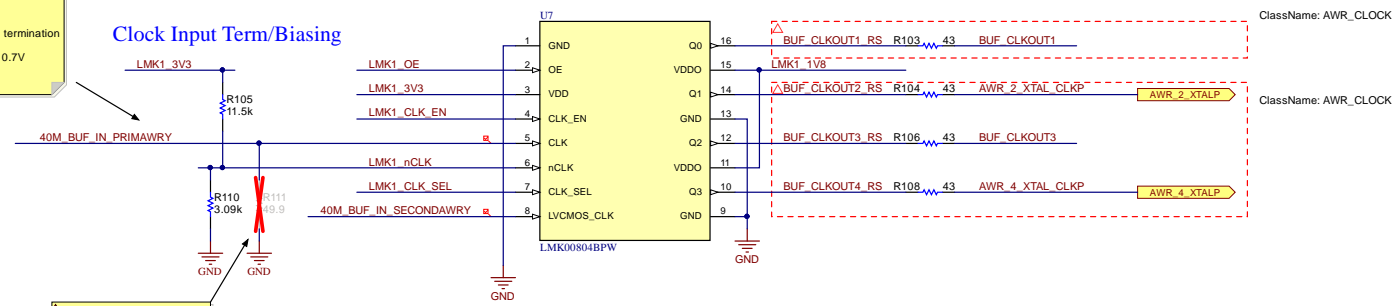


40 MHz Clock Generation and Distribution

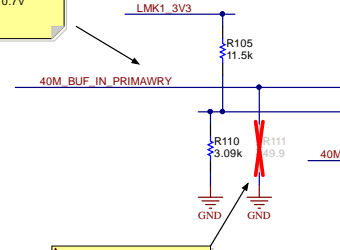
References

LMK00804BEVM User's Guide

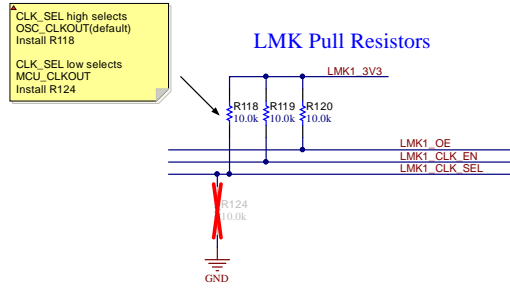
LMK00804B 40MHz Clock Distribution



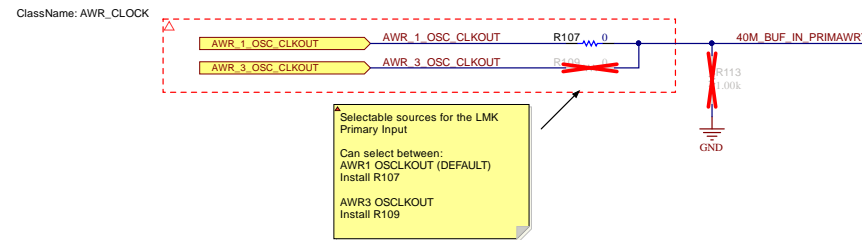
Clock Input Term/Biasing



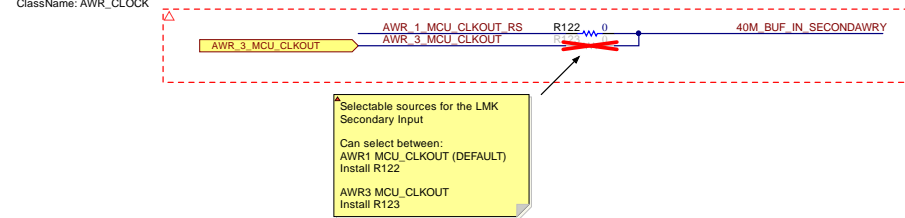
LMK Pull Resistors



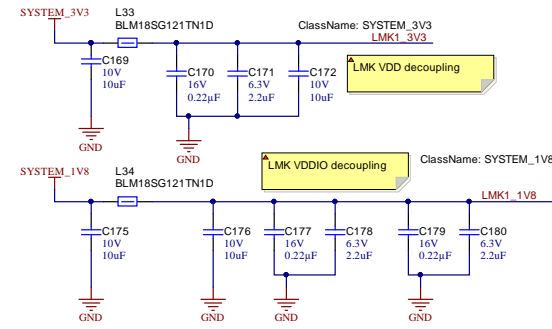
LMK Buffer - PrimAWry Input Select



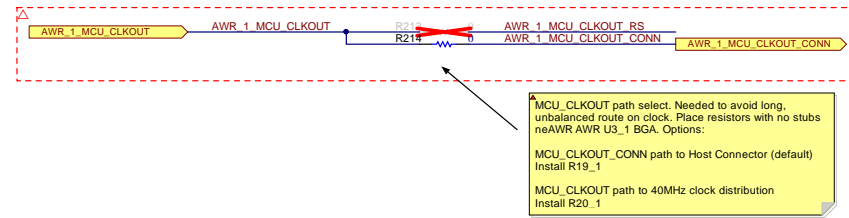
LMK Buffer - SecondAWry Input Select



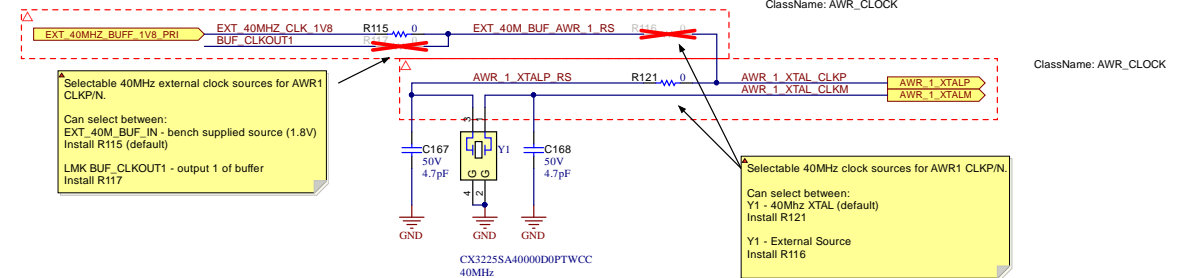
LMK Decoupling and Filtering



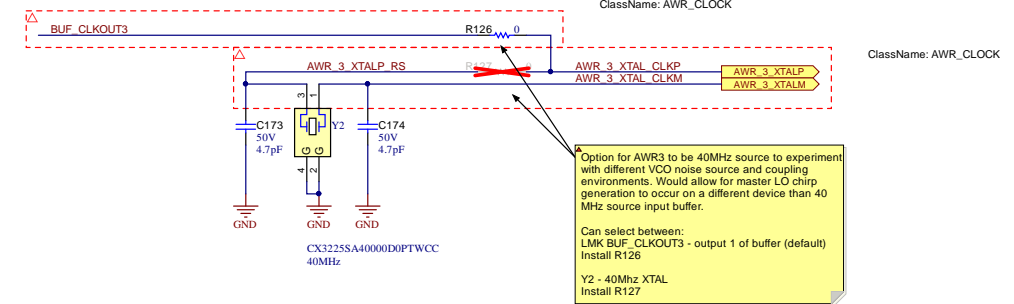
AWR_1 MCU Output Path Select



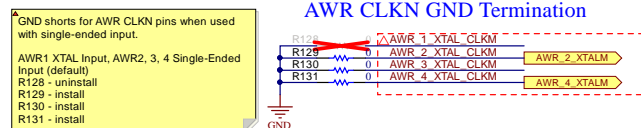
AWR_1 40 MHz Clock Source



AWR_3 40 MHz Clock Source



AWR CLKN GND Termination

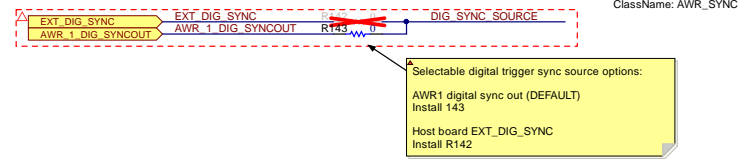


Digital Sync Trigger and 20GHz LO Distribution

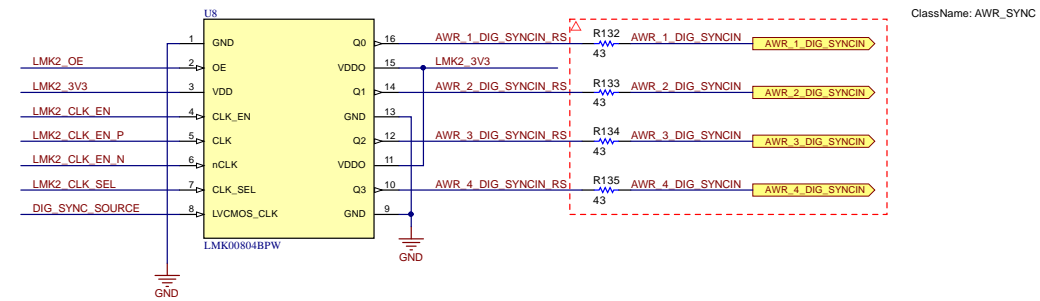
References

LMK00804BEVM User's Guide

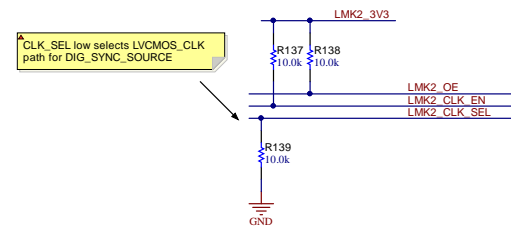
Digital Sync Source Select



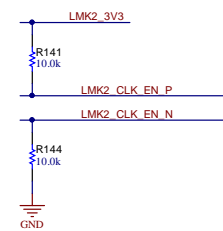
LMK00804B Digital Sync Distribution



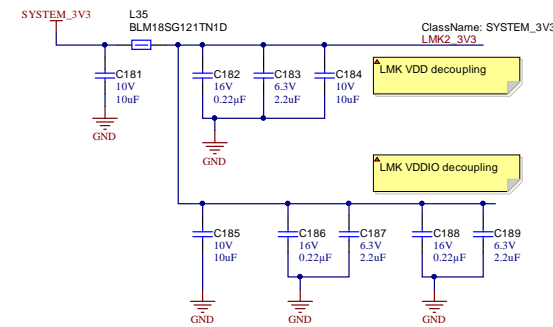
LMK Pull Resistors



LMK Unused Input

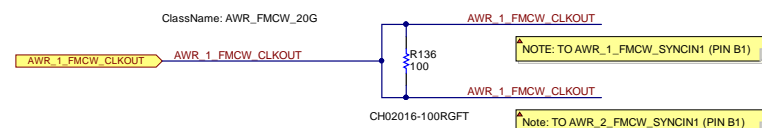


LMK Decoupling and Filtering

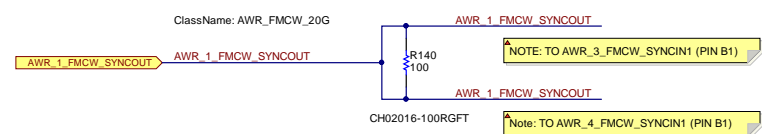


FMCW 20GHz LO SYNC

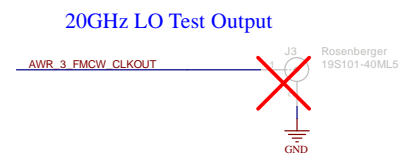
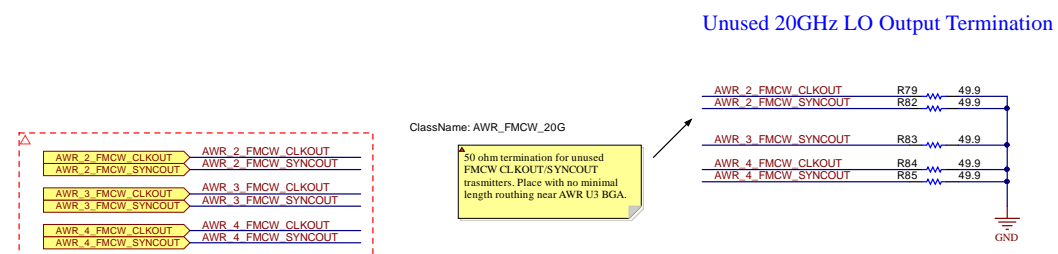
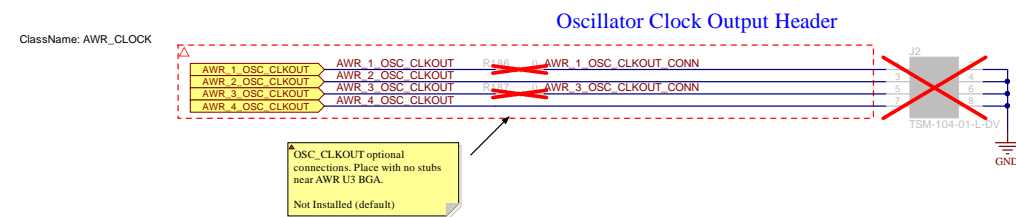
Wilkinson Power Divider #1



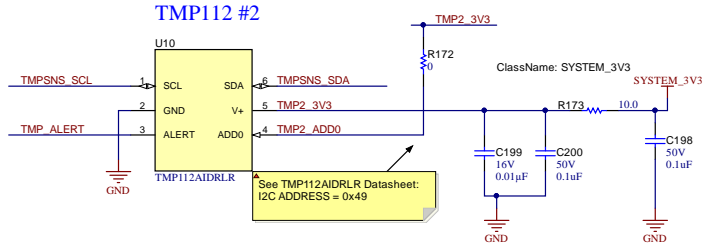
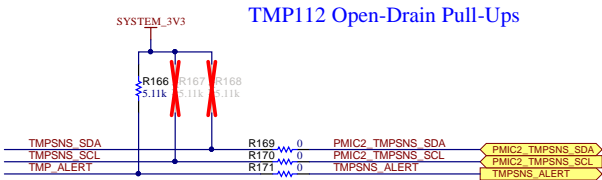
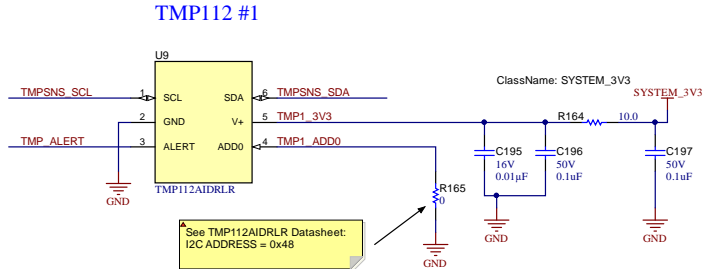
Wilkinson Power Divider #2



Test Headers, Connectors and Terminations

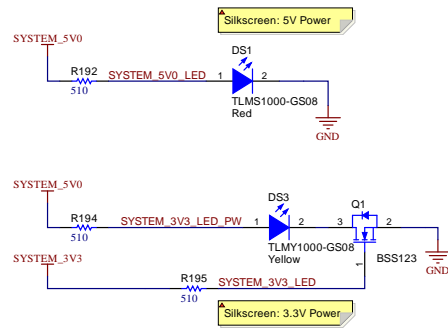


System Temperature Sensors

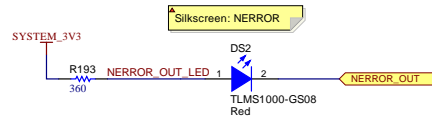


System Indicator LED

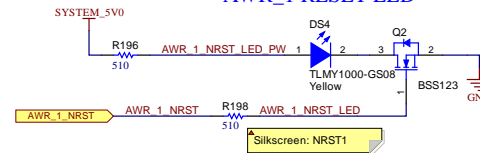
POWER LEDS



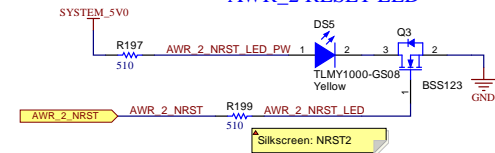
ERROR LEDS



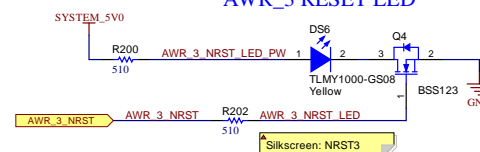
AWR_1 RESET LED



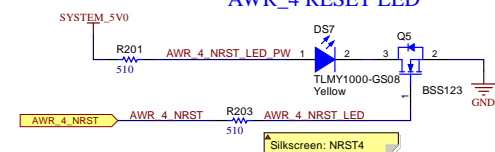
AWR_2 RESET LED



AWR_3 RESET LED



AWR_4 RESET LED



Hardware, Mounting Holes and Logos



PCB Number: PROC054
PCB Rev: E

PCB LOGO
Texas Instruments



PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

PCB LOGO
ESD Susceptible



ZZ1

Assembly Note

These assemblies AWR ESD sensitive, ESD precautions shall be observed.

ZZ2

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3

Assembly Note

These assemblies must comply with workmanship standAWRds IPC-A-610 Class 2, unless otherwise specified.

ZZ4

Assembly Note

R136/R140 require special attention due to no solder-mask RF construction. For any questions, please contact TI design team.

Orderable: MMW_CAS_RF_EVM	Designed for: Public Release	Mod. Date: 8/14/2020
TID #: N/A	Project Title: MMW_CAS_RF-EVM	
Number: PROC054	Rev: E	Sheet Title: HAWR9wAWRe
Rev: Not in version control	Assembly VAWRiant:	Sheet: 18 of 19
Drawn By: a0271760	File: PROC054E_EVM_Hardware_SchDoc	Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave	http://www.ti.com

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Cascade Radar RF Board - Revision History

Revision History			
Rev	Date	Released By	Notes
1	2018/07/09	Randy Rosales rosales.r@ti.com	Initial release for layout cleanup and internal review.
2	2018/07/17	Randy Rosales rosales.r@ti.com	<p>Updating based on 2018/07/09 comments.</p> <p>Combined PMIC_BUCK_EN and PMIC_NRST</p> <p>Combined PMIC1_PGOOD and PMIC2_PGOOD into single SYSTEM_PGOOD</p> <p>Updating NRST generation scheme from LP87524P PMIC</p> <p>Created sepAWRate AWR_X reset generation paths</p> <p>Combined GPIO2 and PGOOD into PGOOD net</p> <p>Removing leftover resistor selection options from the previous LDO and PMIC power paths.</p> <p>Removing first level LC filtering options from the previous LDO and PMIC power paths.</p> <p>Removed: L3, L6, L19, L22</p> <p>Removed: C21, C29, C78, C86</p> <p>Removed: C21, C29, C78, C86</p> <p>This also removed a few power net segments which will now be fed directly from PMIC output</p> <p>Combined AWR_1_1V8_FILTER and AWR_4_1V8_FILTER into AWR_14_1V8_FILTER</p> <p>Combined AWR_2_1V8_FILTER and AWR_3_1V8_FILTER into AWR_23_1V8_FILTER</p> <p>Changing XWR LC filter to use TDK NLCV32T-R10M-EFRD identified by power team analysis</p> <p>PMIC1_AWR_14_1V8 now directly feeds into SYSTEM_1V8 supply - there was no reason to run this through XWR 1.8V LC filter.</p> <p>Added SYSTEM_5V0 to 3.3V resistor divider for LP87524 PMIC pull-up resistors</p> <p>Updated U2 to the Macronix MX25V1635FZQ0 - aligning with other XWR EVM kits</p> <p>Removed R125 - Optional resistor remaining from previously removed option for alternative XTAL input</p> <p>Changed NERROR_OUT LED bias to SYSTEM_3V3</p> <p>Updated coversheet block diagram</p> <p>Updated power distribution block diagram</p>
2	2018/07/17	Randy Rosales rosales.r@ti.com	Added variant information for do not populate stuffing options.
3	2018/07/18	Randy Rosales rosales.r@ti.com	<p>Removed 50 ohm terminations to ground at the J2 OSCCLK_OUT test header</p> <p>Removed test headers on PMIC output rails</p> <p>Added zero-ohm resistor between PMIC GPIO3 and PGOOD</p> <p>Replaced all note, class and netname instances of AWR with XWR for industrial/automotive alignment of schematics</p> <p>Replaced all series termination on LMK00804B output with 43 ohm resistors per LMK00804B datasheet</p> <p>Replaced XWR reset generation circuit with discrete AND gate</p> <p>Required for achieving clean reset of XWR devices across all device mAWRgins</p> <p>Netname error on XWR SPI interface - MISO netname change</p> <p>R112 and EXT_40MHZ_CLK_1V8 removed - this was an alternative clock path that is no longer supported</p> <p>Eliminated RF1/2 channel naming error in PROC054_System_Power.SchDoc and PROC054_System_Top.SchDoc</p>
4	2018/07/21	Randy Rosales rosales.r@ti.com	Changed R54 to pull-up resistor. LP87524P GPIO2 and GPIO3 both configured as open-drain output.
5	2018/07/21	Randy Rosales rosales.r@ti.com	<p>Added 10kohm pull-up to LP87524P GPIO3 - required after change separating out GPIO3 and PGOOD nets</p> <p>Aligned PMIC1 and PMIC2 RF1 and RF2 LC filter components with 1.2V and 1.8V filter</p> <p>Previous RF1 and RF2 LC values were still not merged from removal of LDO option separation of RF1 and RF2 supplies</p>
6	2018/07/28	Randy Rosales rosales.r@ti.com	<p>Changing all layout critical resistors and capacitors to small-outline version in Altium Vault library</p> <p>Required to allow Tesselto to implement original decoupling and series resistor layout near the AWR BGA</p> <p>Will allow for more compact routing throughout the design as well</p> <p>Changed R136, R140 FMCW LO power divider resistor to RF resistor CH02016-100RJFT</p> <p>Changed U3 and U4 PMIC to reference proper P-version in Altium vault.</p> <p>Adding zero-ohm resistors to AWR_1/2/3/4 I2C interfaces, optionally shorting those interfaces to the PMIC1_2C</p> <p>Changed NERROR_OUT LED to sourced from shorted NERROR_OUT</p> <p>Originally being fed AWR_1_ERROR_OUT</p>
7	2018/08/08	Randy Rosales rosales.r@ti.com	<p>Added R188 which shorts AWR_VOUT_PA to AWR_1V0_RF2 supply nets.</p> <p>Recommended for supporting increased current into the RF2 supplies in 1.0V mode supporting simultaneous 3 TX operation</p>
8	2018/08/09	Randy Rosales rosales.r@ti.com	<p>Added burn danger logo</p> <p>Added ESD danger logo</p> <p>Consolidated FMCW 20G LO, digital sync and clock net classes. Created the following net classes:</p> <ul style="list-style-type: none"> AWR_FMCW_20G AWR_CLOCK AWR_SYNC <p>Removed extraneous MCU_CLKOUT_CONN path from XWR2, XWR3 and XWR4</p> <p>Consolidated XWR1 MCU_CLKOUT path output options on PROC054_40MHZ_CLK1 schematic sheet</p> <p>Renamed schematic PROC054_40MHZ_FMCW_SYNC to PROC054_FMCW_SYNC</p> <p>Aligned antennas with AWR prefix naming convention</p> <p>Added all nets on 40MHZ_CLOCK_1 schematic sheet to netclass XWR_CLOCK</p>
9	2018/08/10	Randy Rosales rosales.r@ti.com	<p>Added additional nets to the AWR_SYNC net class</p> <p>Added additional nets to the AWR_FMCW_20G net class</p> <p>Replaced J3 with correct Rosenberger 19S101 part from TI Altium Vault.</p>
10	2018/08/16	Randy Rosales rosales.r@ti.com	Added additional R19 and R20 0-ohm resistors to create optional feedback path for bench supply connector P3
11	2020/01/16	Randy Rosales rosales.r@ti.com	<p>Revision D updates</p> <p>Changing primary IC (U1_1, U1_2, U1_3 and U1_4) to AWR2243P</p> <p>Cleaning up net names, ports, net classes, and notes to reference AWR vs. AWR12 specifically</p>
12	2020/08/13	Randy Rosales rosales.r@ti.com	<p>Revision E updates</p> <p>Changing primary IC (U1_1, U1_2, U1_3 and U1_4) to AWR2243P ES1.1, AWR2243APBGABLQ1</p> <p>Changing AWR VBGAP capacitor (C1_1, C1_2, C1_3 and C1_4) to 47nF capacitor GRM155R71E473KA88D</p> <p>Changing PMIC digital input voltage divider resistors (R34, R59) to from 1.0ohm to 1.0kohm resistors</p> <p>This matches initial design intent</p> <p>Simplified BOM by removing duplicate 0402 0-ohm resistors models on optional signal paths</p> <p>Cleaned up top layer soldermask near edges of RF regions</p> <p>Cleaning up various note spelling errors</p>

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