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TI Precision Designs: Verified Design

Hardware-Compensated Ratiometric 3-Wire RTD System, 0°C – 100°C, 0.005°C Error

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Circuit Description

This ratiometric temperature acquisition system accurately measures temperature over a range of 0°C – 100°C. The design uses a resistance temperature detector (RTD) in a 3-wire configuration to minimize the errors introduced by the lead resistances of a remotely located RTD. A 24-bit delta-sigma (ΔΣ) analog-to-digital converter (ADC) features two integrated precision current sources that excite the 3-wire RTD creating a differential voltage across the RTD that is then converted into a digital output code. The digital output can then be translated into a final temperature result.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
ADS1247	Product Folder
TPS7A4901	Product Folder

TI E2E™ Community

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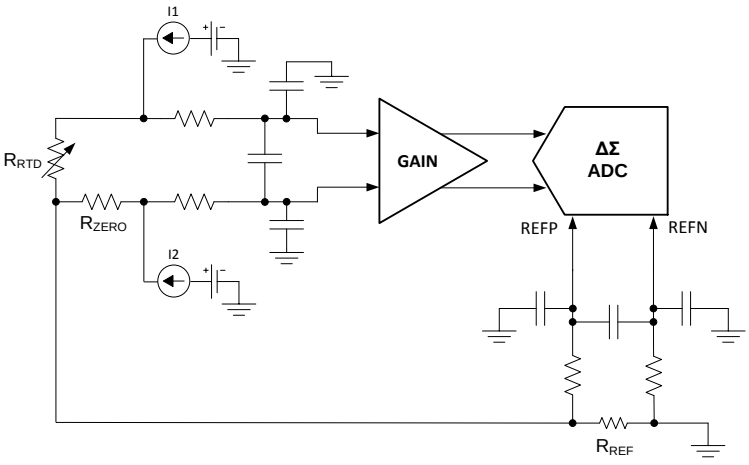

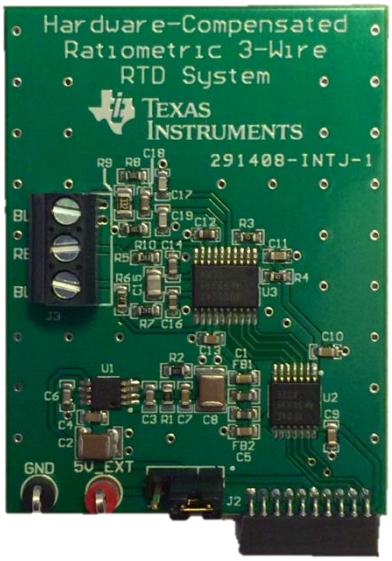

1 Design Summary

The design requirements are as follows:

- RTD Configuration: 3-Wire
- Temperature Range: 0°C – 100°C
- Output: 0.005 °C accurate temperature results
- System Supply Voltage: 4.3 V – 5.5 V
- Generated Supplies:
  - AVDD = 3.3 V
  - DVDD = 3.3 V
- ADC Reference Voltage: 1.65 V

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals and Measured Performance

	Goal	Measured
Unadjusted Precision Resistance Measurement Accuracy (Ω)	±0.01	0.006
Calibrated Precision Resistance Measurement Accuracy (Ω)	±0.002	±0.0012
Calibrated Temperature Measurement Accuracy (°C)	±0.005	±0.004

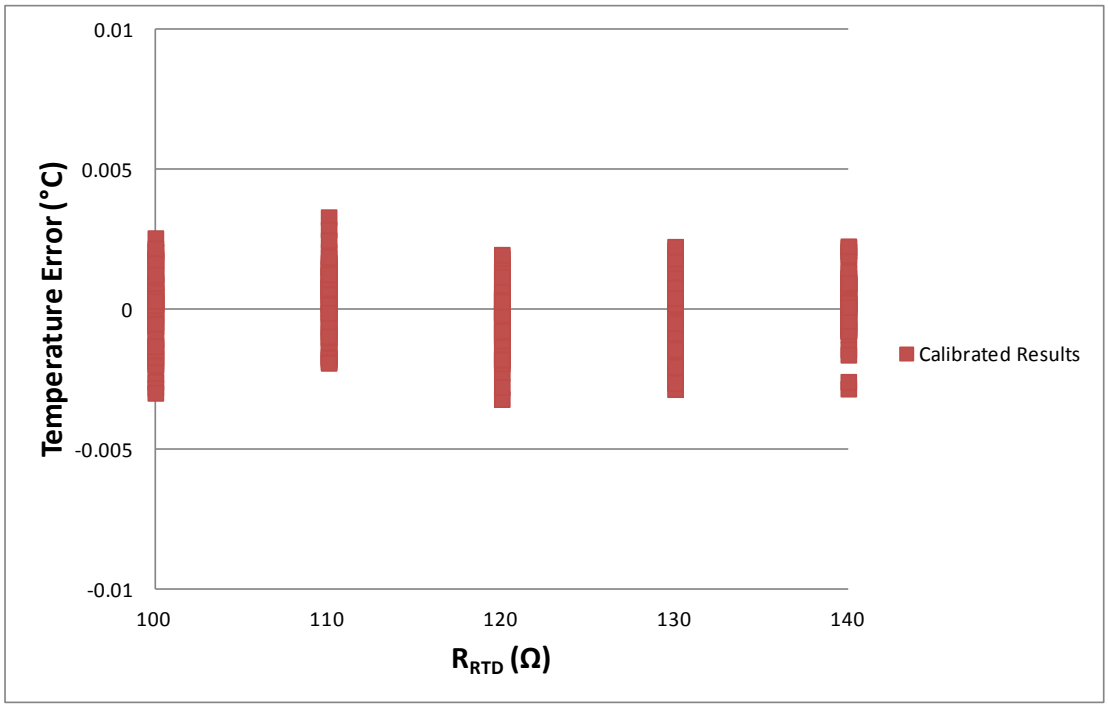

Figure 1. Measured Temperature Accuracy with Resistive Input Representing 0°C – 100°C

2 Theory of Operation

2.1 Resistance Temperature Detector (RTD) Overview

An RTD is a sensing element made of a metal with a predictable resistance characteristics over temperature. The temperature of an RTD can therefore be calculated by measuring the resistance. RTD sensors offer wide temperature ranges, good linearity, and excellent long term stability and repeatability, making them suitable for many precision applications.

The relationship between resistance and temperature of an RTD is defined by the Callendar-Van Dusen (CVD) equations which can be found in Appendix A.3.

Compared to a thermocouple, the main disadvantages of RTD sensors are their cost and required excitation source. The small change in resistance of an RTD over temperature also places demands on the accuracy of the acquisition circuit requiring a precision signal chain. Thermistors have larger changes in resistance over temperature but are much less linear reducing their effectiveness at measuring wider temperature ranges.

2.2 RTD Resistance Measurement

Most RTD applications use a current source as excitation for the RTD element. By driving a known current through the RTD, a voltage potential is developed that is proportional to the resistance of the RTD and the excitation current. This voltage potential is amplified and then fed to the inputs of an ADC, which converts the voltage into a digital output code that can be used to calculate the RTD resistance.

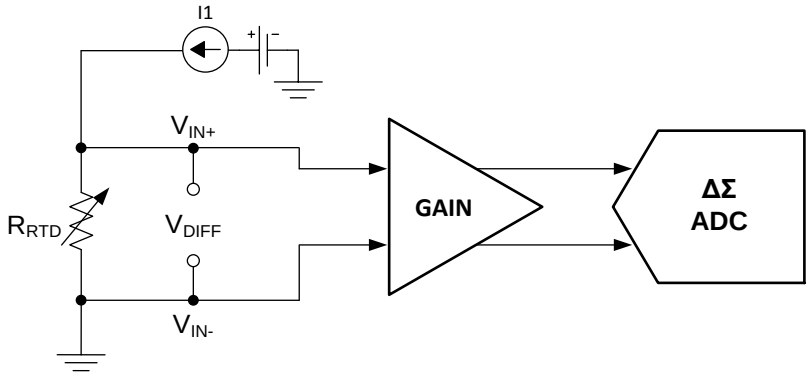

Figure 2. Simplified RTD Application

2.2.1 Ratiometric Measurements

An ADC requires a reference voltage to convert the input voltage into a digital output. In most applications, this reference is fixed and either internally generated or externally applied to the ADC. This 3-wire RTD system uses what is known as a ratiometric configuration to create the reference voltage, increasing system accuracy.

In a ratiometric configuration, the excitation current that flows through the RTD returns to ground through a low-side reference resistor, R_{REF}, as shown in Figure 3. The voltage potential developed across R_{REF}, V_{REF}, is fed into the positive and negative reference pins (REFP and REFN) of the ADC. The V_{REF} voltage sets both the input common-mode voltage as well as the differential input voltage range. Setting V_{REF} to mid-supply results in optimal input circuit performance as well as the largest acceptable differential input voltage range. Therefore, the R_{REF} resistor and excitation current will be sized to produce roughly a 1.65 V external reference for this +3.3 V system. R_{REF} should be selected with low tolerance and low drift since error in the reference voltage will directly translate into error in the conversion result.

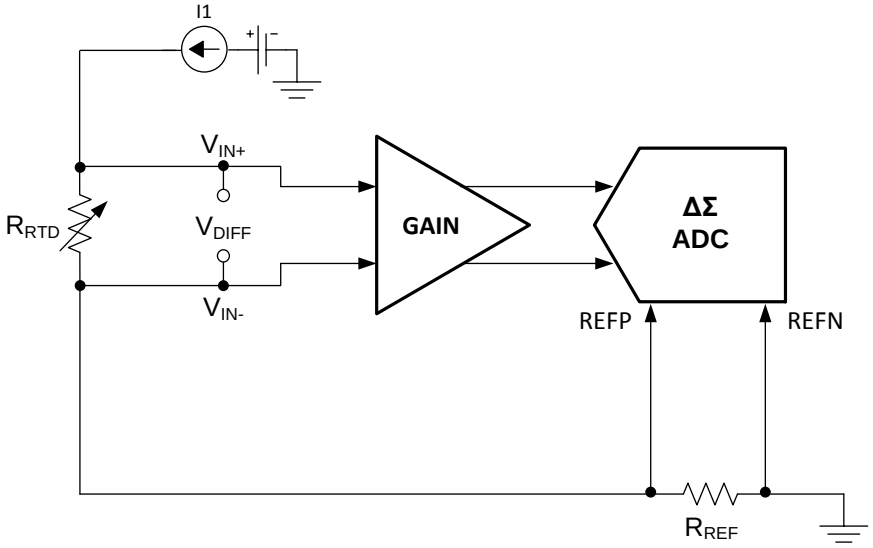

Figure 3. Ratiometric RTD Measurement

The voltage drop across the RTD and R_{REF} resistors is produced by the same excitation source in a ratiometric configuration. Therefore, any changes in the excitation source are reflected in both the RTD differential voltage and the reference voltage. Since the ADC output code is a relationship between the input voltage and the reference voltage, the effects of noise, drift, and accuracy of the current source cancel without affecting the final result. The ratiometric configuration also helps reduce the effects of external noise that appears common to both the inputs and the reference because it should cancel as well.

2.2.2 *Current Sources*

Two precision current sources are typically used in 3-wire RTD applications; refer to Reference 2 for more information on other RTD configurations. The magnitude of the current sources directly affects the magnitude of the RTD voltage. While maximizing the magnitude of the excitation current would seem desirable, higher excitation currents create higher power-dissipation leading to self-heating of the RTD. Errors due to self-heating cannot be easily corrected and should be kept lower than 25% of the total error budget. Keeping the excitation current small will also minimize the heat produced in other signal path components, reducing drift and other additional measurement errors. The typical range of RTD self-heating coefficients is 2.5mW/°C for small elements to 65mW/°C for larger elements. Figure 4 displays the self-heating error in degrees Celcius versus applied excitation current for the range of RTD self-heating coefficients.

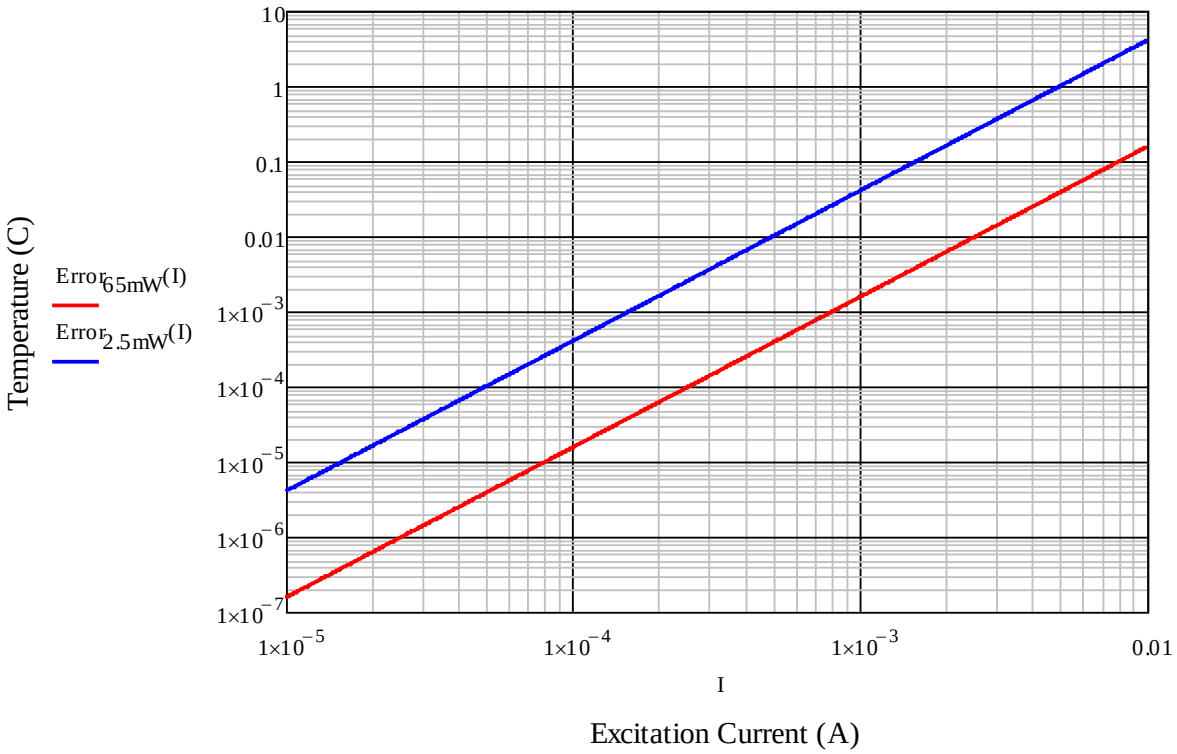

Figure 4: RTD Self-Heating vs. Excitation Current for Different RTD Types

The effects of self-heating on measurement accuracy are also based on the placement of the RTD in the application. An RTD placed in a moving fluid medium will not self-heat because the moving fluid will keep the RTD at the temperature of the fluid. However, in open-air temperature measurements, or other applications where the RTD is surrounded by an insulator, the RTD will self-heat and cause errors.

2.2.3 *Amplification Stage*

The full-scale input range of an ADC is bounded by the reference voltage, V_{REF}. By choosing a smaller value for the excitation current, reducing self-heating, the RTD produces a small change in voltage over the span of the temperature measurement which will not use the full ADC input range. Therefore, a gain stage is required to amplify the RTD voltage to a level that utilizes more of the full-scale ADC input range and maximizes the measurement resolution.

2.2.4 *Hardware Compensated 3-Wire RTD Measurements*

In a hardware compensated 3-wire RTD system, a hardware compensation resistor, R_{ZERO}, is included in the circuit as shown in Figure 5. R_{ZERO} is placed in series with the negative ADC input with the second current source, I_2, flowing through it. The voltage drop across R_{ZERO} subtracts from the voltage drop across the RTD, creating a bipolar voltage input to the PGA that is centered around 0 V. The bipolar voltage allows the system to make use of a larger gain stage, increasing the effective resolution. The value of R_{ZERO} is chosen to equal the resistance of the RTD at the mid-scale temperature value so that the input to the gain stage will swing equally in both the positive and negative directions. A hardware compensated 3-wire RTD system still benefits from RTD lead resistance cancellation as shown in Appendix A.4.

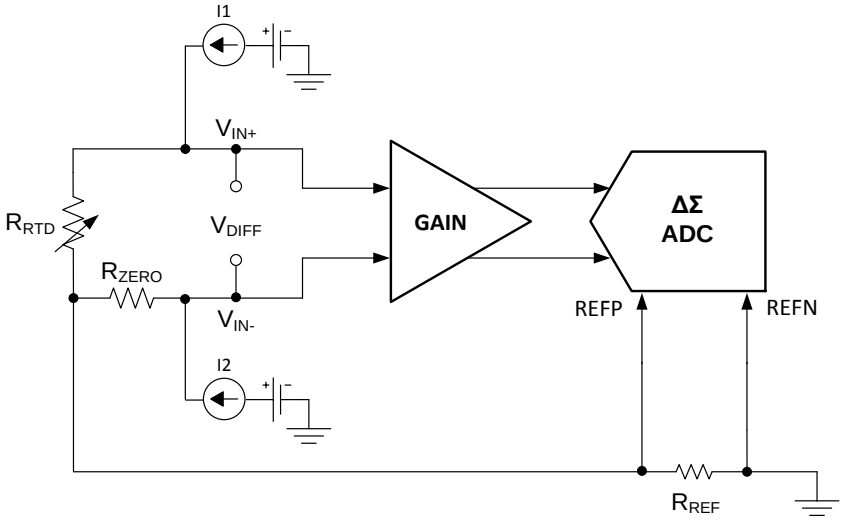

Figure 5. Hardware Compensated 3-Wire RTD System

Figure 6 displays the resulting ADC input signals from a traditional non-compensated RTD system with a temperature range of 0°C - 100°C. The input signal to the PGA spans from 25 mV to 35 mV. As a result of the 25 mV offset voltage, the maximum PGA gain that can be used before the signal exceeds the input limiations of the ADC is 32 V/V. This results in a differential input voltage that does not effectively use the full input range of the ADC.

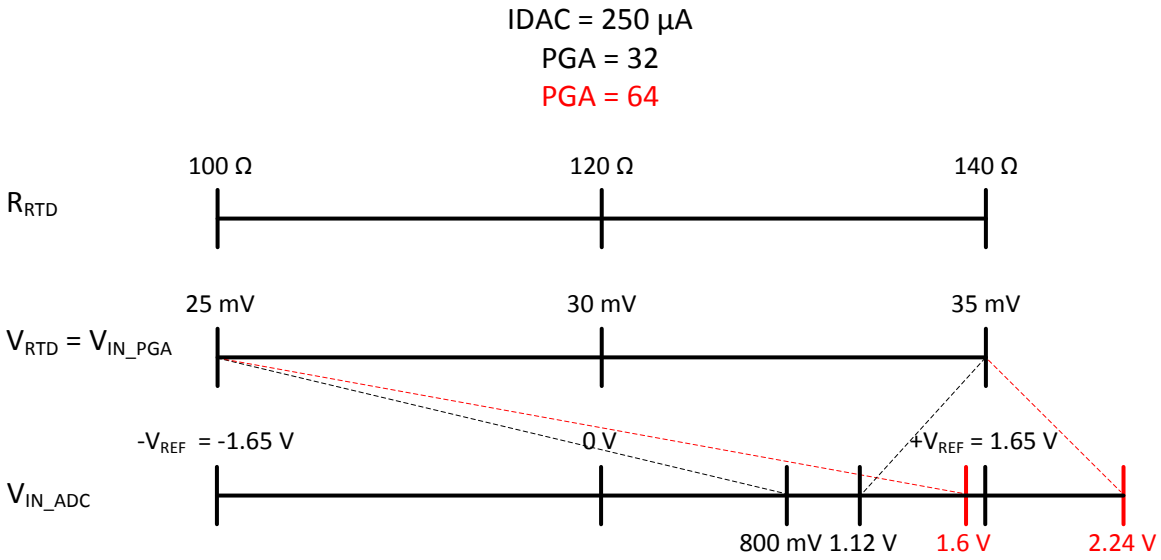

Figure 6: ADC Input Signals in a Traditional RTD System

In a hardware compensated system, the voltage drop across R_{ZERO} subtracts from the RTD voltage removing the 25 mV offset voltage. This results in a PGA input voltage that is centered at 0 V, allowing for the use of higher gains without saturating the ADC inputs as shown in Figure 7.

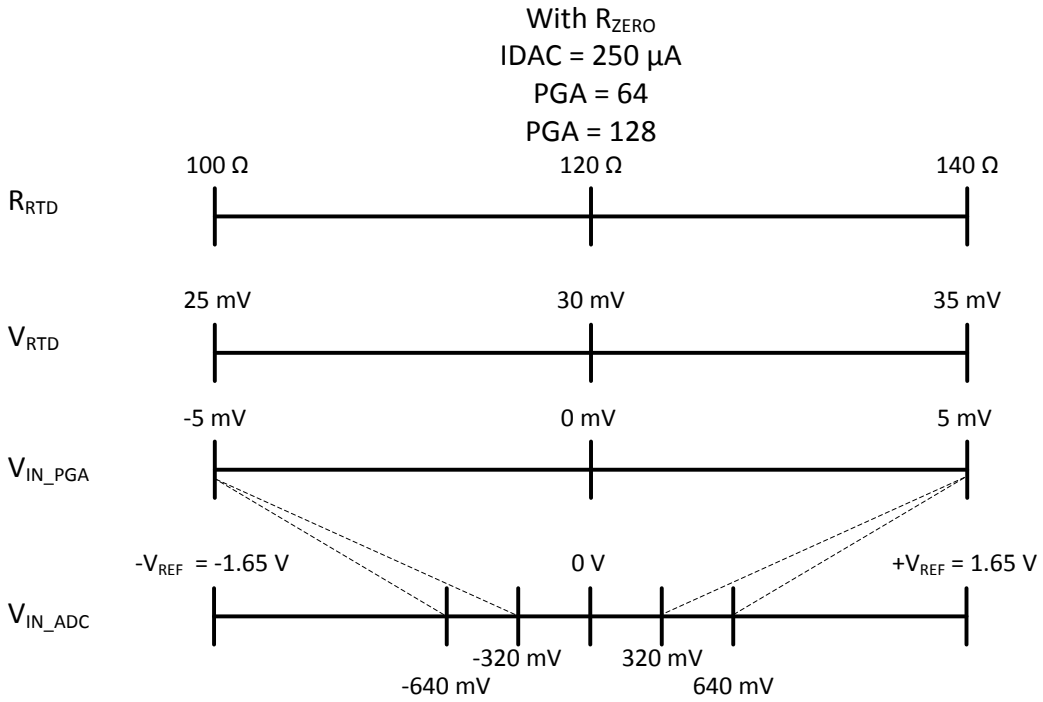

Figure 7: ADC Input Signals in a Hardware Compensated System

2.2.5 *Input and Reference Low-Pass Noise Filters*

Using differential and common-mode low-pass filters at the input and reference paths improves the cancellation of excitation and environment noise. However, it is important to note that the corner frequency of the two differential filters must be well matched as stated in Reference 1. The input and reference filters are shown in Figure 8.

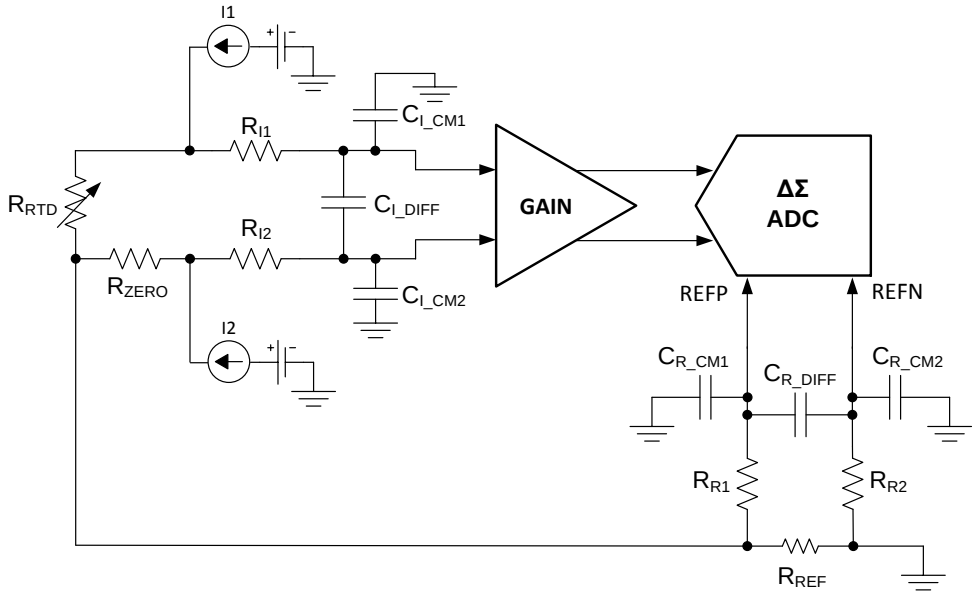

Figure 8: Input and Reference Low-Pass Filtering

3 Component Selection

3.1 ADC – ADS1247

The ADS1247, shown in Figure 9, is a 24-bit, delta-sigma (ΔΣ) ADC that offers a complete front-end solution for RTD applications. It comes from a product family of highly integrated precision data converters, featuring a low-noise, programmable gain amplifier (PGA), a precision ΔΣ modulator, a digital filter, an internal oscillator, and two digitally controlled precision current sources (IDACs). It is a popular industry choice for precision temperature measurement applications.

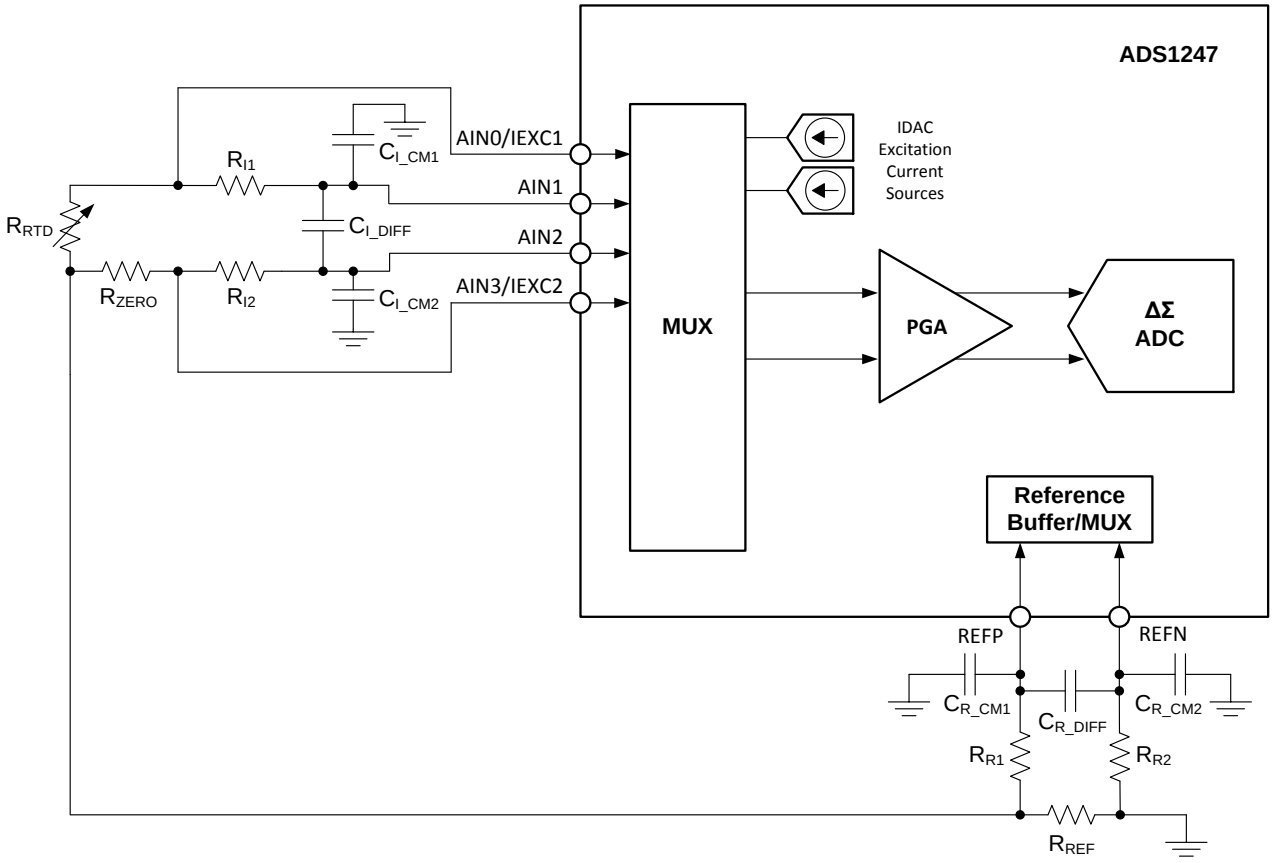

Figure 9: Hardware Compensated Ratiometric RTD System Featuring the ADS1247

3.1.1 *Current Source (IDAC) Configuration*

The ADS1247 features two IDAC current sources capable of outputting currents from 50 µA to 1.5 mA. Based on Figure 4, the excitation currents will be set to 250 µA to keep the errors due to self-heating less than the desired goal of 0.005°C for all types of RTD applications.

The internal reference voltage must be on while using the IDACs, even if an external reference ratiometric reference is used for ADC conversions. Table 2 displays the required register settings to set the IDACs to 250 µA and configure them for the proper output channels.

Table 2. Register Settings for Current Sources

Register (Address)	Register Bits	Bits Name	Bit Values	Comment
MUX1 (02h)	MUX1[6:5]	VREFCON[1:0]	01	Internal Reference ON
IDAC0 (0Ah)	IDAC0[2:0]	IMAG[2:0]	011	IDACs = 250 µA
IDAC1 (0Bh)	IDAC1[7:4]	I1DIR[3:0]	0000	IDAC1 → AIN0
IDAC1 (0Bh)	IDAC1[3:0]	I2DIR[3:0]	0011	IDAC2 → AIN3

3.1.2 *IDAC Multiplex Chopping*

As the equations in Appendix A.4 show, the two current sources must be exactly matched to successfully cancel the lead resistances of the RTD wires. While initial matching of the current sources is important, any remaining mismatch in the two sources can be minimized by using a multiplexer to swap, or "chop," the two current sources between the two inputs. Taking measurements in both configurations and averaging the readings will greatly reduce the effects of mismatched current sources. This design uses the digitally-controlled multiplexer in the ADS1247 to realize this technique. The multiplexer also affords the user some additional flexibility when routing the input voltage signals and excitation current sources on their printed circuit board (PCB) layout.

3.1.3 *Programmable Gain Amplifier (PGA) Configuration*

In this application, the ADC uses a 3.3 V supply for both the analog (AVDD) and digital (DVDD) power supplies. The excitation currents and R_{REF} have been selected to produce a mid-supply 1.65 V reference, allowing for a differential input signal range of ±1.65 V into the ΔΣ modulator.

The maximum allowable PGA gain setting is based on the reference voltage, the RTD resistance change, and the excitation current as shown in Equations 1 – 3.

$$R_{DIFF\_MAX} = R_{ZERO} - R_{RTD\_MIN} = 120\ \Omega - 100\ \Omega$$
$$R_{DIFF\_MAX} = 20\ \Omega \quad (1)$$

$$V_{IN\_PGA(max)} = I_{IDAC} \times R_{DIFF\_MAX} = 250\ \mu A \times 20\ \Omega$$
$$V_{IN\_PGA(max)} = 5\ mV \quad (2)$$

$$PGA_{MAX} = \frac{V_{REF}}{V_{IN\_PGA(max)}} = \frac{1.65\ V}{5\ mV}$$
$$PGA_{MAX} = 330\ V/V \quad (3)$$

Based on Equation 4, the PGA gain is set to the maximum value available in the ADS1247, 128 V/V, as shown in Table 3.

Table 3. Register Settings for PGA

Register (Address)	Register Bits	Bits Name	Bit Values	Comment
SYS0 (03h)	SYS0[6:4]	PGA[2:0]	111	PGA = 128 V/V

3.2 Passive Components

3.2.1 R_{REF}

The value of R_{REF} is selected based on the IDAC setting and the desired V_{REF} voltage of 1.65 V, as shown in Equations 4 - 5.

$$R_{REF} = \frac{V_{REF}}{2 \times I_{IDAC}} \quad (4)$$

$$R_{REF} = \frac{1.65\ V}{2 \times 250\ \mu A} = 3.3\ k\Omega \quad (5)$$

A 3.3 kΩ R_{REF} resistor was chosen resulting in the desired reference voltage as shown in Equation 6. The tolerance and temperature drift of R_{REF} directly affect the measurement gain error, so a 0.01% precision resistor with ±2ppm/°C drift was chosen.

$$V_{REF} = 3.3\ k\Omega \times 500\ \mu A = 1.65\ V \quad (6)$$

3.2.2 *R_{ZERO}*

As shown in Appendix A.3, the impedance range of a PT-100 RTD is 100 Ω – 138.5 Ω for temperatures from 0°C - 100°C. At mid-scale, the RTD will equal 119.25 Ω. Using standard values, R_{ZERO} was chosen to be 120 Ω such that the differential input would swing almost equally in the positive and negative directions. The tolerance and temperature drift of R_{ZERO} directly affect the measurement accuracy. The highest attainable precision for R_{ZERO} was 0.02% with ±5ppm/°C.

3.2.3 *Input and Reference Low-Pass Noise Filters*

The differential filters chosen for this application were designed to have a -3 dB corner frequency at least 10 times larger than the bandwidth of the ADC. The selected ADS1247 sampling rate of 20 SPS results in a -3dB bandwidth of 14.8 Hz. Therefore, the filter -3dB corner frequency was set to be roughly 250 Hz at mid-scale temperature (R_{RTD} = 120 Ω). For proper operation, the differential cutoff frequencies of the reference and input low-pass filters must be well matched. This can be difficult because as the resistance of the RTD changes over the span of the measurement, the filter cutoff frequency changes as well. To mitigate this effect, the two resistors used in the input filter (R_{I1} and R_{I2}) were chosen to be more than an order of magnitude larger than the RTD. Limiting the resistors to at most 20 kΩ will reduce dc offset errors due to input bias current. The two resistors were selected to be approximately two orders of magnitude larger than R_{RTD}:

$$R_{I1} = R_{I2} = 10\ k\Omega \quad (7)$$

The input filter differential capacitor (C_{I_DIFF}) can be calculated as shown in Equation 8.

$$f_{-3dB\_DIFF} = \frac{1}{2 \times \pi \times C_{I\_DIFF} \times (R_{I1} + R_{RTD} + R_{ZERO} + R_{I2})} \quad (8)$$

$$C_{I\_DIFF} \approx 33\ nF$$

To ensure that mismatch of the common-mode filtering capacitors is not translated to a differential voltage, the common-mode capacitors (C_{I_CM1} and C_{I_CM2}) were chosen to be 10 times smaller than the differential capacitor, making them 3.3 nF each. This results in a common-mode cutoff frequency that is roughly twenty times larger than the differential filter, making the matching of the common-mode cutoff frequencies less critical.

$$C_{I\_CM1} = C_{I\_CM2} = 3.3\ nF \quad (9)$$

$$f_{-3dB\_CM+} = \frac{1}{2 \times \pi \times C_{I\_CM1} \times (R_{I1} + R_{RTD} + R_{REF})} \quad (10)$$

$$f_{-3dB\_CM+} = 3.59\ kHz$$

$$f_{-3dB\_CM-} = \frac{1}{2 \times \pi \times C_{IN\_CM2} \times (R_{I2} + R_{ZERO} + R_{REF})}$$
$$f_{-3dB\_CM-} = 3.59 \text{ kHz} \quad (11)$$

The differential reference filter is designed to have a -3 dB corner frequency of 250 Hz to match the differential input filter. The two reference filter resistors were selected to be 20 kΩ, several times larger than the value of R_{REF}. The reference filter resistors should not be sized larger than 20 kΩ or dc bias errors will become significant.

$$R_{R1} = R_{R2} = 20 \text{ k}\Omega \quad (12)$$

The differential capacitor for the reference filter can be calculated as shown in Equation 13.

$$f_{-3dB\_DIFF} = \frac{1}{2 \times \pi \times C_{R\_DIFF} \times (R_{R1} + R_{REF} + R_{R2})}$$
$$C_{R\_DIFF} \approx 15 \text{ nF} \quad (13)$$

To ensure that mismatch of the common-mode filtering capacitors is not translated to a differential voltage, the reference common-mode capacitors (C_{R_CM1} and C_{R_CM2}) were chosen to be 10 times smaller than the reference differential capacitor, making them 1.5 nF each. Again, the resulting cutoff frequency for the common-mode filters is roughly twenty times larger than the differential filter, making the matching of the cutoff frequencies less critical.

$$C_{R\_CM1} = C_{R\_CM2} = 1.5 \text{ nF} \quad (14)$$

$$f_{-3dB\_CM+} = \frac{1}{2 \times \pi \times C_{R\_CM1} \times (R_{R1} + R_{REF})}$$
$$f_{-3dB} = 4.55 \text{ kHz} \quad (15)$$

$$f_{-3dB\_CM-} = \frac{1}{2 \times \pi \times C_{R\_CM2} \times R_{R2}}$$
$$f_{-3dB} = 5.3 \text{ kHz} \quad (16)$$

3.3 Low-Dropout (LDO) Linear Regulator

The RTD acquisition board in this design interfaces with an external PC GUI through a USB interface board to post-process the ADC digital output and display the temperature result. Power for the acquisition board comes from the USB power supply rail. To avoid the inaccuracies and noise from the USB power supply, VDUT may be passed through a high-PSRR low-dropout regulator (LDO) to create the AVDD and DVDD supplies.

The TPS7A4901 comes from a series of high-voltage, ultra-low noise LDOs that are ideal for precision applications. A resistor divider at the LDO output sets the output voltage (V_{LDO_OUT}) proportional to the LDO's internal reference voltage (V_{LDO_REF}). For this device, V_{LDO_REF} = 1.194 V. In order to set V_{LDO_OUT} to the desired 3.3 V, the resistor divider components are selected as:

$$V_{LDO\_OUT} = V_{LDO\_REF} \times (1 + \frac{R1}{R2}) \quad (17)$$

$$R1 = 140\ k\Omega \quad (18)$$

$$R2 = 78.7\ k\Omega \quad (19)$$

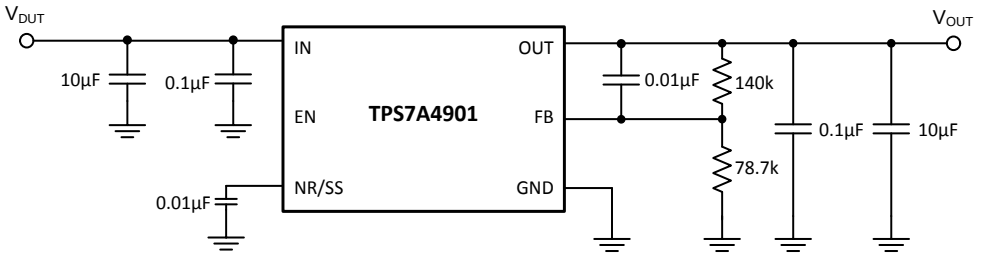

Figure 10. LDO Configuration for +3.3 V Output

4 Simulation

Figure 11 shows the TINA-TI™ circuit used to simulate the behavior of the RTD, input filtering, and PGA in this system. The RTD has been modeled with a PT-100 macromodel that converts an input voltage representative of the RTD temperature into the correct output resistance using the CVD equations. The simplified ADS1247 PGA does not accurately represent the internal circuitry to the ADC; however, it does represent the ideal behavior of the internal PGA.

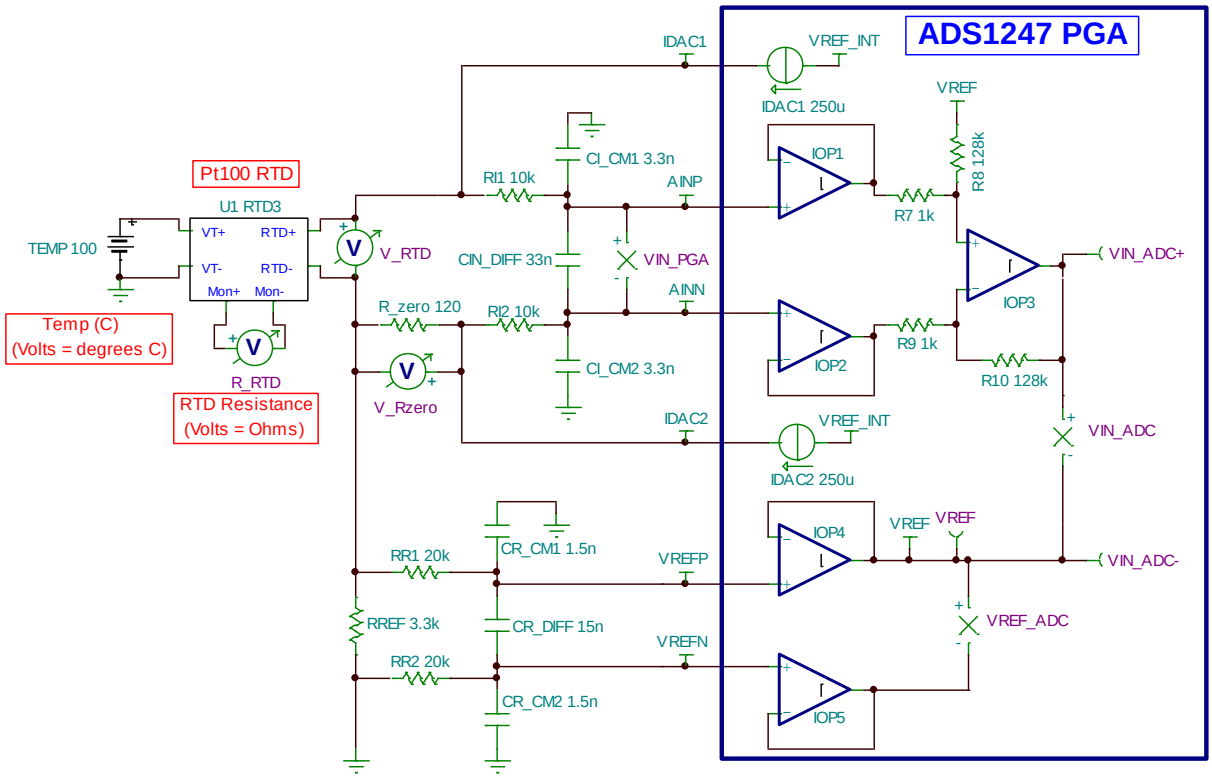

Figure 11. TINA-TI™ Simulation Circuit for the RTD and ADS1247 Inputs

4.1 RTD Transfer Function

Figure 12 displays the RTD resistance and voltage, the R_{ZERO} voltage, and the resulting differential voltage applied to the inputs of the PGA as the RTD temperature is swept from 0°C – 100°C. The results are displayed on the image for the minimum, mid-scale, and maximum temperatures. The 120 Ω value of R_{ZERO} is not exactly mid-scale of the RTD span (100 Ω – 138.5 Ω), so the final bipolar input to the ADC features more negative voltage than positive voltage.

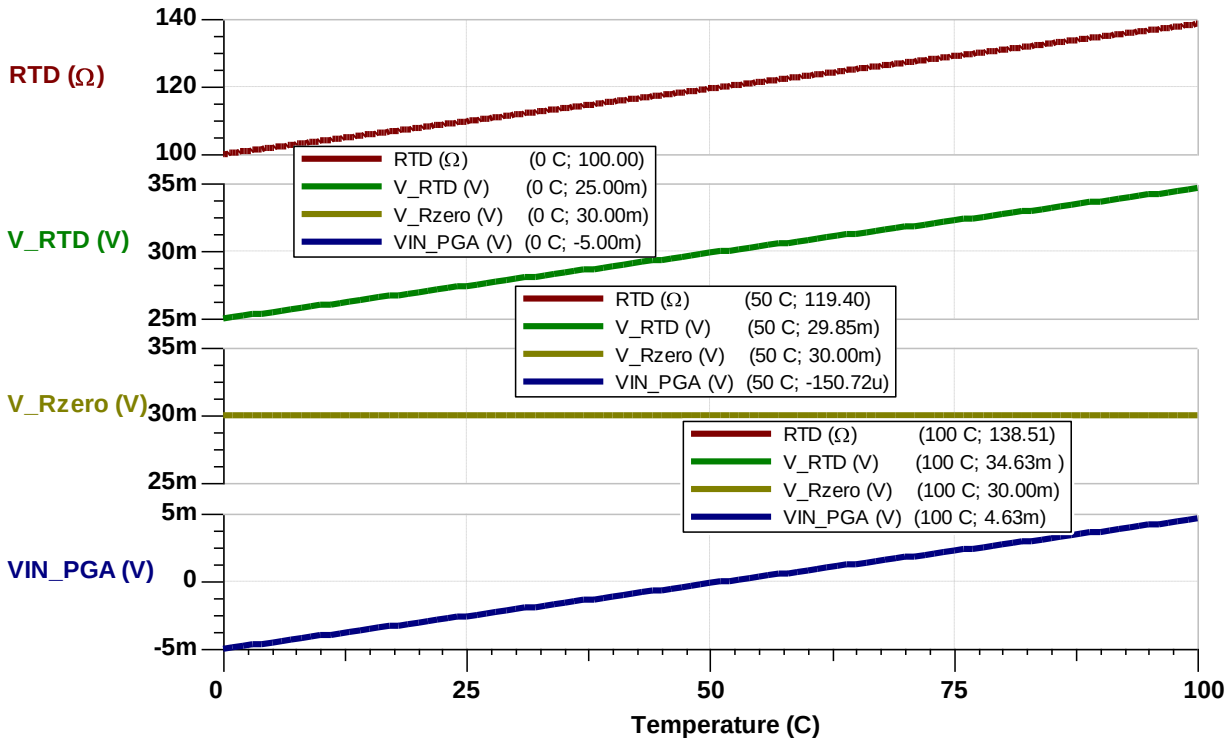

Figure 12. RTD, R_{ZERO}, and PGA Input from 0°C – 100°C

Figure 13 displays the input and the theoretical output of the PGA into the ADC when configured for a gain of 128 V/V. With an input of -5 mV to 4.63 mV, the PGA output is -640 mV to 592.18 mV. The ADC reference voltage, V_{REF}, is also displayed in Figure 13 and is the expected value of 1.65 V.

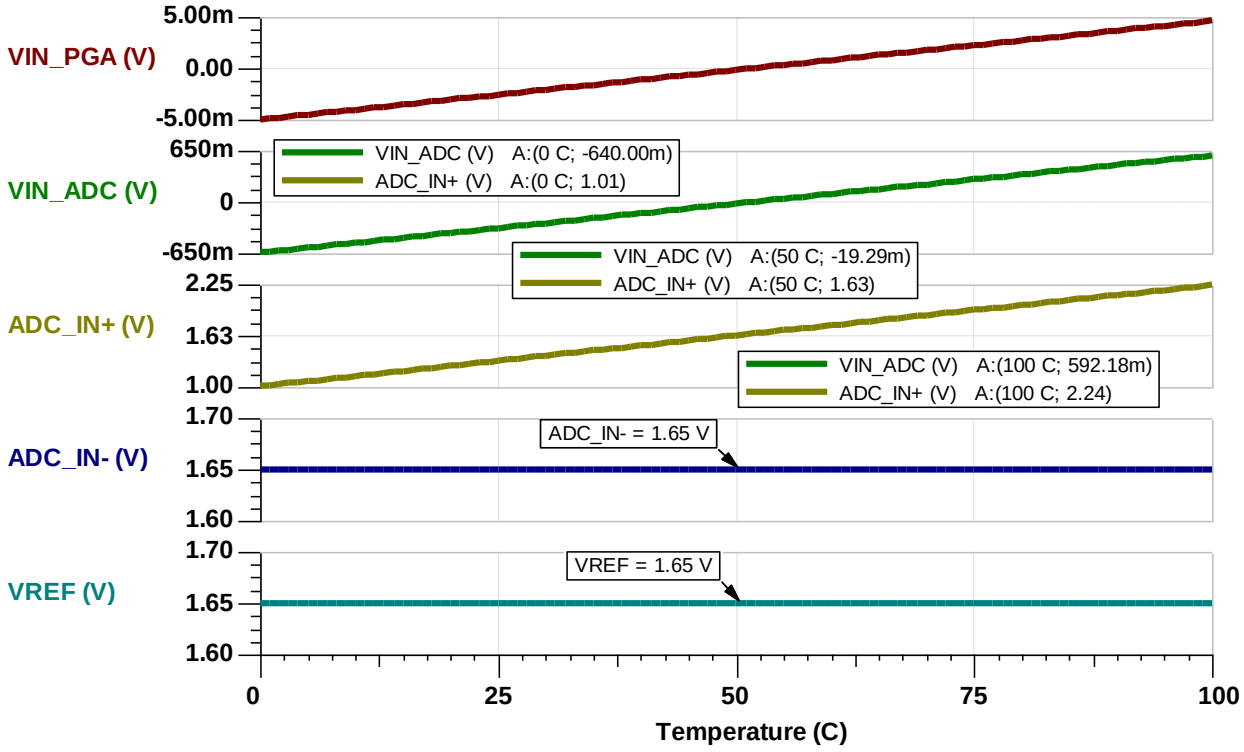

Figure 13. The Input and Output of the PGA and VREF from 0°C – 100°C

4.2 Low-pass Noise Filter Response

The frequency response of the input and reference filters was tested using an ac current generator in place of the IDAC1 source and is shown in Figure 14. The -3 dB cutoff frequency of the filters is near 230 Hz for both filters and is well matched with less than 3 Hz difference between them. The dc magnitude of the results is based on the current-to-voltage transfer function (I*R) as the excitation currents pass through the passive resistors in the signal chain. The results with IDAC2 active are very similar and can be seen in Appendix 0.

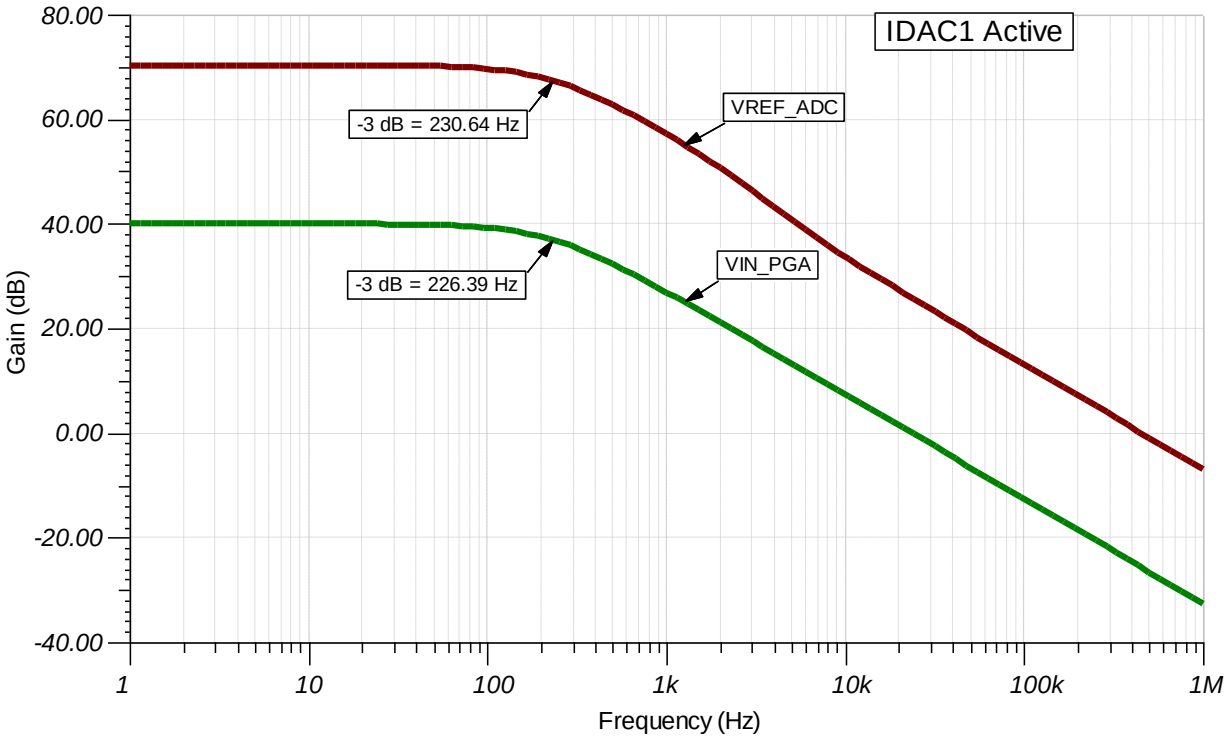

Figure 14. Simulated Filter Frequency Response

4.3 Noise Performance

The circuit and results for the simulated noise performance of the passive components in the design are shown in Figure 15 and Figure 16 respectively. The noise of the IDAC sources was not included because it should cancel with the ratiometric measurement. The extrinsic noise reduction of filtering the inputs is clearly shown in the difference between the magnitudes of noise before and after the filtering.

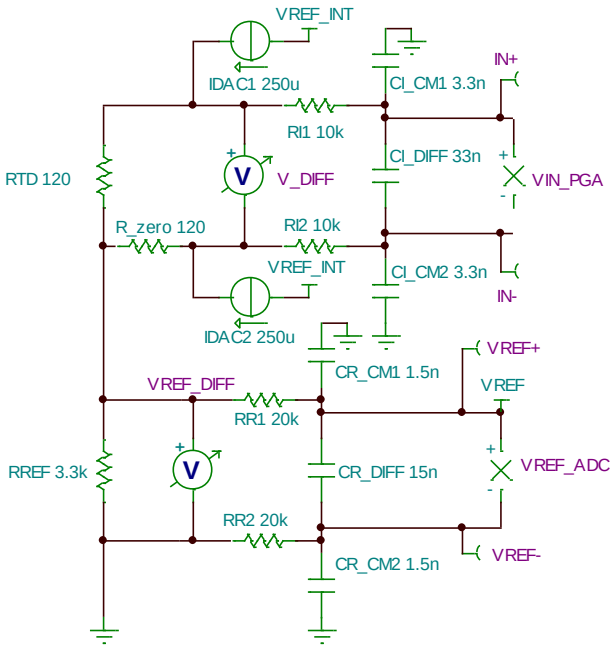

Figure 15. Noise Performance Simulation Schematic

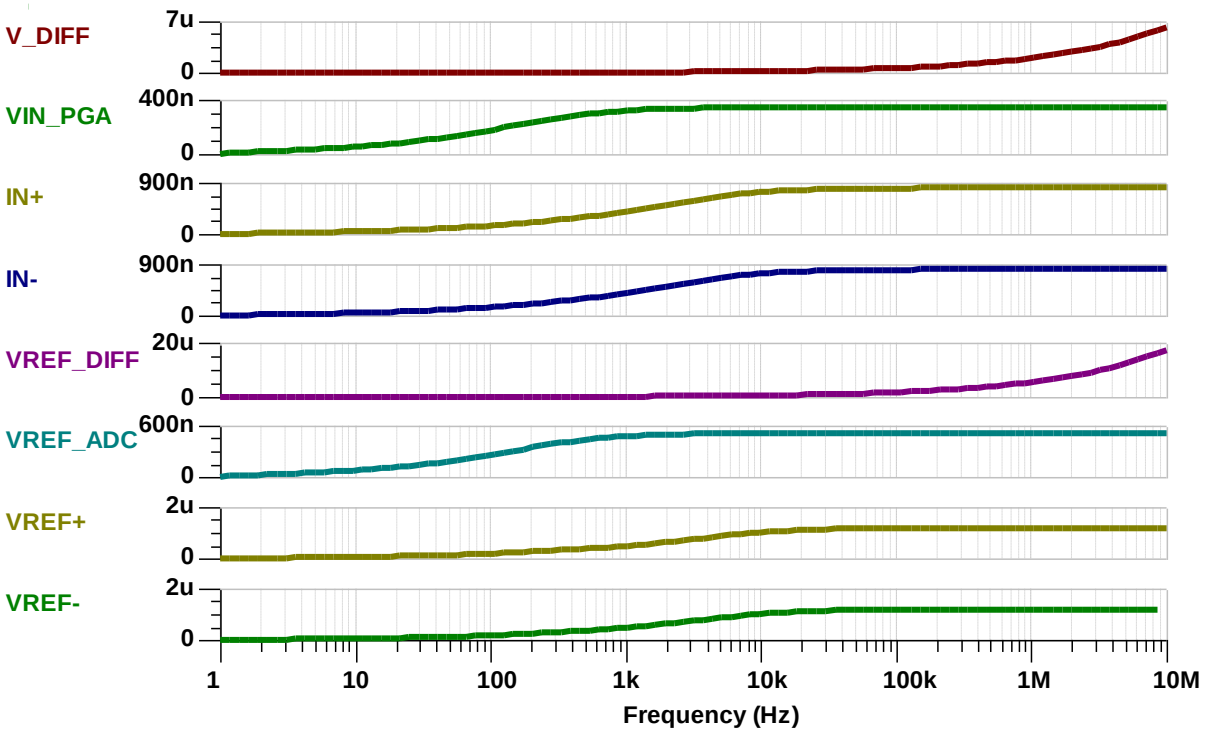

Figure 16. Simulated Noise Performance (y-axis is in Vrms)

5 PCB Design

Providing proper decoupling, grounding, and minimizing cross-over between the analog and digital circuitry return currents is required to achieve optimal performance in all mixed-signal PCB designs. In addition to standard practices, minimizing or balancing PCB trace resistance is a primary concern because the design is based on accurately measuring the difference between the RTD and R_{ZERO}. Implementing a 4-wire Kelvin connection at the RTD, R_{ZERO}, and R_{REF} resistors help to minimize PCB resistance in series with the sense elements by separating the measurement sense and excitation current paths,.

As discussed in Section 2.2.2, the lead resistances of the 3-wire RTD are effectively cancelled when they are equal and the magnitude of the excitation current sources are also equal. The same theory applies to PCB trace resistance in series with the 3 RTD leads. Therefore, the PCB trace resistance in series with R_{ZERO} and the RTD must be balanced, otherwise additional differential signals will be formed. The resistance of the R_{REF} trace is common to both inputs and is cancelled by taking the differential measurement, making it less critical.

Balancing the RTD and R_{REF} trace resistance is accomplished by creating traces of equal length between the terminal block and the R_{ZERO} and RTD connection points. Figure 17 displays these critical PCB layout areas. The full PCB layout is shown in Figure 18.

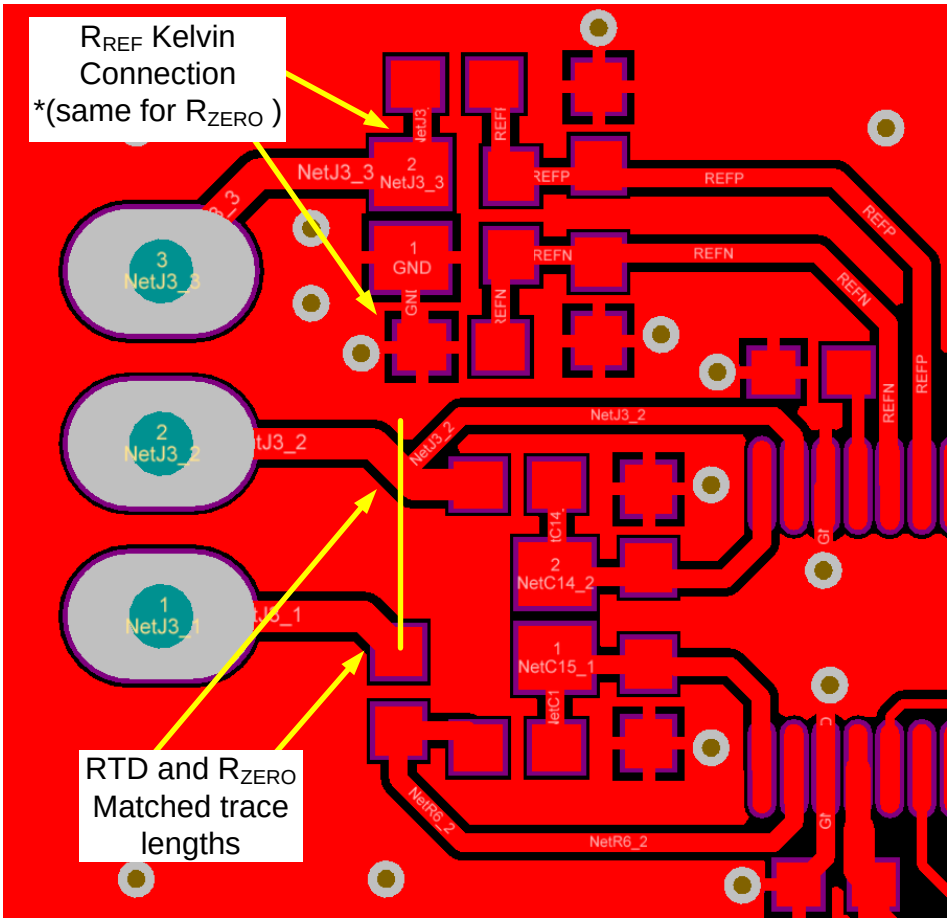

Figure 17. PCB Layout Highlighting Important PCB Layout Concerns

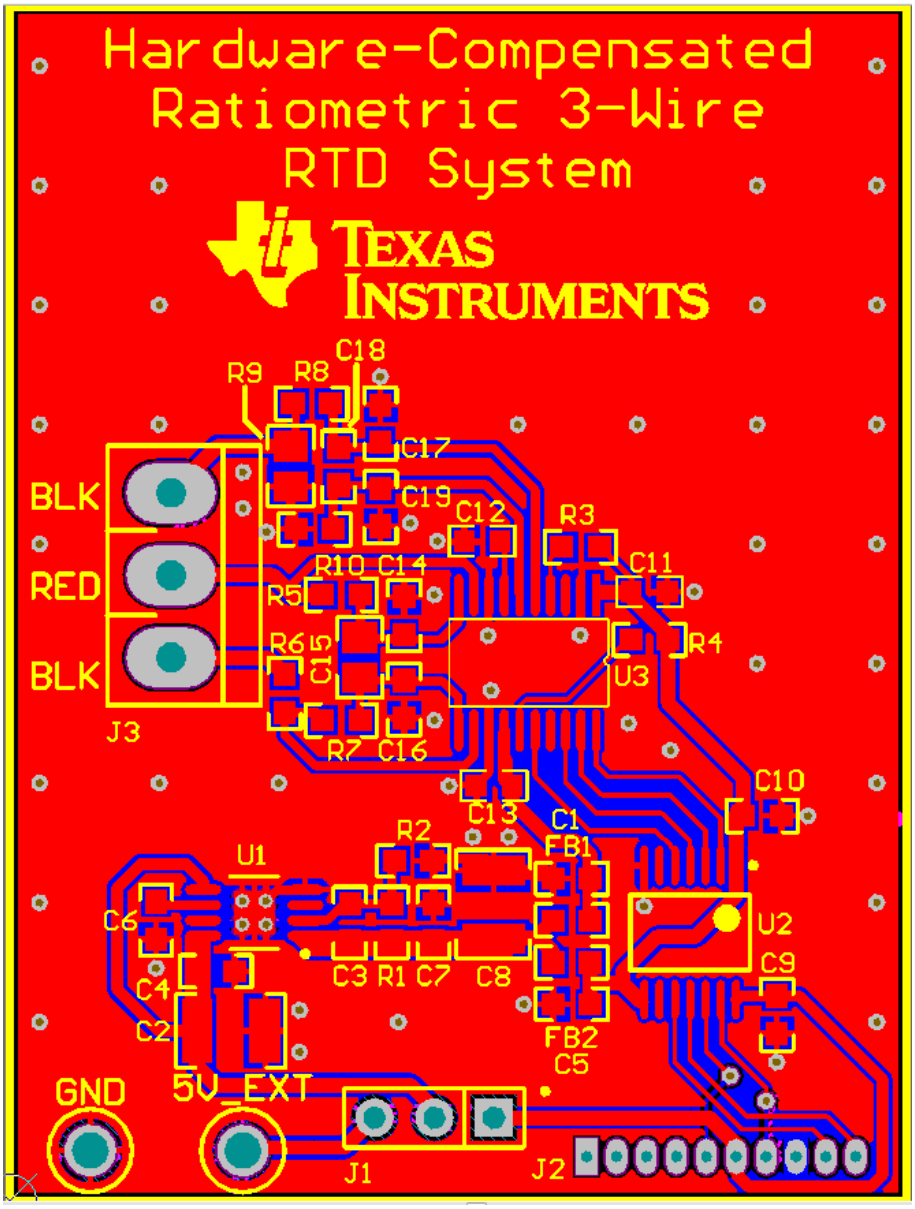

Figure 18. Full PCB Layout

6 Verification & Measured Performance

6.1 Measured Transfer Function with Precision Resistor Input

To test the accuracy of only the acquisition circuit, a series of calibrated high-precision discrete resistors were used as the input to the system. Figure 19 displays the unadjusted resistance measurement accuracy of the system over an input span from 100 Ω to 140 Ω. The offset error can be attributed largely to the tolerance of the R_{ZERO} resistor and the offset of the ADC, while the gain error can be attributed to the accuracy of the R_{REF} resistor and gain error of the PGA and ADC.

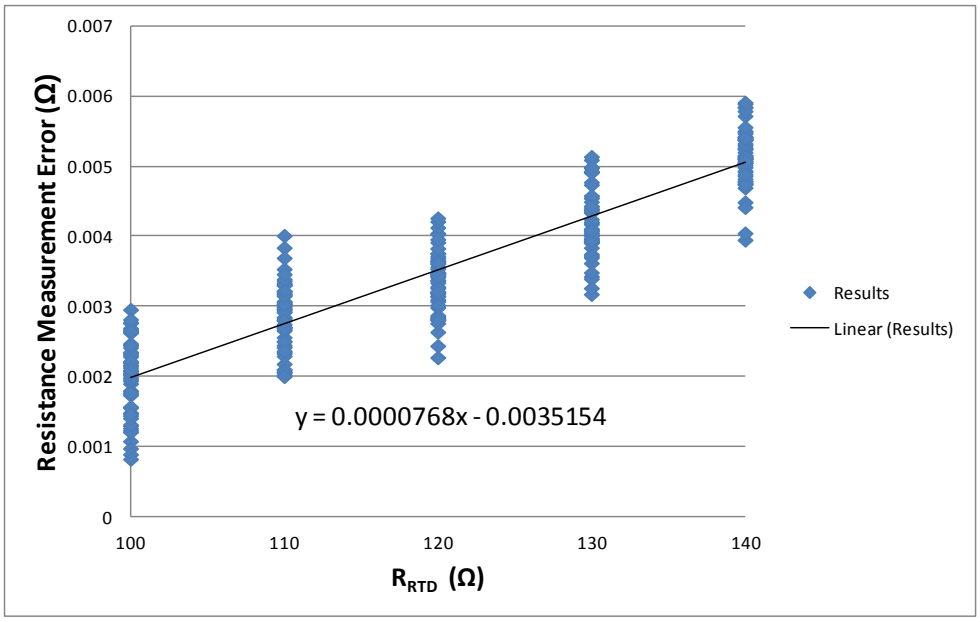

Figure 19. Resistance Measurement Results with Precision Resistors before Calibration

Applying a simple first-order gain and offset calibration yields the calibrated results shown in Figure 20.

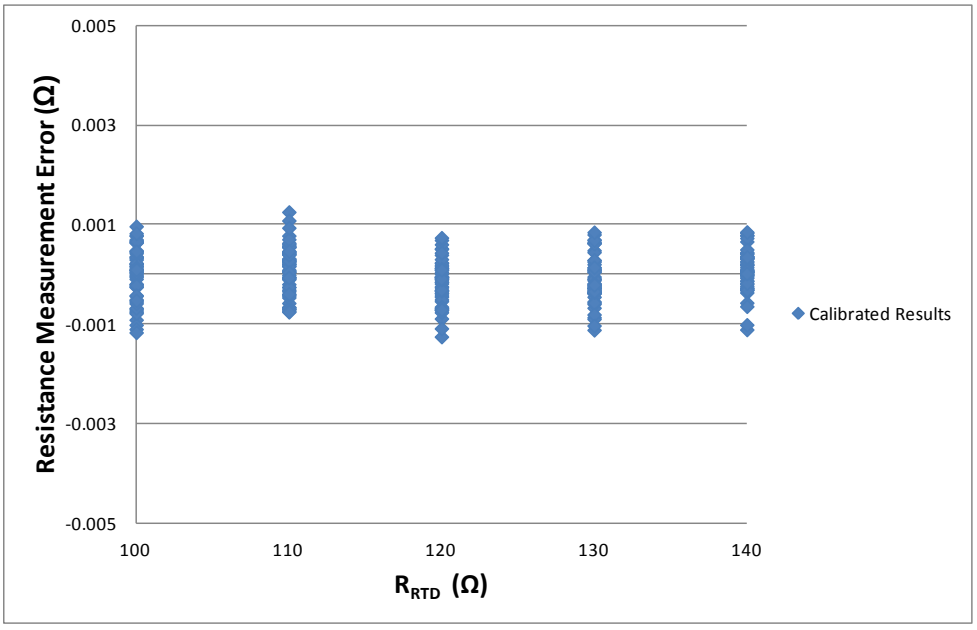

Figure 20. Resistance Measurement Results with Precision Resistors after Calibration

Using the slope of 0.385Ω/°C for a PT-100 RTD, the results in Figure 20 can be roughly converted to temperature error as shown in Figure 21.

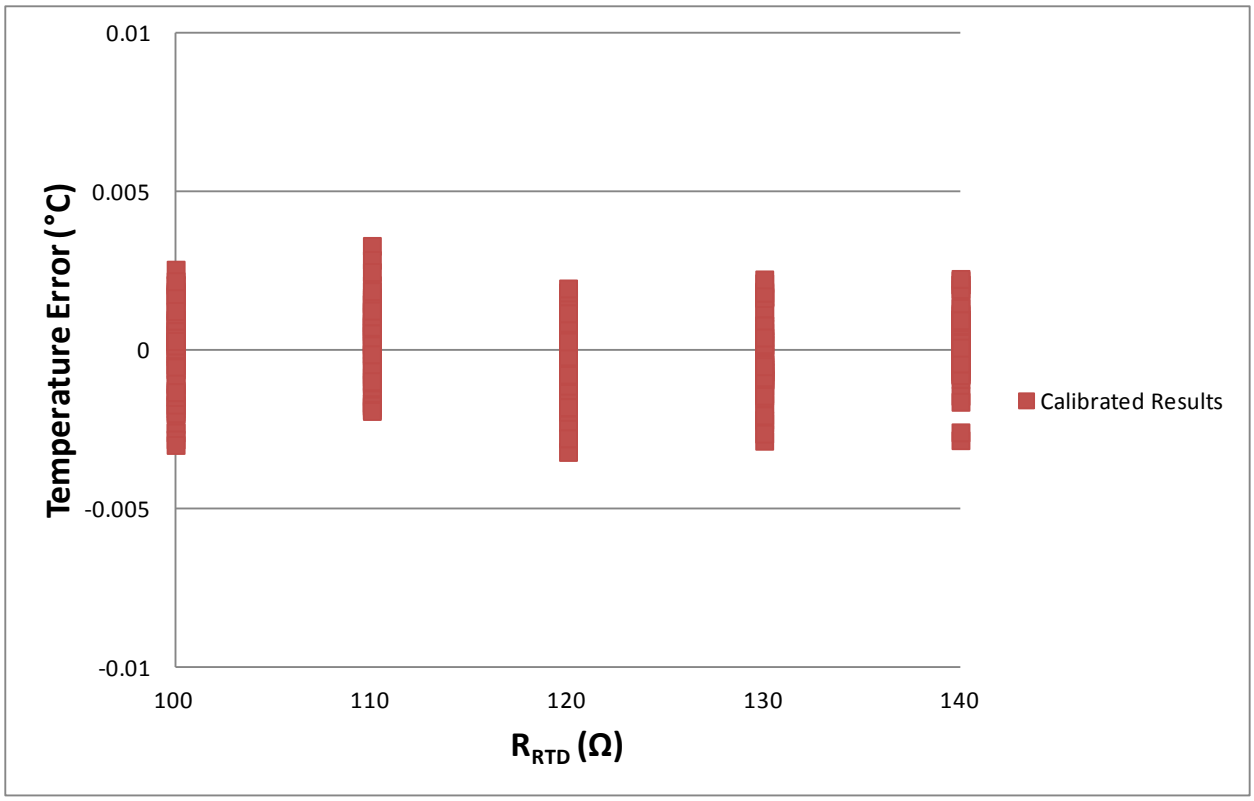

Figure 21: Calculated Temperature Error from Resistance Measurement Error

6.2 Noise Histogram

The peak-to-peak noise of the acquisition system can be approximated from an output code histogram. The RTD was replaced with a 120 Ω, 0.01% 0.05ppm/°C precision resistor, to represent the RTD resistance at mid-scale. Then samples were recorded to generate the histogram plot shown in Figure 22. The peak-to-peak voltage deviation in the histogram is roughly 0.793 µVpp or 515 codes. Equation 20 calculates the Least-Significant Bit (LSB) size of the ADC, which is then used to translate the peak-to-peak voltage to number of codes in Equation 21. The measured noise closely correlates to the value specified in the ADS1247 datasheet of 0.80 µVpp.

$$1\ \text{LSB} = \frac{\pm V_{REF}/\text{PGA}}{2^{24}-1}$$

$$1\ \text{LSB} = \frac{\pm 1.65\ \text{V}/128}{2^{24}-1} = 1.54\ \text{nV} \qquad (20)$$

$$\text{Noise (Codes)} = \frac{793\ \text{nV}}{1.54\ \text{nV}} = 515\ \text{Codes} \qquad (21)$$

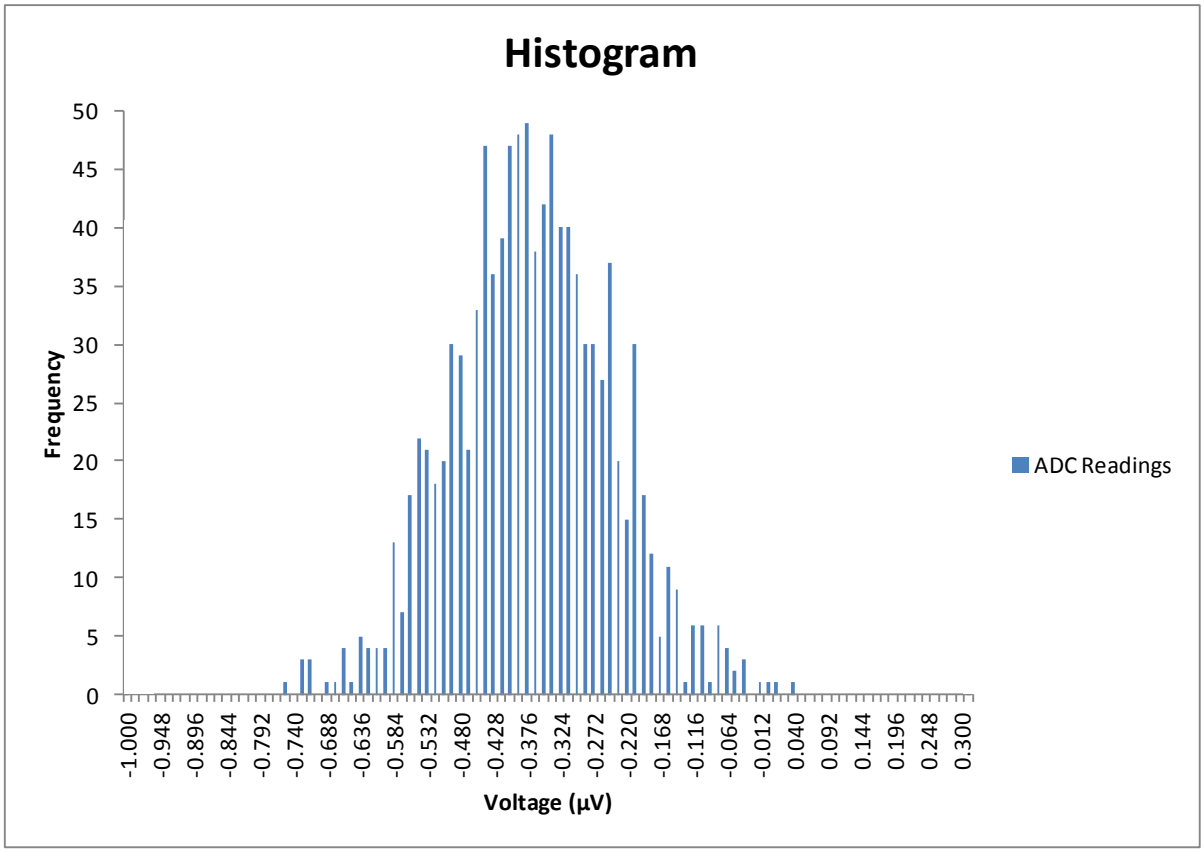

Figure 22. Histogram with R_{RTD} = 120 Ω, 0.01%

Equation 22 calculates relationship between the temperature range and the PGA input voltage range. This relationship can then be used to calculate the total noise in degrees Celsius by multiplying by the peak-to-peak noise voltage as shown in Equation 23.

$$°C/V = \frac{\text{Temp Span}}{\text{Voltage Span}} = \frac{100\ °C}{9.63\ mV} = 10.384\ °C/mV \quad (22)$$

$$\text{Noise}\ (°C_{PP}) = 10.384\ °C/mV \times 793\ nV = 0.0082\ °C_{PP} = \pm 0.0041\ °C \quad (23)$$

The measured temperature noise falls within the accuracy goal of ±0.005°C and can be observed in the results in Figure 21. The noise can be further reduced by applying additional averaging or filtering in software.

7 Modifications

Since the current design only uses roughly ±640 mV of the ±1.65 V allowable input range, the system can be used for temperature range roughly 2.5 times larger than what shown without modification. This design can be easily modified for other RTD types and temperature ranges by changing the IDAC, PGA, R_{REF} and R_{ZERO} selections using the equations shown in the theory and component selection sections.

There are a few other fully integrated products that feature the same required building blocks as the ADS1247 that feature different performance, channel count, and cost. Several of these devices are listed in Table 4.

Table 4. Alternate Fully-Integrated ADC Solutions

ADC	Resolution	Differential Inputs	PGA Range	IDACs Magnitude	Noise	Power Consumption
ADS1147	16	2	1 – 128 V/V	50 µA – 1.5 mA	0.14 µVrms	1.4 mW
ADS1247	24	2	1 – 128 V/V	50 µA – 1.5 mA	0.14 µVrms	1.4 mW
ADS1148	16	4	1 – 128 V/V	50 µA – 1.5 mA	0.14 µVrms	1.4 mW
ADS1248	24	4	1 – 128 V/V	50 µA – 1.5 mA	0.14 µVrms	1.4 mW
ADS1120	16	2	1 – 128 V/V	10 µA – 1.5 mA	0.12 µVrms	0.4 mW
ADS1220	24	2	1 – 128 V/V	10 µA – 1.5 mA	0.12 µVrms	0.4 mW
LMP90100	24	4	1 – 128 V/V	100 µA – 1 mA	0.25 µVrms	1.2 mW

Table 5 features other suitable ADC solutions that feature integrated PGAs.

Table 5. Alternate ADC + PGA Solutions

ADC	Resolution	Differential Inputs	PGA Range	Noise	Power Consumption
ADS1146	16	1	1 – 128 V/V	0.14 µVrms	1.4 mW
ADS1246	24	1	1 – 128 V/V	0.14 µVrms	1.4 mW
LMP90099	24	4	1 – 128 V/V	0.25 µVrms	1.2 mW

Discrete current sources could be comprised of an integrated device such as the REF200 or a circuit such as the designs featured in TIPD101 or TIPD107.

8 About the Author

Ryan Andrews is an applications engineer with the Precision Analog Delta-Sigma ADC team at Texas Instruments, where he supports industrial and medical products and applications. Ryan received his BS in Biomedical Engineering and his BA in Spanish from the University of Rhode Island.

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

9 Acknowledgements & References

1. *Luis Chioye, "RTD Ratiometric Measurement and Filtering Using the ADS1148 and ADS1248 Family of Devices" SBAA201, March 2013.*
2. *Robert Burnham and Nagaraj Ananthapadamanabhan, "Example Temperature Measurement Applications Using the ADS1247 and ADS1248" SBAA180, January 2011.*
3. *Collin Wells, "Signal Conditioning and Linearization of RTD Sensors" 2011 Texas Instruments Technology Day Presentation.*
4. *Omega ®, "The Omega ® Temperature Measurement Handbook™ and Encyclopedia, Vol MMXIV™, 7th Edition.*

Appendix A.

A.1 Electrical Schematic

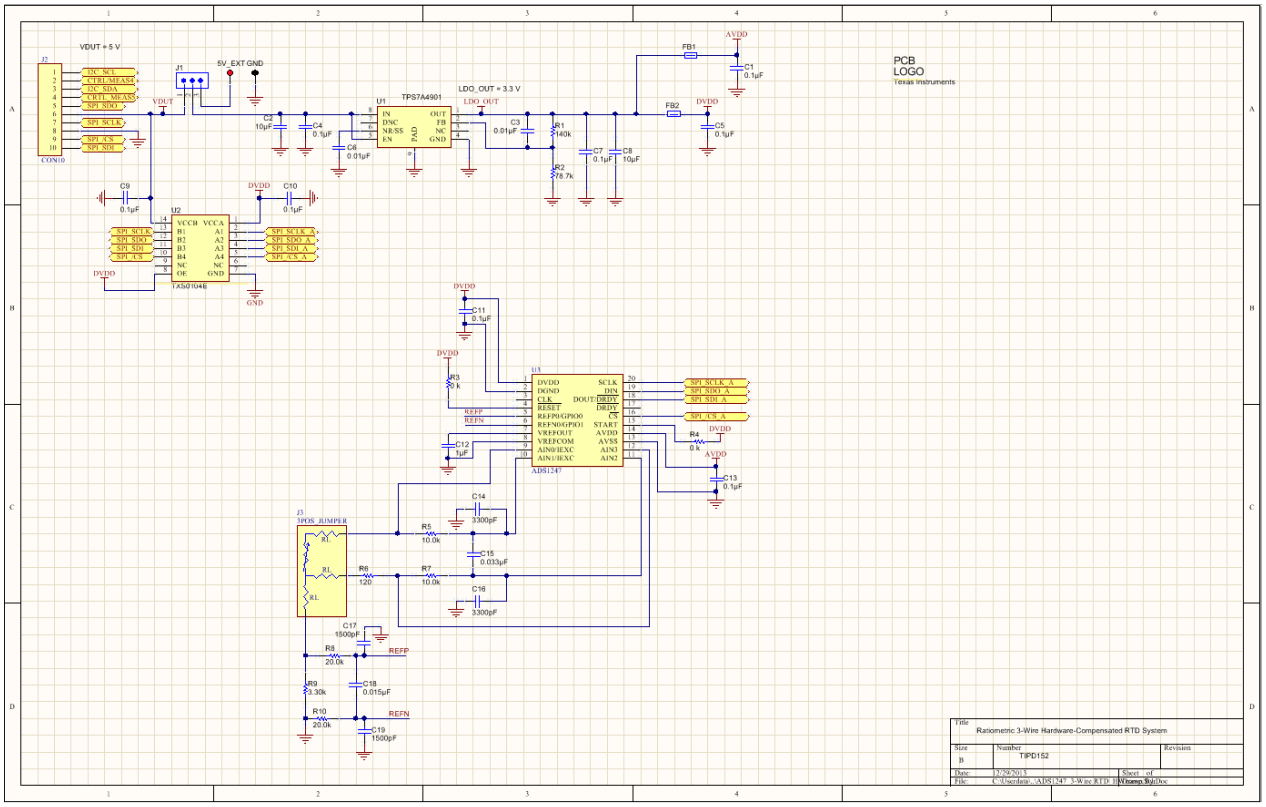

Figure 23. Electrical Schematic

A.2 Bill of Materials

Texas Instruments

Bill of Materials

TI DESIGNS

Item #	Quantity	Designator	Value	Description	Manufacturer	Part Number
1	8	C1, C4, C5, C7, C9, C10, C11, C13	0.1 µF	CAP CER 0.1UF 50V 10% X7R 0603	MuRata	GRM188R71H104KA93D
2	2	C2, C8	10 µF	CAP CER 10UF 25V 20% X7R 1210	TDK	C3225X7R1E106M250AC
3	2	C3, C6	0.01 µF	CAP CER 10000PF 25V 5% NP0 0603	TDK	C1608C0G1E103J080AA
4	1	C12	1 µF	CAP CER 1UF 25V 10% X7R 0603	Taiyo Yuden	TMK107B7105KA-T
5	2	C14, C16	3300 pF	CAP CER 3300PF 25V 5% NP0 0603	Samsung Electro-Mech	CL10C332JA8NNNC
6	1	C15	0.033 µF	CAP CER 0.033UF 25V 5% NP0 0805	TDK	C2012C0G1E333J125AA
7	2	C17, C19	1500 pF	CAP CER 1500PF 25V 5% NP0 0603	MuRata	GRM1885C1E152JA01D
8	1	C18	0.015 µF	CAP CER 0.015UF 25V 5% NP0 0603	Kemet	C0603C153J3GACTU
9	2	FB1, FB2		FERRITE CHIP 600 OHM 200MA 0603	MuRata	BLM18HG601SN1D
10	1	J1		CONN HEADER 3POS .100"SGL GOLD	Samtec, Inc.	TSW-103-07-G-S
11	1	J2		CONN SOCKET 50PIN .050 R/ASNGL	Mill-Max Manufacturing	851-43-050-20-001000
12	1	J3		TERMINAL BLOCK 3.5MM 3POS PCB	On Shore Technology Inc	ED555/3DS
13	1	R1	140 k	RES 140K OHM 1/10W 1% 0603 SMD	Vishay Dale	CRCW0603140KFKEA
14	1	R2	78.7 k	RES 78.7K OHM 1/10W 1% 0603 SMD	Vishay Dale	CRCW060378K7FKEA
15	2	R3, R4	0	RES 0.0 OHM 1/10W JUMP 0603 SMD	Panasonic Electronic	ERJ-3GEY0R00V
16	2	R5, R7	10 k	RES, 10.0k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0710KL
17	2	R8, R10	20 k	RES, 20.0k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0720KL
18	1	R6	120	RES 120 OHM 1/10W .02% 0603	Susumu	RG1608V-121-P-T1
19	1	R9	3.3 k	RES 3.3K OHM 0.1W 0.01% 0805	Susumu	RG2012L-332-L-T05
20	1	TP1		Test Point, TH, Compact, Red	Keystone	5005
21	1	TP2		Test Point, TH, Compact, Black	Keystone	5006
22	1	U1		IC REG LDO ADJ 0.15A 8MSO	Texas Instruments Inc	TPS7A4901DGNR
23	1	U2		IC 4BIT NON-INV TRANSLTR 14TSSOP	Texas Instruments Inc	TXS0104EPWR
24	1	U3		IC ADC 24BIT DEL/SIG LN 20TSSOP	Texas Instruments Inc	ADS1247IPW

Figure 24. Bill of Materials

A.3 PT-100 RTD Information

The PT-100 RTD is a platinum-based RTD sensor. Platinum is a noble metal and offers excellent performance over a wide temperature range. Platinum also features the highest resistivity of commonly used RTD materials, requiring less material to create desirable resistance values. The PT-100 RTD has an impedance of 100 Ω at 0°C and roughly 0.385 Ω of resistance change per 1°C change in temperature, resulting in 119.6 Ω at 50°C and 138.4 Ω at 100°C. Higher-valued resistance sensors, such as PT-1000 or PT-5000, can be used for increased sensitivity and resolution.

Class-A RTDs are a good choice for this application to provide good pre-calibration accuracy and long-term stability. A Class-A RTD will have less than 0.5°C of error at 100°C without calibration and the long-term stability makes accurate infrequent calibration possible. Table 6 displays the tolerance, initial accuracy and resulting error at 100°C for the five main classes of RTDs.

Table 6. RTD Class Tolerance Information

Tolerance Class (DIN-IEC 60751)	Tolerance Values (°C)	Resistance at 0°C (Ω)	Error at 100°C (°C)
***AAA**	+/- (0.03 + 0.0005*t)	100 +/- 0.012	+/- 0.08
AA	+/- (0.01 + 0.0017*t)	100 +/- 0.04	+/- 0.27
A	+/- (0.15 + 0.002*t)	100 +/- 0.06	+/- 0.35
B	+/- (0.3 + 0.005*t)	100 +/- 0.12	+/- 0.8
C	+/- (0.6 + 0.01*t)	100 +/- 0.24	+/- 1.6

*AAA is not included in the DIN-IEC 60751 specification but is an industry accepted tolerance for performance demanding applications.

For positive temperatures the CVD equations is a 2nd-order polynomial Equation 24.

$$RTD(T) = R_0 \times [1 + A(T) + B(T)^2] \quad (24)$$

For negative temperatures from -200°C to 0°C, the CVD equation expands to a 4th-order polynomial shown in Equation 25.

$$RTD(T) = R_0 \times [1 + A(T) + B(T)^2 + C(T)^3 \times (T - 100)] \quad (25)$$

The coefficients in the Calendar Van-Dusen equations are defined by the IEC-60751 standard. R_0 is the resistance of the RTD at 0°C. For a PT-100 RTD with an alpha (α) of 0.00385, the coefficients are:

$$\begin{aligned} R_0 &= 100\ \Omega \\ A &= 3.9083 \times 10^{-3}\ °C^{-1} \\ B &= -5.775 \times 10^{-7}\ °C^{-1} \\ C &= -4.183 \times 10^{-12}\ °C^{-1} \end{aligned} \quad (26)$$

The change in resistance of a PT-100 RTD from 0°C – 100°C is displayed in Figure 25.

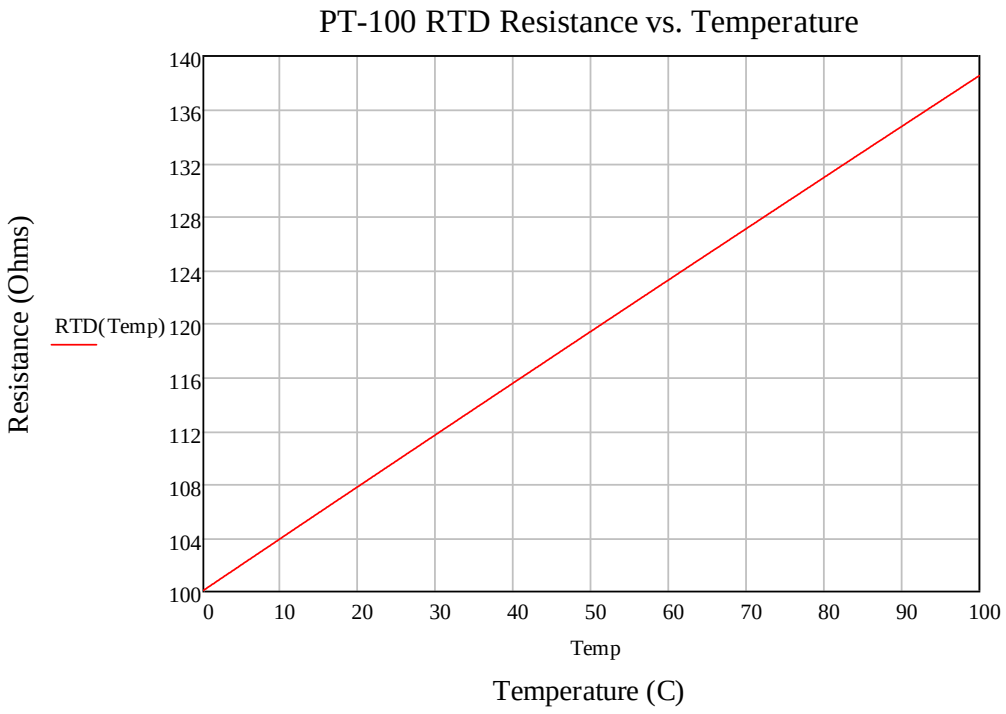

Figure 25. PT-100 RTD Resistance from 0°C – 100°C

While the change in RTD resistance is fairly linear over small temperature ranges, Figure 26 displays the resulting non-linearity if an end-point fit is made to the curve shown in Figure 25. The results show roughly 0.375% non-linearity and illustrate the need for digital calibration.

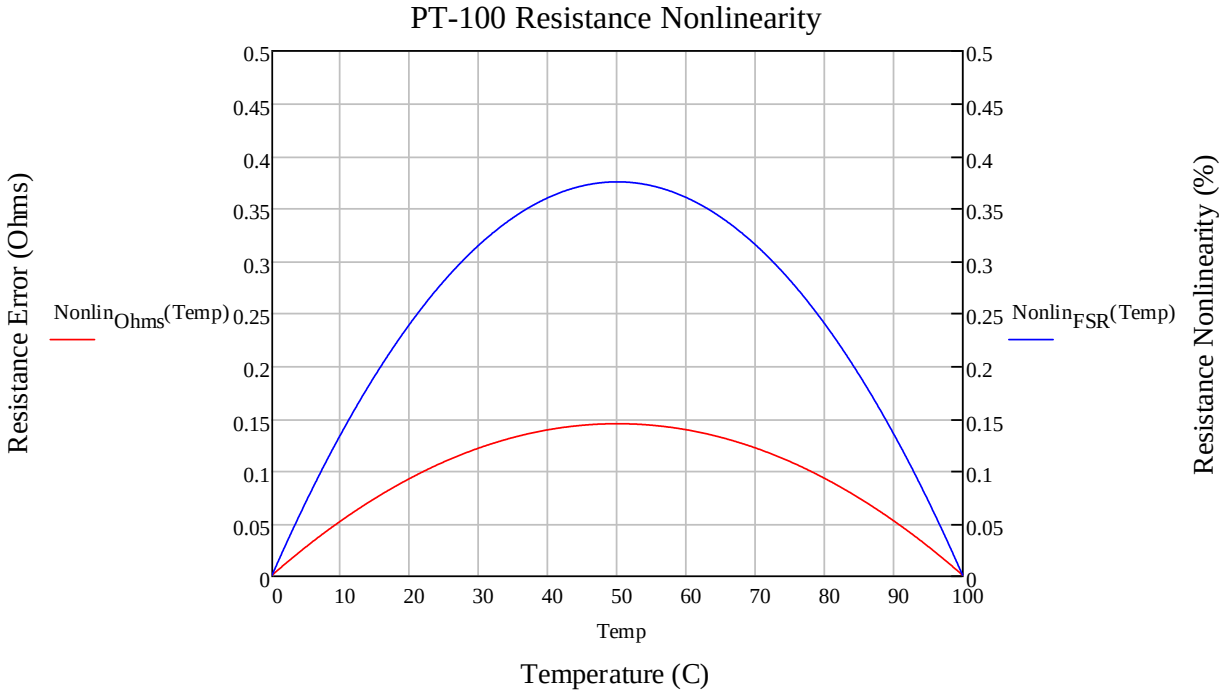

Figure 26. PT-100 RTD Non-Linearity from 0°C – 100°C

A.4 Hardware Compensated 3-Wire RTD Lead Resistance Cancellation

A 3-wire RTD configuration was selected for this application, see Reference 2 for more information on other RTD configurations. The input to the ADC in a hardware compensated 3-wire RTD measurement system and the equations that define its operation are shown in Equations 27 – 30.

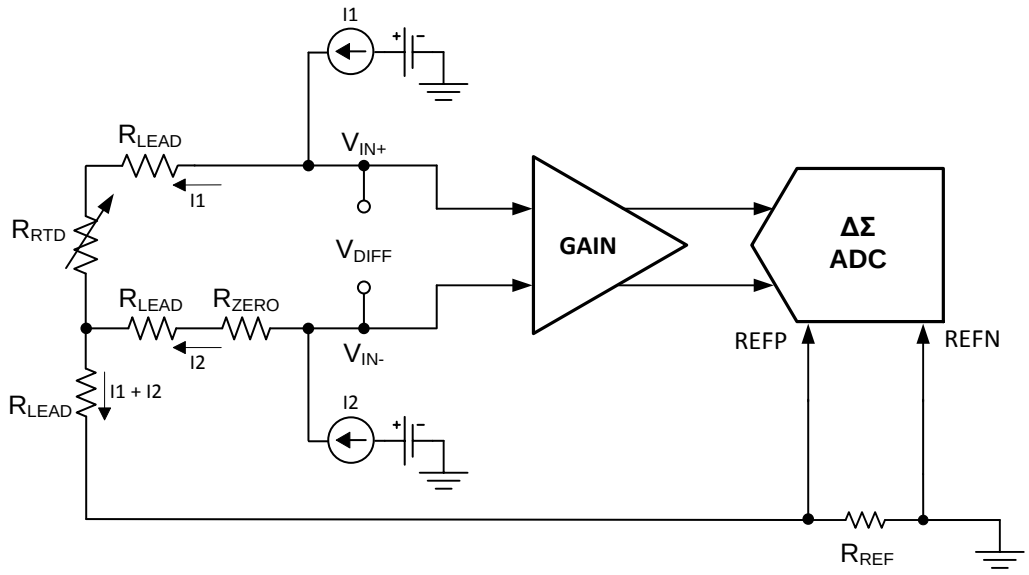

Figure 27. 3-Wire RTD Lead Resistances Canceled by Excitation Currents

$$I1 = I2 = I \quad (27)$$

$$V_{IN+} = I \times (R_{LEAD} + R_{RTD}) + 2I \times (R_{LEAD} + R_{REF})$$
$$V_{IN+} = 3I \times R_{LEAD} + 2I \times R_{REF} + I \times R_{RTD} \quad (28)$$

$$V_{IN-} = I \times (R_{LEAD} + R_{ZERO}) + 2I \times (R_{LEAD} + R_{REF})$$
$$V_{IN-} = 3I \times R_{LEAD} + 2I \times R_{REF} + I \times R_{ZERO} \quad (29)$$

$$V_{DIFF} = V_{IN+} - V_{IN-} = I \times (R_{RTD} - R_{ZERO}) \quad (30)$$

A.5 Additional Simulated Data

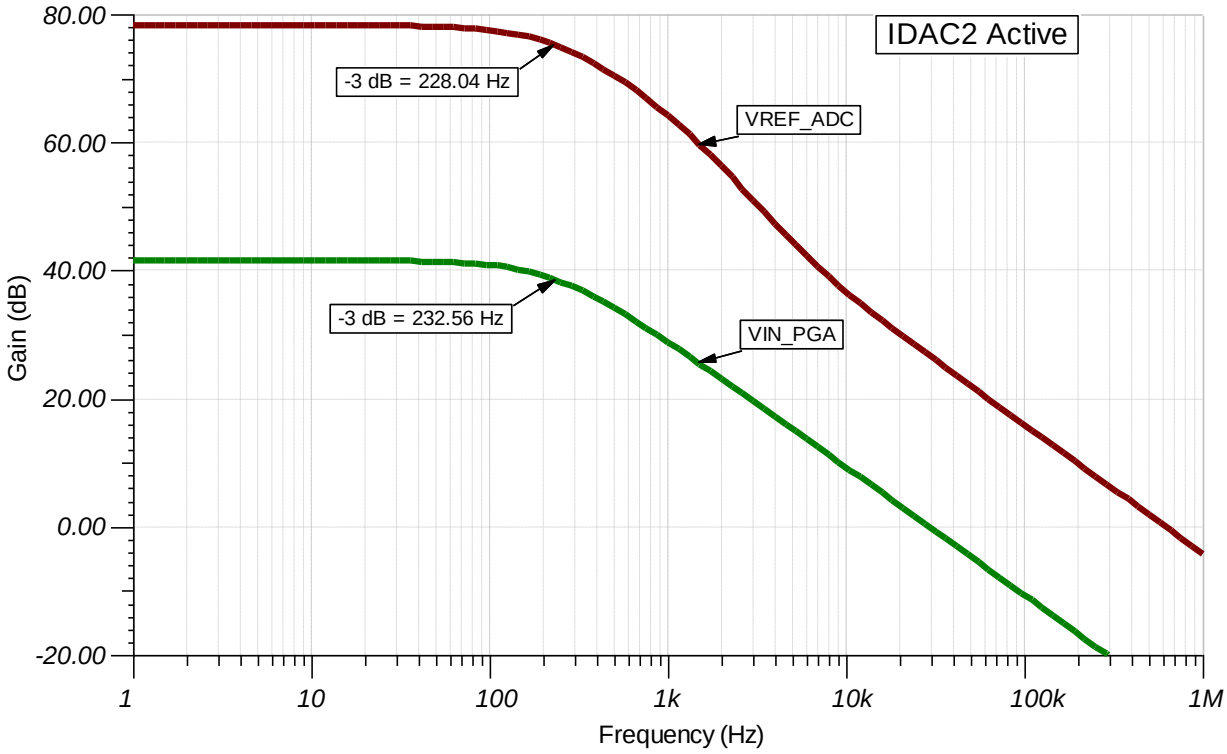

Figure 28. Input Filter Frequency Response with IDAC2 Active

A.6 ADS1247 Register Settings

Table 7 lists the complete register settings for the ADS1247 used in this design. Registers with values marked as “xx” change based on the internal calibration results specific to every ADS1247.

Table 7. ADS1247 Register Settings

Address	Name	Hex Value
00h	MUX0	0A
01h	VBIAS	00
02h	MUX1	20
03h	SYS0	72
04h	OFC0	xx
05h	OFC1	xx
06h	OFC2	xx
07h	FSC0	xx
08h	FSC1	xx
09h	FSC2	xx
0Ah	IDAC0	93
0Bh	IDAC1	30
0Ch	GPIOCFG	00
0Dh	GPIODIR	00
0Eh	GPIODAT	00

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