TI Designs

Turnkey IO-Link Sensor Transmitter

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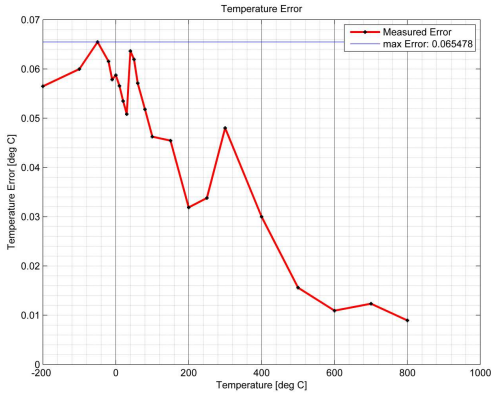
Design Resources

TIDA-00188	Tool Folder Containing Design Files
MSP430FR5738	Product Folder
ADS1220	Product Folder
SN65HVD101	Product Folder

Temperature Error Between the Mean of 1024 Measured Data Points and the PT100-Simulator's Provided Temperatures



Design Features

- IO-Link v1.1 and v1.0 Connectivity Out of the Box (TMG stack, PHY and M12 connector)
- Built-In Analog and Digital Sensors on PCB
- Simple Interfacing of Other Sensors
- Power consumption: 160 mW (in COM3 mode)
- RTD Performance: Maximum Measured Error: 0.17°C (–200°C to 850°C)
- Designed to meet with: IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5 and IEC 60255-5

Featured Applications

- Factory Automation and Process Control
- Building Automation
- Sensors and Field Transmitters
- Portable Instrumentation
- Field actuators

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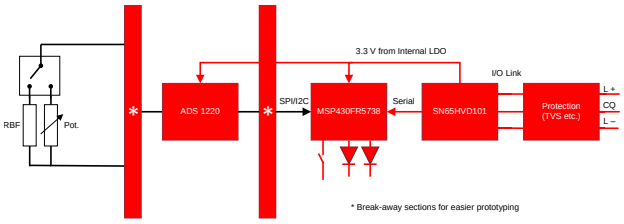
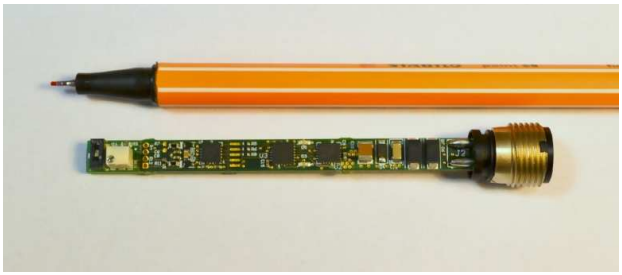
IO-Link
Breakthrough in communication





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2 IO-Link Device — System Description

This design was made with the following targets:

- IO-Link communication with master functional out of the box (see Section 6 for IODD details).
- Digital and analog inputs readable by IO-Link master functional out of the box.
- Easy connection of in-house sensor to the PCB.
- Overhead of signal chain, power and computing enabling prototyping directly with the provided PCB.
- Consideration for both IO-Link certification, mechanical, ESD, and EMC constraints to enable as much as needed reuse of the provided schematics and layout files.

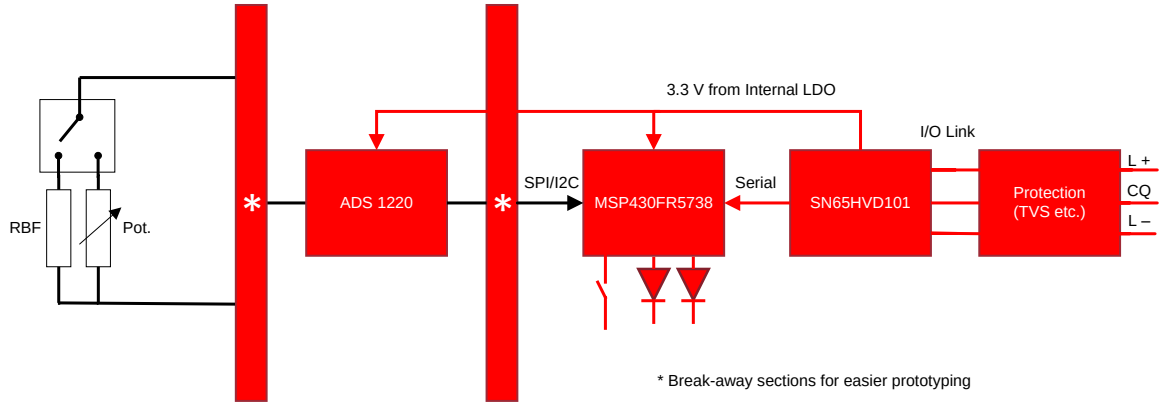


Figure 1. IO-Link Transmitter Overview (System Block Diagram)

2.1 IO-Link Interface

This design contains a totally validated IO-Link PHY and stack (see [1] and [2]). This design also contains a form factor of 6 mm width (compatible with a standard M12 connector). With all three components, this design aims to jump-start IO-Link devices developments.

2.2 IO-Link Sensor Inputs

The design comes with:

- Potentiometer, which the user can actuate to simulate analog input changes and see the result on its IO-Link master out of the box.
- Precision resistor to enable easy calibration (selectable through deep switch)
- Push button, which the user can actuate to simulate digital input changes and see the result on its IO-Link master out of the box.
- Connectors between the 24-Bit Analog-to-Digital Converter (ADC) (ADS1220) and the potentiometer to allow easy connection of an analog sensor.
- Headers for easy interfacing to own sensors with existing electronics.

2.3 Selected Integrated Circuits

The system is leveraging:

- **SN65HVD101**, a dedicated product which is an interface for IO-Link buses and provides full physical layer of the OSI model (PHY) support and a low-dropout regulator (LDO) to power the rest of the system.
- **MSP430FR5738** from the family devices featuring embedded Ferroelectric Random Access Memory (FRAM) nonvolatile memory which brings unique capabilities for field updates and logging
- **ADS1220**, which offers low power ADC with a serial peripheral interface (SPI) for read-back from the microcontroller (MCU).

3 Introduction to the IO-Link Interface

CAUTION

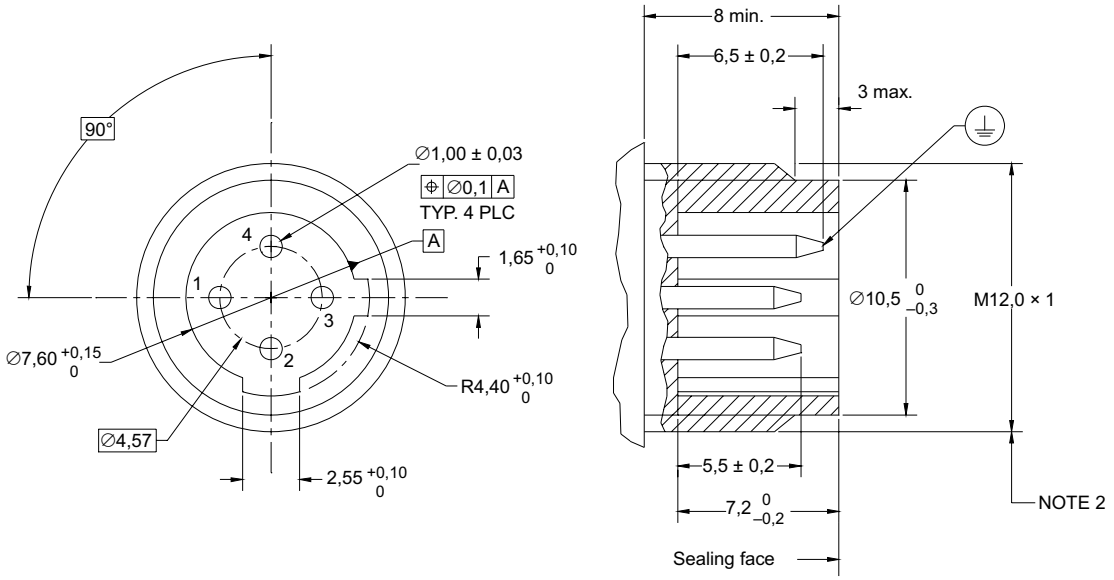
To facilitate a ground-up IO-Link device project, this section provides a quick overview of the IO-Link interface. This section should, under no condition, be considered a reference. Only the reference documents should be used after the initial phase of the project.

IO-Link [(1)] is a simple and cheap point-to-point protocol (standardized as IEC 61131-9) for the industrial automation and control applications.

Though the IO-Link clearly states that a master can have several ports, each of which can have a unique device connected to it, the rest of this document refers to a connection between the master and the device to avoid a to heavy “master-port” naming of a potentially misleading “port” denomination.

3.1 IO-Link Physical Connectors

The IO-Link connectors pin assignment is based on IEC60947-5-2 [4] with extensions specified in IO-Link Interface and System Specification v1.1.2 [1]. Figure 2 is a capture of the M12 connector selected for this project from [4].



NOTE 1 Pin identification numbering is not necessary.

NOTE 2 For a provisional period, the use of 1/2”-20UNF-2A is permissible as an alternative to M12 on a.c. proximity switches.

NOTE 3 The protective earth pin shall be omitted for class II proximity switches.

Figure 2. M12 ∅ 4-Pin Integral Connector (Defined by IEC 60947.5.2)

(1) “IO-Link™ is a trade name of the *IO-Link Community*. This information is given for the convenience of users of this international Standard and does not constitute an endorsement by IEC of the trade name holder or any of its products. Compliance to this standard does not require use of the registered logos for IO-Link™. Use of the registered logos for IO-Link™ requires permission of the *IO-Link Community*. [1]

The electrical connections are shown in Figure 3, and are extracts from [1].

Pin	Signal	Designation	Remark
1	L+	Power supply (+)	See Table 7
2	I/Q P24	NC/DI/DO (port class A) P24 (port class B)	Option 1: NC (not connected) Option 2: DI Option 3: DI, then configured DO Option 4: Extra power supply for power Devices (port cla ss B)
3	L-	Power supply (-)	See Table 7
4	C/Q	SIO/SDCI	Standard I/O mode (DI/DO) or SDCI (see Table 6 for electrical characteristics of DO).
5	NC N24	NC (port class A) N24 (port class B)	Option 1: Shall not be connected on the Master side (port class A). Option 2: Reference to the extra power supply (port class B)
NOTE M12 is always a 5 pin version on the Master side (female) .			

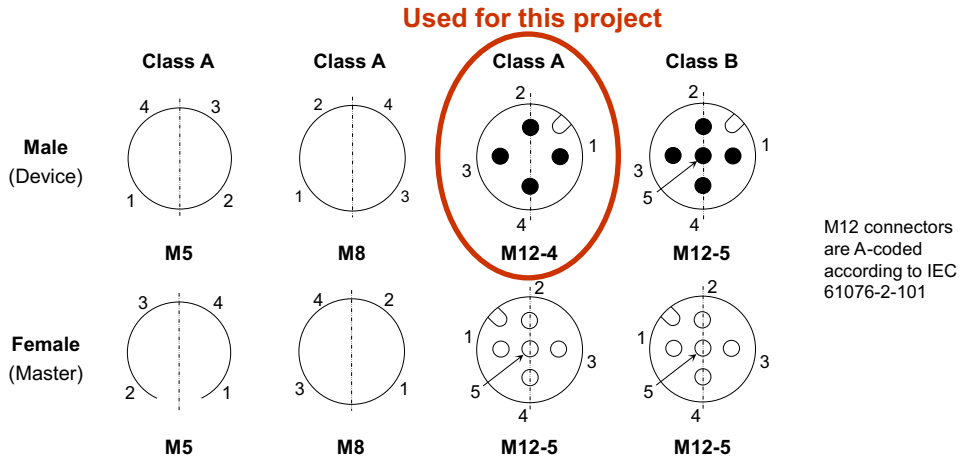


Figure 3. M12-4 Pin Layout and Assignments

It should be noted that according to [1], the current project is only using the port Class A definition.

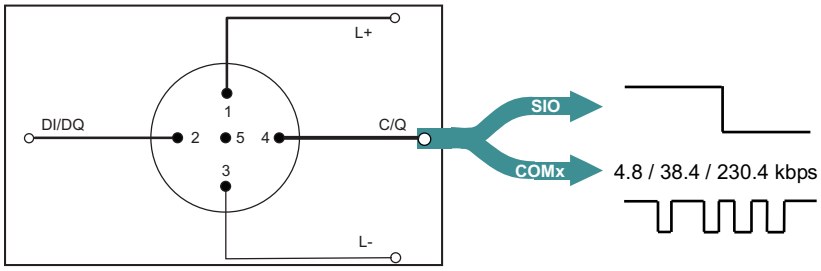
Cables are also specified by [1], with a maximum length of 20 m and associated maximum resistance and capacitance.

3.2 IO-Link Device Power

The IO-Link device (class A) can draw its power from the L+ line and is only allowed to draw up to 200 mA (see [1] for more details) from a voltage, which varies between 18 and 30 volts (see [1]). The IO-Link device must be functional less than 300 ms (see [1]) after the supply passes the 18-V threshold.

3.3 IO-Link Communication Layer

The IO-Link communication can be seen as having two modes. The first mode is a back-up, quasi-static mode which ensures backward compatibility with standard I/O (SIO) mode specified in IEC61131-2 [5]. The second mode is the newly defined dynamic mode for bi-directional communication (SDCI) defined by [1]. A good overview is provided by Figure 4 (combined extract from [1] and [5]).



Pin	Signal	Definition	Standard
1	L+	24 V	IEC 61131-2
2	I/Q	Not connected, DI, or DO	IEC 61131-2
3	L-	0 V	IEC 61131-2
4	Q	"Switching signal" DI (SIO)	IEC 61131-2
	C	"Coded switching" (COM1, COM2, COM3)	IEC 61131-9

Figure 4. SIO versus SDCI (or IEC61131-9 versus IEC61131-2)

The switch between SIO mode and SDCI is master initiated.

The master will issue a wake-up command to the device (which consists in shorting the 80 µs CQ line with at least 500 mA (IQPKHM) [1]. The device must be ready for communication in less than 500 µs (TREN).

After the wake-up request (WURQ), the master will wait for the device to be enabled for TREN [1]. The master will then try to identify the highest transmission rate supported by the device by sending a test message (M-sequence type 0). See Section 3.3.2 - Data Link Layer for details.

Following the wake-up attempt, should communication fail, the device switches back to SIO mode within a time window of 60 ms to 300 ms (TDSIO [1]).

If communication is successful, it occurs on a frame basis.

3.3.1 Physical Layer

3.3.1.1 Handshake

The master will issue a wake-up command to the device (which consists in shorting the CQ line for 80 µs with at least 500 mA (IQPKHM) [1]. The device must be ready for communication in less than 500 µs (TREN).

The short from the master will be made in such a way that the master shorts the CQ line to the opposite value driven by the device to ensure the device senses the current surge the master is driving on the CQ line (see Figure 5).

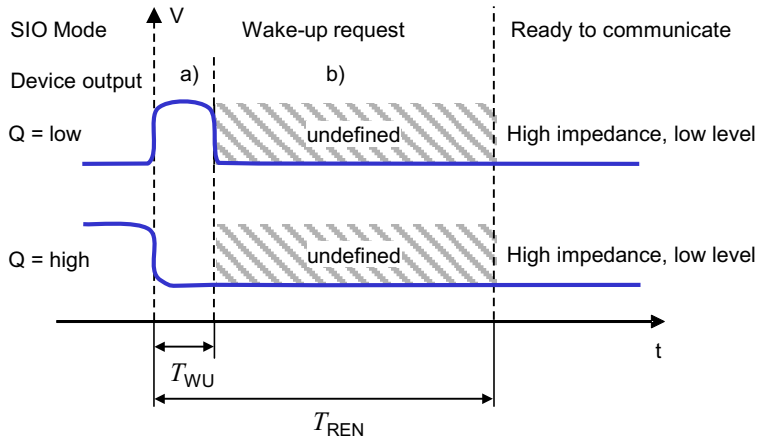


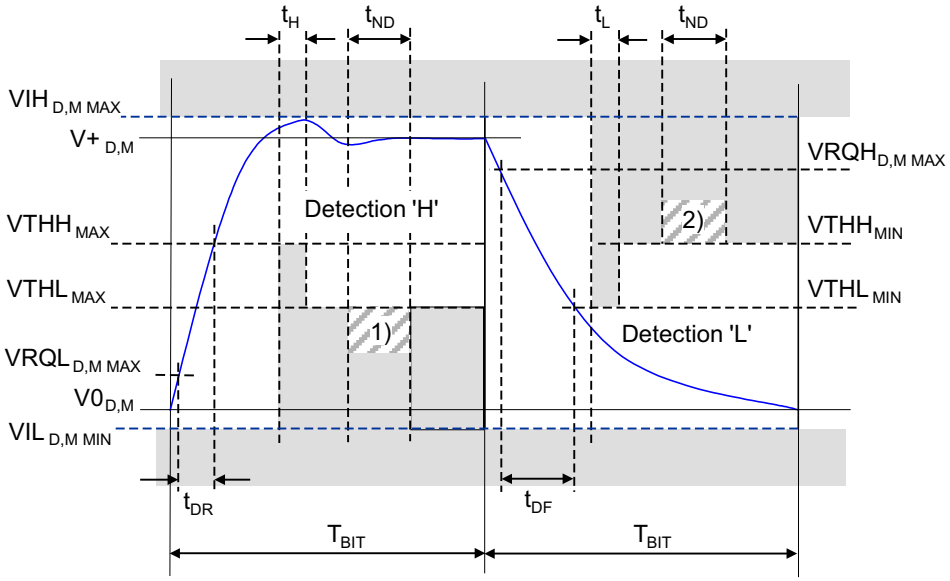
Figure 5. Wake-Up Request

3.3.1.2 Physical Layer - Modulation

Communication is done with a universal asynchronous receiver or transmitter (UART) frame consisting of 11 bits (1 start bit + 8 bit data + 1 bit parity + 1 STOP bit).

Bits are transmitted over the CQ line with a simple non-return-to-zero (NRZ) (that is, a logical '0' is 24 V between CQ and L- and logical '1' is 0 V between CQ and L–).

Bits duration are defined by the transmission rate (the highest transmission rate at which the device can detect the test message sent by the master), the eye diagrams are illustrated by Figure 6 and Figure 7.



In the figure, 1) = no detection 'L'; and 2) = no detection 'H'

Figure 6. Eye Diagram for the 'H' and 'L' Detection

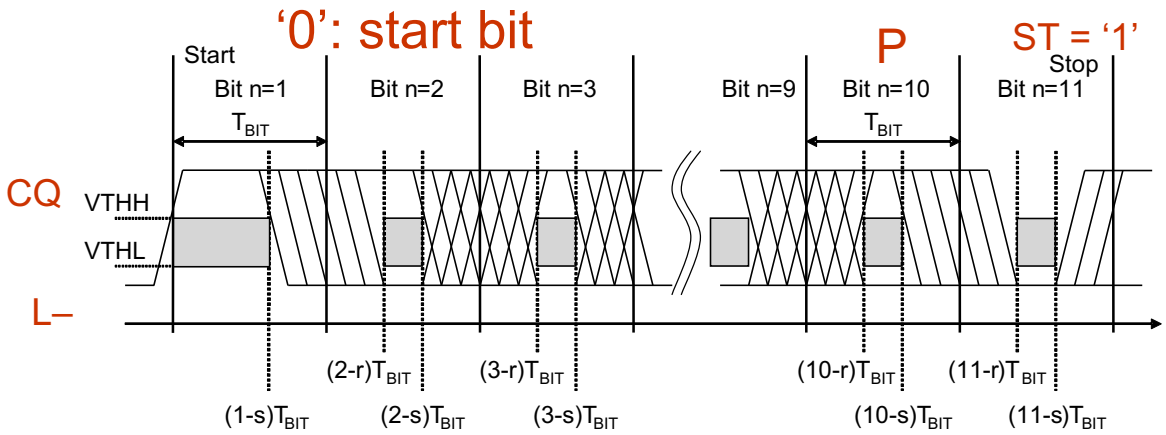


Figure 7. Eye Diagram for the Correct Detection of a UART Frame

3.3.2 Data Link Layer

3.3.2.1 Transmission Frame

Communication between a master and its associated device takes place in a fixed schedule, called the message sequence (M-sequence) time (t M-sequence) defined in [1] of which Figure 8 is an extract.

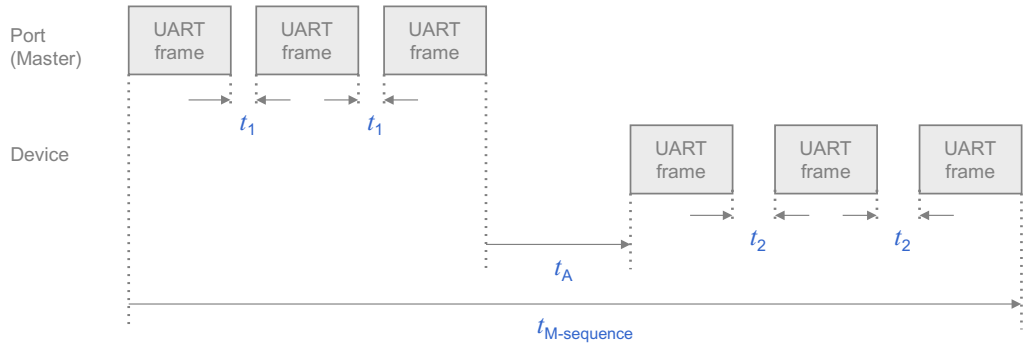


Figure 8. M-Sequence Timing

3.3.2.2 Transmission Rate Negotiation

After the WURQ, the master will send a test message with M-sequence TYPE_0 and should the device be capable of deciphering, the device should answer within tA to the master (see Figure 9 and Figure 10).

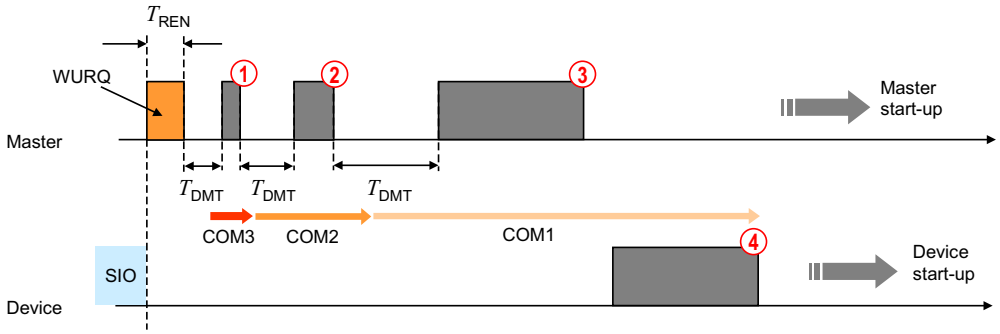


Figure 9. Example of Successful Transmission Rate Negotiation

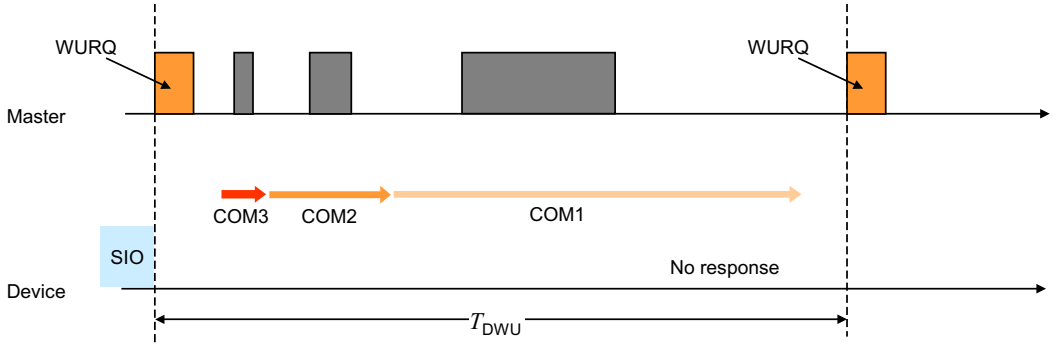


Figure 10. Example of Failed Transmission Rate Negotiation

3.3.2.3 Data Link Layer Services

Once established, the master and devices have access to services summarized in Table 1.

Table 1. Service Assignments Within Master and Device

SERVICE NAME	MASTER	DEVICE
DL_ReadParam	R	I
DL_WriteParam	R	I
DL_ISDUTransport	R	I
DL_ISDUAbort	R	I
DL_PDOutputUpdate	R	
DL_PDOutputTransport		I
DL_PDInputUpdate		R
DL_PDInputTransport	I	
DL_PDCycle	I	I
DL_SetMode	R	
DL_Mode	I	I
DL_Event	I	R
DL_EventConf	R	
DL_EventTrigger		R
DL_Control	I / R	R / I
DL_Read	R	I
DL_Write	R	I
Key (See[1][2])		
I Initiator of service		
R Receiver (responder) of service		

(1) I Initiator of a service (towards the layer above)
(2) R Receiver (responder) of a service (from the layer above)

3.3.3 Application Layer

Once established, the Master will then be able to access the structure and services of the device application layer as illustrated by Figure 11.

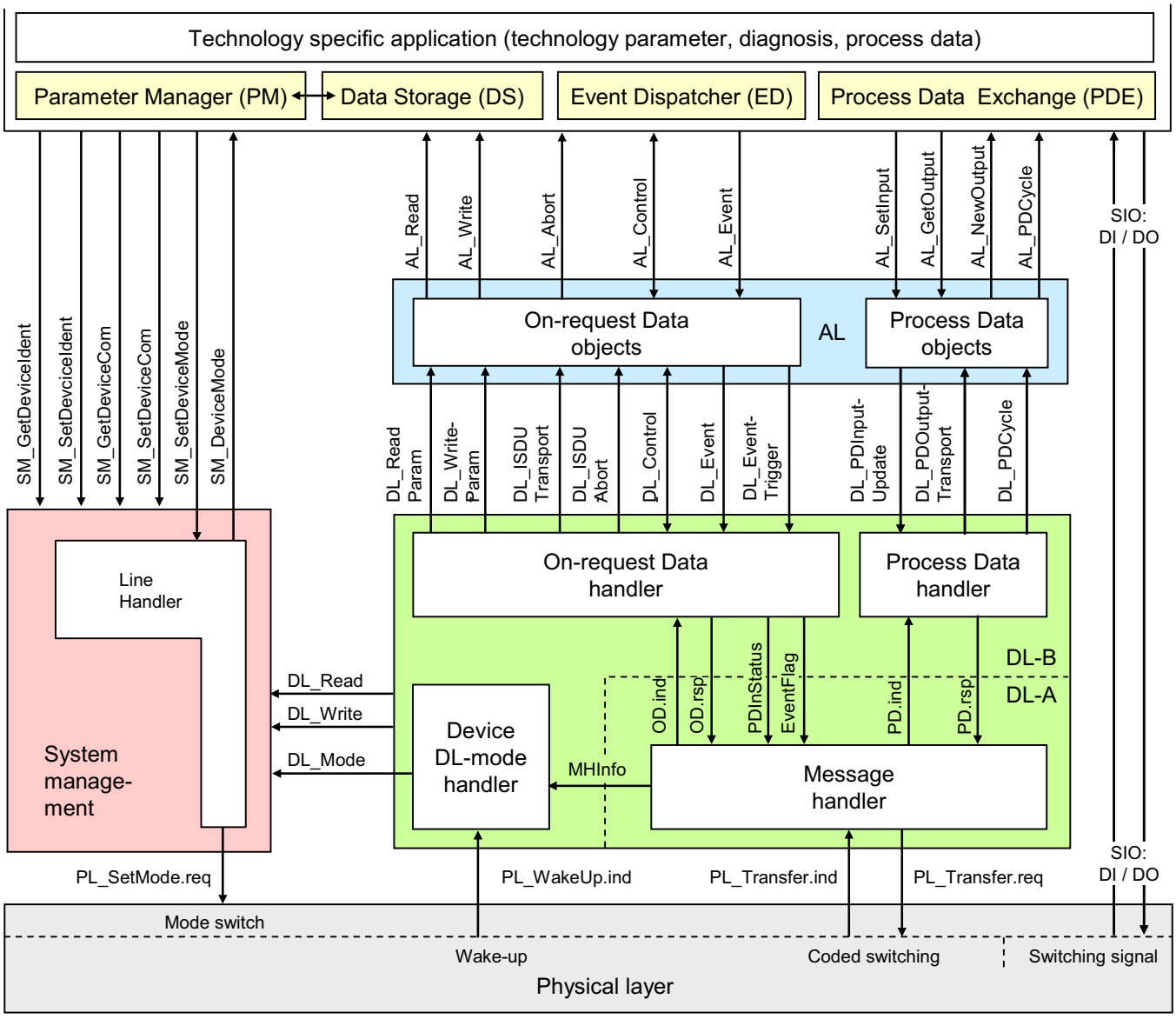


Figure 11. Structure and Services of the Device Application Layer

4 Block Diagram

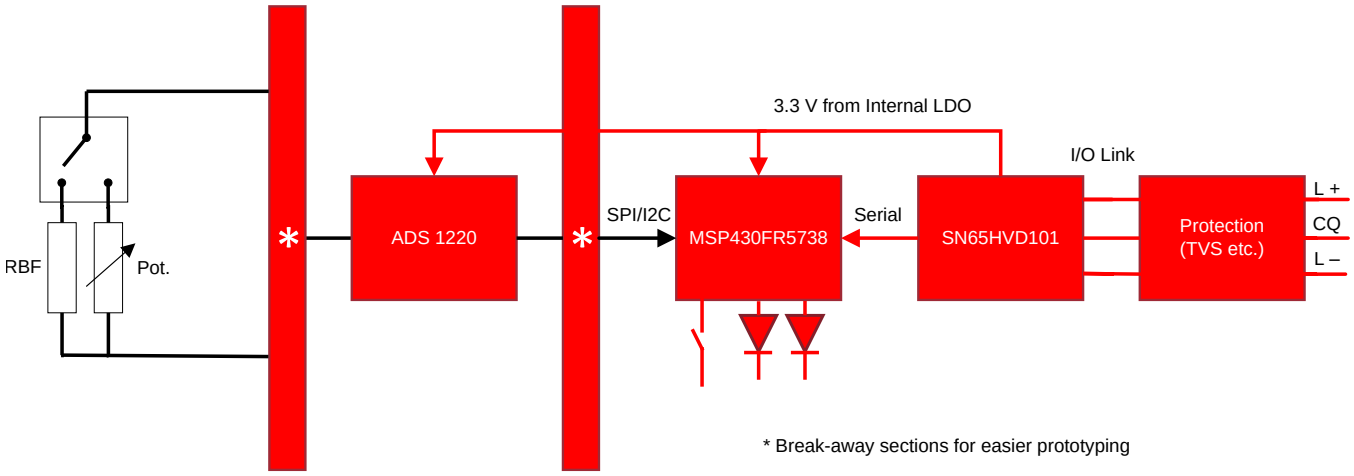


Figure 12. IO-Link Sensor Block Diagram

For more information on each of these devices, see the respective product folders at www.ti.com.

4.1 Highlighted Products

The system is leveraging the following semiconductor integrated circuits:

- **SN65HVD101** is a dedicated product which is an interface product for IO-Link buses which provides a full PHY support and LDO to power the rest of the system.
- **MSP430FR5738** from the family of devices featuring embedded FRAM nonvolatile memory which brings unique capabilities for field updates and logging.
- **ADS1220**, which offers low power ADC with SPI for read back from the MCU.

The design comes with:

- Potentiometer, which is fitted to enable easy simulation of analog sensor and read-back through IO-Link
- Precision resistor to enable easy calibration (selectable through deep switch)
- Push button, which is fitted to enable easy simulation of digital sensor and read-back through IO-Link
- Header, which is fitted to enable easy connection of smart sensor for read-back through IO-Link (SW adaptation will likely be needed)

4.2 SN65HVD101

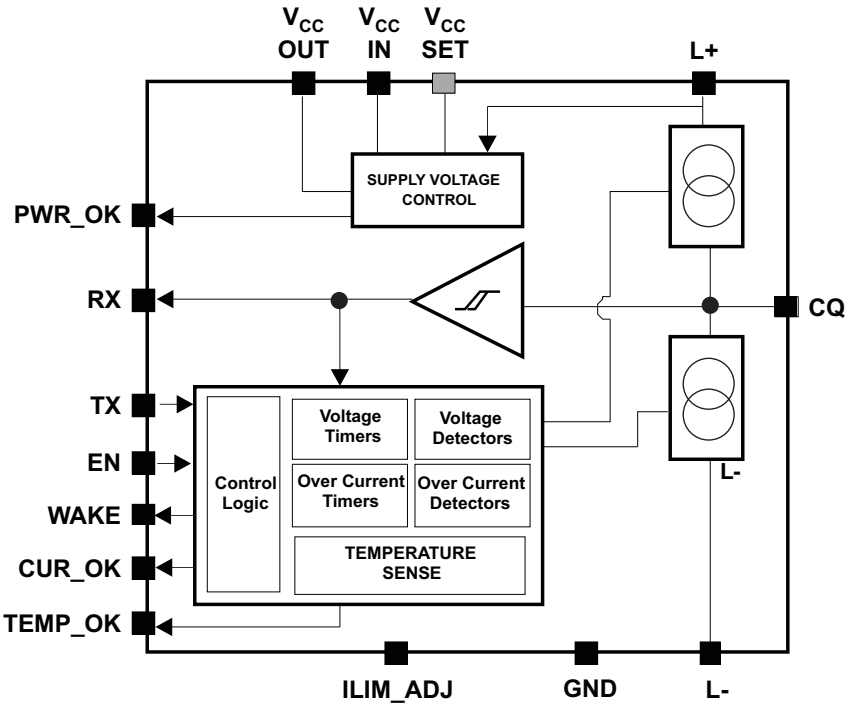


Figure 13. SN65HVD101 (IO-Link PHY for Device Nodes) Block Diagram

- Configurable CQ output: push-pull, high-side, or low-side for SIO mode
- Remote wake-up indicator
- Current limit indicator
- Power-good indicator
- Overtemperature protection
- Reverse polarity protection
- Configurable current limits
- 9-V to 36-V supply range
- Tolerant to 50-V peak line voltage
- 3.3-V and 5-V configurable integrated LDO
- 20-pin QFN package (4.0 mm × 3.5 mm)

4.3 MSP430FR5738

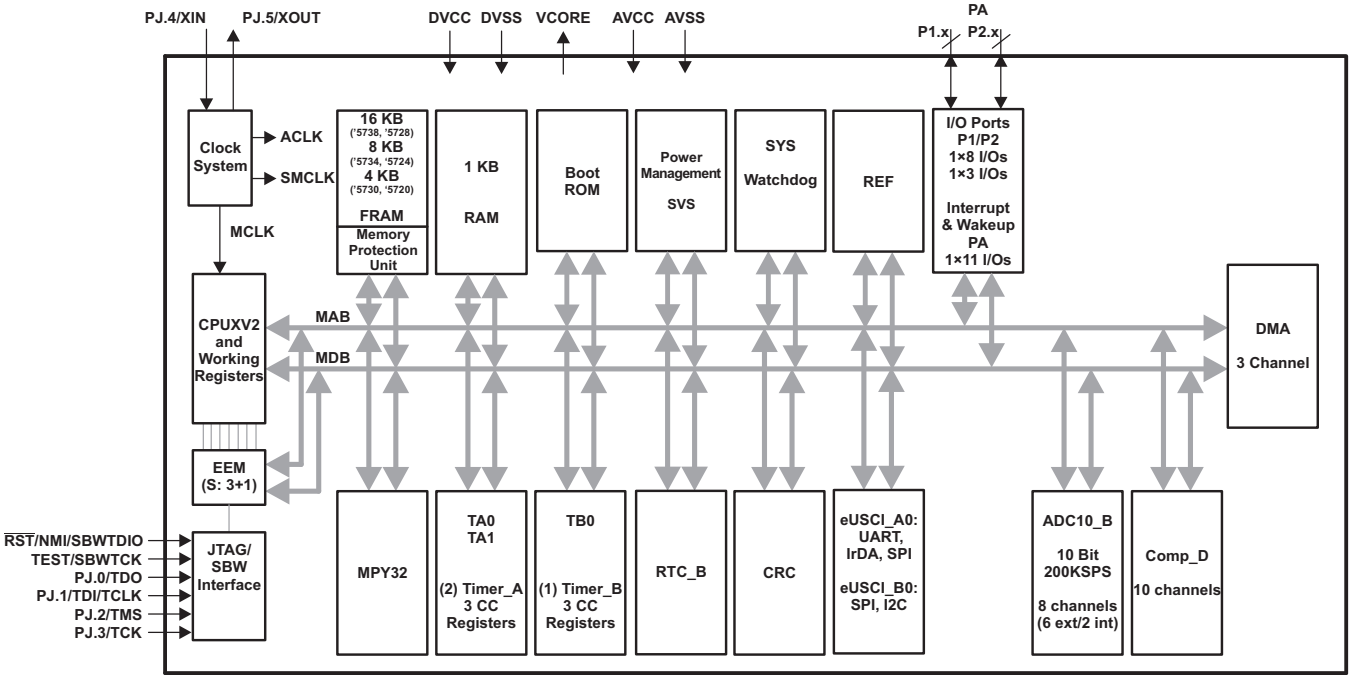


Figure 14. MSP430FR5738 Block Diagram

Embedded MCU 16-Bit RISC Architecture Up to 24-MHz Clock

- Wide supply voltage range (2 V to 3.6 V)
- Optimized ultra low power modes (81.4 µA/MHz in active and 320 nA in shutdown (LPM4.5))
- Ultra-low-power ferroelectric RAM
- 16-KB nonvolatile memory
- Ultra-low-power writes
- Fast write at 125 ns per word (16KB in 1 ms)
- Built-in error coding and correction (ECC) and MPU
- Universal memory = program + data + storage
- 10^{15} write cycle endurance

Intelligent Digital Peripherals

- 32-bit hardware multiplier (MPY)
- 3-channel internal DMA
- RTC with calendar and alarm functions
- 16-bit Cyclic redundancy checker (CRC)
- High-performance analog
- Enhanced serial communication

4.4 ADS1220

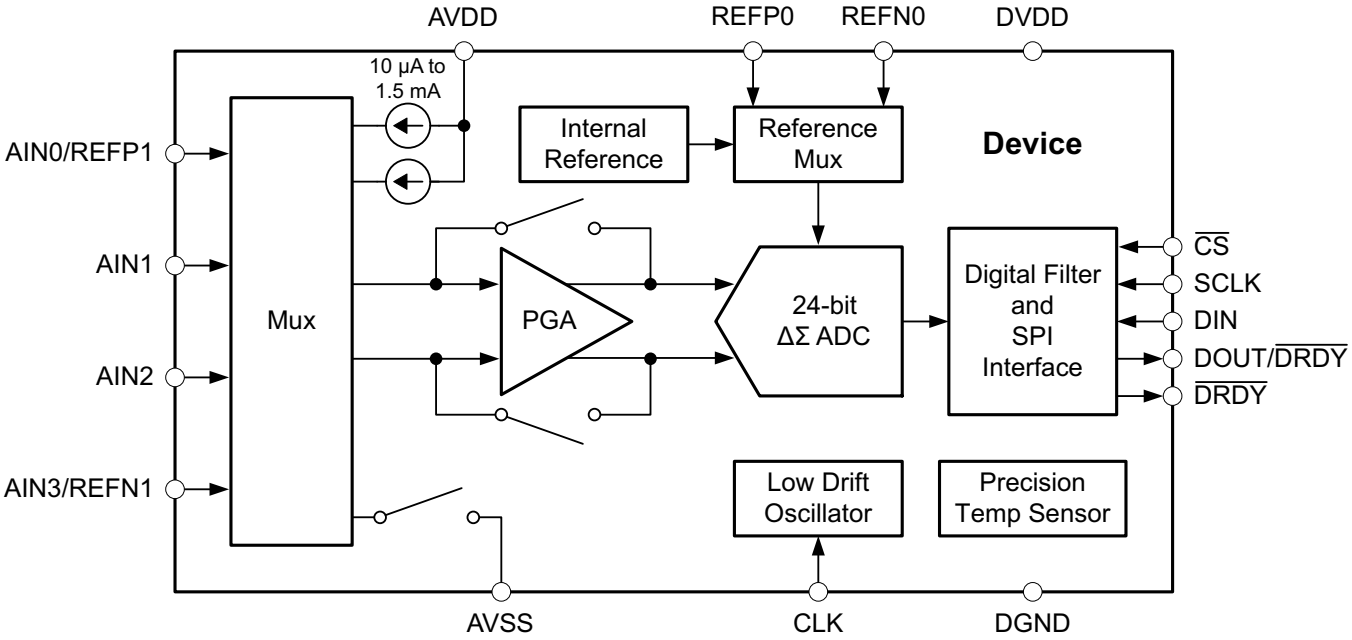


Figure 15. ADS1220 Block Diagram

- Low current consumption:
  - Duty-cycle mode: 120 µA
  - Normal mode: 415 µA
- Wide supply range: 2.3 V to 5.5 V
- Programmable gain: 1 V/V to 128 V/V
- Programmable data rates: up to 2 kSPS
- Simultaneous 50-Hz and 60-Hz rejection at 20 SPS with a single-cycle settling digital filter
- Low-noise PGA: 90 nV_{RMS} at 20 SPS
- Dual-matched programmable current-sources: 10 µA to 1500 µA
- Internal 2.048-V reference: 5 ppm/°C (typical) drift
- Internal oscillator: 2% (maximum) accuracy
- Internal temperature sensor
- Two differential or four single-ended inputs
- SPI™-compatible interface
- Package: 3.5 mm × 3.5 mm × 0.9 mm QFN

5 Circuit Design and Component Selection

5.1 PCB Area

Head transmitters have a standardized footprint defined by the connector sizes: M5, M8, M12.

This design uses the industry standard size M12 connector and enables the PCB width to fit with a pipe of a similar diameter as the connector.

The design uses the PCB divided in four different functional areas to provide an easier starting point for new projects, as well as rapid prototyping with breakaway sections.

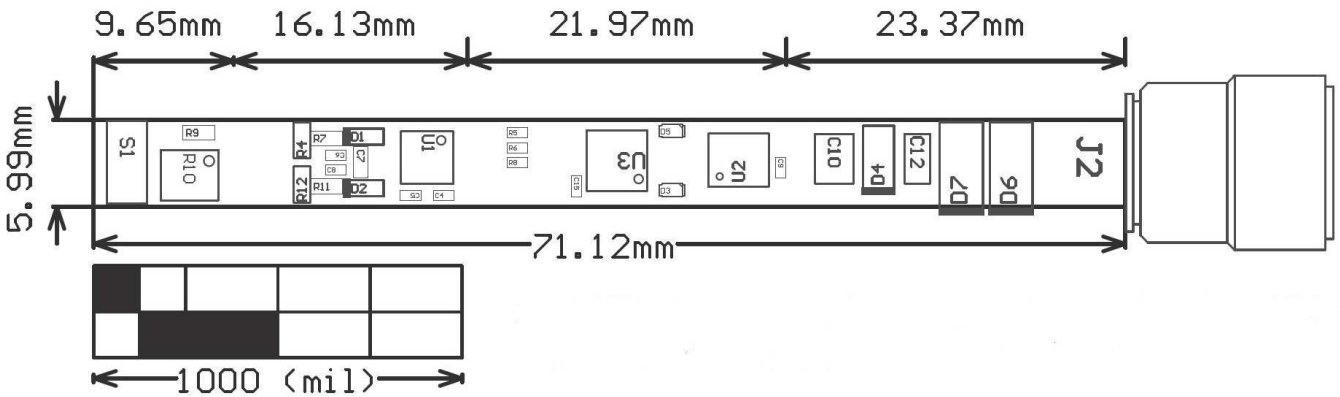


Figure 16. Full System PCB Dimensions

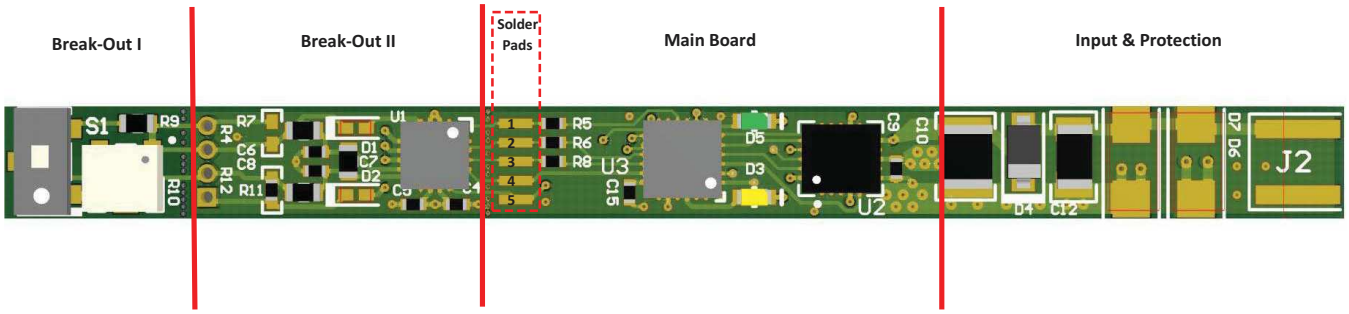


Figure 17. Functional Sections of the PCB

5.2 Power and Protection Design

The IO-Link device design is powered off the IO-Link interface by way of the L+ (24-V nominal) and L- (GND) terminals. According to the IO-Link interface and system specification [1], an IO-Link device must be able to operate with a supply voltage ranging from 18 V to 30 V.

The IO-Link PHY SN65HVD101 (U2) used in the design operates with supply voltages from 9 V to 30 V, providing a lot of margin compared to 18 to 30 V. The IO-Link PHY SN65HVD101 integrates a linear voltage regulator powering internal parts of the PHY itself. The linear voltage regular also powers the MSP430 (U3) device and the ADS1220 (U1) device. The linear regulator is set-up to provide a 3.3-V rail (VCC) on its VCCOUT-terminal by grounding the VCCSET-terminal (terminal 1 of U2).

The IO-Link PHY (U2) provides three indicator outputs (PWR_OK, CUR_OK, and TEMP_OK) which signal fault conditions of the power supply (undervoltage condition of VCC or L+). The three indicator outputs also signal overcurrent in or out of the CQ-pin. The three indicator outputs also signal over-temperature of the die by driving the respective terminals to a logic LOW state, while the outputs have a high impedance under normal operating conditions. The indicator output signals are fed into the MSP430 (U3) device.

The L+ and CQ pins of the SN65HVD101 device offer a ±40-V absolute maximum steady voltage rating, which is furthermore extended to ±50 V for transients with pulse width less than 100 µs.

The IO-Link PHY (U2) margin and the ability of the PHY to withstand even negative voltages ease the design because of the robustness of the solution against ESD and Burst and Surges as defined in the Standards IEC 61000-4-2, IEC 6100-4-4, and IEC 6100-4-5.

The design uses an additional transient protection circuitry consisting of the TVS diodes (D6, D7, D8) and bypass capacitors C10, C12 and C13 to be in compliance with Standards IEC 61000-4-2, IEC 6100-4-4, and IEC 6100-4-5.

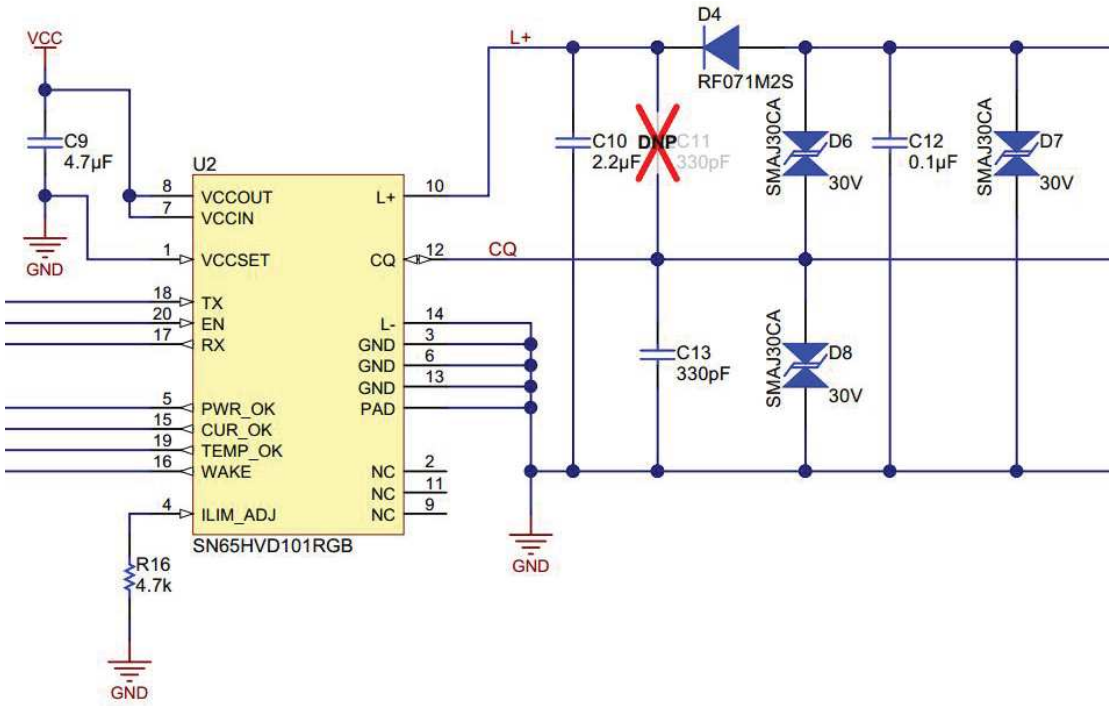


Figure 18. Power and Data Interface with Protection Circuitry

The IO-Link specification does not require a surge transient test (IEC61000-4-5) because of the limitation of maximum cable length to 20 meters. However, the use of the design in applications using digital input or output and with cable lengths exceeding 30 m requires surge testing. The design uses the assumption that the surge test is the most severe of the three transient test cases. The design also uses the assumption that the surge test is the test with the highest energy level. Therefore, special care was used in selecting the right transient voltage suppressor (TVS) as a clamping device.

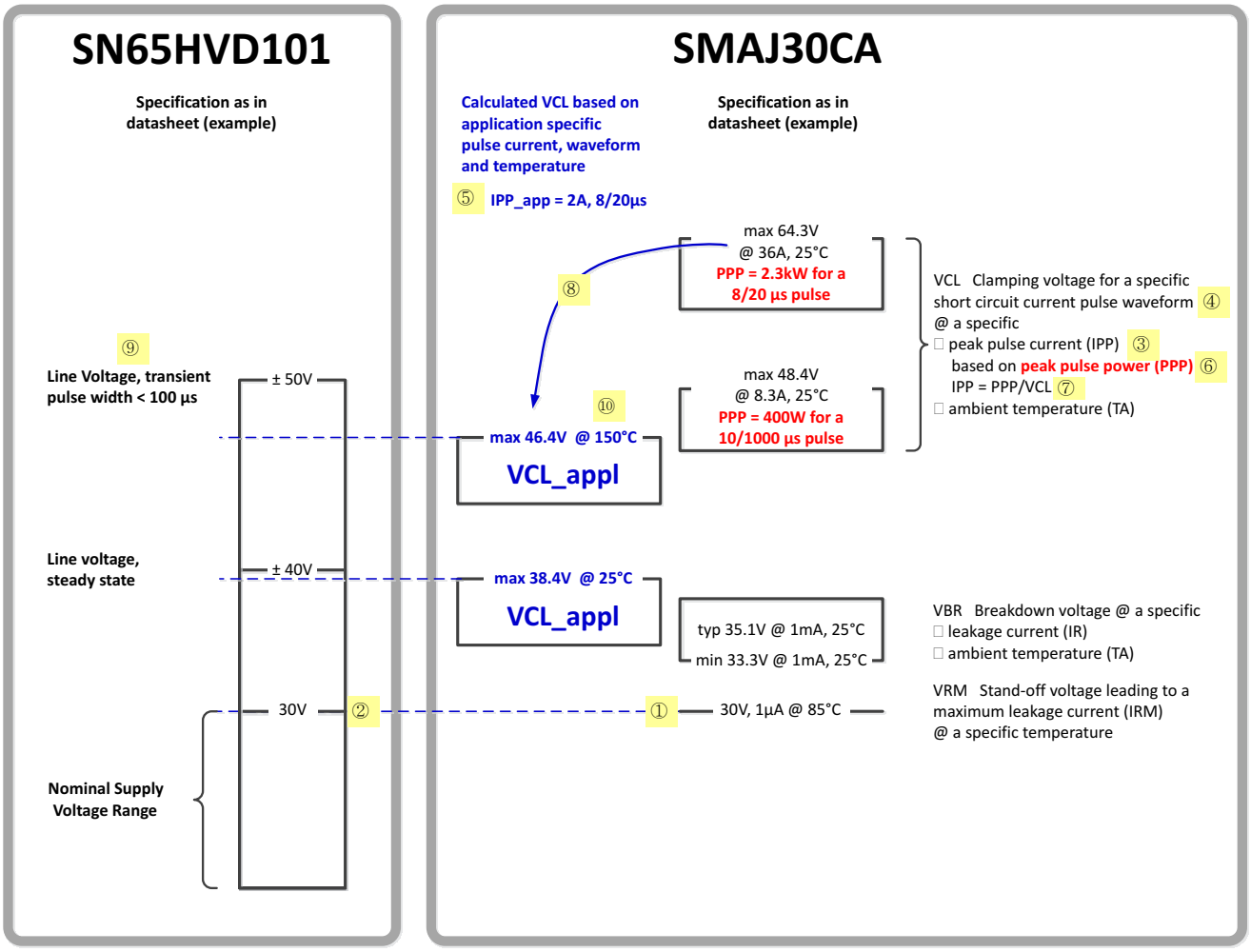


Figure 19. SN65HVD101 Device and SMAJ30CA Device

In order to choose TVS Diodes appropriately, three requirements must be satisfied:

1. VRM, the TVS' stand-off voltage ① (the voltage when the TVS does not conduct) must be greater than or equal to the transceiver's maximum signal and supply voltage of 30 V ② to prevent the TVS from conducting during normal operation.
2. IPP, the TVS' peak pulse current ③ at the short circuit pulse waveform ④ must be greater than the application-specific peak pulse current IPP_app ⑤. The open circuit voltage of the combination wave generator (surge generator) and the impedance of the generator and the coupling device determines the application-specific peak pulse current IPP_app ⑤. Most TVS' specify the IPP for a 10/1000 µs pulse only. However, the pulse used for the surge test is mostly an 8/20 µs pulse. In this case, the pulse rating curve in the datasheet can be used to derive the peak pulse power PPP ⑥ for a specific pulse width of 20 µs. IPP can then be derived ⑦ by dividing the PPP by the estimated clamping voltage VCL at this IPP level. The VCL for an 8/20 µs pulse will be much larger than the VCL for the 10/1000 µs pulse. It is recommended to contact the TVS manufacturer when estimated values are used unless there is a large margin between IPP and IPP_app.
3. When the TVS conducts and becomes low-impedance to shunt the surge current to ground, the TVS' application-specific clamping voltage VCL_appl ⑧ must be lower than the transceiver's maximum transient stand-off voltage ⑨ of ±50 V. To obtain the application specific clamping voltage, the TVS' VCL needs to be reduced according to the reduction of the TVS' IPP to the application specific IPP_app. Some data sheets provide the differential resistance for the specific pulse waveform, which helps greatly to determine the reduction of the TVS' IPP to the application specific IPP_app. If differential resistance for the specific pulse waveform is not supplied and if there is not enough margin, the TVS manufacturer should be contacted. The VBR and VCL voltages in the TVS' data sheets are often given for an ambient temperature of 25°C only. Because those voltages usually have a positive temperature coefficient, the VCL values need to be corrected accordingly to ensure that requirement 3. is fulfilled even at the maximum ambient temperature of the application specific case and under the conditions of multiple repetitive surges which heat up ⑩ the TVS. The temperature coefficient is given in most data sheets.

For the special case of this small size IO-Link device design, a 1.2 µs/50 µs 1 kV pulse applied by way of a 500 Ω impedance has been considered according to IEC 60255-5. The resulting peak current through the clamping device (TVS) is then roughly 1 kV / 500 Ω = 2 A . The SMAJ30CA device is a bidirectional TVS and fulfills the above mentioned requirements by clamping voltages with both polarities. The SMAJ30CA device has a stand-off voltage VRM of 30 V, a minimum breakdown voltage VBR of 33.3 V, and an application specific clamping voltage of roughly 46.3 V at the 2-A current level and at a junction temperature of 150°C.

In case of other end applications, the more severe requirements of IEC61000-4-5 (using coupling impedances of 40 Ω + 2 Ω) may be applicable. The open circuit voltage of this surge pulse has the same 1.2 µs/50 µs double exponential waveform, resulting in an 8/20 µs short circuit current shape of the combination wave generator used in this test. The reduced 40 Ω + 2 Ω coupling impedance (compared to the 500 Ω) increases the peak current at a 1 kV surge level to roughly 1 kV / 42 Ω = 23.8 A.

D4 provides an additional level of reverse polarity protection. While the SN65HVD101 device can withstand negative voltages up to –40 V (in steady state) and up to –50 V (transient) as expressed previously, the diode avoids the supply voltage bypass capacitor C10 being discharged during a negative pulse. The diode enables that the design will recover much faster from such a negative surge event.

5.3 Front-End Design

For guidance on designing the input filtering of the ADS1220 device, please refer to its data sheet [7].

5.4 Design Your Own Sensor Application

5.4.1 Hardware

5.4.1.1 Connecting Your Own Sensors to the IO-Link Demo Board

The design of the IO-Link Demo board is to either use the on-board circuit for connecting RTDs or connect your own digital sensors using the SPI/I^2C interface from the MSP430FR5738 device. The SPI/I^2C interface uses the eUSCI_B0 Module of the MSP430FR5738 device. In synchronous mode, the eUSCI_B0 connects the device to an external sensor by way of three terminals: UCB0SIMO, UCB0SOMI, and UCB0CLK. In I^2C mode, the eUSCI_B0 module provides an interface between the MSP430FR5738 device and I^2C-compatible sensors by way of two terminals: UCB0SDA and UCB0SCL. To connect other sensors, you need to break away the part of the board with the ADS1220 device (see Section 5.4.1.2). After breaking the ADS1220 board, the eUSCI_B0 terminals are available on the board for connecting digital sensors by way of SPI or I^2C.

5.4.1.2 Break-Away Board Options

Beyond the flexibility of the built-in front-end, the PCB was also designed to offer two different places where the signal chain can be interrupted, thanks to break-away sections that interface in-house designs:

Hardware Options (Break-out)

The TI Design is a complete IO-Link sensor solution with the analog front-end including a potentiometer and push button to simulate an actual sensor.

For evaluation purposes the user has two additional options by removing one or both break-out sections.

CAUTION

Please be careful breaking off the break-out sections. Due to the small form factor and small trace width, it is recommended to use a saw to remove the sections rather than breaking them away.

1. 1. Break-out I
   (a) Removes the push-button and the potentiometer
   (b) J2 can be used as the sensor interface in 2-, 3- and 4-wire mode (see Figure 20 - Analog Front-End)
2. 1. Break-out II
   (a) Removes ADS1220 and the input filtering
   (b) The user has now access to the soldering pads (see Figure 17 - Functional Sections of the PCB)
      (i) Pad 1: CS
      (ii) Pad 2: CLK
      (iii) Pad 3: SIMO
      (iv) Pad 4: SOMI
      (v) Pad 5: DRDY
      (vi) Pad 6: SW

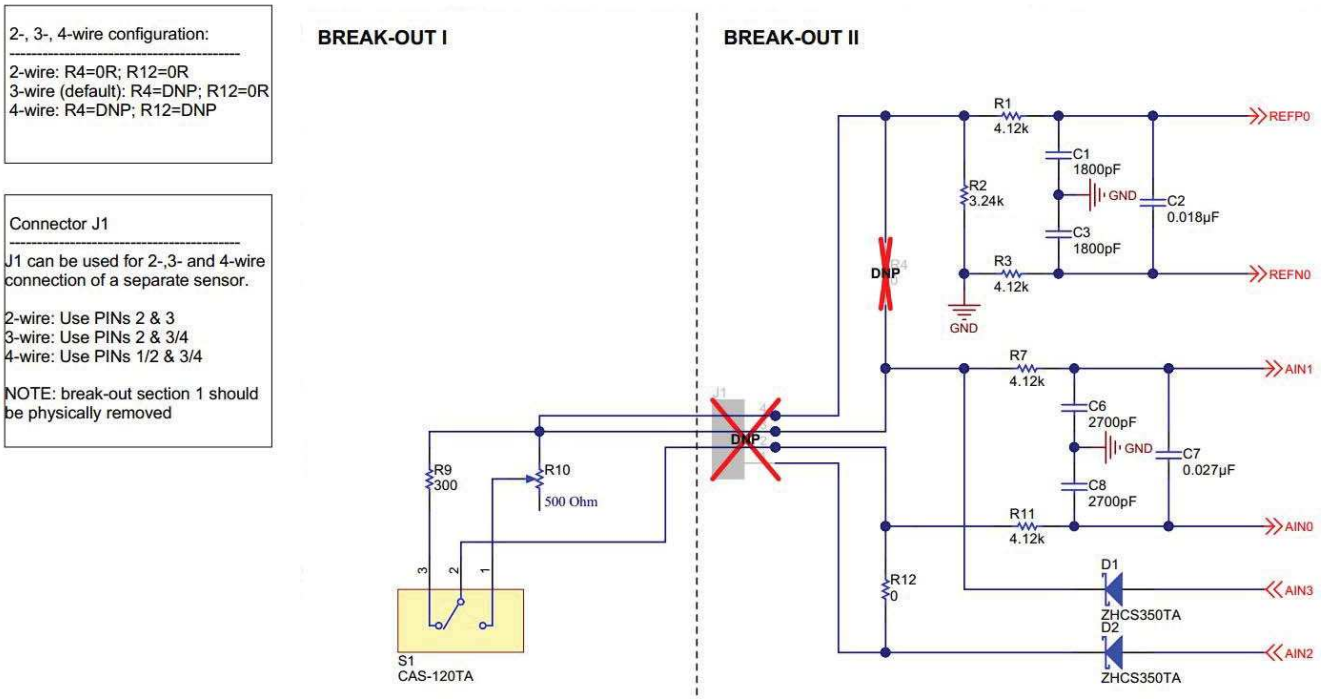


Figure 20. Analog Front-End Schematics

5.4.2 Software Update

For MSP430 Firmware updates, Code Composer Studio is recommended. Code Composer Studio™ (CCStudio) is an integrated development environment (IDE) for Texas Instruments (TI) embedded processor families. CCStudio comprises a suite of tools used to develop and debug embedded applications. It includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators, real-time operating system and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. For Programming and Debugging the MSP430FR5738 implements an Embedded Emulation Module (EEM). It is accessed and controlled through either 4-wire JTAG mode or Spy-Bi-Wire mode. On this Reference Design the Spy-Bi-Wire mode is supported only. For more details on how the features of the EEM can be used together with Code Composer Studio (CCS), see *Advanced Debugging Using the Enhanced Emulation Module,* (SLAA393). The 2-wire interface is made up of the SBWTCK (Spy-Bi-Wire test clock) and SBWTDIO (Spy-Bi-Wire test data input/output) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the RST/NMI pin of the device. For Programming and debugging purposes the SBWTCK, SBWTDIO, VCC and GND from the Debugger needs to be connected on J1.

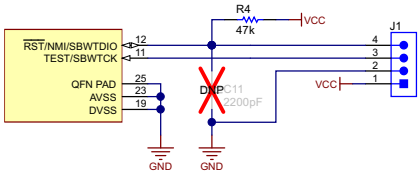


Figure 21. JTAG Connection (Pin 1 is Marked on PCB)

With the proper connections, an MSP430 Debugger Interface (such as the MSP-FET430UIF, see [13]) can be used to program and debug code on the Reference Design.

5.4.3 Power During Debugging

CAUTION

Special care should be taken during debug to avoid damages due to different power domain in conflicts (IO-Link power and debugger tools power), read this section carefully.

The SN65HVD101 integrates a linear voltage regulator, which supplies 3.3 V to the IO-Link Demo Board if a voltage in the range of 9 V to 30 V is supplied to L+. Normally the MSP430FR5738 is powered from this 3.3 V.

If this local 3.3 V supply from the SN65HVD101 is used during debug, make sure VCC_Target pin from the Debugger Interface is connected to VCC. If there is no local power and power from the Debugger Interface is used, make sure VCC_Tool pin from the Debugger Interface is connected to VCC and disconnect VCC_Target pin (see Figure 22 - Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)).

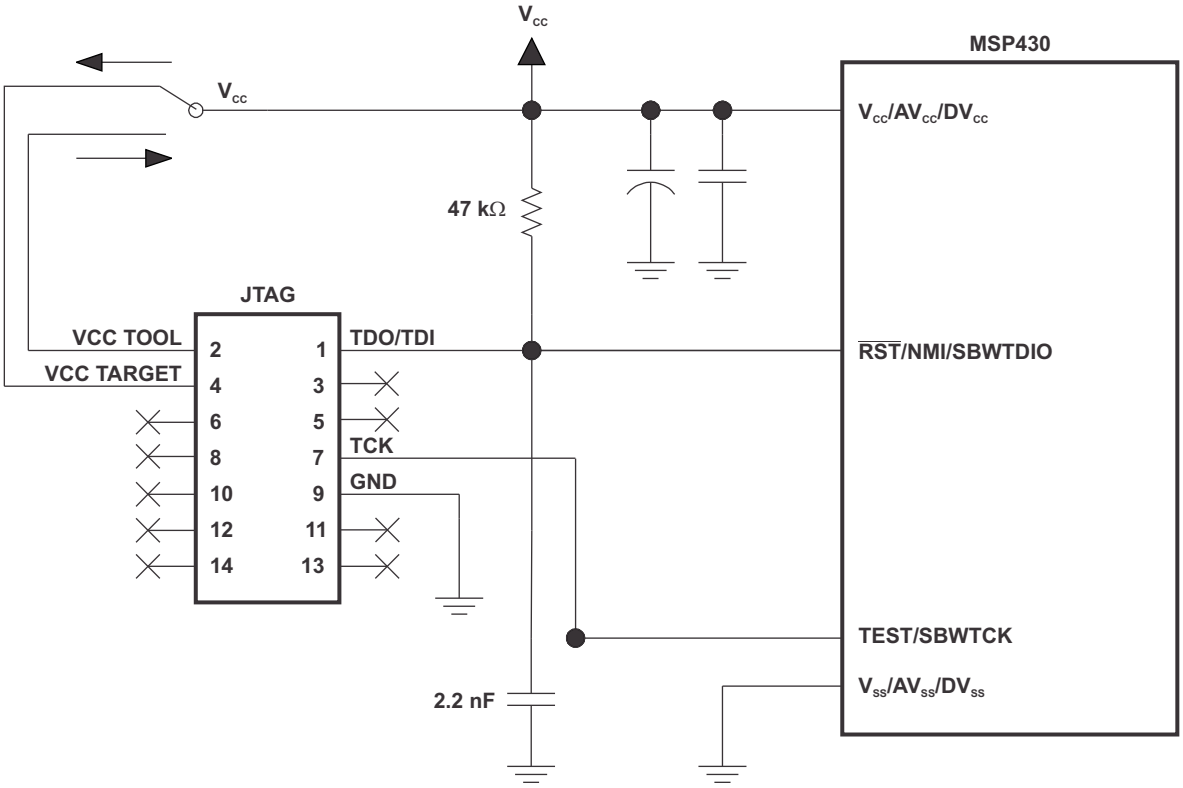


Figure 22. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire) View From Separate "Debugger Interface" Board

6 Software Description

The demo software is a complete implementation according to IO-Link specification V1.1.2 and test specification V1.1. The IO-Link demo software supports data storage, block parameterization, and device access locks. The software also shows a high-precision temperature measurement, which is simulated with a potentiometer. The button on the board can be used to teach upper and lower switch points. For more information on the IO-Link stack software contact TMG: http://www.tmgte.com/partner/texas-instruments.

7 Test Setup

7.1 Front-End Test Setup and Results

The Test Setup is meant to measure the analog performance of the front-end. Figure 23 - Front-End Test Setup shows the setup.

A PT100-Simulator was used as a sensor reference to measure the respective temperature values. The PT100-Simulator (Type 1049 from Time Electronics) has 23 fixed precision resistors representing the equivalent temperatures. The tolerances of the precision resistors' equivalent temperatures (according to the Callendar-van-Dusen formula) [13] are graphically shown in Figure 24 - Temperature Error versus Temperature of PT100 sensors (Class AA, A, B) and the PT100 simulator" together with the different PT100 sensor classes (AA, A, B). It can be seen that the precision of the Simulator is at least better than the Class A PT100 Elements and similar to Class AA. Figure 24 shows an overview of the provided Temperatures of the PT100-Simulator. It also shows the corresponding resistor values when using the Callendar-van-Dusen formula. The actual measured resistor values with precision 8.5 digit multi-meter and the resulting real temperatures are also listed in Table 2 - PT100 Simulations.

With this information the errors contributing from our reference can be minimized which allows a more accurate system performance analysis.

In order to measure the front-end from each 'temperature' 1024 captures were taken after offset and gain calibration of the ADS1220. Those values are stored inside the MSP430 memory and can be read using Code Composer Studio.

A Matlab script is being used to provide for each temperature data-set a histogram, including Mean value and Standard deviation.

Figure 25 shows the temperature error for the 23 temperature measurements. For this plot, the mean values were taken and compared to the "Equivalent Temperatures of the PT100-Simulator" listed in Table 2 - PT100 Simulations. Figure 24 compares this error to the different PT100 sensor classes.

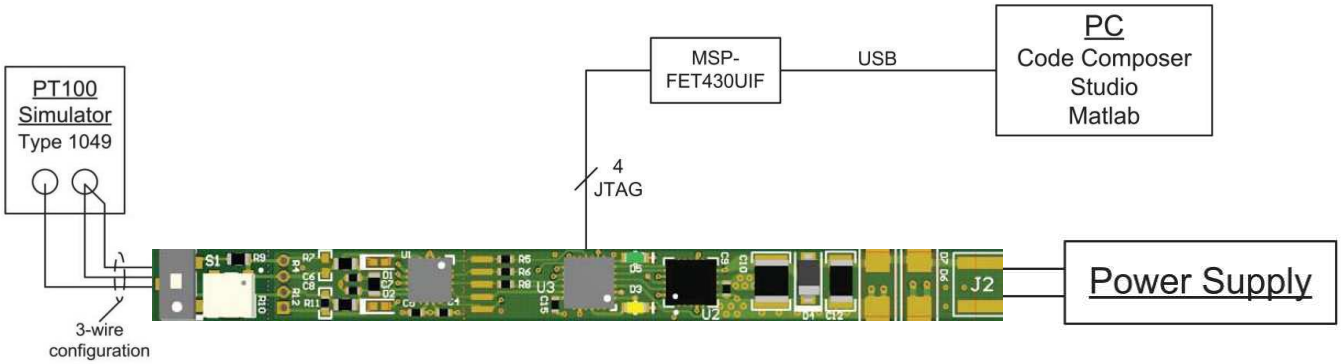


Figure 23. Front-End Test Setup

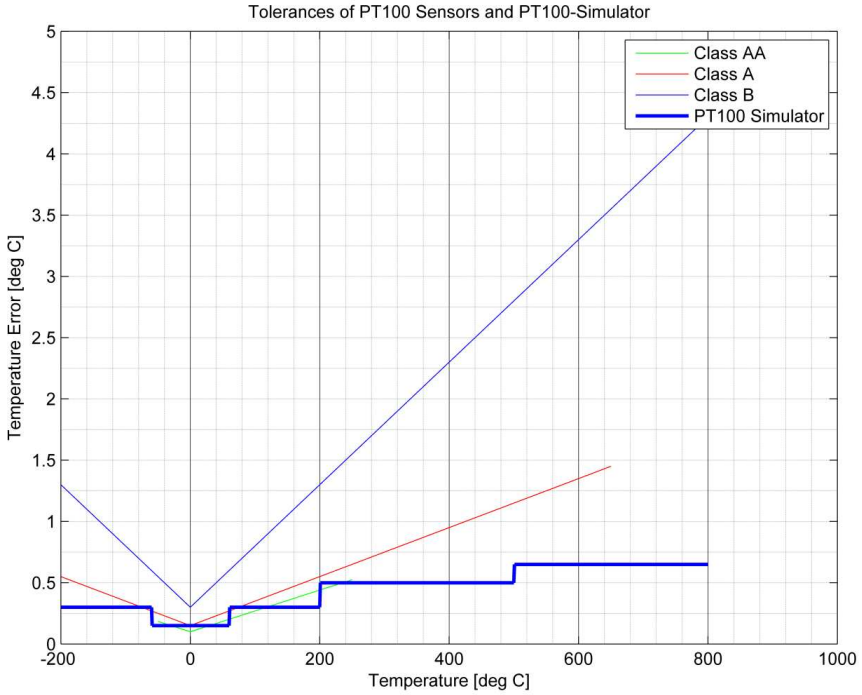


Figure 24. Temperature Error versus Temperature of PT100 Sensors (Class AA, A, B) and the PT100 Simulator

Table 2. PT100 Simulations

Temperature [°C]	Corresponding Resistor Values according to Callendar-van-Dusen formula [Ω]	Measured resistor values (8.5 digit multi-meter) [Ω]	Equivalent Temperatures of the PT100-Simulator [°C]	Temperature Delta
–200	18.520	18.583	–199.854	0.146
–100	60.256	60.309	–99.870	0.130
–50	80.306	80.352	–49.885	0.115
–20	92.160	92.166	–19.984	0.016
–10	96.086	96.099	–9.967	0.033
0	100.000	100.043	0.109	0.109
10	103.903	103.939	10.094	0.094
20	107.794	107.833	20.102	0.102
30	111.673	111.707	30.088	0.088
40	115.541	115.568	40.070	0.070
50	119.397	119.419	50.056	0.056
60	123.242	123.312	60.183	0.183
80	130.897	130.935	80.100	0.100
100	138.506	138.610	100.276	0.276
150	157.325	157.411	150.229	0.229
200	175.856	175.877	200.057	0.057
250	194.098	194.088	249.972	0.028
300	212.052	212.063	300.032	0.032
400	247.092	247.087	399.985	0.015

Table 2. PT100 Simulations (continued)

Temperature [°C]	Corresponding Resistor Values according to Callendar-van-Dusen formula [Ω]	Measured resistor values (8.5 digit multi-meter) [Ω]	Equivalent Temperatures of the PT100-Simulator [°C]	Temperature Delta
500	280.978	280.986	500.026	0.026
600	313.708	313.715	600.022	0.022
700	345.284	345.363	700.256	0.256
800	375.704	375.716	800.040	0.040

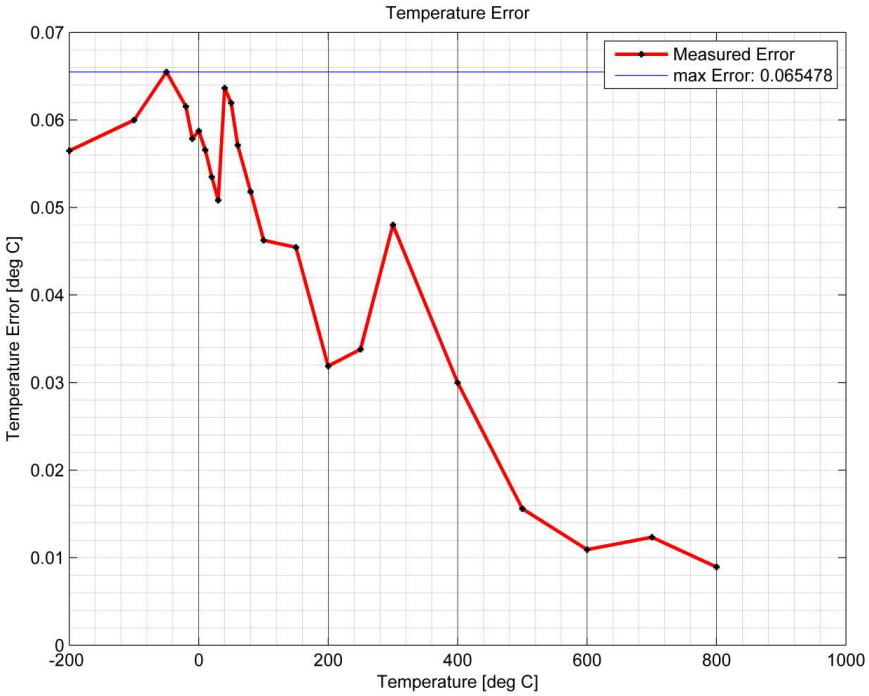


Figure 25. Temperature Error Between the Mean of 1024 Measured Data Points and the PT100-Simulator's Provided Temperatures

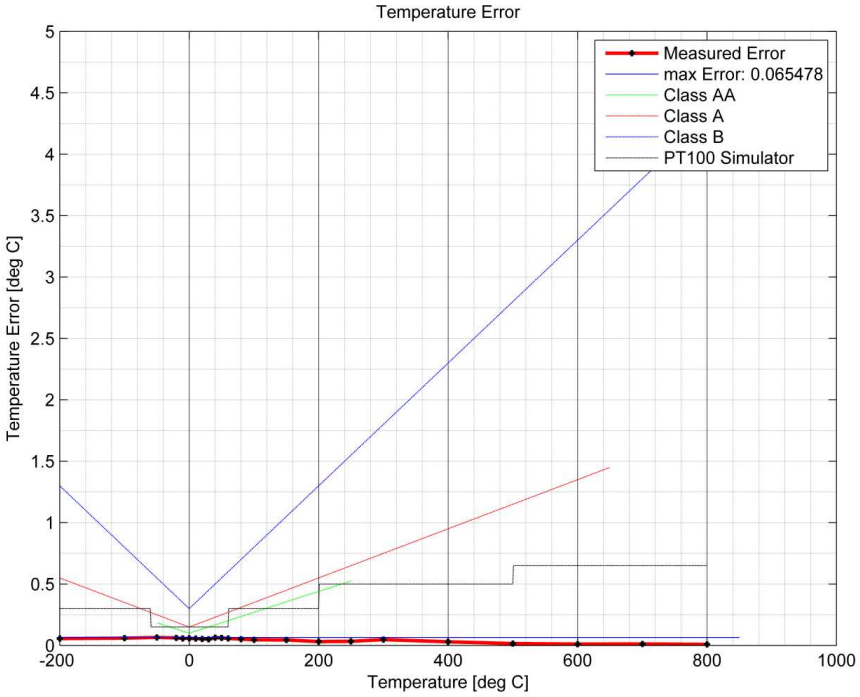


Figure 26. Temperature Error of the TI Design Compared to the Tolerance of the Different PT100 Element Classes

7.2 IO-Link Test Setup

For IO-Link test setup documentation please refer to the separate document [8].

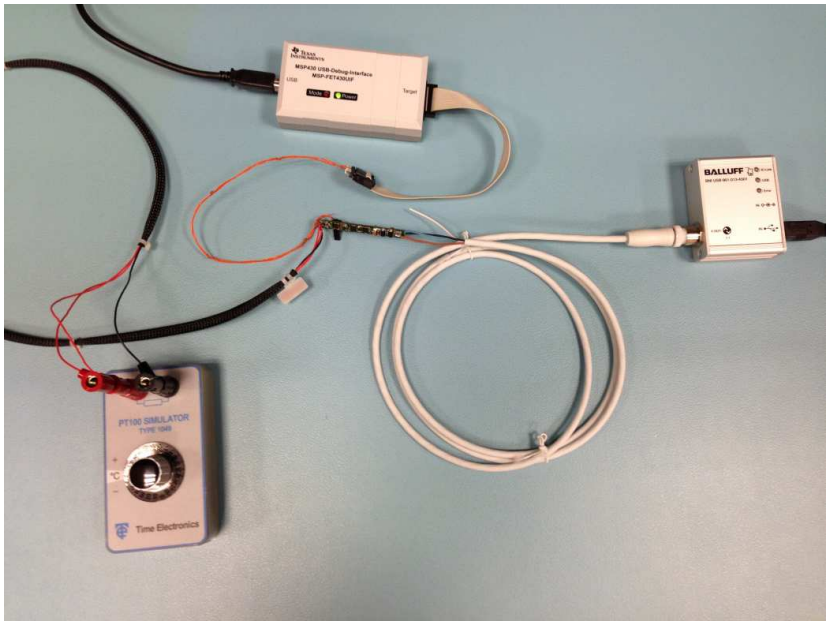


Figure 27. IO-Link Transmitter Design Test-Setup with PT100 Simulator and Balluff IO-Link Master

8 Test Results

For test results documentation please refer to the separate document [8].

8.1 IO-Link System Test Results

For test results documentation please refer to the separate [8].

9 Design Files

9.1 Schematics

To download the Schematics, see the design files at TIDA-00188.

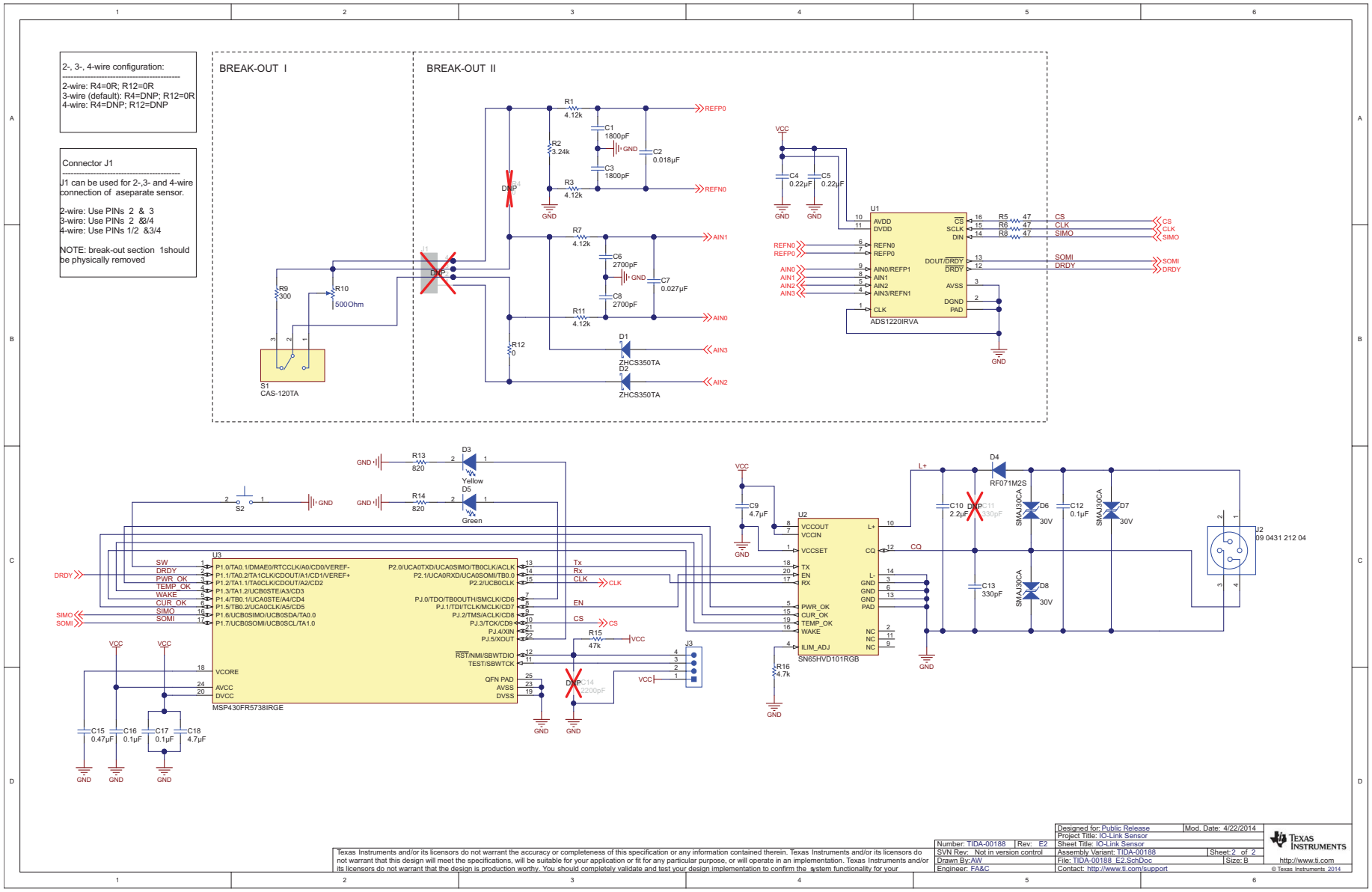


Figure 28. Full PCB Schematics

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00188. Table 3 shows the BOM for the Turnkey IO-Link Sensor Transmitter.

Table 3. BOM(1)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate	
							Part Number	Manufacturer
C1, C3	2	1800pF	CAP, CERM, 1800pF, 100V, +/-10%, X7R, 0402	0402	GRM155R72A182KA01D	MuRata		
C2	1	0.018uF	CAP, CERM, 0.018uF, 100V, +/-10%, X7R, 0603	0603	C0603C183K1RACTU	Kemet		
C4, C5	2	0.22uF	CAP, CERM, 0.22uF, 6.3V, +/-10%, X5R, 0402	0402	GRM155R60J224KE01D	MuRata		
C6, C8	2	2700pF	CAP, CERM, 2700pF, 100V, +/-10%, X7R, 0402	0402	GRM155R72A272KA01D	MuRata		
C7	1	0.027uF	CAP, CERM, 0.027uF, 100V, +/-10%, X7R, 0603	0603	C0603C273K1RACTU	Kemet		
C9, C18	2	4.7uF	CAP, CERM, 4.7uF, 6.3V, +/-20%, X5R, 0402	0402	C1005X5R0J475M050BC	TDK		
C10	1	2.2uF	CAP, CERM, 2.2uF, 100V, +/-10%, X7R, 1210	1210	GRM32ER72A225KA35L	MuRata		
C12	1	0.1uF	CAP, CERM, 0.1uF, 100V, +/-5%, X7R, 1206	1206	12061C104JAT2A	AVX		
C13	1	330pF	CAP, CERM, 330pF, 100V, +/-10%, X7R, 0402	0402	GRM155R72A331KA01D	MuRata		
C15	1	0.47uF	CAP, CERM, 0.47uF, 6.3V, +/-10%, X5R, 0402	0402	GRM155R60J474KE19D	MuRata		
C16, C17	2	0.1uF	CAP, CERM, 0.1uF, 6.3V, +/-10%, X5R, 0402	0402	C1005X5R0J104K	TDK		
D1, D2	2	40V	Diode, Schottky, 40V, 0.35A, SOD-523	SOD-523	ZHCS350TA	Diodes Inc.		
D3	1	Yellow	LED, Yellow, SMD	LED, 1.3x0.65x0.8mm	LY L29K-J1K2-26-Z	OSRAM		
D4	1	200V	Diode, Ultrafast, 200V, 1A, SOD-123	SOD-123	RF071M2S	Rohm		
D5	1	Green	LED, Green, SMD	1.7x0.65x0.8mm	LG L29K-G2J1-24-Z	OSRAM		
D6, D7, D8	3	30V	Diode, TVS, Bi, 30V, 400W, SMA	SMA	SMAJ30CA	Bourns		
J2	1		M12 Socket, 4Pos, TH	M12 Conn D12x14.3	09 0431 212 04	Binder-Connector		
J3	1		Header, 4x1, 50mil, R/A, SMT	Header, 50mil, R/A,SMT	850-10-004-40-001000	Mill-Max		
R1, R3, R7, R11	4	4.12k	RES, 4.12k ohm, 0.1%, 0.1W, 0603	0603	RG1608P-4121-B-T5	Susumu Co Ltd		
R2	1	3.24k	RES, 3.24k ohm, 0.1%, 0.333W, 1206	1206	PFC-W1206R-12-3241-B	TT Electronics/IRC		
R5, R6, R8	3	47	RES, 47 ohm, 5%, 0.063W, 0402	0402	CRCW040247R0JNED	Vishay-Dale		
R9	1	300	RES, 300 ohm, 0.1%, 0.1W, 0603	0603	RG1608P-301-B-T5	Susumu Co Ltd		
R10	1	500 Ohm	TRIMMER 500 OHM 0.125W SMD	3.52x4.16x3.94mm	3223W-1-501E	Bourns		
R12	1	0	RES, 0 ohm, 5%, 0.063W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		
R13, R14	2	820	RES, 820 ohm, 5%, 0.063W, 0402	0402	CRCW0402820RJNED	Vishay-Dale		
R15	1	47k	RES, 47k ohm, 5%, 0.063W, 0402	0402	CRCW040247K0JNED	Vishay-Dale		
R16	1	4.7k	RES, 4.7k ohm, 5%, 0.063W, 0402	0402	CRCW04024K70JNED	Vishay-Dale		
S1	1		Switch, Slide, SPDT 100mA, SMT	Switch, 5.4x2.5x2.5mm	CAS-120TA	Copal Electronics		
S2	1		Switch, Push Button SMD	2.9x2x3.9mm SMD	SKRKAEE010	Alps		
U1	1		Low-Power, Low-Noise, 24-Bit Analog-to-Digital Converter for Small Signal Sensors, RVA0016A	RVA0016A	ADS1220IRVA	Texas Instruments		None

(1) Unless otherwise noted in the Alternate Part Number and/or Alternate Manufacturer columns, all parts may be substituted with equivalents.

Table 3. BOM[(1)] (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate	
							Part Number	Manufacturer
U2	1		IO-LINK PHY for Device Nodes, RGB0020A	RGB0020A	SN65HVD101RGB	Texas Instruments		None
U3	1		24 MHz Mixed Signal Microcontroller, 1024 B SRAM and 17 GPIOs, –40 to 85°C, RGE0024G	RGE0024G	MSP430FR5738IRGE	Texas Instruments		None
C11	0	330pF	CAP, CERM, 330pF, 100V, +/-10%, X7R, 0402	0402	GRM155R72A331KA01D	MuRata		
C14	0	2200pF	CAP, CERM, 2200pF, 6.3V, +/-10%, X7R, 0402	0402	GRM155R70J222KA01D	MuRata		
J1	0		Header, 4x1, 50mil, R/A, TH	Header, 4x1, 50mil, R/A	850-10-004-20-001000	Mill-Max		
R4	0	0	RES, 0 ohm, 5%, 0.063W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		

9.3 PCB Layout and Component Placement

9.3.1 Component Placement

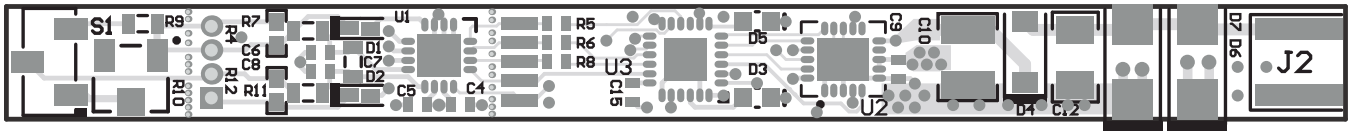


Figure 29. Top Layer View

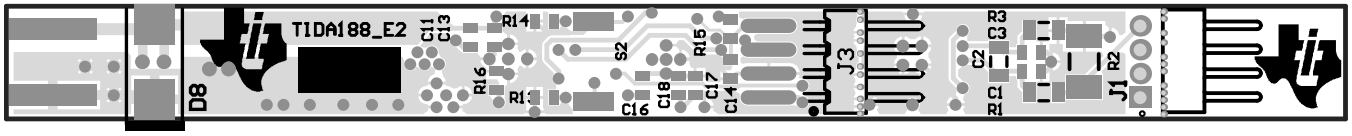


Figure 30. Bottom Layer View

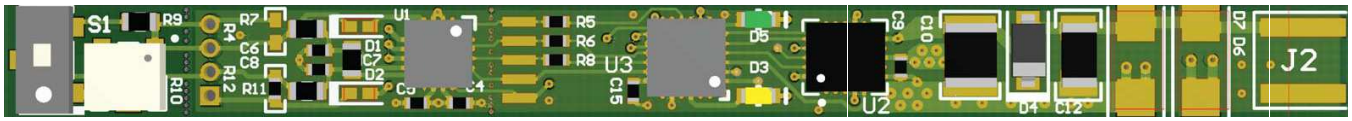


Figure 31. View of the IO-Link Transmitter Design (Top)

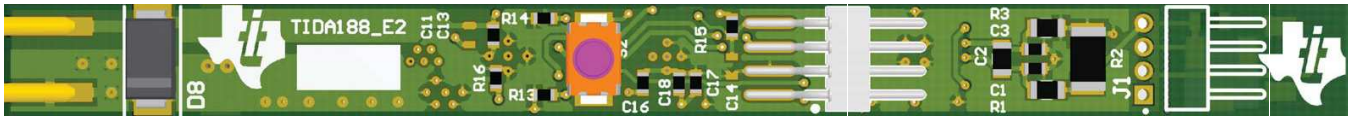


Figure 32. View of the IO-Link Transmitter Design (Bottom)

9.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00188.

9.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00188.

10 References

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2. *IO-Link Test Specification v1.1,* IO-Link Community
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4. *IEC60947-5-2:2007, Low-voltage switchgear and controlgear – Part 5-2: Control circuit devices and switching elements – Proximity switches,* IEC2007
5. *IEC 61131-2, Programmable Controllers – Part 2: Equipment Requirements and Tests,* IEC
6. *IO-Link System Description Technology and Application,* IO-Link Company Community
7. *Low-Power, Low-Noise, 24-Bit, Analog-to-Digital Converter for Small-Signal Sensors,* ADS1220 data sheet (SBAS501)
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10. *Mixed Signal Microcontroller,* MSP430FR5738 data sheet (SLAS639)
11. *IO-Link PHY for Device Nodes,* SN65HVD101 data sheet (SLLSE84)
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13. *Supplementary Information for the ITS-90 Section 1: Introduction,* BIPM document, B. Fellmuth
14. *IEC 61000-4-2, Electromagnetic Compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test*
15. *IEC 61000-4-4, Electromagnetic Compatibility (EMC) - Part 4-4: Testing and measurement techniques – Section 4: Electrical fast transient/burst immunity test*
16. *IEC 61000-4-5, Electromagnetic Compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test*
17. *IEC 60255-5, Electrical Relays - Part 5: Insulation coordination for measuring relays and protection equipment - Requirements and tests*

11 About the Author

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Revision History

Changes from Original (April 2014) to B Revision	Page
• Changed IO-Link Transmitter image.	1
• Updated Highlighted Products list.	11
• Changed Full System PCB Dimensions and Functional Sections of the PCB images.	15
• Updated Power and Protection Design section.	15
• Changed the *Software Description* section to a workable link that leads to an online request for IO-Link software information.	23
• Changed reference number 8 to the correct source for obtaining IO-Link software details (http://www.tmgte.com/partner/texas-instruments).	32

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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