TI Designs

Interface to a 5-V BiSS® Position Encoder

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Design Resources

TIDA-00175	Tool Folder Containing Design Files
SN65HVD77	Product Folder
TPS54040A	Product Folder
TPS24750	Product Folder
LMZ14201	Product Folder
TLV70025/18	Product Folder
SN74AVC8T245	Product Folder

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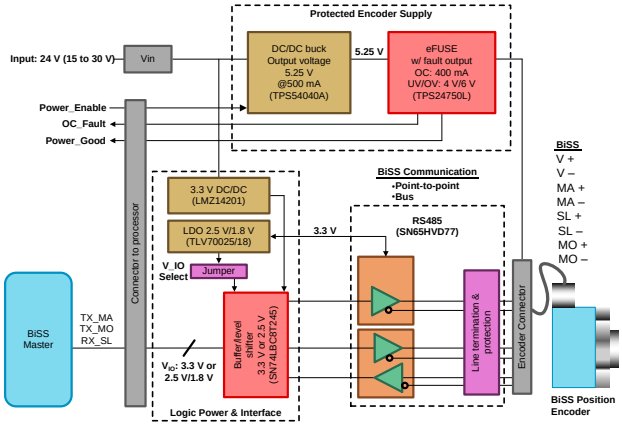
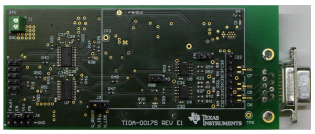
Design Features

- Meets Bidirectional Synchronous Serial Interface (BiSS Interface) Clock Frequency Recommendation (10 MHz up to 10 m and 1 MHz up to 100m), BiSS Point-to-Point, and Bus Configuration
- 3.3-V Supply Full-Duplex RS485 Transceiver with IEC-ESD
- Wide Input (15- to 30-V DC) High-Efficiency (>85%) 5.25-V and 350-mA DCDC Power Supply with Lowest Output Ripple (<20 mV_{pp}) for Encoders
- Encoder Power Supply with Inrush-Current Limit for Hot-plug And Protection against Overcurrent (400 mA), Overvoltage, and Undervoltage with Fault Feedback and Disconnect
- Option to Shutdown Encoder Power Supply at Fault or to Save Power When No Encoder Is Connected
- Configurable 3.3-V, 2.5-V, or 1.8-V I/O Interface to Processors to run BiSS Master
- Design Meets EMC Immunity Requirements for ESD, Fast Transient Burst, and Surge According to IEC61800-3

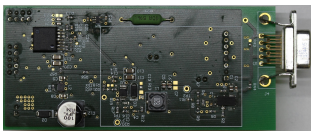
Featured Applications

- Servo Drives, Position Control, AC Drives





Top View



Bottom View

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1 System Description

1.1 TI Design Overview

This design implements a hardware interface to connect to a 5-V position encoder with a BiSS or SSI digital interface. A simplified system block diagram is shown in Figure 1, with the TI Design represented by the box in grey. The major building blocks are the protected 5-V power supply for a 5-V BiSS or SSI encoder and the RS422 or R485 full-duplex transceivers, including line termination and EMC protection. An auxiliary 3.3-V power supply and digital interface with configurable I/O voltage is provided for flexibility to connect to various processors which can implement the BiSS master protocol (B-Mode, C-Mode) or SSI.

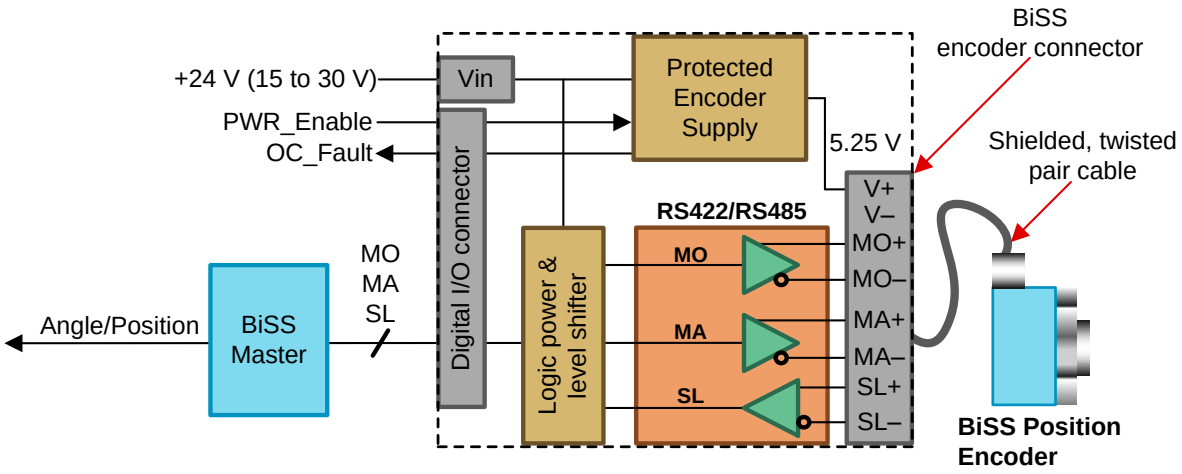

Figure 1. TIDA-00175 Simplified System Block Diagram

This design is intended to work with wide-input voltage range from 15 V to 30 V (24-V nominal) with reverse-polarity protection. The 5-V encoder power supply features inrush current limitation and overcurrent protection. The RS485 PHY is BiSS- and SSI-compliant and implements both BiSS point-to-point and bus structure. The digital interface supports 3.3 V, 2.5 V, or 1.8 V to connect the processor to run the BiSS protocol. The processor, however, is not part of this design.

The design is tested for IEC 61800-3: EMC requirements and specific test methods applicable in adjustable-speed, electrical-power drive systems.

This TI design is typically a subsystem as part of an industrial drive, for example, a servo drive. A simplified block diagram of a servo drive with an interface to a position encoder with BiSS (Bidirectional Synchronous Serial) interface is shown in Figure 2.

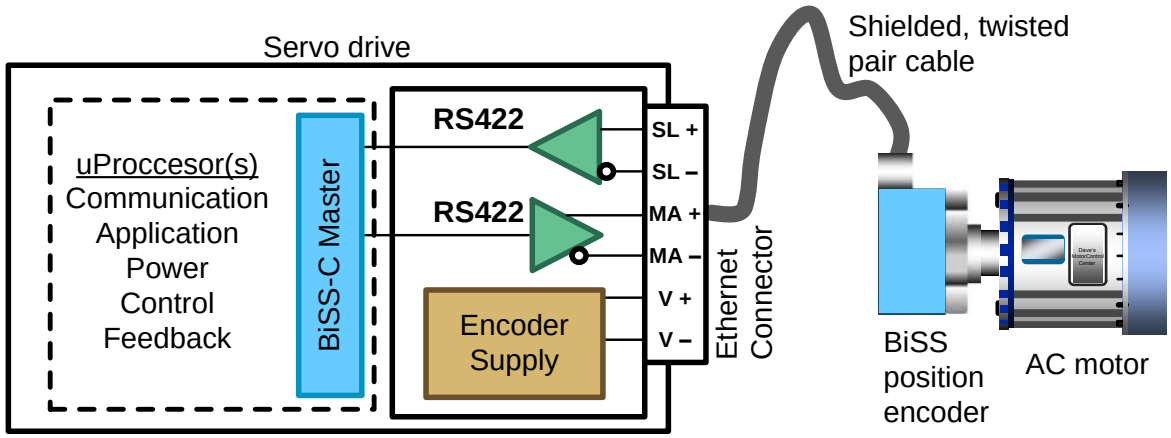

Figure 2. Industrial Servo Drive with BiSS Position Encoder Interface

1.2 BiSS Interface

The BiSS interface is an Open Source protocol introduced by iC-Haus GmbH. BiSS defines a digital bidirectional serial interface for actuators and sensors, such as rotary or position encoders. BiSS details can be found at BiSS Interface. BiSS allows serial-synchronous data communication in unidirectional mode or bidirectional mode (BiSS-C continuous mode). The BiSS interface is hardware-compatible to the serial-synchronous interface (SSI).

The BiSS protocol defines each subscriber into the following data sections: sensor data, actuator data, and register data. Each section can have various setups according to access and transmission performance, depending on the different sensor application. This protocol is referred to as the *BiSS Master* that sends and receives data from the position encoder.

The BiSS interface has two PHY options. One option is based on the TIA/EIA-422 standard and the other option uses the LVDS TIA/EIA-644 standard.

1.2.1 BiSS-C Point-to-Point

Today, this point-to-point configuration is often used with BiSS position or rotary encoders, as shown in Figure 3. In the point-to-point configuration, only one device with one or more sensors is operated on the master. The MO line is eliminated, and the SL line is routed back directly from the slave.

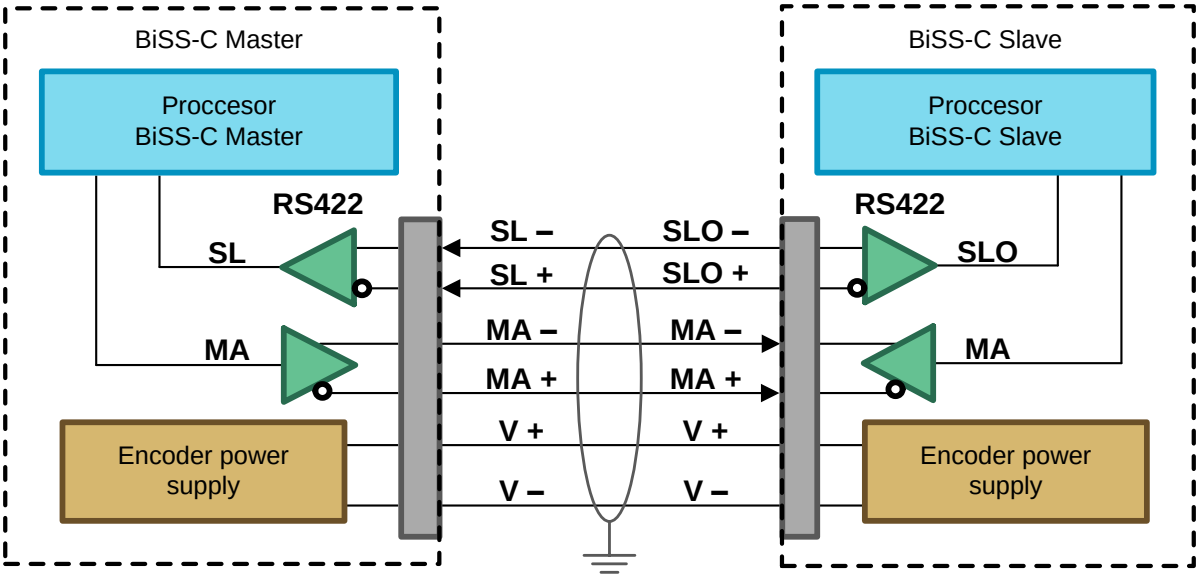

Figure 3. BiSS-C Point-to-Point Structure

1.2.1.1 RS422

The point-to-point structure is based on two signals only, MA and SL. Respectively, there are four differential signals MA+, MA- and SL+, SL- in unidirectional full-duplex mode. BiSS specifies a differential-line transmitter and receiver according to EIA standard RS422 for the differential signals MA+, MA-, SL+, and SL-.

Two lines are for the unidirectional differential data receive (SL+ and SL-) and are transmitted in full-duplex mode. Two lines are for the differential clock and data transmit signal (MA+ and MA-). Two additional wires are for the encoder power supply V+ and V-, where V- is typically the GND.

The MA-clock frequency is variable. The recommended MA-clock frequency depends on the cable length, as outlined in Figure 4. Figure 4 has been generated using Table 1 in the document *BiSS Interface: AN15: BiSS C MASTER OPERATION DETAILS (preliminary), Rev A2*, (MASTER OPERATION DETAILS).

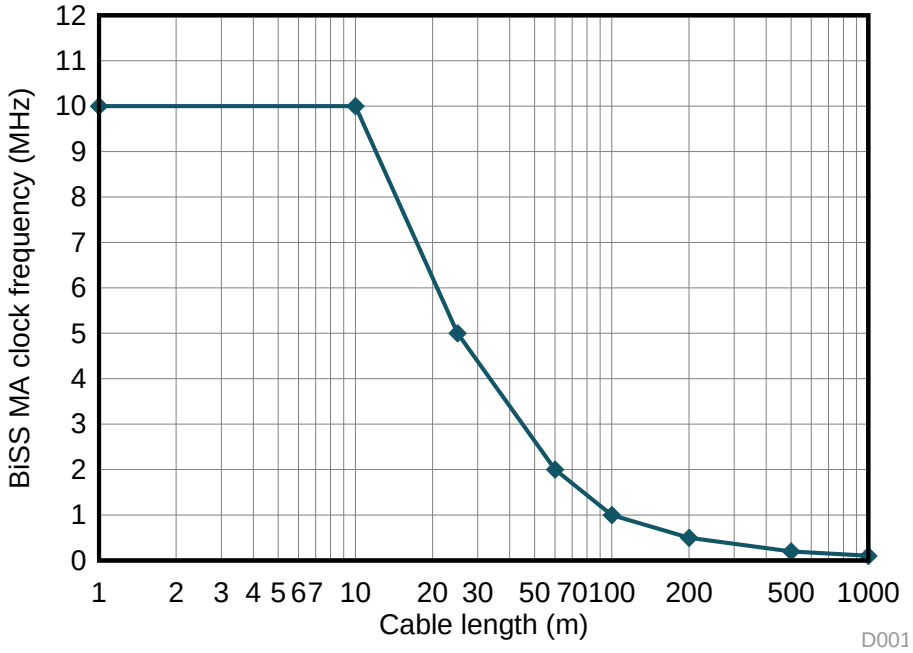

Figure 4. Recommended BiSS MA-Clock Frequencies versus Cable Length

Depending on the encoder, as well as the encoder cable, the maximum cable length or the maximum-achievable clock frequency can vary. Normally, the encoder manufacturer defines this limit in the manufacturer data sheet and recommends an appropriate cable for use with the manufacturer's encoder. The quality of the cable has an impact on the encoder's digital-communication performance and achievable reach. For example, the power wires in the encoder cable may have a thicker gauge to minimize the voltage drop for long cables. Typically, encoder vendors recommend the corresponding cables for their encoders.

For a BiSS master interface to work with several different encoders, achieving a 10-MHz, MA-clock frequency communication with a 60-m cable, would safely cover most use encoder cases. Once again, the cable quality is critical to work at 100-m or more cable lengths.

1.2.1.2 Transmission Frame

The BiSS master starts the transmission frame with the clock MA. The first rising edge at MA is used for the synchronization of the slaves. With the second rising edge of MA, the slaves set the SLO line to *0* and generate an acknowledge signal (Ack). In the point-to-point configuration, the start bit is generated by the last slave. The start bit is then passed on synchronously with the clock MA from each slave delayed by one clock pulse, while the CDS bit is either passed on by the slave or is set according to the rules of the control. The output of the slave device (SLO) is directly connected to the SL input of the master in this case.

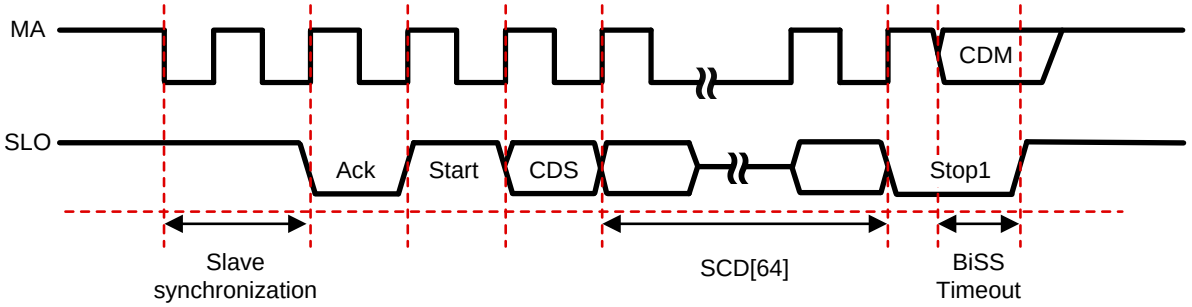

Figure 5. BiSS-C Data Frame for a Point-to-Point Setup

1.2.1.3 Line Delay Compensation

The total signal delay from the clock pulse MA to the input of the SL signal can be detected by the master and compensated respectively. To determine the line delay, the master measures the delay from the second rising MA edge to the falling edge of the Ack bit of the slave response (SL: *Ack*), as shown in Figure 6. The line delay is carried out again with each BiSS frame. Therefore, the line delay also takes aging and temperature-dependent drift effects into account. See Figure 6.

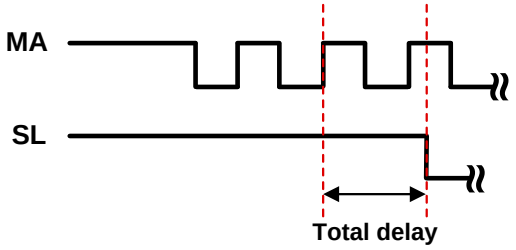

Figure 6. Line Delay Measurement

The line delay is specified to be 40-µs maximum. The line delay compensation enables accelerated communication with high data rates of typically 10 Mbps. Table 1 outlines an extract of timing requirements with respect to the signal MA.

Table 1. Timing Requirements(1)

No.	Symbol	Parameter	Condition	Min.	Max.	Unit
01	$1/T_{MA}$	Clock frequency	Signal MA	80	1)	kHz
08	$t_{LineDelay}$	Propagation delay MA → SL	Measured from the second rising MA edge to the first falling SL edge	0	40	µs
09	$t_{LineJitter}$	Delay jitter MA → SL	Within a BiSS frame	-25	25	$\%T_{MA}$
1) 10 MHz with						

(1) *BiSS Interface: PROTOCOL DESCRIPTION (C-Mode), Rev C5*, (PROTOCOL DESCRIPTION).

1.2.2 BiSS Bus Configuration

The BiSS bus configuration adds the MO signal to the MA and SL signals. Therefore, a total of 6 differential-data lines and a further two supply lines are required. A system block diagram for the BiSS bus configuration is shown in Figure 7. The BiSS bus configuration creates new options using several encoders or actuators on a single data string (such as multiple encoders per motor due to gearing or other mechanical slip that needs to be compensated in the end application).

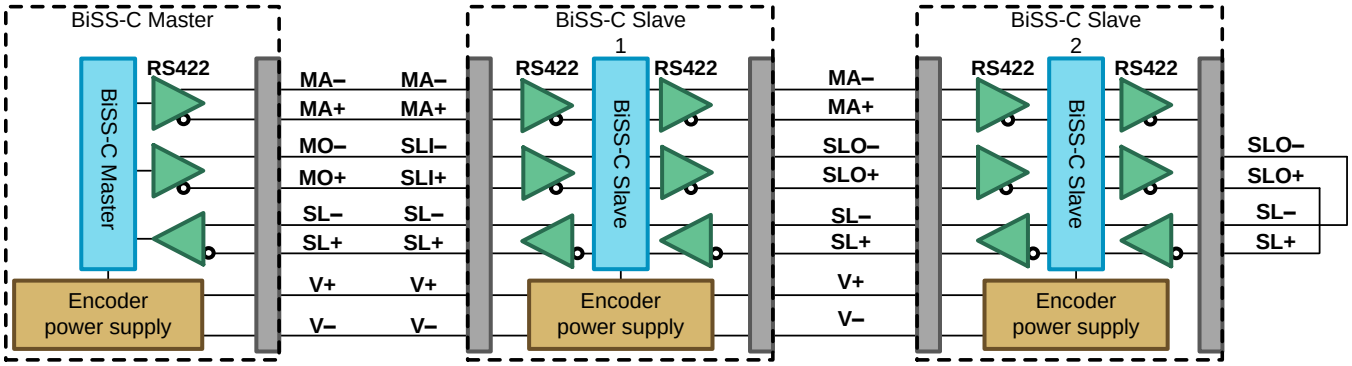

Figure 7. BiSS (C-Mode) Bus Structure

When working in bus mode, the first slave in the chain changes bits on the rising edge. Then the second slave in the chain changes bits on the following rising edge delayed by one clock, and so forth. This bits change process means that the bit change happens with one clock pulse delay per added slave into the system, as shown in Figure 8.

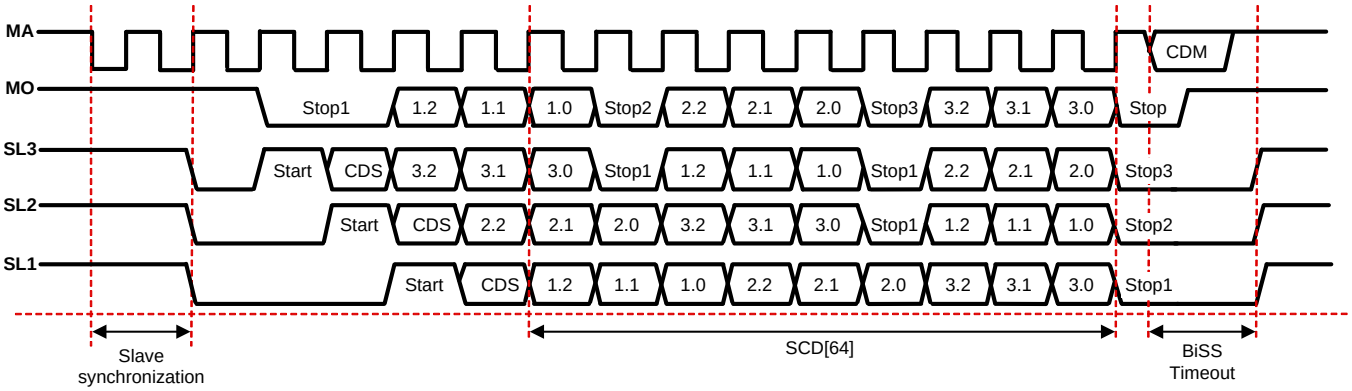

Figure 8. BiSS-C Data Frame for a Bus Structure Setup

1.3 Industry Standard Synchronous Serial Interface

The BiSS interface is hardware-compatible to SSI. With SSI, the BiSS MA signal changes to the CLOCK signal. The BiSS SL signal changes to DATA signal. SSI is a unidirectional serial data transmission over RS422. The CLOCK frequency is specified from 80 kHz to 2 MHz.

2 Design Feature Details

As outlined in Section 1, the major building blocks are the protected 5-V power supply for a 5-V BiSS or SSI encoder and the RS422 or R485 full-duplex transceivers, including line termination and EMC protection. An auxiliary 3.3-V power supply and digital interface with configurable I/O voltage is provided for flexibility to connect to various processors which can implement the BiSS master protocol (B-Mode, C-Mode) or SSI.

Features Overview

- Input: Wide input voltage range: 24 V (15 V to 30 V) with reverse polarity protection
- Digital I/O: Digital interface with 3.3 V, 2.5 V, or 1.8 V, to connect the processor to run the BiSS protocol (2)
- RS422: BiSS and SSI-compliant RS485 PHY implementing both BiSS point-to-point and bus structure
- Encoder Supply: 5-V encoder power supply with inrush limitation and overcurrent protection
- Design tested for IEC 61800-3: EMC requirements and specific test methods applicable in adjustable-speed, electrical-power drive systems

(2) The BiSS master communication protocol is not part of this TI design

2.1 RS422 and RS485 Encoder Interface

BiSS specifies the RS422 standard, which leads to a discussion of RS422 versus RS485 transceivers. RS485 was chosen for this design due to backwards compatibility and better performance.

Table 2. Summary Comparison of RS-485 and RS-422 Specifications(1)

PARAMETER	RS-422	RS-485	UNIT
Number of driver and receivers	1/10	32/32	
Maximum data rate	10	>10	Mbps
Maximum common-mode voltage	±7	-7 to 12	V
Driver differential output level	2 ≤ |VOD| ≤ 10	1.5 ≤ |VOD| ≤ 5	V
Driver load	≥ 100	≥ 60	Ω
Driver output short-circuit current limit	150 to GND	250 - to -7 or 12V	mA
Receiver input resistance	4	12	kΩ

(1) From the following document: SLLA070 Application Report, *RS-422 and RS-485 Standards Overview and System Configurations*, (SLLA070). For a detailed comparison on the two standards, please see this application report.

A SubD-9 female connector and an 8-pin header are available to connect to a BiSS position encoder based on 3.3-V supply RS485 full-duplex transceivers with 120-ohm termination. The SubD-9 female connector provides the differential signals SL+, SL-, MA+ and MA-, V+, (5.25 V), and V-(GND). The SubD-9 female connector also provides optional MO+, MO- in the case of sensors compatible to the BiSS bus configuration. The default state of the MO, MA, and SL signals is HIGH.

To minimize voltage rails, a 3.3-V supply RS485 transceiver with 5-V tolerant I/O, low-quiescent power, and IEC-IEC is proposed. Due to 3.3-V I/O, the RS485 transceiver can typically connect directly to a processor.

Table 3. Encoder Input Features

FEATURE	SPECIFICATION
Type	BiSS, SSI
PHY	RS485, full-duplex transceiver with 3.3-V supply and IEC-ESD
Termination	120-ohm
Isolation	No
BiSS Frequency	10-MHz MA-clock frequency
Connector and signals	SubD-9 female, 8-pin header: SL+, SL-, MA+, MA-, V+, (5.25 V), V-(GND), MO+, MO-
MA and MO default state	High

2.2 Logic Interface

The logic digital interface allows connection to a processor for the BiSS master as well as for control of the encoder power supply. The connector provides the BiSS signals MA, MO, and SL as well as the encoder power supply, overcurrent-fault signal Enc_OC_Fault, and the encoder power supply enable signal Enc_PWR_Enable. The design supports 3.3-V, 2.5-V, and 1.8-V I/O voltage.

2.3 Encoder Power Supply with Protection

BiSS encoders are typically available with either a 5-V or 10-V to 30-V supply rail. The power supply in this design has been configured for BiSS encoders with a 5-V supply rail at a ±10% tolerance, for example, a Baumer GBPAS BiSS-C. For BiSS encoders with supply voltages of 10 V to 30 V, the DCDC buck can be configured through passive components changes to provide, for example, 15-V output. Please refer to Section 4.2.

The 5-V, BiSS-encoder power supply is split into two functional blocks: a high-efficiency DCDC buck converter with wide input voltage range and an eFUSE to implement the protection feature, as shown in Figure 9.

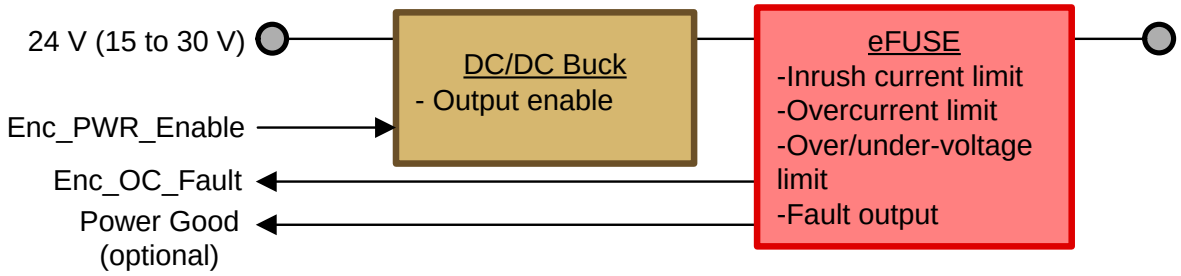

Figure 9. Block Diagram of the Encoder Power Supply with eFUSE Protection

2.3.1 DCDC Buck Converter

To maximize the cable length with 5-V supply BiSS encoders, the design specifies the default supply voltage at 5.25 V. The 5.25 V assumes a worst case tolerance of ±4% to remain below the maximum-encoder input voltage of 5.5 V at short cables. The higher voltage provides a higher voltage margin and allows for a longer cable length.

The DCDC power supply specification is outlined in Table 4. The 24-V input voltage is assumed to be derived from a standard isolated 24-V power supply on the drive. An additional feature of the power supply is an enable pin to save power when no encoder is connected or to switch off the power supply, in case of, for example, an external short.

Table 4. Part I: Encoder Power Supply Generic Specification

ENCODER POWER SUPPLY PARAMETERS	BiSS ENCODER (1)	TIDA-00175
Input voltage, nominal (range) (2)		24-V DC (17 V to 30 V)
Output voltage range	5-V DC or 10 to 30 V	5.25 V
Output voltage accuracy	< ±10% (1)	< ±4%
Output voltage, low frequency ripple	(1)	<30 mV_{pp}
Output current (nominal)	(1)	350 mA
Output voltage start-up time (0 V → Up)	(1)	<30 ms
Efficiency at 5 V,35 0mA		>85% (incl. eFUSE)
DC/DC switching frequency		700 kHz
Output enable and disable (3)		Yes

(1) Encoder vendor specific.
(2) Assuming an isolated 24-V DC voltage (SELV).
(3) Adjustable through passive component change. Option to synchronize with external clock.

2.3.2 Overcurrent Protection and Inrush-Current Limit with eFUSE

An eFUSE was added to electronically limit the inrush current during power-up or hot plugin of the encoder in case of large bulk capacity. This eFUSE was also added to disconnect the power supply from the encoder in case of a overcurrent (OC) condition, such as a short in the encoder cable, as shown in Figure 10.

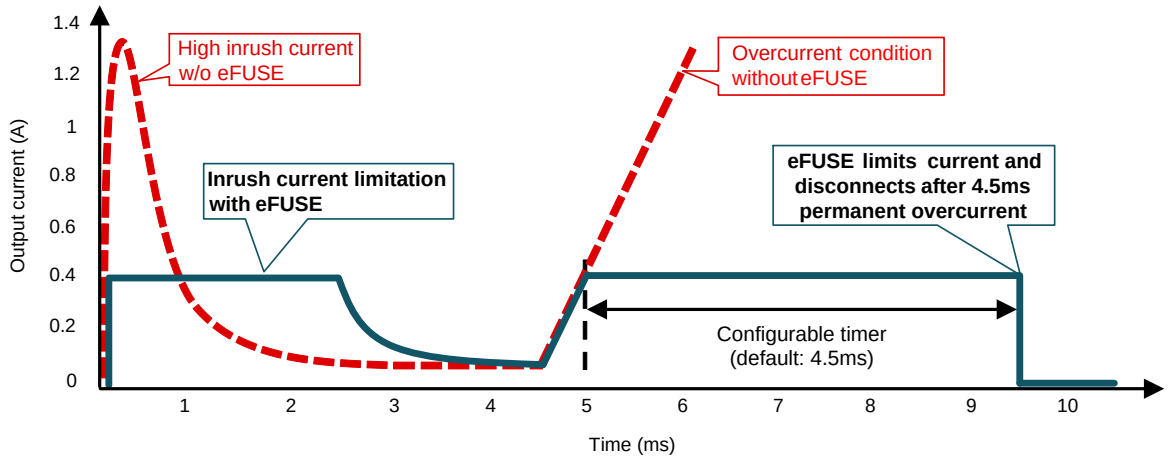

Figure 10. Inrush-Current Limitation and Overcurrent Protection through eFUSE

Further fault conditions are overvoltage (OV) and undervoltage (UV). A fault flag (Enc_OC_Fault) is made available on the digital I/O connector to allow a host processor to recognize the fault condition and optionally switch-off (disable) the power supply. An eFUSE provides the advantage of configurable limits, which are quite constant over the temperature range. The eFUSE can be re-enabled by power cycling. Therefore, it is possible to also react on temporary faults, such as a short due to a defect cable, without harming the electronics. The complete features are specified in Table 5.

Table 5. Part II: Encoder Power Supply Protection Specification

PROTECTION FEATURES: ENCODER POWER SUPPLY	TIDA-00175
Output voltage enable and disable pin	Yes
eFUSE: In-rush current limit	400 mA [0 to 85°C] (configurable)
eFUSE: Overcurrent trip limit	400 mA for more than 4.5 ms (programmable, see turn-off time below)
eFUSE: Overvoltage trip limit	6 V (configurable)
eFUSE: Undervoltage trip limit	4 V (configurable)
eFUSE (turn-off time)	4.5 ms (configurable)
eFuse: Maximum capacitive load. The capacitiy is a function of the eFUSE inrush-current limit and the eFUSE turn-off time. CMAX = ILIM x turn-off / Venc	CMAX = Q/U = 400 mA × 4.5 ms / 5.25 V = 346 uF
eFuse: Fault indication	Yes

2.3.3 EMC Immunity Requirements According to IEC61800-3

IEC618000-3 specifies the EMC requirements for adjustable-speed electrical power drive systems. The intention of this TI design is use in such drives. IEC618000-3, as shown in Table 6, specifies the minimum requirements for EMC, applicable, for example for case or cabinet and connectors.

This design is assumed to be part of a servo drive, and only the connector for the BiSS encoder can be accessed, and only shielded cables are used. According to IEC61800-3, the connector therefore falls under *Ports for process measurement and control lines, DC auxiliary supplies lower than 60 V*. Since the encoder cable can exceed 30 m, ESD, EFT, surge, and conducted RF common mode, this statement applies per Table 6 for use in the second environment.

Table 6. Extract of IEC61800-3 EMC Requirements for Second Environment

PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION
Enclosure ports	ESD	IEC61000-4-2	±4 kV CD or 8 kV AD, if CD not possible	B
	Radiated RF	IEC61000-4-3	80-1000Mhz, 10V/m, 80% AM (1kHz) 1.4-2 GHz, 3 V/m, 80% AM (1 kHz) 2 GHz to 2.7 GHz, 3 V/m, 80% AM (1 kHz)	A
Ports for control lines and DC auxiliary supplies <60 V	Fast transient burst	IEC61000-4-4	±2 kV/5 kHz, capacitive clamp	B
	Surge 1,2/50 µs, 8/20 µs	IEC61000-4-5	±1 kV. Since shielded cable >20m, direct coupling to shield (2 ohm/500 A)	B
	Conducted RF	IEC61000-4-6	0.15 MHz to 80 Mhz, 10 V/m, 80% AM (1 kHz)	A

The performance (acceptance) criterion is defined, as follows:

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module shall continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module shall continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module shall continue to operate as intended automatically, after manual restart, or power off, or power on.

3 Block Diagram

The major building blocks are the protected-encoder power supply and the RS485 transceivers including line termination and EMC protection. A SubD-9 female connector and 8-pin header are made available to connect a 5-V, BiSS position encoder. An auxiliary power supply and logic level interface with adjustable I/O voltage level was added to connect to a processor for the BiSS Master protocol.

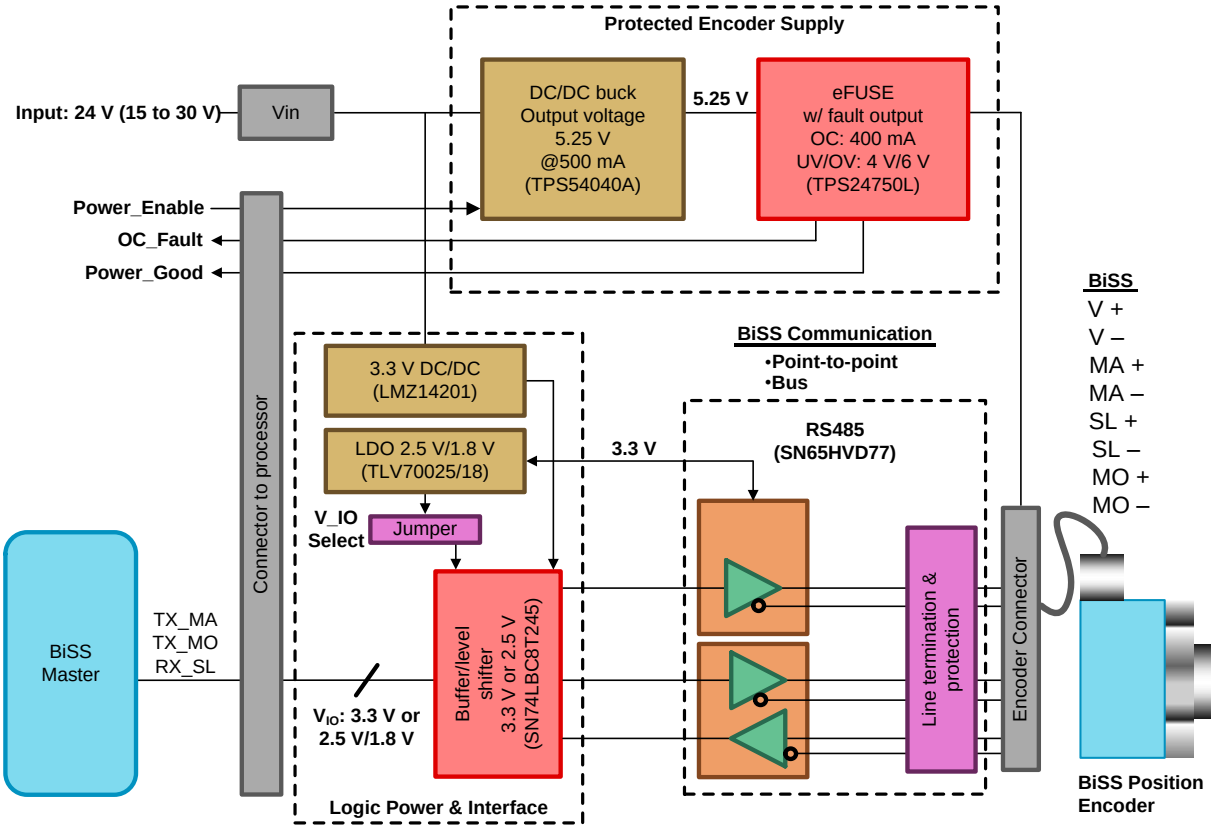

Figure 11. System Block Diagram of TIDA-00175: Interface to a 5-V, BiSS Position Encoder

4 Circuit Design and Component Selection

4.1 BiSS RS485 Communication and Logic

As outlined in Section 2, a RS485 full-duplex transceiver is preferred versus a RS422 transceiver. A RS485 transceiver offers better performance, such as higher common mode voltage range and higher input receiver impedance.

4.1.1 RS485 Transceiver

The maximum clock frequency with BISS is 10 MHz, which equals a baud rate of 20 Mbps. Therefore, a BiSS-compliant RS485 transceiver has to be specified at a minimum baud rate of 20 Mbps.

With longer cables, the signal is attenuated and low-pass filtered, respectively. To maximize the data rate with longer cables, a faster than 20-Mbps transceiver is recommended.

Figure 12 outlines the scenario with long cable lengths, such as 60 m or more. The differential clock or data signals will be attenuated and low-pass filtered. The time to detect the input thresholds become shorter and signal edges will be missed if the receiver is not fast enough. A faster than 20-Mbps transceiver will be able to detect these much shorter signal levels outside the threshold and bit errors are reduced. Or, the other way around, a higher clock rate can be achieved. Therefore, a 50-Mbps transceiver was chosen for this design.

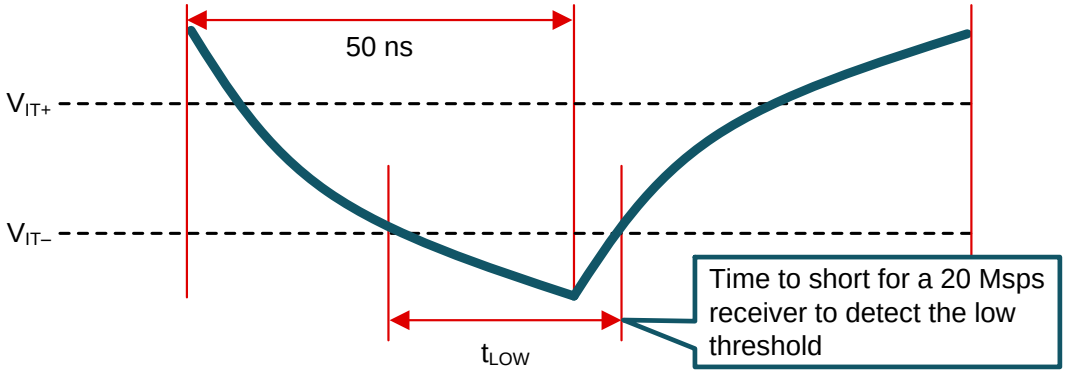

Figure 12. RS485 Receiver Threshold Timing for High-Attenuated, Low-pass Filter Signals

For this design, only a RS485 full-duplex transceiver with a 3.3-V supply was considered. Table 7 lists three RS485 transceivers with more specific parameters.

Table 7. RS485 Parameters (1)

Parameter	SN65HVD30	SN65HVD74	SN65HVD77
Supply voltage (recommended)	3.3 V	3.3 V	3.3 V
5-V tolerant inputs	Y	Y	Y
Baud rate (maximum)	26 Mbps	20 Mbps	50 Mbps
Driver rise/fall time (typical)	5/5 ns	7 ns	3 ns
Driver propagation delay low-high and high-low (typical)	10/9 ns	10 ns	10 ns
Receiver rise/fall time (typical)	5/6 ns	5 ns	3 ns
Receiver propagation delay low-high and high-low (typical)	26/2 9ns	60 ns	25 ns
Supply current (quiescent) driver and receiver enabled	2.1 mA (max)	1.1 mA (max)	1.1 mA (max)
Glitch-free power-up and power-down protection for hot-plugging applications	Y	Y	Y
IEC61000-4-2 ESD (absolute maximum ratings)	N/A	±12kV (CD)	±12 kV (CD)
IEC61000-4-4 EFT (absolute maximum ratings)	N/A	±4 kV	±4 kV
Operation free-air temperature	-40 to 85°C (125°C)	-40 to 125 °C	-40 to 125 °C

(1) From Data Sheets *SM65HVD30, 3.3 V FULL-DUPLEX RS-485 DRIVERS AND RECEIVERS*, (SM65HVD30) and *SN65HVD7x 3.3-V Full-Duplex RS-485 Transceivers With ±12-kV IEC ESD*, (SN65HVD7x).

This design uses SN65HVD77, since SN65HVD77 is >20 Mbps for higher receiver sensitivity at longer cables, and has a very fast driver rise and fall time, which yields a longer reach versus SN65HVD77. Further benefits are low-propagation delay and IEC-ESD and IEC-EFT immunity.

The RS485 transceiver propagation delay is less critical with BiSS, since BiSS offers propagation (line) delay compensation. The propagation delay of the encoder cable adds significant delay especially at higher cable lengths. As a rule of thumb, a cable contributes to a propagation delay of approximately 5 ns/m. A 25-m cable, for example, contributes to a propagation delay of 250 ns for the slave data SL versus the master MA-clock signal.

4.1.1.1 RS485 Termination and Transient Protection

The 120-ohm termination resistor is added on the receiver lines SL+ and SL- on the master.

Pulse-proof resistors R32, R38, R42, R42 and R53, R55 are added into the A, B and Y, Z bus lines, if transient voltage is higher than the specified maximum voltage of the transceiver-bus terminals. These resistors limit the residual clamping current into the transceiver and prevent the transceiver from latching up. In SL receive mode, due to the low input current of typical 240 uA, the voltage drop across the 10-Ω resistors is negligible. In the MA and MO transmit direction, the voltage drop across both 10-Ω resistors is around 15%, and therefore results in a slightly lower transmit differential voltage.

To further improve immunity against common-mode noise, 220 pF bypass capacitors C29, C31, C32, C33, C37, and C38 are added at each bus line A, B and Y, Z to GND. The capacitor value can be adjusted accordingly and the adjustment is a tradeoff between data rate and noise immunity.

For test purposes, a TVS diode was added, but not populated. Since the connector and corresponding encoder cable are shielded, the surge pulse is applied to the cable shield only. The TVS diode is required only for equipment without a shielded cable. In that case, the surge would be coupled into all four differential signal lines with a 160-Ω each source coupling impedance each, to get a resulting 40 ohms.

The bus terminals of the SN65HVD7x transceiver family possess on-chip ESD protection for ±12 kV IEC61000-4-2 contact discharge. However, because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. A complete list of layout guidelines can be found in the SN65HVD7x Data Sheet, *SN65HVD7x 3.3-V Full-Duplex RS-485 Transceivers With ±12-kV IEC ESD*,(SN65HVD7x) and in Section 7.5.

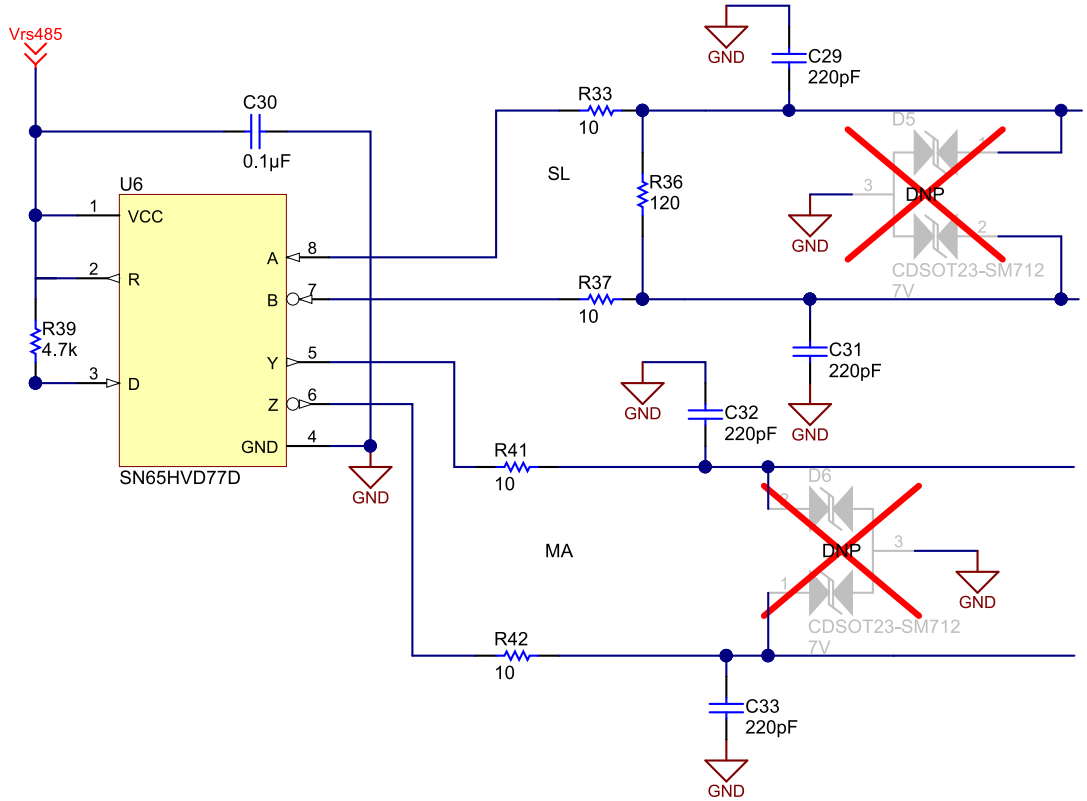

Figure 13. RS485 Transceiver Configuration for BiSS SL+/SL- and MA+/MA-

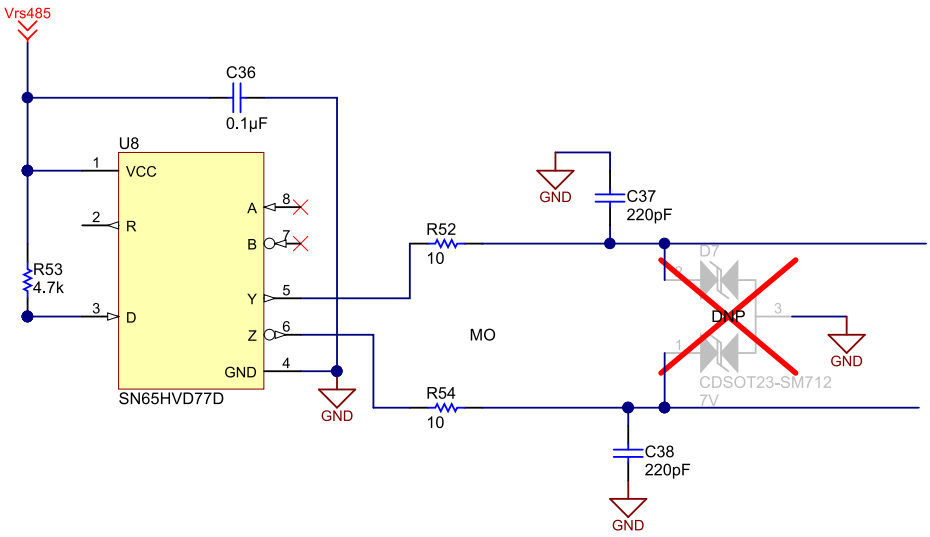

Figure 14. RS485 Transceiver Configuration for BiSS MO+/MO-

Digital Interface

To support lower than 3.3-V I/O, for example, 2.5 V or 1.8 V, an optional buffer and level shifter SN74AVC8T245 was chosen which operates from 1.2 V to 3.6 V. For ease of design and component sampling, an 8-channel device was used for this design. A 4-channel device SN74AVC4T245 would have been sufficient also. All signals not used were pulled down using a 4.7-k ohm resistor to avoid floating, undetermined input signals.

4.1.2 Logic Power Supply

The RS485 transceivers and the optional level shifter require two voltage rails: a 3.3-V rail for the RS485 transceivers and one side of the level shifter, as well as the I/O voltage rail for the other side of the level shifter. The second rail can be 3.3 V, 2.5 V, or 1.8V.

4.1.2.1 DCDC Buck Converter with 3.3-V Output

The DCDC buck has been chosen for a 24-V input with wide range from 15 V and 30 V and an output voltage at 3.3 V at 350 mA. The assumption is that the 24-V bus voltage is already isolated (SELV). Therefore, this power supply does not need to be isolated and Buck (step-down) topology is optimum. The specifications for this power supply are as follows.

- Input voltage range V_{IN}: 15 V to 30 V, 24-V nominal
- Output voltage V_{OUT}: 3.3 V, at 300 mA (or higher)
- Target switching frequency: approximately 700 kHz
- Non-isolated

The assumption is made for this design that in the engineers's application, the 3.3-V rail will also be used to power other components of the system like the MPU or MCU and other digital logic. For performance as well as high integration and ease of use, the design uses a power module with buck topology, which integrates FET and inductor.

The TI power module presents several advantages. The module is really easy to design with, saves time to market, and saves on development cost. The TI power module is already tested for EMI and EMC. There is also the fact that the external components, usually found next to a controller (inductors, FETs, diodes, and so forth) are integrated, which saves board space and cost of manufacturing (size of the PCB, components count, and so forth). With all these requirements in mind, the LMZ142001 fits the needs for this design. The LMZ142001 device is a Buck topology, 6-V to 42-V input, 0.8-V to 6-V at 1-A output, constant ON time power module. The LMZ142001 requires few external components: a resistor divider to set the enable voltage, a resistor divider to set the output voltage, a resistor to set the ON time, one capacitor to set the soft start time, and input and output capacitors.

To ensure proper output ripple performance of the LMZ14201, the capacitor C18 was added, as shown in Figure 15.

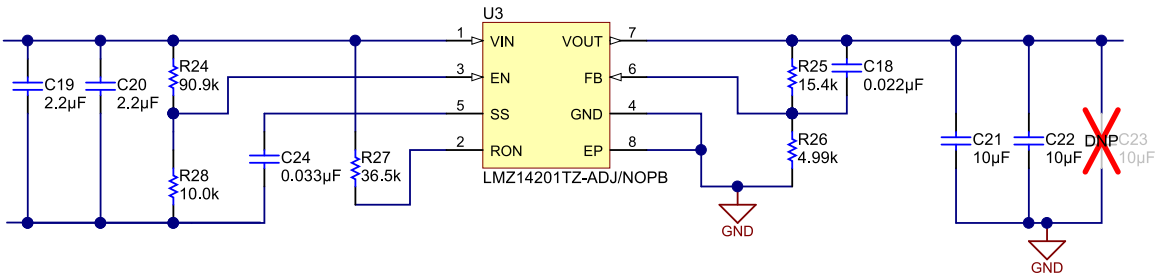

Figure 15. 3.3-V Logic Power Supply Schematic: Power Module LMZ14201

For the details on the part and on how to calculate the external components around the LMZ14201, refer to the LMZ14201 Data Sheet, *LMZ14201 1A SIMPLE SWITCHER® Power Module with 42V Maximum Input Voltage*, (LMZ14201) and on the TIDA-00175 Design Calculator Excel sheet, described in Section 4.3.

To ensure the module is working in continuous conduction mode, a 10-ohm resistor was added as additional load. This load is simulating the additional current, normally drawn from additional components in the customer's end application.

For layout guidelines, please refer to the LMZ14201 Data Sheet, *LMZ14201 1A SIMPLE SWITCHER® Power Module with 42V Maximum Input Voltage*, (LMZ14201) and Section 7.5.

4.1.2.2 I/O Voltage Supply

For the I/O voltage of the level shifter, a jumper was built in to either supply from a 2.5-V or 1.8-V LDO or the 3.3-V rail. The 3.3-V rail is the default option and the jumper is explained in Section 5.2. The specifications for this LDO are: V_{IN} = 3.3 V, V_{OUT} = 2.5 V or 1.8 V, $_{IOUT}$ = 100 mA and drop out voltage <0.7 V. The 2.5-V option was chosen as default for this design.

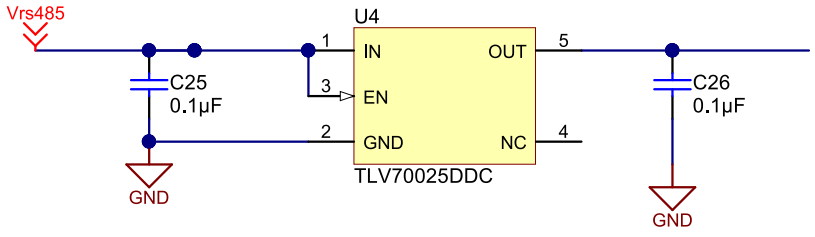

Figure 16. Power Supply for 2.5-V I/O Voltage (Optional)

The LDO for this design needs an easy to use, cost effective part. The TLV70025 fits these criteria. The TLV70025 is a 2-V to 5.5-V input, 2.5-V at 200 mA LDO. The TLV70025 only requires input and output capacitors. Please note that the TLV700XX family offers a wide range of voltage options, pin-to-pin compatible to each other: 1.2 V, 1.3 V, 1.5 V, 1.8 V, 1.9 V, 2.2 V, 2.5 V, 2.8 V, 2.9 V, 3 V, 3.1 V, 3.2 V, 3.3 V, and 3.6 V. For the details on the part, refer to the TLV700xx Data Sheet, (*200-mA, Low-IQ, Low-Dropout Regulator for Portable Devices* TLV700xx).

4.2 5-V, BiSS Encoder Power Supply with Protection

The encoder supply can be split into three blocks. These blocks are the input filter, the DCDC buck, and the eFUSE for overcurrent, overvoltage, and undervoltage protection.

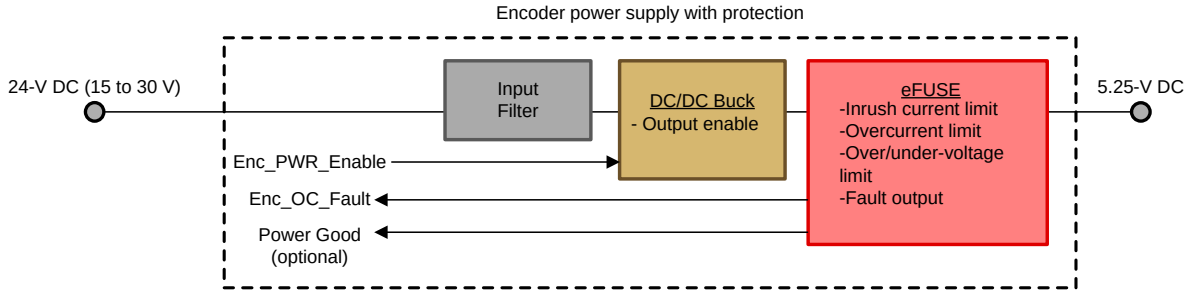

Figure 17. Protected-Encoder Power Supply Block Diagram

4.2.1 Input Filter

Conducted EMI are generated by the normal operation of switching circuits. Large discontinuous currents are generated by the power switches *turn* and *off*. In a buck topology, large discontinuous currents are present at the input. The voltage ripple, created by these discontinuous currents, can couple into the rest of the system and cause EMI issues. To prevent these EMI issues, an input filter is used to reduce the input-voltage ripple accordingly. In this design, the input filter consists of a PI-filter with the cutoff frequency around 1/10 of the switching frequency of the converters to produce 40 dB of attenuation at the switching frequency. The converters for this design have a switching frequency of approximately 700 kHz, therefore, for the input filter, see Equation 1.

$$fc = \frac{1}{2 \times \pi \times \sqrt{L1 \times C9}} \quad (1)$$

L is usually in the range of 1 µH to 10 µH. This design sets L1 to 4.7 µH and fc to 70 kHz. The resulting capacitor value is 1 µF for C9.

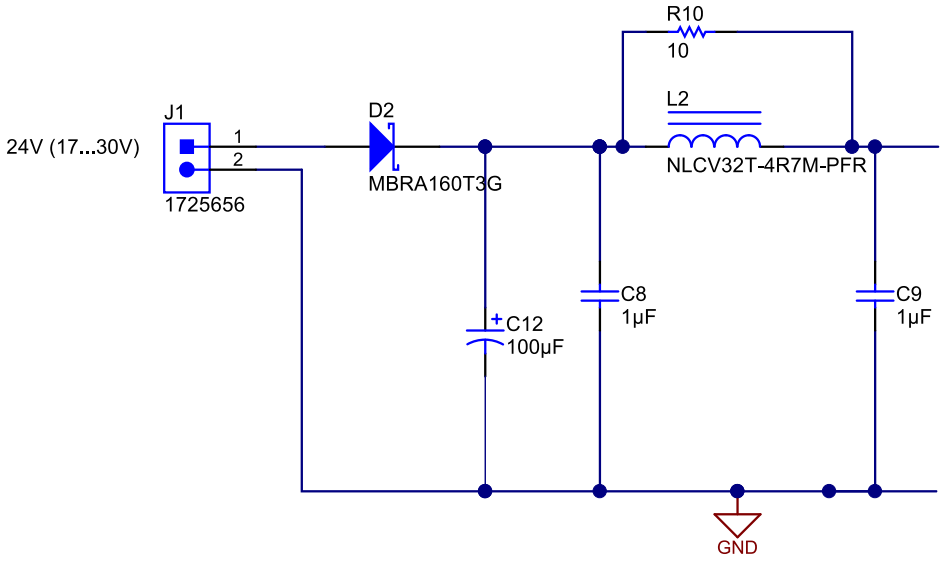

Figure 18. Input Filter including Reverse-Polarity Protection

4.2.2 DCDC Buck (TPS54040A)

The specifications for the 5-V, BiSS-encoder power supply are as follows.

- Input voltage: V_{IN} = 15 V to 30 V, 24-V nominal, reverse polarity protection
- Output voltage: V_{OUT} = 5.25 V at 350 mA (to take advantage of a higher-voltage margin to yield longer cable lengths)
- DC Accuracy = 5.25 V ±4%
- Switching frequency = 700 kHz, adjustable and an option to synchronize to external clock
- Output voltage ripple max 30 mV_{pp}
- Output voltage can be switched on and off (enable signal)
- High efficiency: >85% at 5.25-V and 350-mA output
- Non-isolated

This design uses the TPS54040A buck converter with integrated FET, 3.5-V to 42-V input voltage, and 0.8-V to 39-V output voltage at 500-mA output current. The TPS54040A frequency can be adjusted from 100 kHz to 2.5 MHz or can be synchronized with an external clock. The frequency can also be enabled and disabled. All these features make the TPS54040A a good fit for the design requirements.

NOTE: The TPS54040A is pin-to-pin compatible with the TPS5401, which is a lower cost version of the TPS54040A with similar performance but less accurate output-voltage and enable threshold.

NOTE: The TPS54040A is pin-to-pin compatible with the TPS54140, TPS54240, TPS54340, and TPS54540, which have the same specifications as the TPS54040A with respectively 1.5-A, 2.5-A, 3.5-A, and 5-A capability.

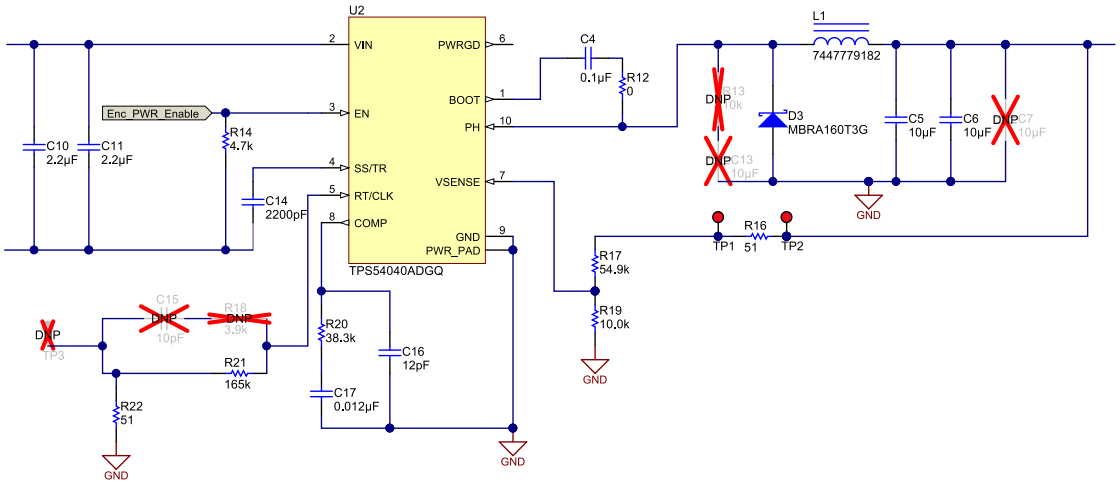

Figure 19. Protected-Encoder Power Supply Schematic: DCDC Converter TPS54040A

4.2.2.1 Setting the Output Voltage: Passive Components Calculation

Although the passive components in this design were selected for 5.25-V, the TSP54040A can also support BiSS encoders with 10-V to 30-V supply.

The output voltage of 5.25 V is set through the feedback voltage at the V_{SENSE} pin. With R19 = 10 k and R17, there is a yield for the corresponding voltage divider from the output to the V_{SENSE}, as shown in Equation 2.

$$R19 = 10k\left(\frac{5.25\ V - 0.8\ V}{0.8\ V}\right) = 55.6\ k \quad (2)$$

The design uses R17 = 54.9 from E96 series, which yields 5.2 V.

For the details on the part and on how to calculate the complete components around the TPS54040A, click on the following links: TPS54040A Data Sheet, *0.5 A, 42 V Step Down DC/DC Converter with Eco-mode™*, (TPS54040A) and the TIDA-00175 Design Calculator Excel sheet, described in Section 4.3.

4.2.2.2 Accuracy of the Output Voltage

The TPS54040A internal voltage reference has a tolerance of ±2% and the feedback resistors R17 and R19 to V_{SENSE} have a tolerance of ±1%. The error at the V_{SENSE} pins can be calculated as follows:

$$V_{SENSE}(\Delta 1, \Delta 2) = \frac{R19(1+\Delta 1)}{R17(1+\Delta 2)+R19(1+\Delta 1)} \times V_{OUT} \quad (3)$$

Δ1 and Δ2 are the tolerances of the resistors used. The worst case error yields Δ1 and Δ2 with opposite signs. With the resistor values R17 = 54.9 k and R19 = 10 k and a tolerance of ±1%, the maximum negative and positive error at V_{SENSE} is -1.68% and 1.7%. Including the 2% tolerance of the TPS54040A, the total DC error will be between ±3.7%. The total DC error meets the specification of ±4% and ensures the output voltage remains below 5.5 V even under worst case tolerances. If desired, further improvement can be achieved using 0.1% resistors in the feedback path.

4.2.2.3 External Switching Frequency Option

With multiple switching power supplies on the PCB, multiple switching frequencies coexist. Multiple switching frequencies may yield undesirable subharmonic-beat frequencies and further EMI.

Synchronization of the switching frequencies, when applicable, can help solve this problem (with undesirable subharmonic-beat frequencies and further EMI). In this design, the switching frequency of the TPS54040A is set to 700 kHz with resistors R21+R22. If synchronization is required, the user can populate C15 and R18 and apply an external clock through TP3.

In case the TPS54040A is synchronized to an external clock, the complete design should be calculated with the external clock frequency, with the exception of the resistor which sets the default switching frequency (R_{FSET} in Figure 20 (R21 in this design).The default switching frequency set by R21 should then be set to a frequency close to, but lower than, the external clock, such as 500 kHz in this case.

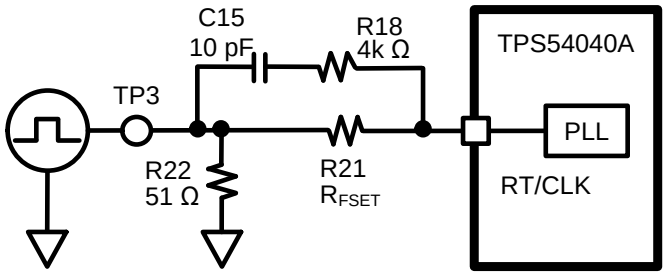

Figure 20. Synchronizing to a System Clock

For more details, refer to the TPS54040A Data Sheet, *0.5 A, 42 V Step Down DC/DC Converter with Eco-mode™*, (TPS54040A).

4.2.2.4 Do Not Populate (DNP) Components or Components Change

On the TPS54040A schematics, some components are marked as DNP. Using TP3, C15, and R18 in case of synchronization of the switching frequency to an external clock was previously discussed in Section 4.2.2.3.

C7: C5 and C6 are used as output capacitors. In case more capacitance is required, C7 can be populated. The footprint of C7 can also be used to measure the output voltage generated by U1.

R12: In case there is too much ringing on the switch node, a solution could be to slightly slow down the switching speed of the MOSFET. Slowing down the switching speed can be achieved by increasing R12 (in series with the bootstrap capacitor C4) from zero ohms to usually approximately two ohms. Please refer to SLPA010 Application Report, *Ringing Reduction Techniques for NexFET™ High Performance MOSFETs*, (SLPA010) for information on how to use and calculate this resistor.

R13, C13: Another way of reducing the ringing and overshoot of the MOSFET is to add a snubber network. R13 and C13 are placed here in case a snubber is added to the design. Refer to the SLPA010 Application Report, *Ringing Reduction Techniques for NexFET™ High Performance MOSFETs*, (SLPA010) on how to use and calculate a snubber network.

4.2.2.5 Layout Guidelines

Please refer to the TPS54040A Data Sheet, *0.5 A, 42 V Step Down DC/DC Converter with Eco-mode™*, (TPS54040A) and Section 7.5.

4.2.3 eFuse Protection

The specifications for the eFuse are:

- Maximum voltage drop at 350 mA: <25 mV
- Overcurrent limit: 400 mA
- Inrush-current limit: 400 mA
- Overcurrent fault time: 4.5 ms
- Maximum capacitive load: 330 uF
- Overvoltage limit: (OVP): 6 V
- Undervoltage lockout (UVLO): 4 V
- Latch or disconnect when fault is detected
- Fault feedback

The TPS24750 is a 12-A eFuse, 2.5-V to 18-V bus operation with integrated MOSFET with 3-mΩ R_{DSON}. The TPS24750 has overvoltage protection, an UVLO, and a programmable curent and power limit with a programmable fault timer. This design uses the TPS24750 part because the part fits the design requirements, has a very low-series resistance to minimize voltage drop, and has an external-sense resistor for precise current-limit detection.

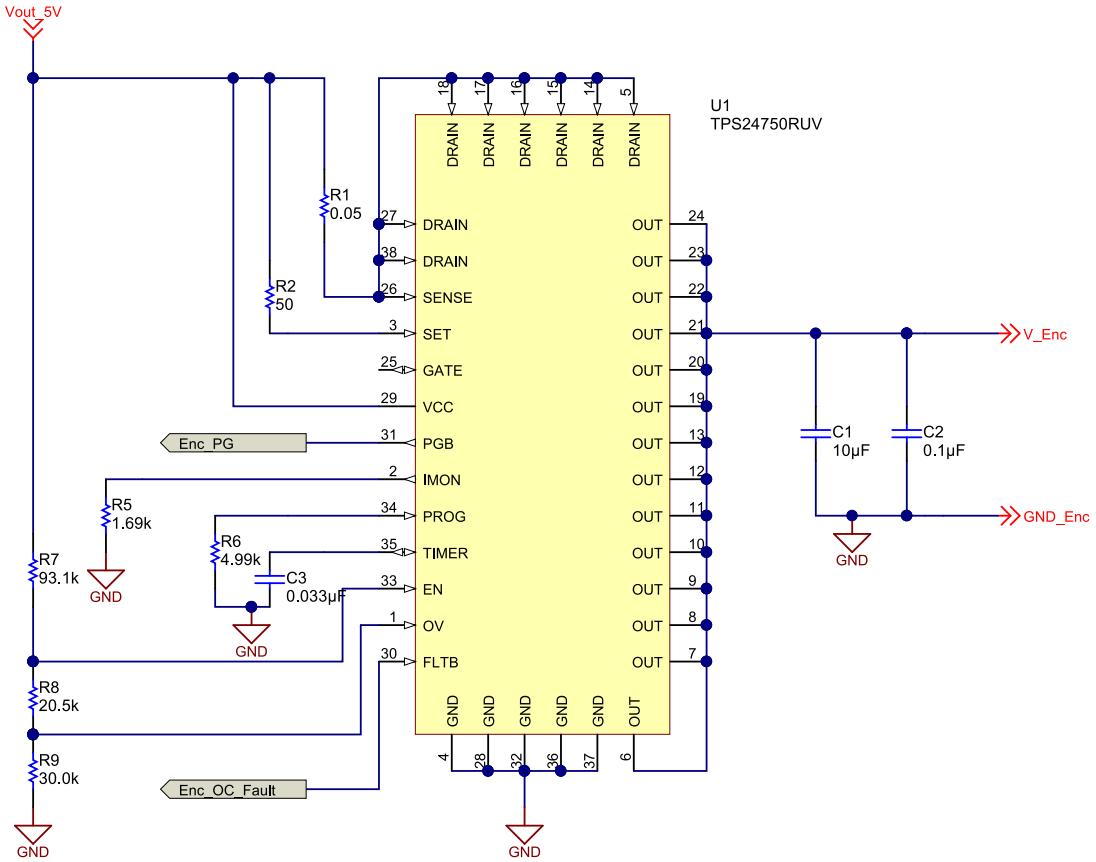

Figure 21. Protected-Encoder, Power-Supply Schematic: eFuse TPS24750

4.2.3.1 Setting Current and Voltage Limits

A key feature of the TPS24750 is the inrush-current limit and the fault timer to switch off in case of an overcurrent. The current limit is set as follows.

$$I_{LIM} = \frac{0.675\ V \times R_{SET}}{R_{IMON} \times R_{SENSE}} \quad (4)$$

with R_{SENSE} = R1 = 0.05 ohm, R_{SET} = R2 = 50 ohm and I_{LIM} = 400 mA.

Next, calculate R_{IMON} = R5 = 1.69 kohm.

The fault timer period t_{FAULT}, to disconnect in case of overcurrent is set through capacitor CT at the TPS24750 TIMER pin as follows:

$$C_T = \frac{10\ uA}{1.35\ V} \times t_{FAULT} \quad (5)$$

with t_{FAULT} = 4.5 ms, the result is C_T = C3 = 33 nF.

For the details on how to calculate all the passive components with the TPS24750, refer to the TPS24750 Data Sheet, *12A eFuse Circuit Protector with Current Monitor*, (TPS24750) and to the TIDA-00175 Design Calculator Excel sheet, described in Section 4.3.

4.2.3.2 Layout Guidelines

Refer to refer to the TPS24750 Data Sheet, *12A eFuse Circuit Protector with Current Monitor*, (TPS24750) for layout guidelines for the TPS24750. Please pay special attention to the layout for the sense resistor R_{SENSE}. Refer also to Section 7.5.

4.3 Power Supply Design Calculator

The TIDA-00175 Design Calculator Excel sheet was created to help calculate the components values for the power supplies. The Design Calculator Excel sheet includes the equation present in this design, as well as the equation present in the applicable data sheets.

This Excel sheet has to be used in a sequential order from top to bottom.

This document contains three sheets:

- Design: In this sheet, the user enters his specification and chooses the components he wishes to use.
- BOM + Schematic: This sheet recaps the components chosen in the design sheet and shows where to place the components in the schematic.
- Components Data: This sheet recaps some parameters of the TI components required for the calculations on the design sheet.

There are four different colors used in these Excel documents:

User input specifications
Calculated component
User selected standard component
Calculated design parameter

Figure 22. Excel Document Color Code

- **Yellow cells:** The user will enter the different specifications of his design.
- **Blue cells:** These cells are the results of the equations needed to select a component.
- **Green cells:** These cells allow the user to choose a standard value closest to the value calculated in the blue cells next to green cells.
- **Red cells:** These cells are design parameters that are calculated along the process (for example, the duty cycle or the current flowing in the inductor).

  Here is a short example:

Vencoder - TPS54040A				
power supply requirements	**Parameter**	**Value**	**Value chosen**	**Description**
	vinstart (V)		10.00	Enable voltage
	vinstop (V)		9.00	Disable voltage
	dVin (%)		1.00	input voltage ripple
	dVopp (V)		0.05	output ripple voltage requirement
	dVo (V)		0.10	output voltage transient requirement during step load changes
	kind		0.30	inductor ripple constant (usually between 0.2 and 0.4)
	ioh (A)		0.30	output current under heavy load
	iol (A)		0.00	output current under light load
	vfd (V)		0.50	forward voltage of schottky diode
	vosc (V)		0.10	output voltage during short circuit
power stage design	**Parameter**	**Value**	**Value chosen**	**Description**
	R19 (kΩ)		10	low side feedback resistor for adjusting output voltage. Usually 10kΩ
eq1 in d/s	R17 (kΩ)	55.63	54.90	High side feedback resistor for adjusting output voltage
	Dmax	0.35		maximum duty cycle
	Dnom	0.22		nominal duty cycle
	Dmin	0.18		minimum duty cycle

Figure 23. Extract of the TIDA-00175 Design Calculator Excel Sheet

In Figure 23, the user will fill the yellow cells according to his specification. Once all the yellow cells are filled, the user will arrive to the first green case. This green cell is R19, the low-side resistor, which is needed to set the output voltage of the TPS54040A. The recommendation is to use 10 kΩ.

This 10-kΩ value and some of the specifications entered previously in the yellow cells, such as the output voltage of the TPS54040A is then used to calculate the feedback resistor R17 at 55.63 kΩ (blue cell).

The user will then choose the closest standard value wanted to implement in his design. In this case, a choice was made from E96 series 54.9 kΩ.

The next three cells are the maximum, nominal, and minimum-duty cycle, calculated from the maximum, nominal, and minimum-input voltage and output voltage set by the user in previously-filled yellow cases.

The user then continues in a top-to-bottom sequence.

4.4 Connectors

To connect a BiSS position encoder, an 8-pin header (2.54 mm) and a SubD-9 female connector was chosen. The SubD-9 female connector has the same pin-out as used with the iC-Haus GmbH MB4U BiSS, SSI, PC-USB 2.0 ADAPTER. The connector to the external processor for the BiSS-C Master that was chosen for this design is a 5 × 2 header with 2.54-mm spacing. The connector to control the encoder power supply that was chosen is a 4 × 2 header with 2.54-mm spacing. For details on the connector assignment, refer to Section 5.2.

5 Getting Started

5.1 PCB Overview

A picture of the PCB top and bottom is shown in Figure 24. To minimize PCB size, components are mounted on the top and bottom layer.

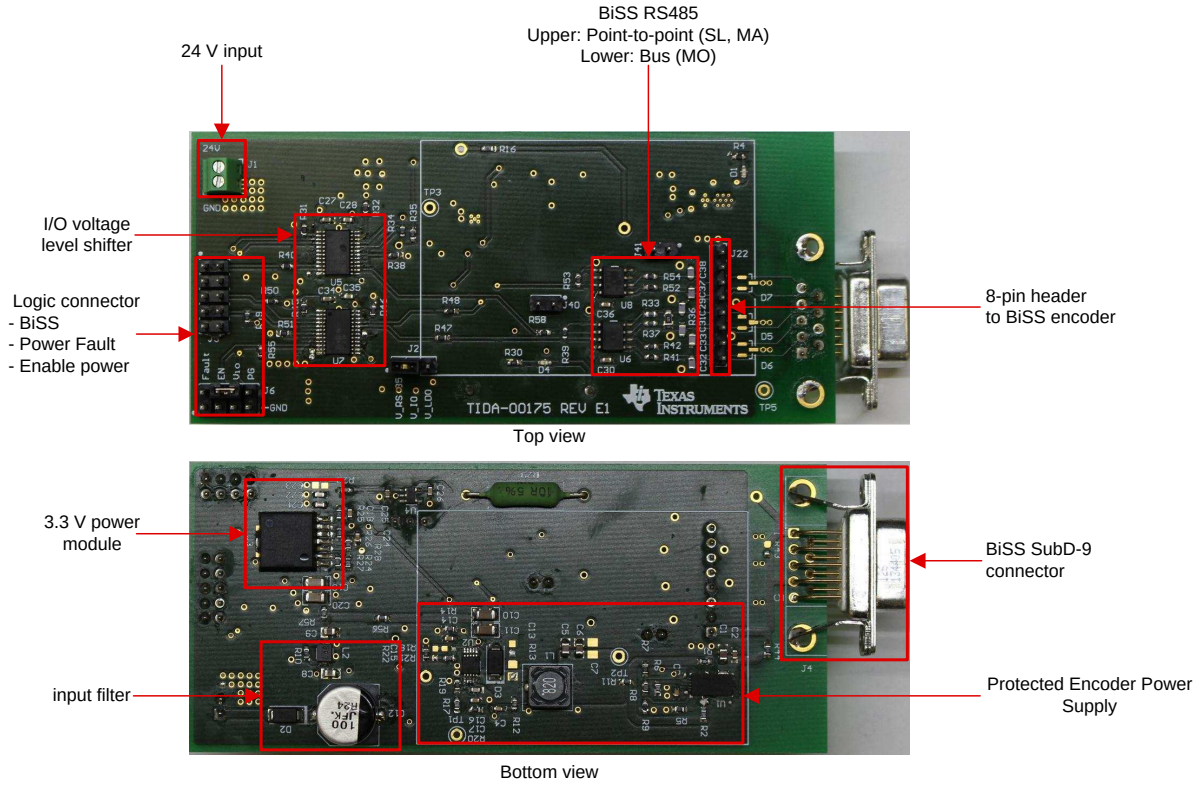

Figure 24. TIDA-00175 PCB Top and Bottom View with Functional Blocks

5.2 Connectors and Jumper Settings

The connector assignment and jumper settings are outlined in Table 8 through Table 11.

Table 8. Jumper J2: GPIO voltage selection

JUMPER	SETTING	DESCRIPTION
J2	1-2	Select 3.3-V I/O (default)
	2-3	Select 2.5-V I/O

This jumper is used to select the voltage level of the level shifter to the I/O part of the system.

Table 9. J22: Encoder 8-Pin Connector

CONNECTOR	PIN	DESCRIPTION (BLANK = NOT CONNECTED)
J22	1	V+
	2	V-
	3	MO-
	4	MO+
	5	SL+
	6	SL-
	7	MA-
	8	MA+

Table 10. J4: Encoder SubD-9 Female Connector

CONNECTOR	PIN	DESCRIPTION (BLANK = NOT CONNECTED)
J4	1	-
	2	MA+
	3	MA-
	4	V+
	5	MO-
	6	V-
	7	SL+
	8	SL-
	9	MO+

The PCB default configuration for this design is that the V+ (5.25 V) and V- (GND) are used to support 5-V BiSS/SSI encoders. If an external power supply is desired in case of a 10-V to 30-V supply. Remove the 0 ohms resistors R44 to disconnect the protected 5.25-V encoder supply. Then connect the external supply to J22, pin 1 (10 V to 30 V) and GND to J22, pin 2.

Table 11. J3 and J6: Digital Connector

CONNECTOR	PIN	SIGNAL	PIN	SIGNAL	DESCRIPTION
J3	1	GND	2	RX_SL (O)	BiSS SL
	3	GND	4	-	-
	5	GND	6	TX_MO (I)	BiSS MO
	7	GND	8	TX_MA (I)	BiSS MA
	9	GND	10	-	
J6	1	GND	2	Fault (O)	Encoder power supply fault indication
	3	GND	4	En (I)	Turn on encoder power supply
	5	GND	6	Vio (O)	GPIO voltage
	7	GND	8	PG(O)	Encoder power supply power good

6 Test Results

Tests were conducted for each of the individual subsystems: the RS485 transceivers, the protected encoder power supply, and an application test with a BiSS-C position encoder as well.

The RS485 clock/data driver (signals MA+, MA- or MO+, MO-) and the RS485 slave data receiver (signal SL+, SL-) were tested for maximum error-free data rate versus cable length, signal integrity (eye diagram), and transceiver-propagation delay.

The protected encoder power supply was tested for steady state, transient response, and efficiency. Finally, a test was performed with a Baumer 5-V BiSS-C position encoder GBPAS – BiSS-C and an iC-Haus GmbH BiSS Master, to which was connected this TI Design. The test report according to IEC61800-3, for IEC61000-4-2 (ESD), IEC61000-4-4 (Fast Transient Burst), and IEC61000-4-5 (Surge) is available in a separate document at TIDA-00175.

6.1 RS485 Transceiver Performance

6.1.1 Test Setup

Figure 25 shows the setup of the RS485 transceiver performance test and the test equipment used.

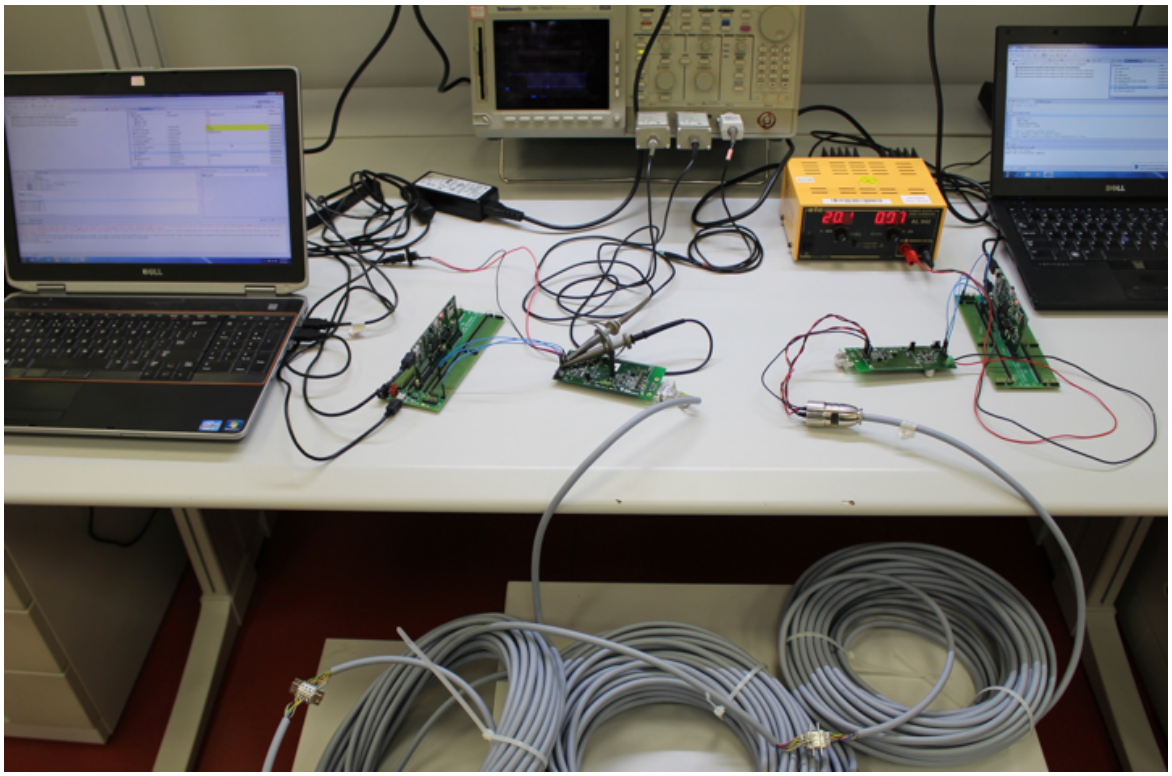

Figure 25. Picture of Test Setup for RS485 Performance Measurements

Table 12. Test Equipment

TEST EQUIPMENT	PART #
Baumer IVO PVC encoder cable (5 × 2 LiY 0.14 mm^2) with M23 connector. Cable length: 10 m with M23, 25 m with M23, 25 m and 35 m: Maximum length with M23 connector 85 m	Z 130.A02, Z 130.007
Random pattern generator and bit error analyzer (up to 50 MHz) via SPI	TMS320F28377D Experimenter Kit with internal TI test SW
Oscilloscope	Tektronix TDS794D, P6330/P6339A diff/passive probes

To generate the test pattern for the RS485 performance tests, a TMS320F28377D MCU to was used to implement a high-speed SPI Master to transmit the SPI master clock (MA or MO), as well as to receive and analyze the data (SL) from the slave device at the cable far end. To compensate for the cable propagation delay, delay compensation in software was implemented on the SPI Master. Another MCU was used on the cable far end to realize the SPI slave interface to transmit the synchronous random test data through the full-duplex interface. A block diagram of the test setup is shown in Figure 26.

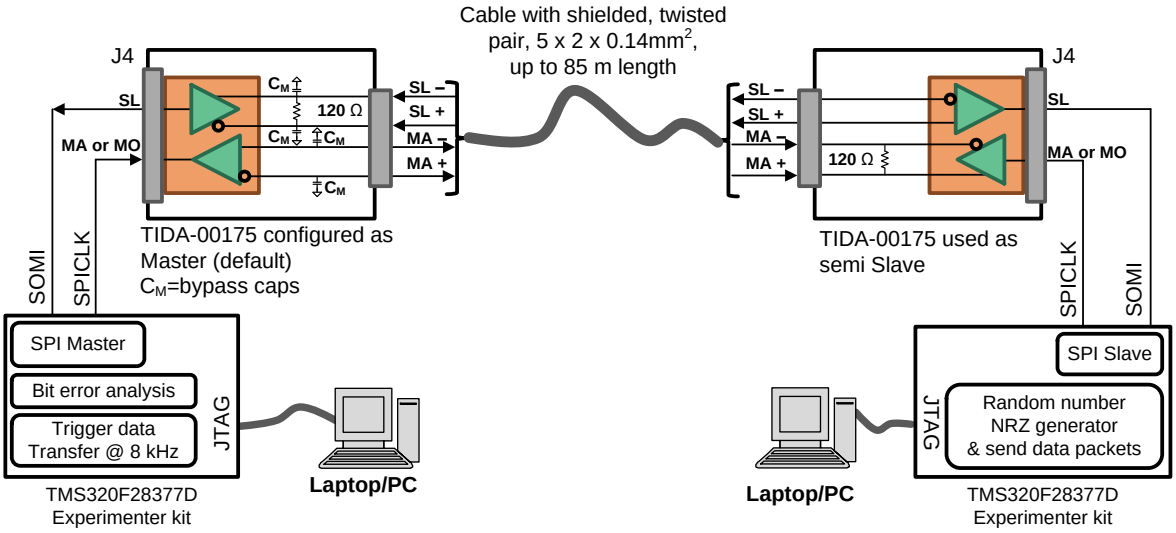

Figure 26. Test Setup for TIDA-00175 RS485 Performance Measurements

The SPI Master was connected to this design through connector J4. The SPI Master clock is configurable up to 50 MHz. The SPI Slave was connected to this design, but with swapped SL and MA signals and again connected to an SPI slave through connector J4.

Master and slave were connected through Baumer IVO PVC cables (5 × 2 LiY 0.14 mm^2) with a total of 85 m length.

In test mode *RATE_REACH*, a new SPI transmission was initiated at an 8-kHz rate. Each data packet sent was 64-bit. The first 16-bit word was the random number. The second 16-bit word was the byte-swapped random number. The third 16-bit word was the bit-inverted random number. The fourth 16-bit word was the packet counter, as shown in Figure 27. The random number was generated using the C function rand() on the slave device. This *RATE_REACH* mode was used for measuring the maximum clock frequency versus cable length.

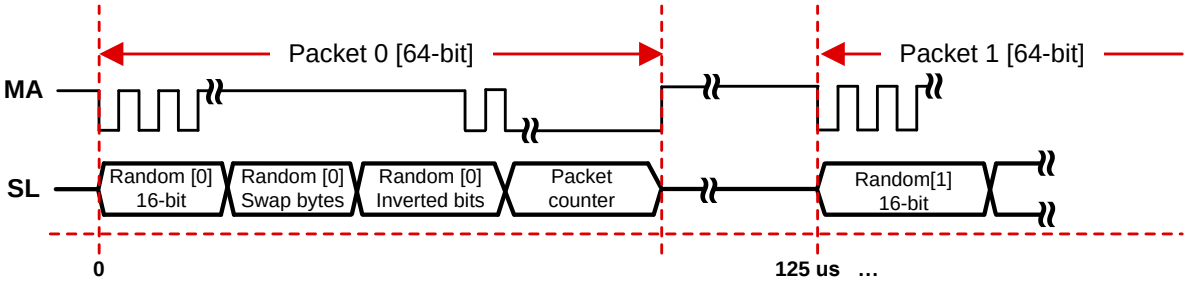

Figure 27. Test Pattern Transmitted over RS485 Link (Slave Timing)

The Master increased the MA-clock frequency until a bit error occurred on the received data frame (SL). Only if no bit error occurred, was the test passed and only then can we claim an *error free data rate*, with BER <10^{-7} due to a limited 60 s test time. This scenario should simulate a typical servo drive's inner current control loop (FOC) running at, for example, 8 kHz, and requesting a new digital-angle position through BiSS interface at this rate.

In test mode EYE_DIAGRAM, a 16-bit random number (NRZ) was continuously generated and sent to a configurable SPI Master clock through the MA channel. Therefore, in mode EYE_DIAGRAM, the BiSS MA signal was connected to SPI SIMO. The SPI Master clock was used to trigger the oscilloscope and measure the data at the far end of the cable on the slave side with a 120-ohm termination resistor.

6.1.2 Encoder Cable

The encoder cable has a significant impact on the performance of the RS422 and RS485 communication, especially at longer cable lengths. Appropriate cables are typically recommended by the specific encoder vendor.

The cable should be at least single-shielded and the wires should be separate, twisted pairs for each of the individual differential signals to minimize crosstalk between the differential signals. The cable impedance should match the 120-ohm termination, as typically used with RS422 and RS485 BiSS encoders.

For longer distances, cables are often recommended which have higher wire gauge for the supply wires (for example 0.5 mm^2) versus the communication signal wires (for example 0.14 mm^2) to reduce the supply voltage drop across the cable. Reducing the supply voltage drop is especially important for 5 V ±10% encoders at longer cables, since the voltage margin is small.

The losses of the cable limit the maximum cable length, especially with 5-V encoders. To verify, a test was conducted with multiple cable lengths of the BAUMER IVO encoder cable (5 × 2 × 0.14mm^2) for the differential MA+, MA- and SL+, SL- signals as well as for V+ and V-. The voltage was measured at this reference design's protected encoder output connector J4 and at the far end of the cable, depending on load current. For the test, a single wire was used for each V+ and V-.

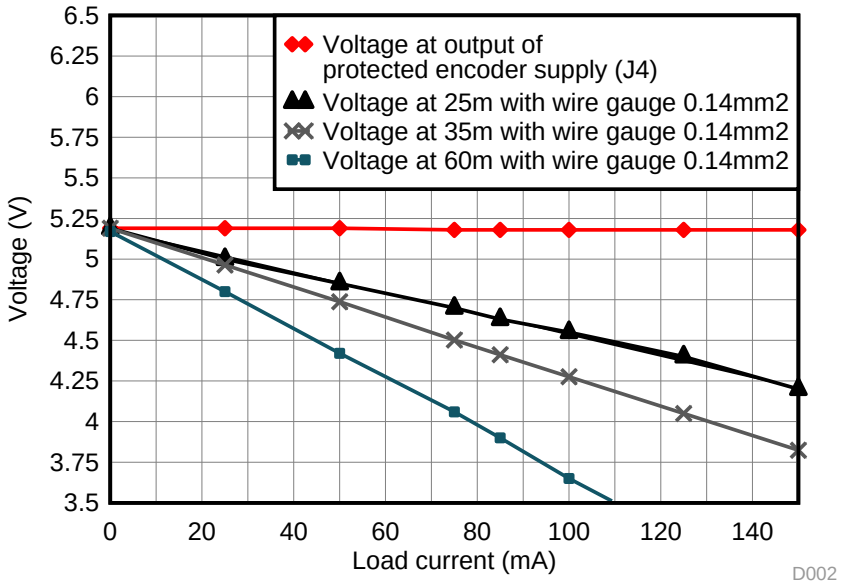

Figure 28. Encoder Supply Voltage versus Load Current with Single Wire Gauge 0.14 mm^2 at Different Lengths

It is important to mention that the cable has a significant contribution to the propagation delay at longer cable lengths, which by far exceeds the propagation delay of the RS485 transceivers. The propagation delay of the cable depends on the cable's electrical parameters and as a rule of thumb, approximately 5 ns/m is used.

Table 13 shows the propagation delay in one direction, measured with the Baumer IVO PVC cable at 10 m, 60 m, and 85 m length.

Ideally, the propagation delay is proportional to the inverse of the square root of the relative permittivity $\varepsilon_{r,}$ as well as the relative permeability μ_r. For PVC, the relative permittivity $\varepsilon_{r,}$ is approximately 4 to 4.5 at 1 MHz. Assuming μ_r is approximately 1, a propagation speed of 0.3/sqrt(4) [m/ns] = 0.15 [m/ns]. The inverse is 6.6 ns/m.

Table 13. Baumer IVO PVC Cable Propagation Delay

CABLE LENGTH	PROPAGATION DELAY (APPROXIMATELY 6.5 NS/M)
10 m	65 ns
60 m	395 ns
85 m	555 ns

6.1.3 RS485 Maximum Error-Free, MA-Clock Frequencies versus Cable Length

The diagrams in Figure 29 through Figure 31 show the maximum clock frequency versus cable length. The maximum clock frequency versus cable length is equal to the maximum synchronous data rate in full-duplex mode without any bit errors, as specified previously. It is important to remember that the cable parameters have a significant impact on the RS485 signal integrity, especially at longer loops. All tests referenced the Baumer IVO PVC cable with 5 × 2 LiY 0.14 mm^2 wires.

On the master side, indicated by *M*, three 3.3-V RS485 transceivers were tested and compared: SN65HVD30, SN65HVD74 and SN65HVD77. Each transceiver was tested either with 220-pF bypass capacitors (as default in this reference design) or without the capacitors. This is indicated in Figure 29 through Figure 31. For example, HVD77 with 220 pF means that a SN65HVD77 has been used as master transceiver with bypass caps, generating MA ± signals and receiving SL± signals.

On the slave side (encoder emulator, marked with *S*), the SN65HVD77 with a 120-ohm termination on the MA signal and no bypass capacitors was used.

In Figure 29 through Figure 31, the maximum data rate was capped according to the maximum baud rate of the device, even if the measured data rate was higher.***Start Here

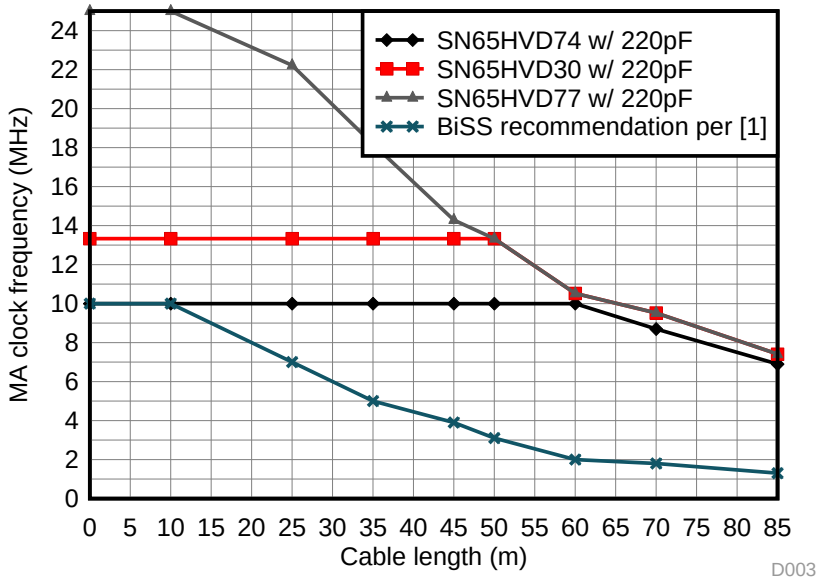

Figure 29. Maximum Error-Free Clock Frequency (MA, MO) for HVD77, HVD74, and HVD30 RS485 Transceiver on Master Side (Default with 220-pF Bypass Caps) Slave: HVD77

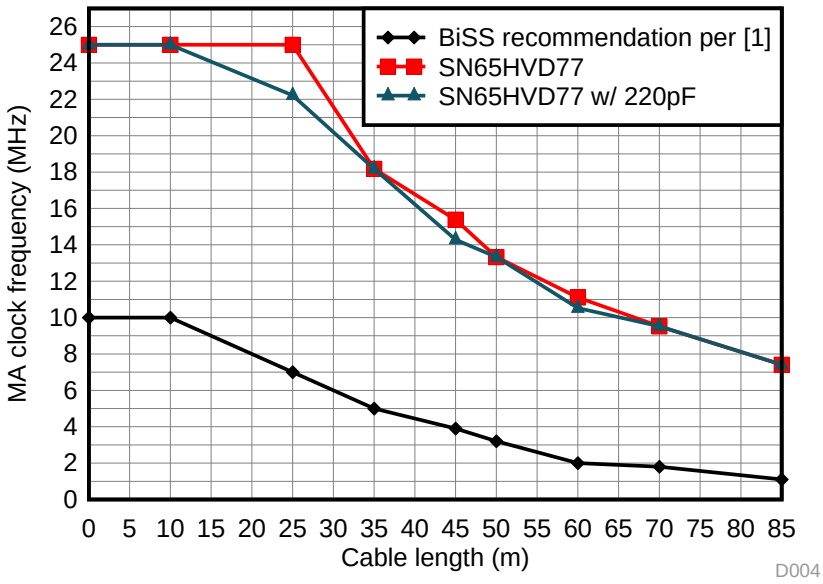

Figure 30. Maximum Error-Free Clock Frequency (MA, MO) for HVD77 with and without 220-pF Bypass Caps on the Master Slave: HVD77

Further tests were conducted to measure the receive sensitivity at longer cable lengths with high-attenuation and low-pass filtering effects. For these tests, the SN65HVD77 RS485 transceiver was used at the master without bypass caps. On the slave side, three RS485 transceivers HVD77, HVD74, and HVD30 were tested in configuration without bypass caps. The MA frequency was increased until the slave device started to loose clock edges. The critical-signal path is the MA signal, since the MA signal runs at twice the baud rate of the SL signal. For example, at 10-MHz SPI clock, MA runs at 20 Mbaud while SL runs at 10 Mbaud.

As indicated in Section 4, transmit and receive signals at longer cables are highly-attenuated and low-pass filtered. Highly-attenuated and low-pass filtered cables can result in an almost triangle waveform signal. Therefore, the RS485 transceiver with a higher baud rate (rise, fall-times) will likely achieve better performance. The SN65HVD77 transceiver was chosen because this transceiver has a high baud rate.

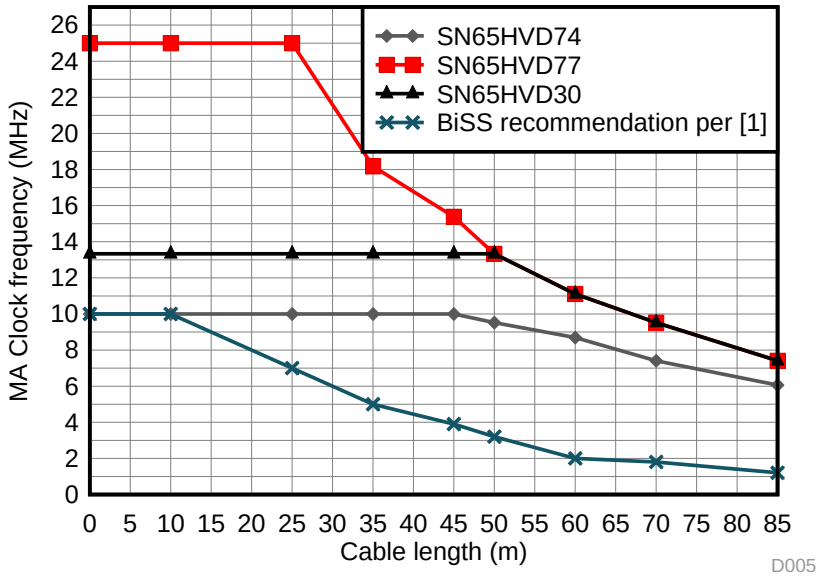

Figure 31. Maximum Error-Free Clock Frequency (MA, MO) for Different Slave RS485 Transceivers HVD77, HVD74, and HVD30 Configurations without Bypass Caps Master = HVD77

6.1.4 RS485 Eye Diagrams

The images in Figure 32 through Figure 43 show the eye diagrams using random NRZ data measured differentially with 120-ohm termination at the cable end (slave-receive side) with a differential Tektronix probe. The SPI master clock was connected to channel 1 of the scope to trigger sampling of the differential +MA, -MA signal terminated with 120-ohm at the far cable end.

The master clock was measured single-ended at the output of the TMS320F28377D-pin SPICLK and is shown as reference (Ch1, 5V/div, 25 ns) on the scope plots also.

Measurements were conducted at cable lengths 10 m, 60 m, and 85 m at the maximum error-free (BER<10^{-7}) MA-clock rates for HVD77.

Measurements at 10-m Cable Length:

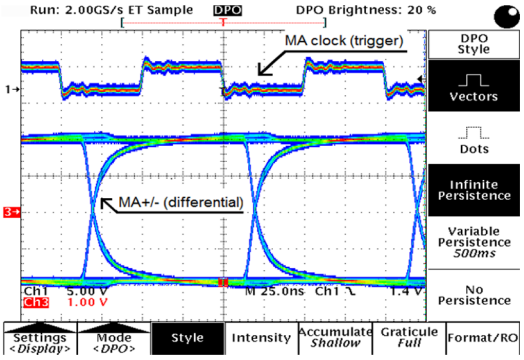

Figure 32. Eye Diagram HVD77 at Data Rate 10 MHz, 10-m Cable, 120-Ohm Termination with 220 pF)

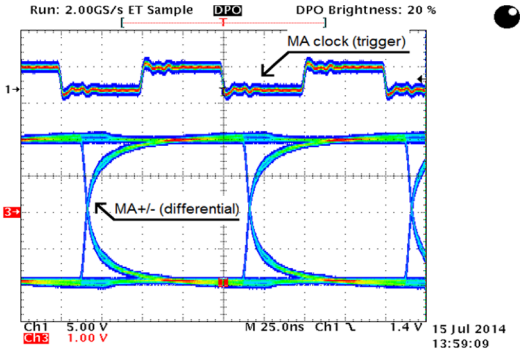

Figure 33. Eye Diagram HVD77 at Data Rate 10 MHz, 10-m Cable, 120-Ohm Termination without 220 pF

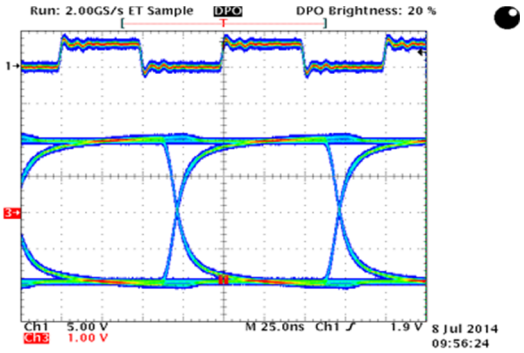

Figure 34. Eye Diagram HVD74 at Data Rate 10 MHz, 10-m Cable, 120-Ohm Termination with 220 pF

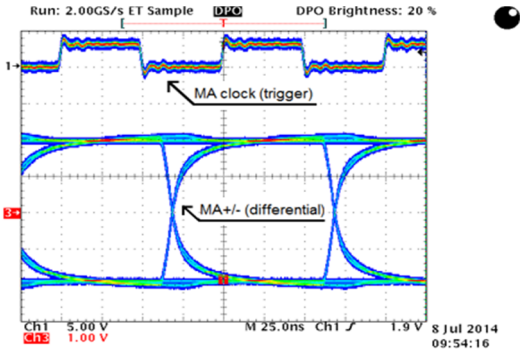

Figure 35. Eye Diagram HVD74 at Data Rate 10 MHz, 10-m Cable, 120-Ohm Termination without 200 pF

Measurements at 60-m Cable Length:

The jitter of the received differental-NRZ random data at the cable far end with 120-ohm termination at the maximum BiSS clock frequency of 10 Mhz is approximately 25% (0.75 UI-open). The steady state differential voltage is around ±2 V_{pp}. However, the rise or fall time from 10% to 90% is more than a clock cycle and the effective differential voltage in the eye is approximately only ±0.8 $V_{pp.}$

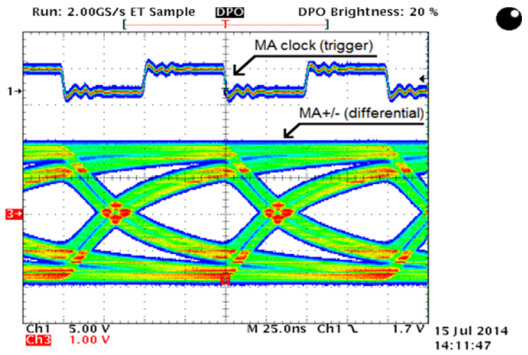

Figure 36. Eye Diagram HVD77 at Data Rate 10 MHz, 60-m Cable, 120-Ohm Termination with 220 pF

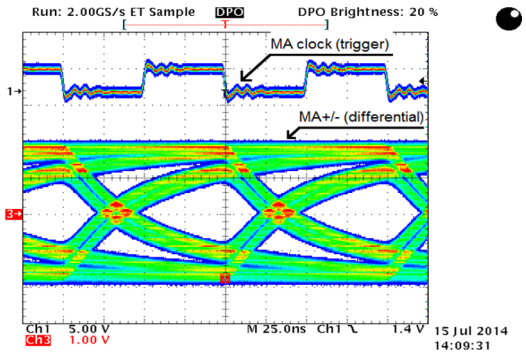

Figure 37. Eye Diagram HVD77 at Data Rate 10 MHz, 60-m Cable, 120-Ohm Termination without 220 pF

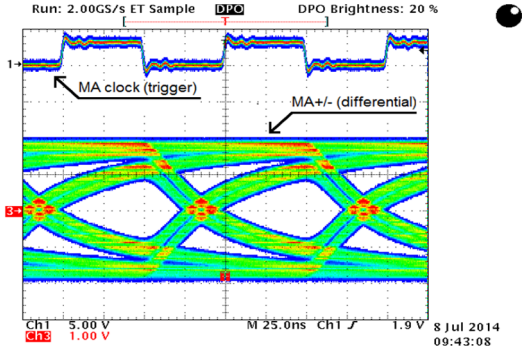

Figure 38. Eye Diagram HVD74 at Data Rate 10 MHz, 60-m Cable, 120-Ohm Termination with 220 pF

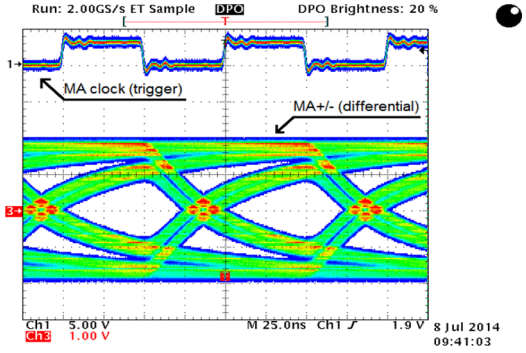

Figure 39. Eye Diagram HVD74 at Data Rate 10 MHz, 60-m Cable, 120-Ohm Termination without 220pF

Measurements at 85-m Cable Length

At 85 m, the maximum frequency was 7.4 Mhz. At the 7.4 Mhz frequency, the jitter of the received differential NRZ random data at the cable far end with 120-ohm termination was 35% (0.65 UI-open) and the steady state differential voltage was approximately ±1.8 V_{pp}. The rise or fall time from 10% to 90% is more than a clock cycle. The effective differential voltage in the eye is approximately only ±0.6 V_{pp}. An impact on the 220-pF bypass capacitor on the Master could not be seen at this length anymore, due to stronger impact on the cable.

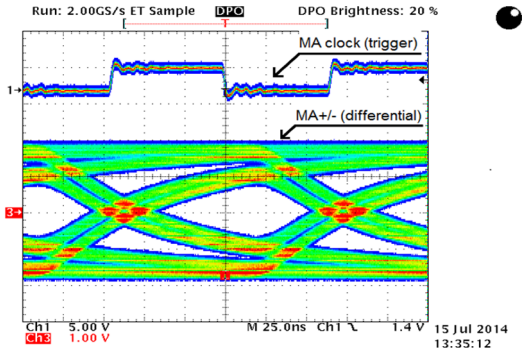

Figure 40. Eye Diagram HVD77 at Data Rate 7.4-MHz, 85-m Cable, 120-Ohm Termination with 220 pF

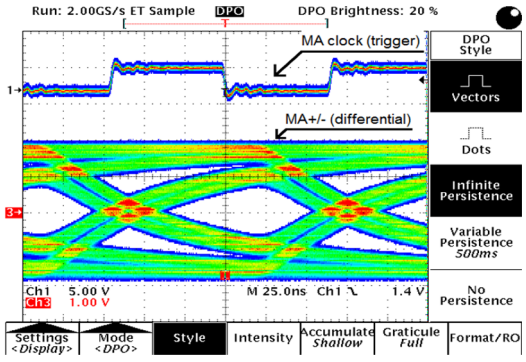

Figure 41. Eye Diagram HVD77 at Data Rate 7.4-MHz, 85-m Cable, 120-Ohm Termination without 220 pF

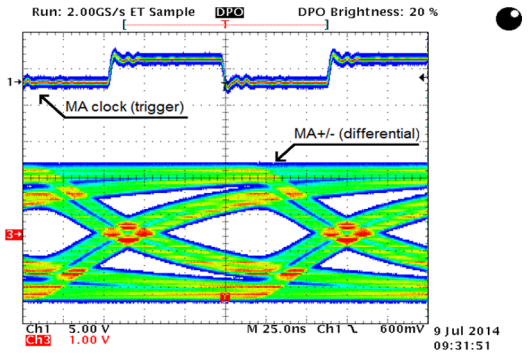

Figure 42. Eye Diagram HVD74 at Data Rate 7.4-MHz, 85-m Cable, 120-Ohm Termination with 220pF

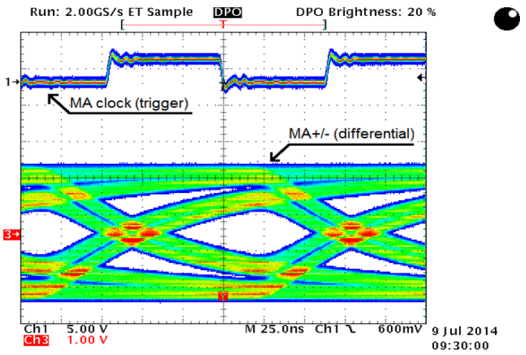

Figure 43. Eye Diagram HVD74 at Data Rate 7.4-MHz, 85-m Cable, 120-Ohm Termination without 220pF

RS485 Driver Output Single-Ended and Differential at Encoder Connector J4

Figure 44 and Figure 45 show the BiSS MA+ and MA- clock signal measured at the J4 encoder-connector (with the default 220-pF bypass caps) with a 10-m cable and a 120-ohm termination at the cable far end. Both signals were measured single-ended versus GND and differentially measured with a differential probe. The common mode voltage of MA+ (Ch1 black) is approximately 2 V, with the upper voltage 3 V, and the lower voltage 1 V. The differential voltage (MA+) – (MA-) is approximately ±2 V_{pp}.

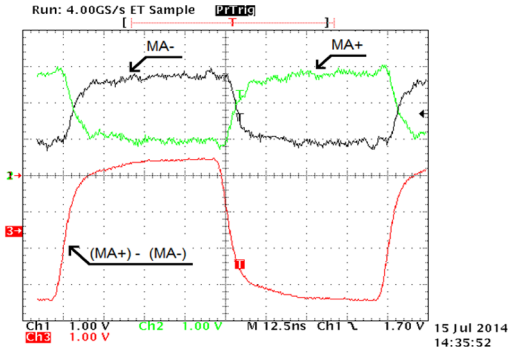

Figure 44. SN65HVD77 MA+, MA- Common Mode and Differential Voltage Measured at Connector J4

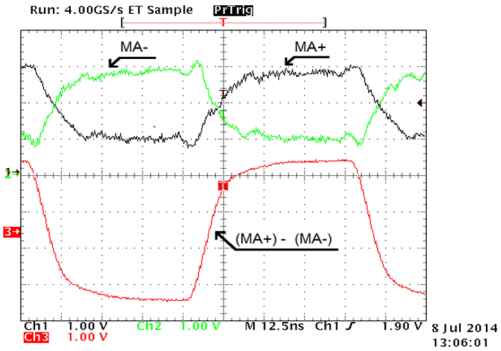

Figure 45. SN65HVD74 MA+, MA- Common Mode and Differential Voltage Measured at Connector J4

6.1.5 RS485 Driver and Receiver Propagation Delay

The RS485 driver and receiver-propagation delay was measured at the SN65HVD77 and SN65HVD74 terminals, respectively. Figure 46 shows the driver propagation-delay of the SN65HVD74 RS485 driver (Y, Z) and Figure 47 shows the receiver (A, B) with 120-ohm termination. The driver propagation-delay is measured from logic input to differential output for the driver and the opposite is measured for the receiver propagation delay.

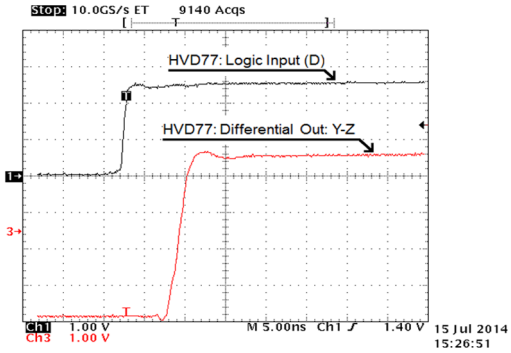

Figure 46. SN65HVD77 Driver Propagation Delay Ch1 (Black) = Logic Signal, Ch3 (Red) Differential Signal Y-Z or A-B

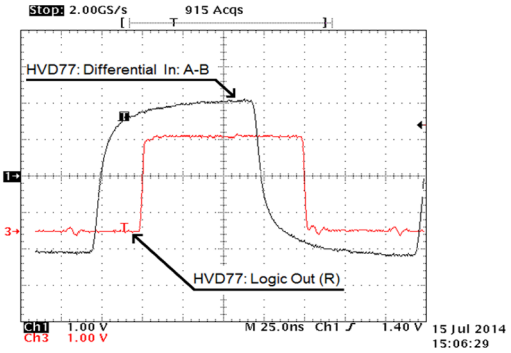

Figure 47. SN65HVD77 Receiver Propagation Delay Ch1 (Black) = Logic Signal, Ch3 (Red) Differential Signal Y-Z or A-B

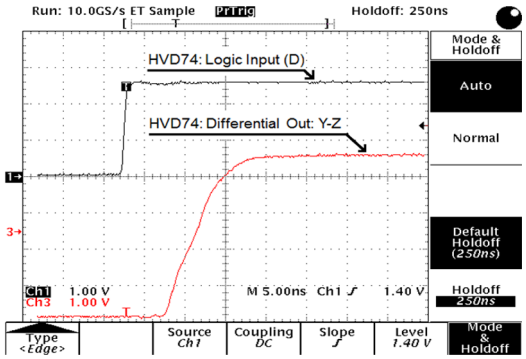

Figure 48. SN65HVD74 Driver Propagation Delay Ch1 (Black) = Logic Signal, Ch3 (Red) Differential Signal Y-Z or A-B

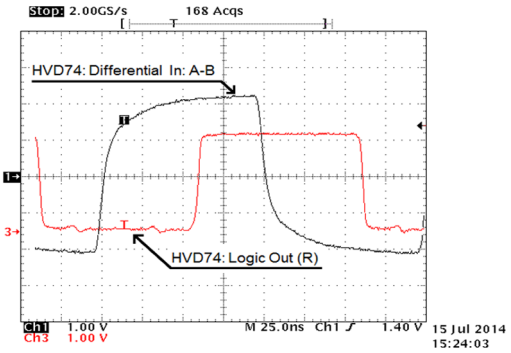

Figure 49. SN65HVD74 Receiver Propagation Delay Ch1 (Black) = Logic Signal, Ch3 (Red) Differential Signal Y-Z or A-B

6.2 Protected Encoder Power Supply Performance

6.2.1 Output Voltage Ripple

The output-voltage ripple of the encoder supply remains below 20 mV_{pp} over the entire output current range. Figure 50 and Figure 51 show the encoder-supply voltage ripple at 300-mA load current and 20-mA load current with the oscilloscope in AC-coupling mode. The ripple at 700-kHz switching frequency can hardly be seen.

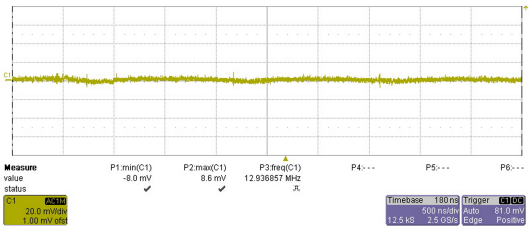

Figure 50. Encoder Supply Voltage Ripple at 24-V Input and 5.15-V Output with 300-mA Load

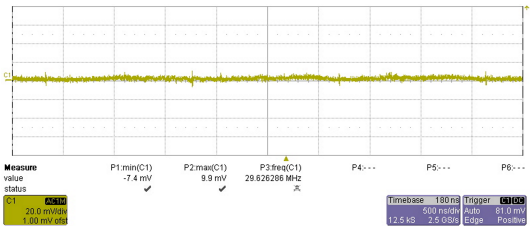

Figure 51. Encoder Supply Voltage Ripple at 24-V Input and 5.15-V Output with 100 mA Load

6.2.2 Output-Voltage Characteristics

Figure 52 and Figure 53 show the output voltage, depending load current, and input voltage. There is almost negligible impact on the output voltage at a 1% maximum. The output voltage stays well between 5.17 V and 5.12 V.

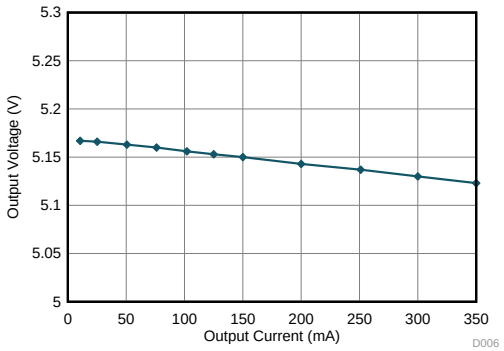

Figure 52. Output Voltage versus Output Current

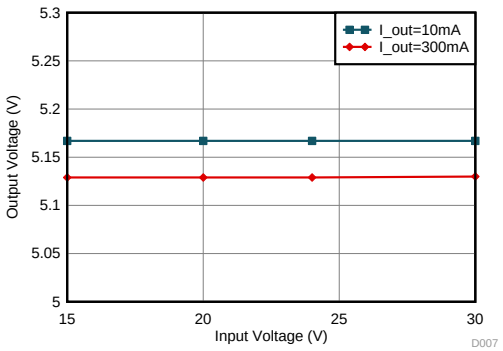

Figure 53. Output Voltage versus Input Voltage at 10-mA (Red) and 300-mA (Blue) Load Current

6.2.3 Efficiency

The efficiency was calculated by measuring the voltage and current through the 24-V input connector (J1) and the voltage and current through the encoder sub-D9 connector (J4).

Measuring through J1 and J4 means that this efficiency curve includes the input filter, the DC/DC converter (TPS54040A), and the eFuse (TPS24750). This design achieves 85% efficiency overall above 200-mA load current.

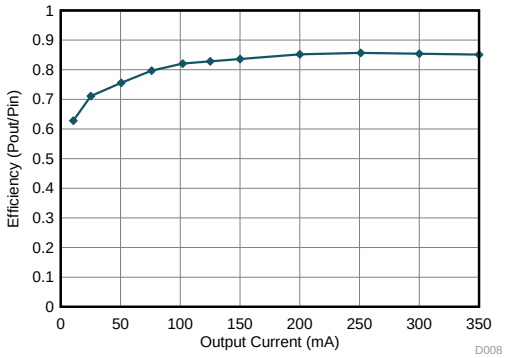

Figure 54. Efficiency of Protected-Encoder Power Supply

6.2.4 Startup

The start-up time of the output voltage at the encoder connector (J4), when enabled, is asserted is approximately 2 ms, mainly due to the soft start implemented in the TPS54040A (the soft start can be changed).

In Figure 55, the yellow curve is the enable signal, and the red curve is the output voltage at the encoder connector (J4).

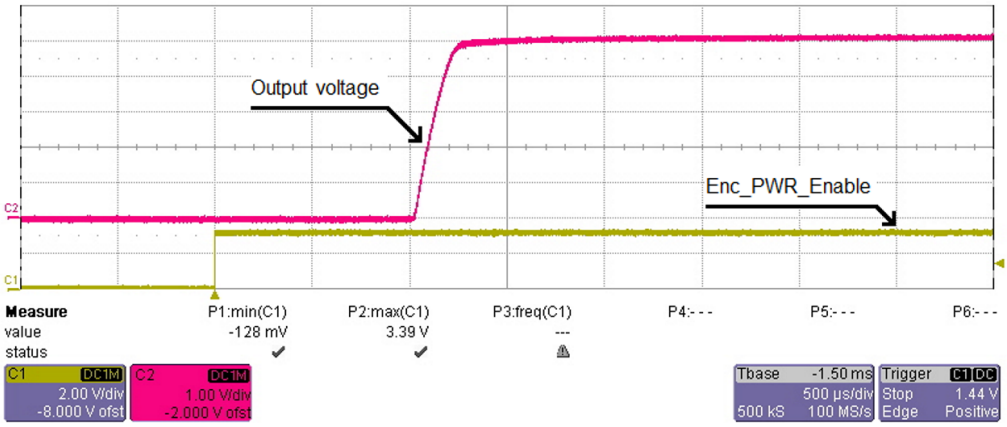

Figure 55. Output Voltage Ramp-Up (Red) with Enable Signal (Yellow) Asserted (Input: 24 V, Output: 5.2 V at 300 mA)

6.2.5 Shutdown

The shutdown time of the output voltage at the encoder connector (J4) is around 1 ms, mainly due to the output capacitors. In Figure 56, the yellow curve is the power supply enable signal and the red curve is the output voltage at the encoder connector (J4).

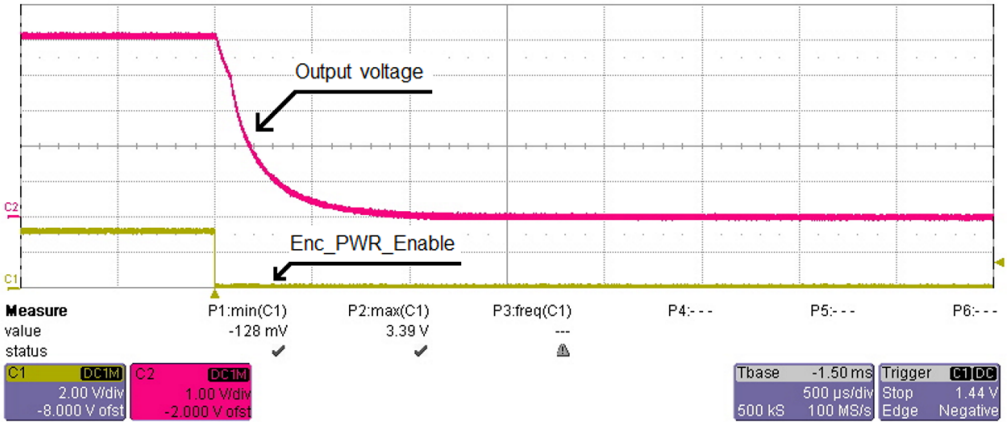

Figure 56. Output Voltage Ramp-Down (Red) with Enable Signal (Yellow) De-asserted (Input: 24 V, Output: 5.2 V at 300 mA)

6.2.6 Switch Node Waveforms

Here are the switch node waveforms at nominal load and a light load as shown in Figure 57 through Figure 62. These curves were measured across the diode D3.

At nominal output current, the state is in continuous conduction mode and the PWM duty cycle reflects the ratio between input voltage and output voltage.

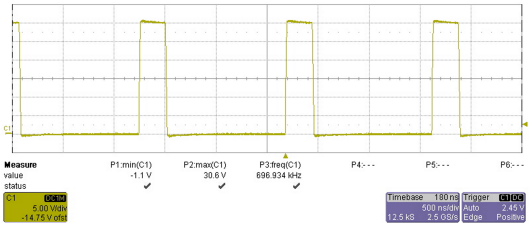

Figure 57. Voltage at Switch Node across D3: Input Voltage 30 V, Output Voltage 5.2 V, 300 mA

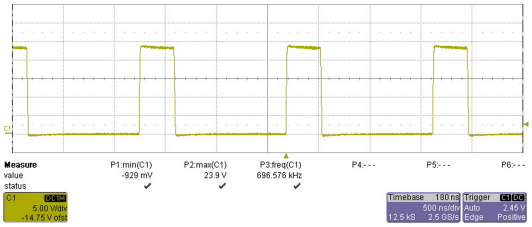

Figure 58. Voltage at Switch Node across D3: Input Voltage 24 V, Output Voltage 5.2 V, 300 mA

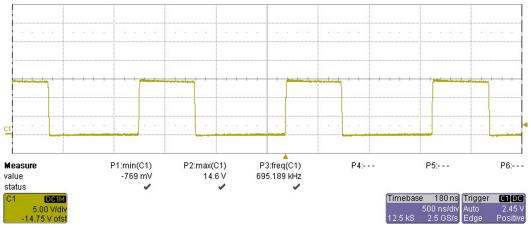

Figure 59. Voltage at Switch Node across D3: Input Voltage 15 V, Output Voltage 5.2 V, 300 mA

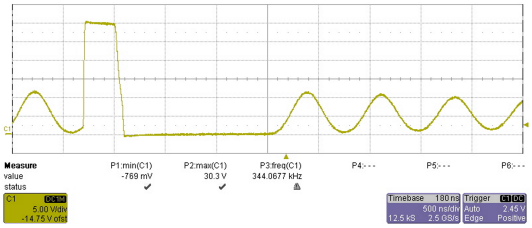

Figure 60. Voltage at Switch Node across D3: Input Voltage 30 V, Output Voltage 5.2 V, 10 mA

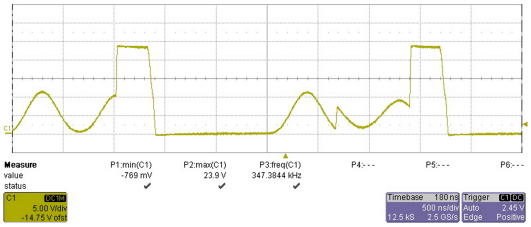

Figure 61. Voltage at Switch Node across D3: Input Voltage 24 V, Output Voltage 5.2 V, 10 mA

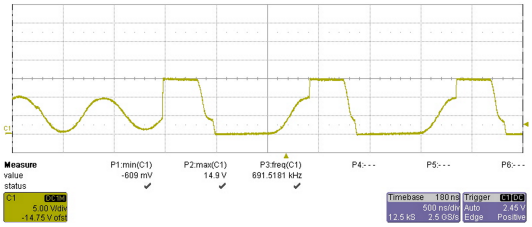

Figure 62. Voltage at Switch Node across D3: Input Voltage 15 V, Output Voltage 5.2 V, 10 mA

6.2.7 Bode Plots

The bode plot allows verifying that the loop is stable. A second order compensation has been implemented through R20, C17, and C16. The Bode plots have been measured for the 24-V nominal input voltage as well as for lower input voltage limit of 15 V and upper limit of 30 V. The output voltage was set to 5.2 V.

The values of the compensation circuit were calculated using the TIDA-00175 Design Calculator Excel sheet, described in Section 4.3. As shown in Table 14 and Figure 63 through Figure 65, there is enough phase and gain margin for the entire input voltage range.

Table 14. Phase and Gain Margin

	PHASE MARGIN	GAIN MARGIN
Input: 30 V, output: 5.2 V at 300 mA	81 degree	-25 dB
Input: 24 V, output :5.2 V at 300 mA	80 degree	-25 dB
Input: 15 V, output: 5.2 V at 300 mA	77 degree	-25 dB

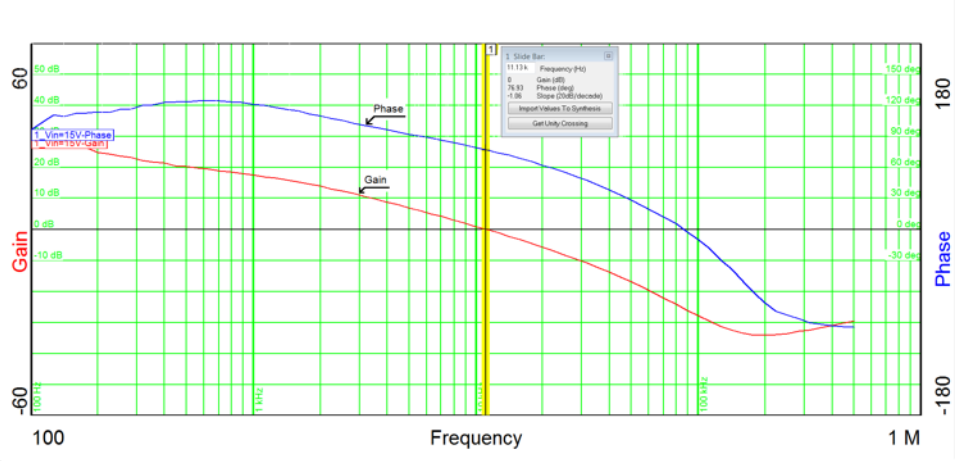

Figure 63. Bode Plot: Input Voltage: 15 V, Output 5.2 V , 300 mA

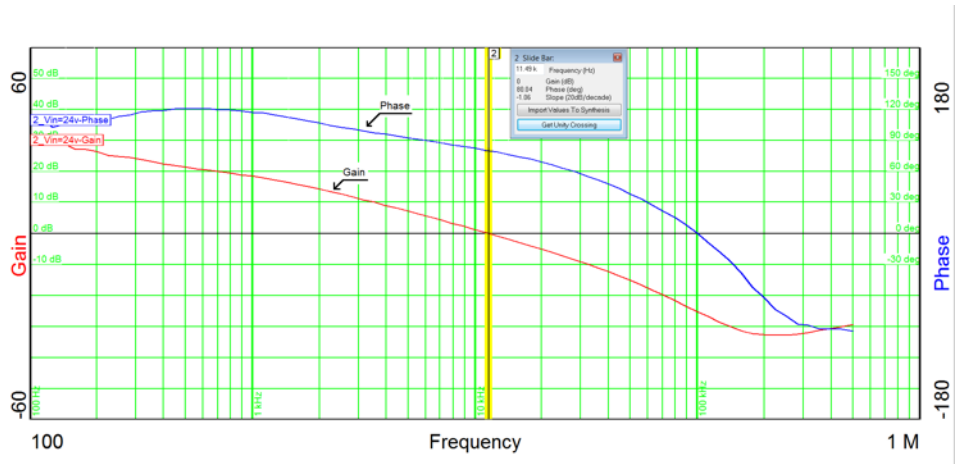

Figure 64. Bode Plot: Input Voltage: 24 V, Output 5.2 V, 300 mA

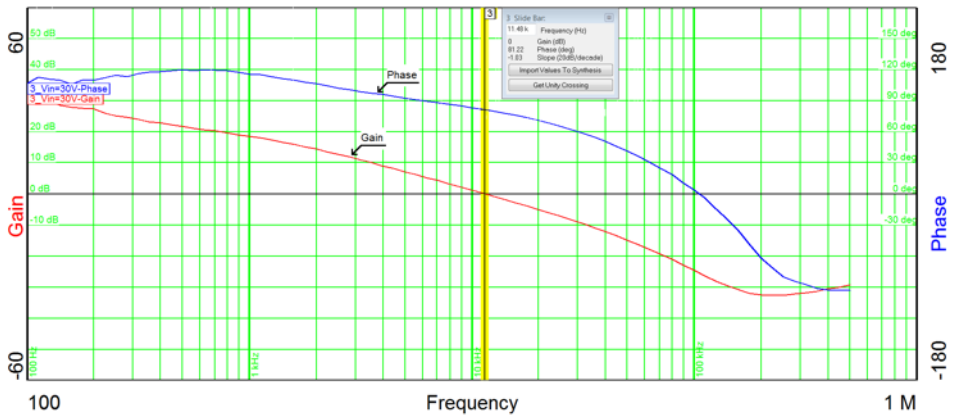

Figure 65. Bode Plot: Input Voltage: 30 V, Output 5.2 V, 300 mA

6.2.8 Overcurrent Protection Limit

The overcurrent limit was tested with nominal-input voltage and an electronic load. The load current was increased until the overcurrent protection was triggered.

NOTE: The eFUSE initially tripped at 340 mA at 25°C ambient temperature. The reason for the threshold being lower than expected was due to the PCB layout. The trace to the 0.05-ohm sense resistors R1 was shared with the output current path. This sharing led to an additional 0.01-ohm parasitic resistance in series to the sense resistor R1.

To compensate for for the threshold being lower than expected, the R_{IMON} resistor R5 was reduced from 1.69 kohm to 1.37 kohm. This reduction was applied for all the test measurements.

An improved layout guideline *Kelvin connection* can be found in Section 7.5 inFigure 91.

With the resistor change R5 = 1.69 kohm, the overcurrent measurement results are shown in Figure 66. The blue waveform is the current, measured with a current probe and 100-mA/V gain. Therefore, 40 mA equals 400 mA. The yellow signal is the overcurrent fault signal Enc_OC_Fault at connector J6. The red signal is the encoder-output voltage at connector J4.

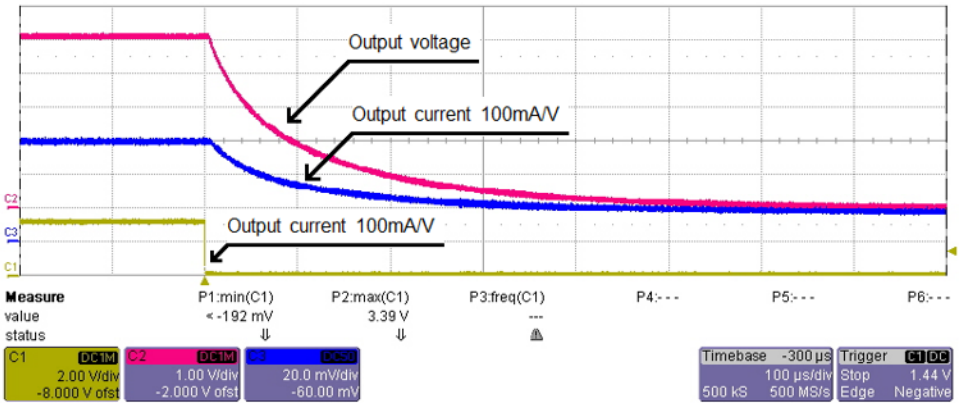

Figure 66. Output Voltage Shutdown (Red) During an Overcurrent Event (Current-Limit: 400 mA, Input: 24 V, Output: 5.2 V)

6.2.9 Overcurrent Fault Timer

The function of the overcurrent fault timer was tested during start-up by adding a resistive load of 1-ohm and 5-ohm, during which both drew more than the maximum current specified, as shown in Figure 67.

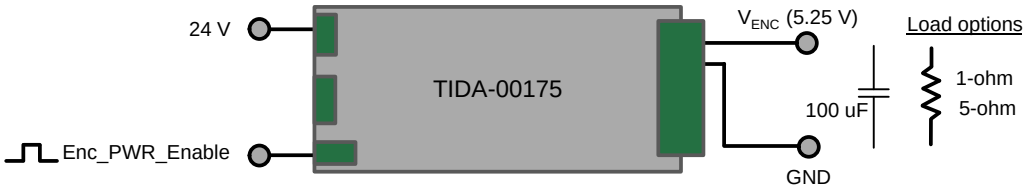

Figure 67. Test Setup for Inrush-Current and Overcurrent-Fault Timer Tests

Figure 68 and Figure 69 show that the current is limited to 400 mA in both cases until the fault timer expires after 4.5 ms and the eFUSE disconnects to prevent damage from the power supply. The current limits can also be seen as the supply voltage at the output of the encoder supply V+ drops accordingly.

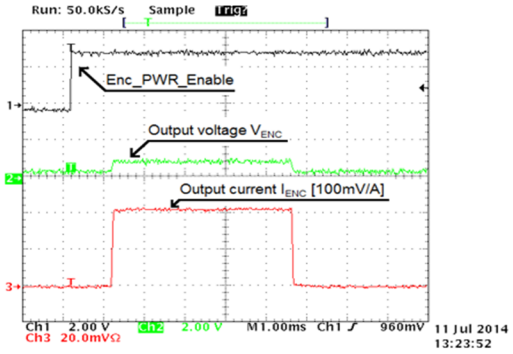

Figure 68. eFUSE Overcurrent Protection with Disconnect after 4.5 ms with 1-Ohm Load

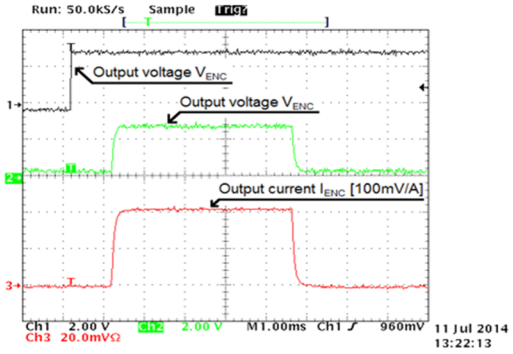

Figure 69. eFUSE Overcurrent Protection with Disconnect after 4.5 ms with 5-Ohm Load)

6.2.10 Inrush-Current Limitation

A 100-uF load capacitor was used to test the inrush-current limitation feature of the eFUSE. As shown in Figure 70, the eFUSE limits the inrush current to 400 mA until the capacitor is charged. The output voltage ramps up to nominal 5.25 V respectively. Therefore, hot plug-in is possible even with encoders which have a large bulk capacity. However, it will be required to adjust the fault timer accordingly to the maximum bulk-capacitive load to prevent unwanted fault trigger and disconnect during power-up. Ch1 is the Enc_PWR_Enable signal. Ch2 the encoder output voltage. Ch3 is the encoder output current measured with a current probe at 100-mV/A scale.

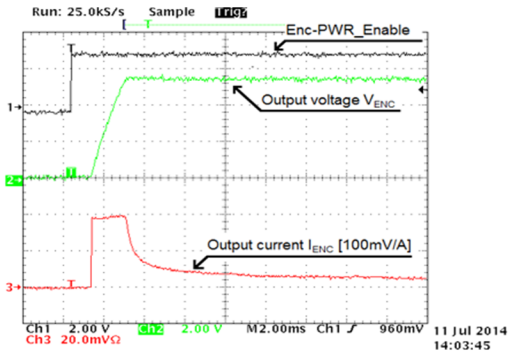

Figure 70. eFUSE: Inrush-Current Limitation with 100-uF Capacitive Load at Encoder Power Supply Startup

6.3 Performance Test with BiSS-C Encoder

6.3.1 Test Setup

For the system test with the TIDA-00175 analog interface and with the BAUMER GBPAS BiSS-C position encoder, the iC-Haus GmbH MB4U BiSS, SSI, PC-USB 2.0 ADAPTER was used. However, the iC-Haus GmbH MB4U BiSS, SSI, PC-USB 2.0 ADAPTER provides RS422 differential output. Therefore, an internal RS485-to-3.3-V TTL level shifter to connected to the TIDA-00175 design was added as shown in Figure 71 and Table 15.

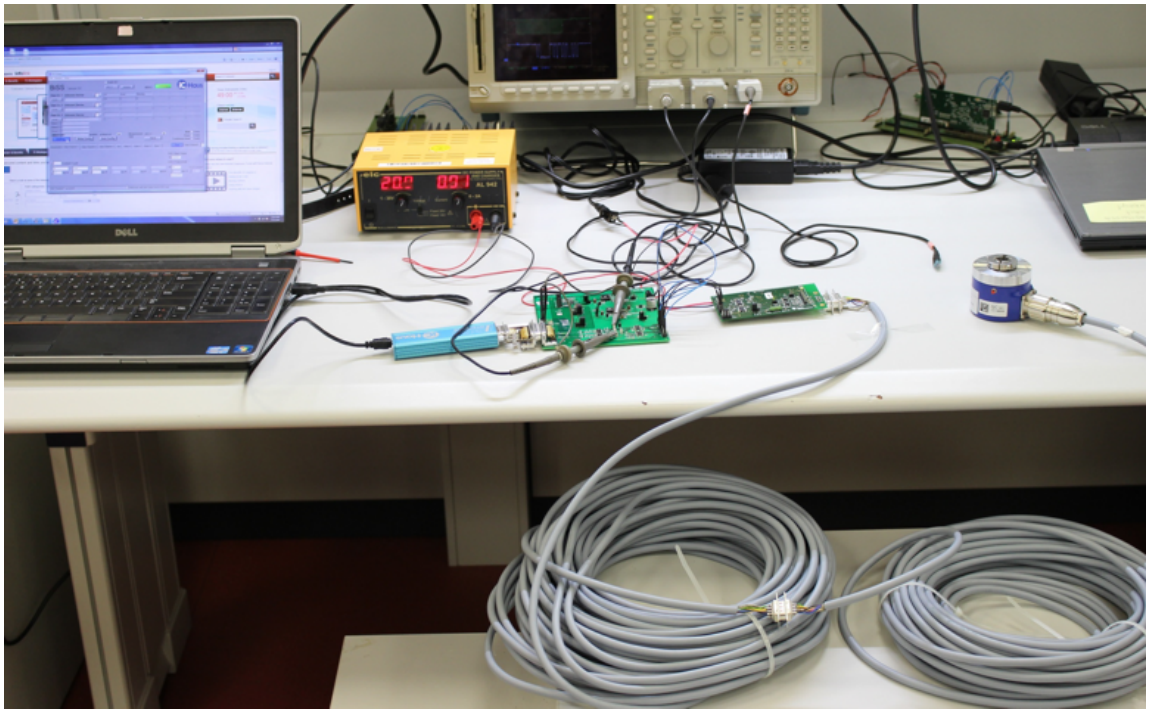

Figure 71. Picture of Test Setup for the TIDA-00175 Test with BAUMER Encoders

Table 15. Test Equipment

TEST EQUIPMENT	PART NUMBER
BiSS Position Encoder	Baumer GBPAS BiSS-C
BAUMER IVO PVC shielded cable (5 x 2 LiY 0.14mm2) with M23 female connector	Z 130.A02, Z 130.007
BiSS Master	iC-Haus GmbH MB4U BiSS, SSI, PC-USB 2.0 ADAPTER
RS485-to-3.3-V TTL level shifter	Internal TI EVM
BiSS Master GUI	iC-Haus GmbH BiSS Reader GUI version D2

6.3.2 Results

The Baumer GPBAS BISS-C position encoder was tested with 5-V DC [±10%] supply voltage.

Encoder Power Supply Startup — Inrush-Current Limitation

To verify the startup (inrush-current limitation) of the protected encoder power supply, the voltage was measured at the encoder subD-9 connector J4 pin 4 (V+) and pin 2 (signal V ±GND) directly connected to the BAUMER GBPAS BiSS-C encoder. The signal Enc_PWR_Enable was set, which enables the protected-encoder supply. The scope plot in Figure 72 shows the waveform with Enc_PWR_Enable on Ch2, the protected encoder output voltage on Ch1, and the encoder current on Ch3 with 100 mA/V. The inrush current is limited to 400 mA during the start-up and the output voltage rise was linear until 5.25 V, as expected.

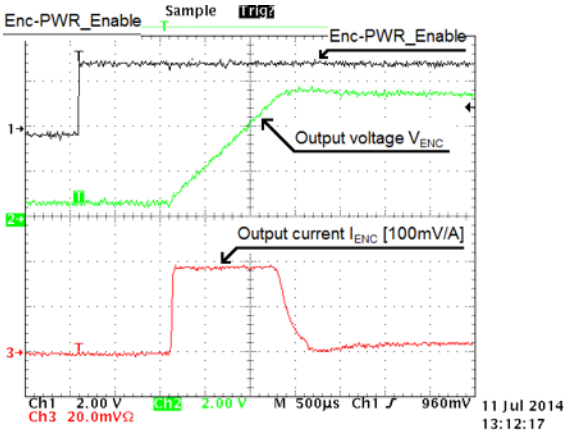

Figure 72. Protected-Encoder Power-Up with Baumer GBPAS BiSS-C Encoder

BiSS-C Master MA-Clock Frequency versus Cable Length with TIDA-00175

The BiSS maximum clock rate versus cable length with Baumer encoder and Baumer IVO cable is shown in Table 16. Due to the voltage drop across the Baumer IVO cable, tests were stopped after 60 m. For longer distances, encoder cables with larger wire gauges such as 0.5mm^2 (Baumer HEK8) are better suited. However, Baumer HEK8 was not available at the time of testing.

Table 16. BiSS-C Master MA-Clock Frequency versus Cable Length with TIDA-00175

CABLE LENGTH [m]	VOLTAGE AT ENCODER [V]	BISS RATE [MHz]	COMMENT
10	5.0	10	
25	4.7	10	
35	4.6	10	
45	4.5	10	
50	4.4	10	Below recommended operating supply range (1)
60	4.2	10	Below recommended operating supply range (1)

(1) Testing longer cables was not continued due to voltage drop across the 0.14 mm^2 wire gauge at cables longer than 60 m. For longer cables encoder cables with larger wires gauges such as 0.5mm^2 (Baumer HEK8) are better suited.

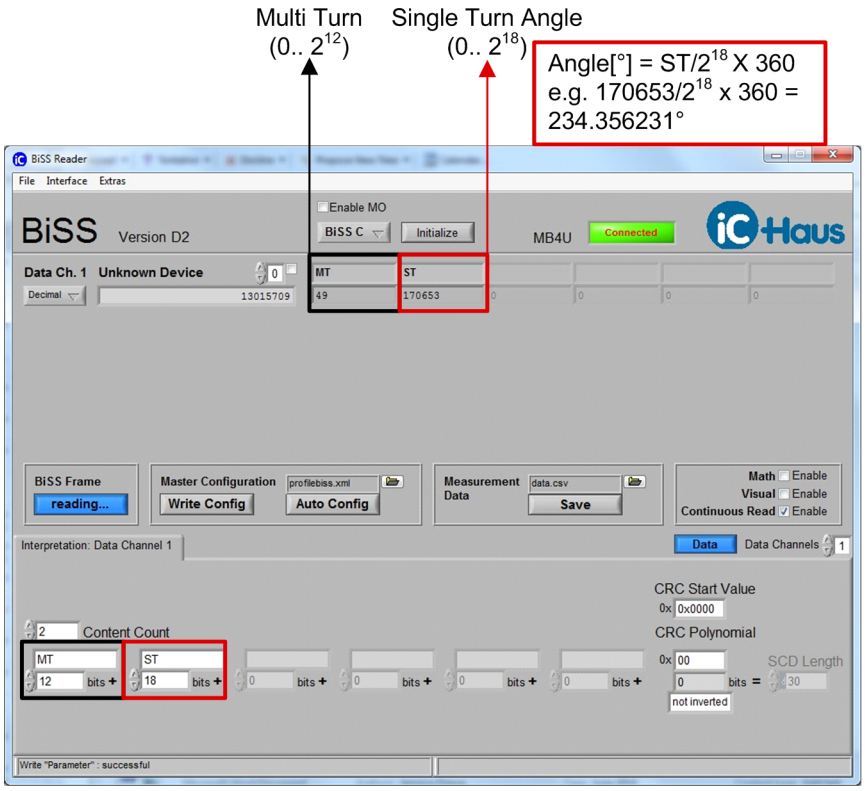

Figure 73. iC-Haus GmbH BiSS Master GUI

Figure 74 shows a BiSS frame measured at a MA-clock frequency of 10 MHz at the logic interface of the TIDA-00175. Figure 74 also shows the overall propagation delay at the BiSS Master. The overall propagation delay at the BiSS Master was approximately 1250 ns – 200 ns = 1050 ns.

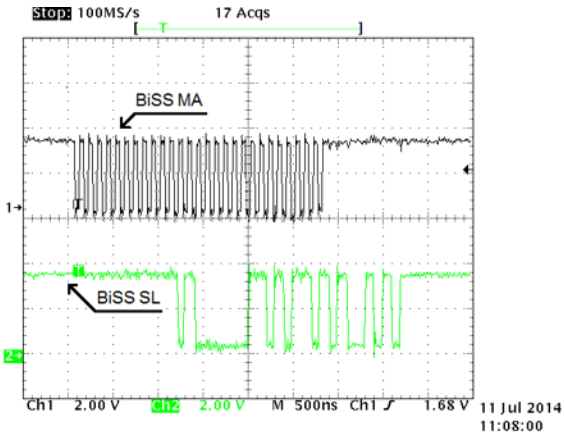

Figure 74. BiSS Frame at 10-MHz, MA-Clock Frequency, 60-m Cable Length: Measured at J2 Connector MA (Ch1) and SL (Ch2)

6.4 EMC Test Results

The design is tested according to IEC61800-3 for ESD, EFT, and Surge with reference to standard IEC61000-4-2, IEC61000-4-4, IEC61000-4-5, respectively. See the EMC test results document in the TIDA-00175 document folder at TIDA-00175.

7 Design Files

7.1 Schematics

To download the Schematics, see the design files at TIDA-00175.

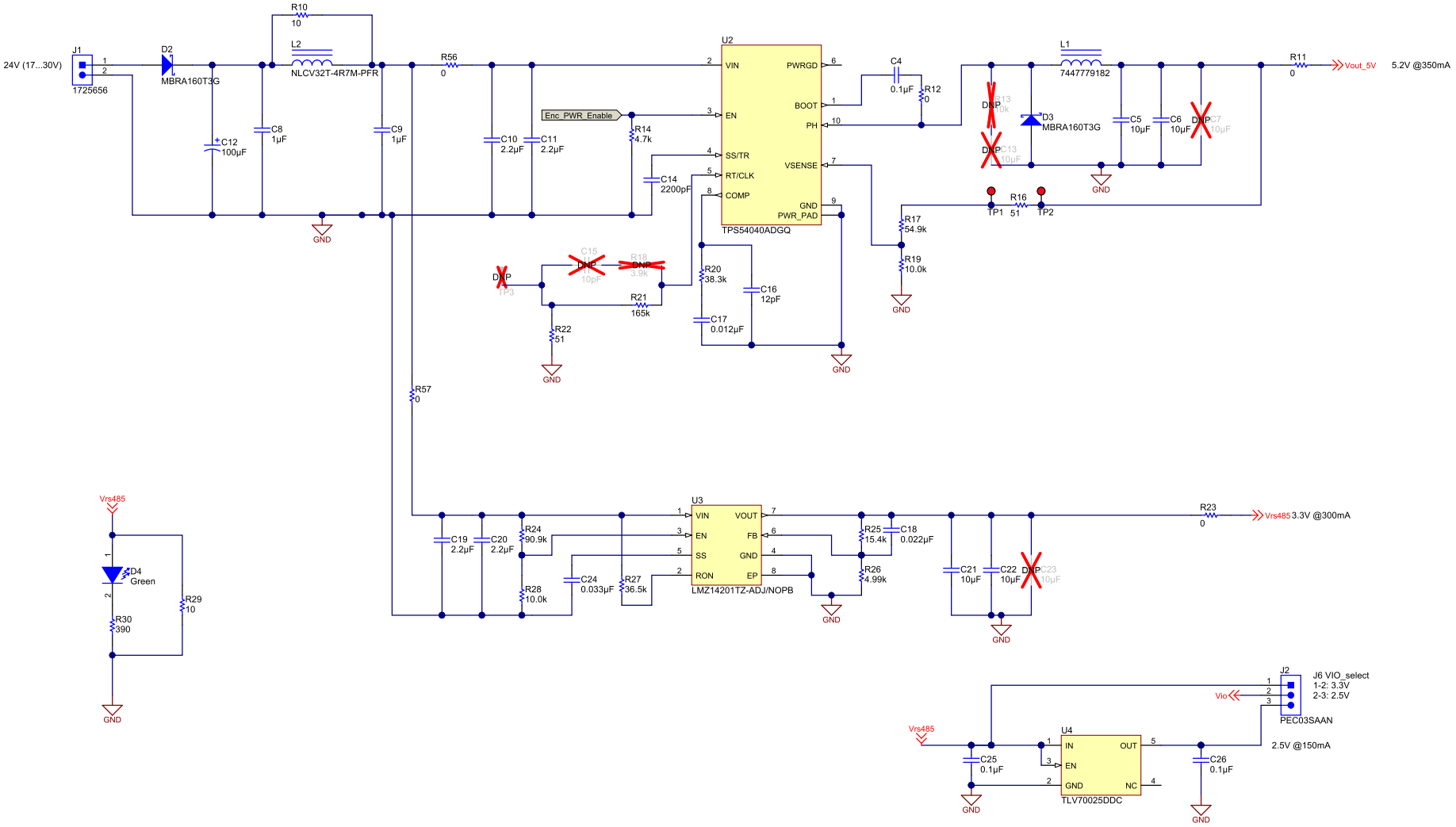

Figure 75. Power Supply

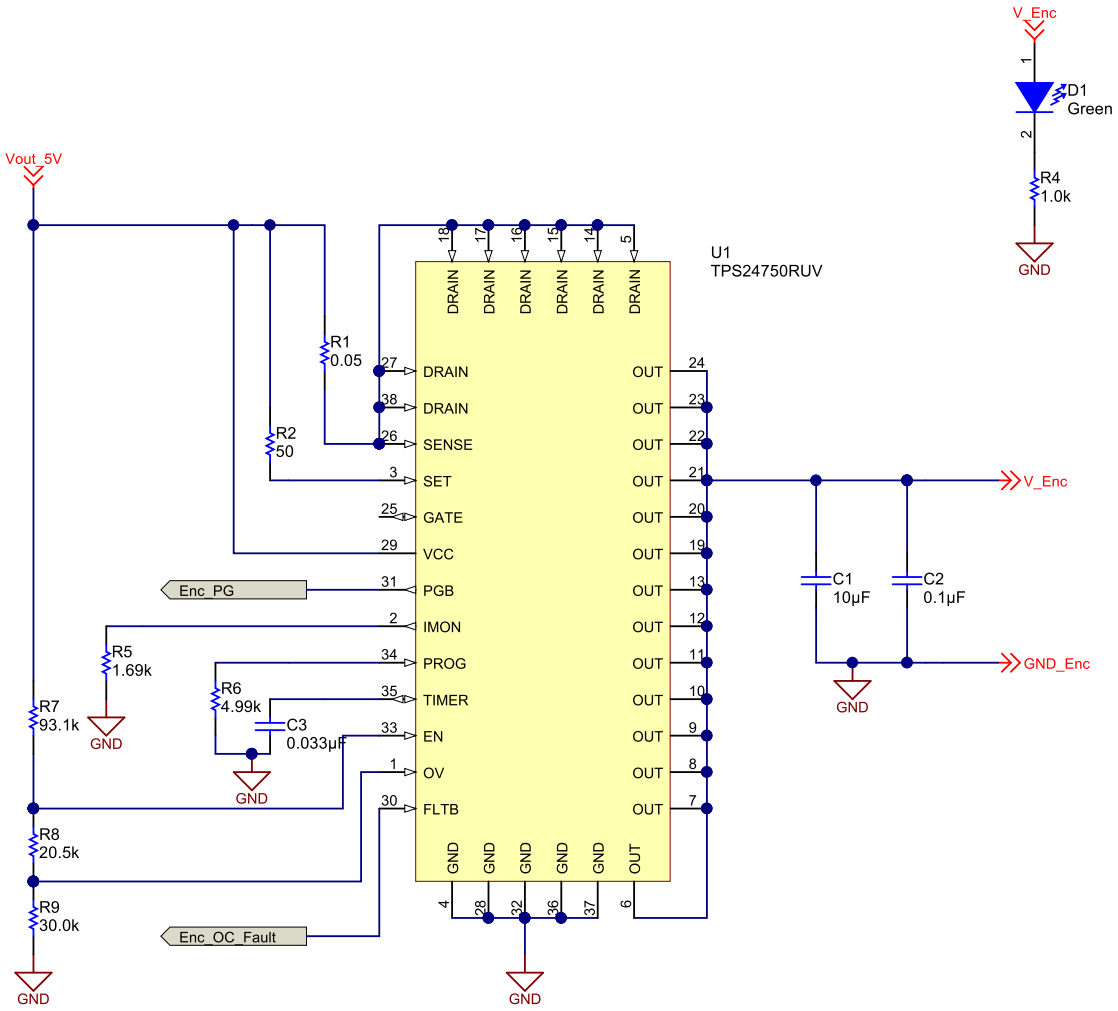

Figure 76. eFUSE

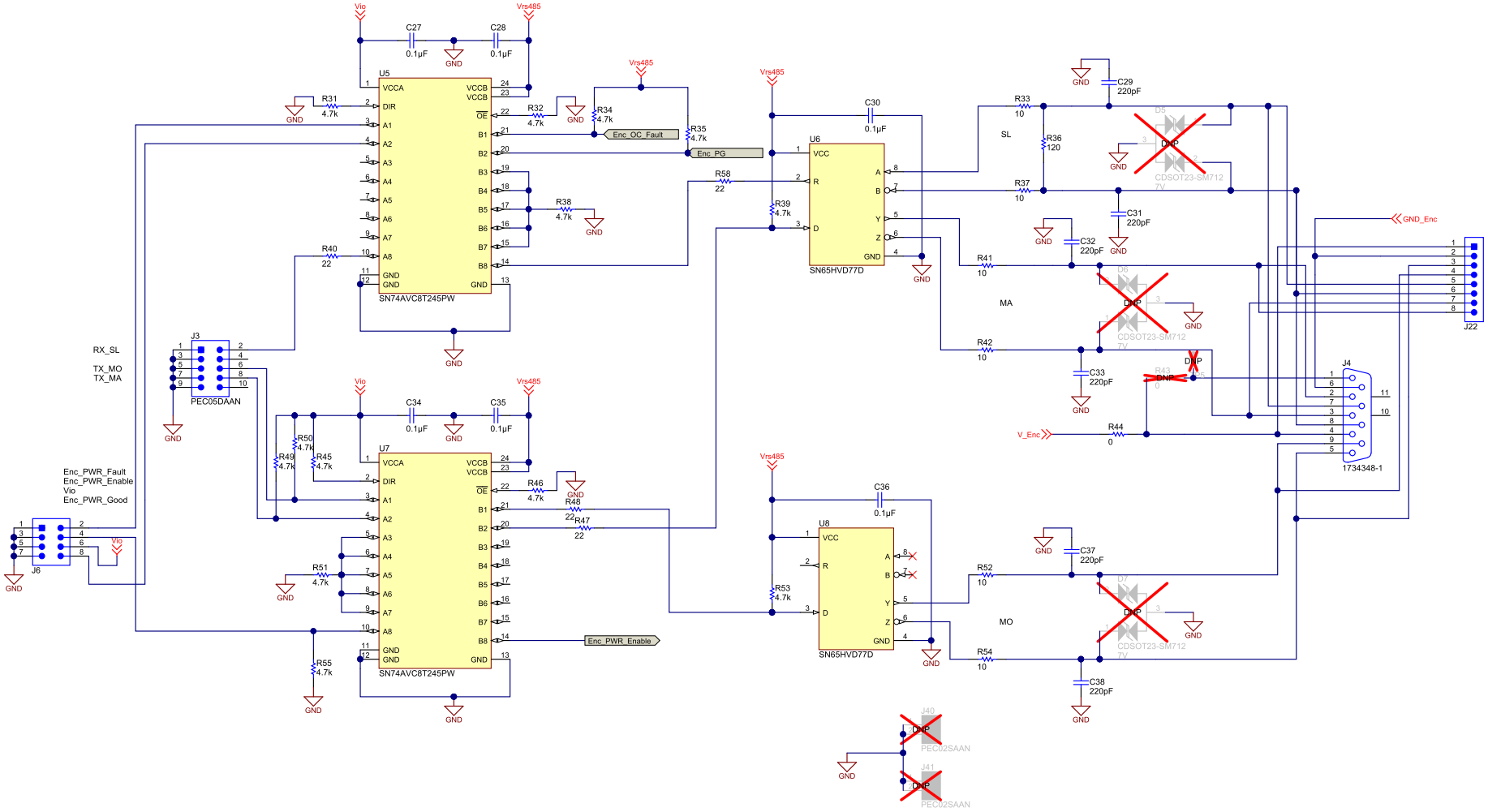

Figure 77. Signal Chain

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00175.

Table 17. BOM(1)

QUANTITY	DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGEREFERENCE	FITTED
3	C1, C5, C6	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 0805	TDK	C2012X5R1E106K125AB	0805	Fitted
4	C10, C11, C19, C20	2.2uF	CAP, CERM, 2.2uF, 50V, +/-10%, X5R, 1206	MuRata	GRM31CR61H225KA88L	1206	Fitted
1	C12	100uF	CAP, AL, 100uF, 63V, +/-20%, 0.35 ohm, SMD	Panasonic	EEE-FK1J101P	SMT Radial G	Fitted
1	C14	2200pF	CAP, CERM, 2200pF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C222KA01D	0603	Fitted
1	C16	12pF	CAP, CERM, 12pF, 50V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C1H120JA01D	0603	Fitted
1	C17	0.012uF	CAP, CERM, 0.012uF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H123KA01D	0603	Fitted
1	C18	0.022uF	CAP, CERM, 0.022uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C223KA01D	0603	Fitted
1	C2	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	TDK	C1608X7R1E104K	0603	Fitted
2	C21, C22	10uF	CAP, CERM, 10uF, 10V, +/-20%, X5R, 0603	TDK	C1608X5R1A106M	0603	Fitted
1	C24	0.033uF	CAP, CERM, 0.033uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C333KA01D	0603	Fitted
6	C27, C28, C30, C34, C35, C36	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X5R, 0603	AVX	06033D104KAT2A	0603	Fitted
6	C29, C31, C32, C33, C37, C38	220pF	CAP, CERM, 220pF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H221KA01D	0603	Fitted
1	C3	0.033uF	CAP, CERM, 0.033uF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H333KA61D	0603	Fitted
3	C4, C25, C26	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X5R, 0603	MuRata	GRM188R61C104KA01D	0603	Fitted
2	C8, C9	1uF	CAP, CERM, 1uF, 50V, +/-10%, X7R, 0805	MuRata	GRM21BR71H105KA12L	0805	Fitted
2	D1, D4	Green	LED, Green, SMD	OSRAM	LG L29K-G2J1-24-Z	1.7x0.65x0.8mm	Fitted
2	D2, D3	60V	Diode, Schottky, 60V, 1A, SMA	ON Semiconductor	MBRA160T3G	SMA	Fitted
1	J1		Header, 2 Pos, 6A, 63V, TH	Phoenix Contact	1725656	6.2x8.5x5.54 mm	Fitted
1	J2		Header, 100mil, 3x1, Tin plated, TH	Sullins Connector Solutions	PEC03SAAN	Header, 3 PIN, 100mil, Tin	Fitted

(1) Substitutions made according to Alternate PartNumber must meet data sheet parameters, not just the Description specified.

Table 17. BOM[(1)] (continued)

QUANTITY	DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGEREFERENCE	FITTED
1	J22		Header, 8x1, 100mil, Tin, TH	Sullins Connector Solutions	PEC08SAAN	Header, 8x1, 100mil, TH	Fitted
1	J3		Header, 100mil, 5x2, Tin plated, TH	Sullins Connector Solutions	PEC05DAAN	Header, 5x2, 100mil, Tin	Fitted
1	J4		Conn D-SUB RCPT R/A 9POS GOLD/FL, TH	TE Connectivity	1734348-1	D-SUB 9 PIN	Fitted
1	J6		Header, 100mil, 4x2, Tin plated, TH	Sullins Connector Solutions	PEC04DAAN	Header, 4x2, 100mil, Tin	Fitted
1	L1	82uH	Inductor, Shielded Drum Core, Ferrite, 82uH, 0.84A, 0.25 ohm, SMD	Wurth Elektronik eiSos	7447779182	WE-PD-M	Fitted
1	L2	4.7uH	Inductor, Wirewound, Ferrite, 4.7uH, 0.9A, 0.2 ohm, SMD	TDK	NLCV32T-4R7M-PFR	3.2x2.2x2.5mm	Fitted
1	R1	0.05	RES, 0.05 ohm, 1%, 0.1W, 0603	Panasonic	ERJ-L03KF50MV	0603	Fitted
7	R10, R33, R37, R41, R42, R52, R54	10	RES, 10 ohm, 5%, 0.25W, 0603	Vishay-Dale	CRCW060310R0JNEAHP	0603	Fitted
6	R11, R12, R23, R44, R56, R57	0	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Fitted
14	R14, R31, R32, R34, R35, R38, R39, R45, R46, R49, R50, R51, R53, R55	4.7k	RES, 4.7k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06034K70JNEA	0603	Fitted
2	R16, R22	51	RES, 51 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060351R0JNEA	0603	Fitted
1	R17	54.9k	RES, 54.9k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060354K9FKEA	0603	Fitted
2	R19, R28	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	0603	Fitted
1	R2	50	RES, 50 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060350R0FKEA	0603	Fitted
1	R20	38.3k	RES, 38.3k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060338K3FKEA	0603	Fitted
1	R21	165k	RES, 165k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603165KFKEA	0603	Fitted
1	R24	90.9k	RES, 90.9k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060390K9FKEA	0603	Fitted
1	R25	15.4k	RES, 15.4k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060315K4FKEA	0603	Fitted
1	R27	36.5k	RES, 36.5k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060336K5FKEA	0603	Fitted
1	R29	10	RES, 10 ohm, 5%, 3W, TH	Vishay Draloric	AC03000001009JAC00	Axial resistor	Fitted
1	R30	390	RES, 390 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603390RJNEA	0603	Fitted
1	R36	120	RES, 120 ohm, 5%, 0.5W, 0805	Panasonic	ERJ-P06J121V	0805	Fitted
1	R4	1.0k	RES, 1.0k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031K00JNEA	0603	Fitted
4	R40, R47, R48, R58	22	RES, 22 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060322R0JNEA	0603	Fitted

Table 17. BOM[(1)] (continued)

QUANTITY	DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGEREFERENCE	FITTED
1	R5	1.69k	RES, 1.69k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031K69FKEA	0603	Fitted
2	R6, R26	4.99k	RES, 4.99k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K99FKEA	0603	Fitted
1	R7	93.1k	RES, 93.1k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060393K1FKEA	0603	Fitted
1	R8	20.5k	RES, 20.5k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060320K5FKEA	0603	Fitted
1	R9	30.0k	RES, 30.0k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0730KL	0603	Fitted
2	TP1, TP2	Red	Test Point, Miniature, Red, TH	Keystone	5000	Red Miniature Testpoint	Fitted
1	U1		2.5 to 18 V Positive Voltage 10A Integrated Hot-Swap Controller, RUV0036A	Texas Instruments	TPS24750RUV	RUV0036A	Fitted
1	U2		0.5 A, 42 V Step Down DC/DC Converter with Eco-mode, DGQ0010D	Texas Instruments	TPS54040ADGQ	DGQ0010D	Fitted
1	U3		1A SIMPLE SWITCHER® Power Module with 42V Maximum Input, 7 pin TO-PMOD	National Semiconductor	LMZ14201TZ-ADJ/NOPB	TZA07A	Fitted
1	U4		200-mA, Low-IQ, LDO Regulator for Portable Devices, DDC0005A	Texas Instruments	TLV70025DDC	DDC0005A	Fitted
2	U5, U7		8-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS, PW0024A	Texas Instruments	SN74AVC8T245PW	PW0024A	Fitted
2	U6, U8		3.3-V Full-Duplex RS-485 Transceivers With ±12-kV IEC ESD, D0008A	Texas Instruments	SN65HVD77D	D0008A	Fitted
0	C13	10uF	CAP, CERM, 10uF, 6.3V, +/-20%, X5R, 0603	MuRata	GRM188R60J106ME47D	0603	Not Fitted
0	C15	10pF	CAP, CERM, 10pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H100D	0603	Not Fitted
0	C23	10uF	CAP, CERM, 10uF, 10V, +/-20%, X5R, 0603	TDK	C1608X5R1A106M	0603	Not Fitted
0	C7	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 0805	TDK	C2012X5R1E106K125AB	0805	Not Fitted
0	D5, D6, D7	7V	Diode, TVS, Bi, 7V, 400W, SOT-23	Bourns	CDSOT23-SM712	SOT-23	Not Fitted
0	J40, J41		Header, 100mil, 2x1, Tin plated, TH	Sullins Connector Solutions	PEC02SAAN	Header, 2 PIN, 100mil, Tin	Not Fitted
0	R13	10k	RES, 10k ohm, 5%, 0.125W, 0805	Vishay-Dale	CRCW080510K0JNEA	0805	Not Fitted
0	R18	3.9k	RES, 3.9k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06033K90JNEA	0603	Not Fitted
0	R43	0	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Not Fitted
0	TP3	White	Test Point, Miniature, White, TH	Keystone	5002	White Miniature Testpoint	Not Fitted
0	TP5	Red	Test Point, Miniature, Red, TH	Keystone	5000	Red Miniature Testpoint	Not Fitted

7.3 Layer Plots

To download the layer plots, see the design files at TIDA-00175.

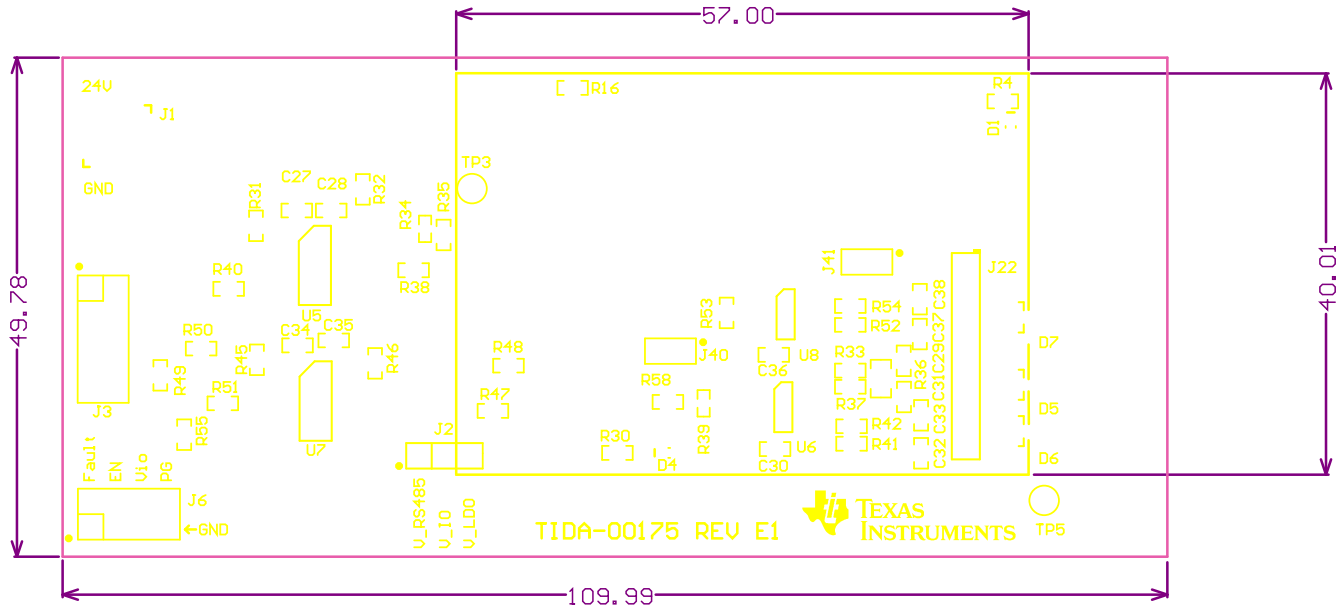

Figure 78. Top Overlay

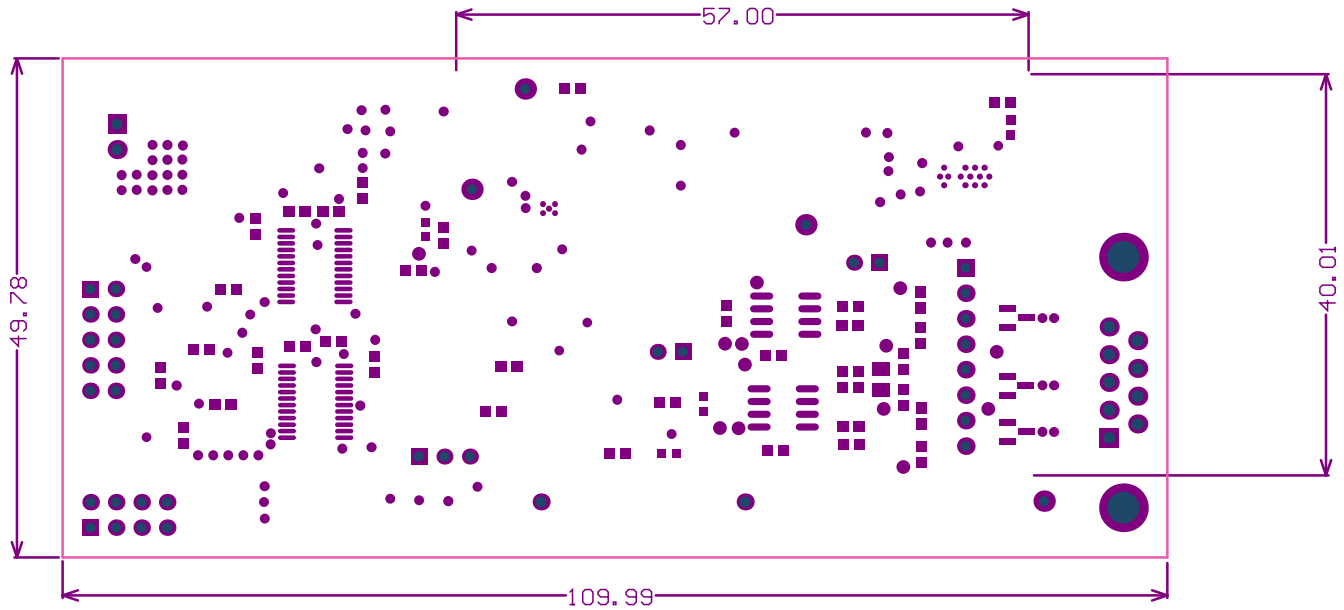

Figure 79. Top Solder Mask

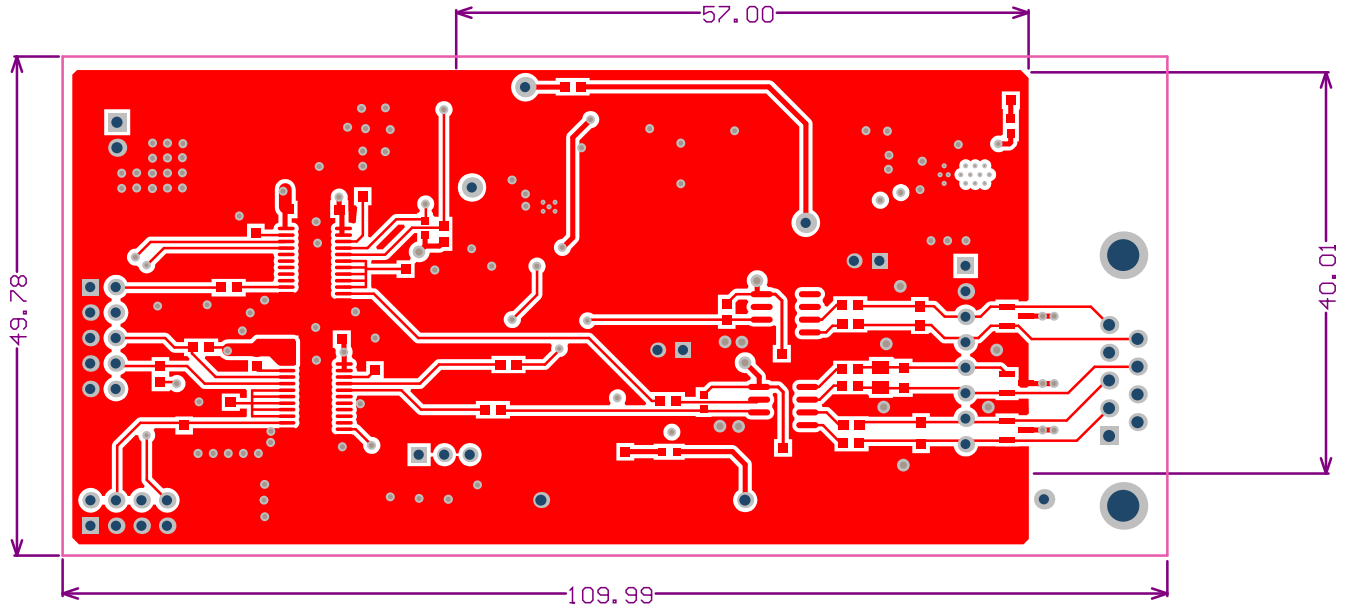

Figure 80. Top Layer

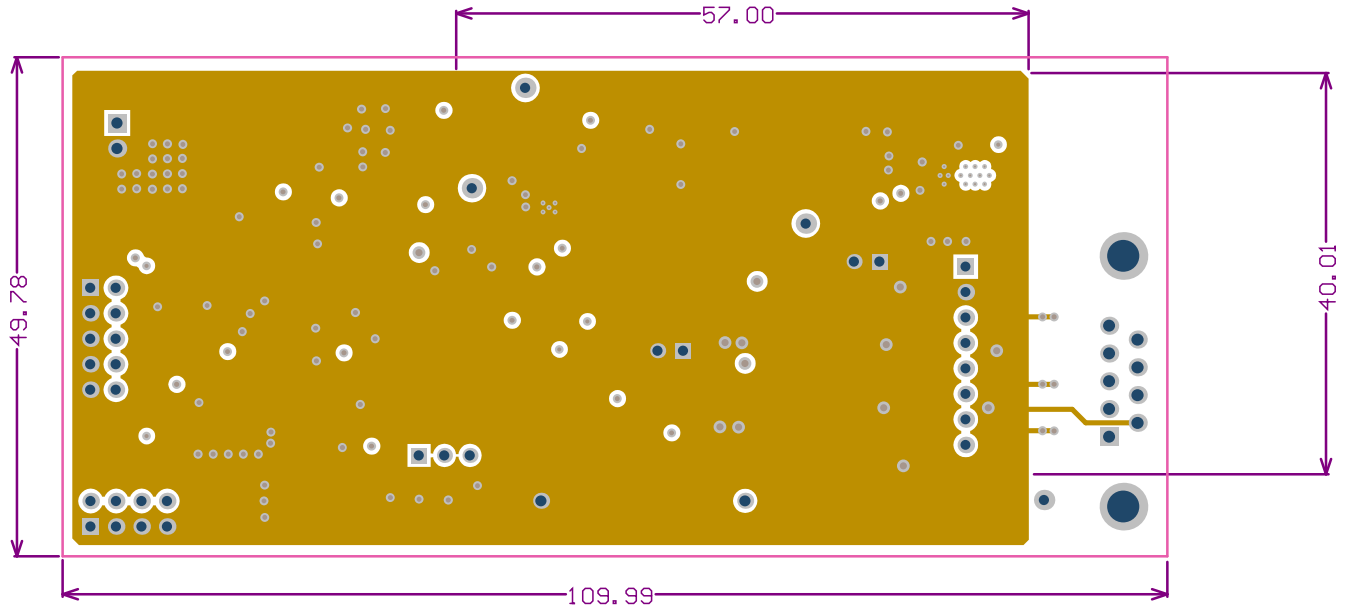

Figure 81. Mid Layer 1: GND

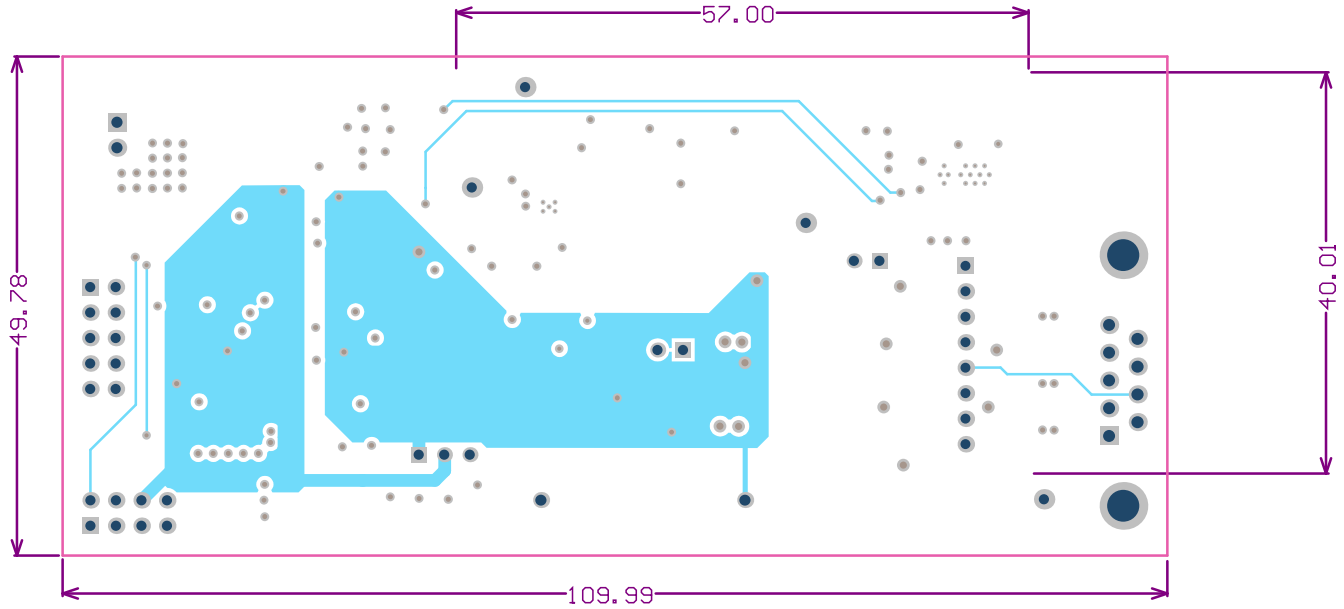

Figure 82. Mid Layer 2: Supply Plane

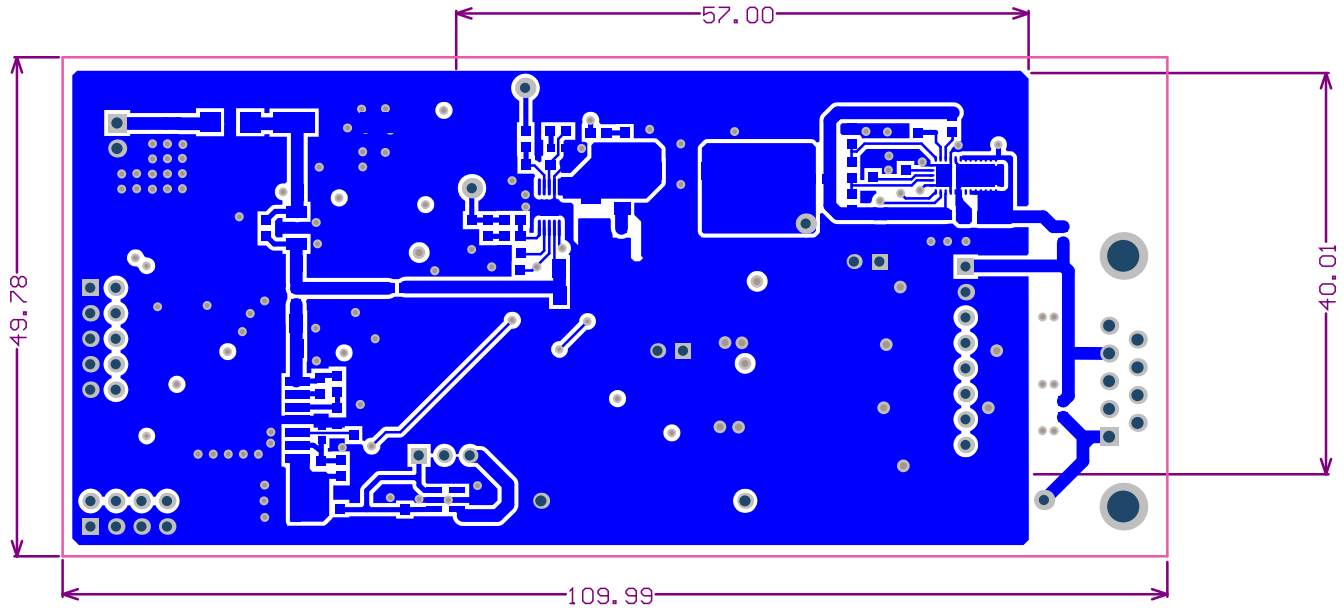

Figure 83. Bottom Layer

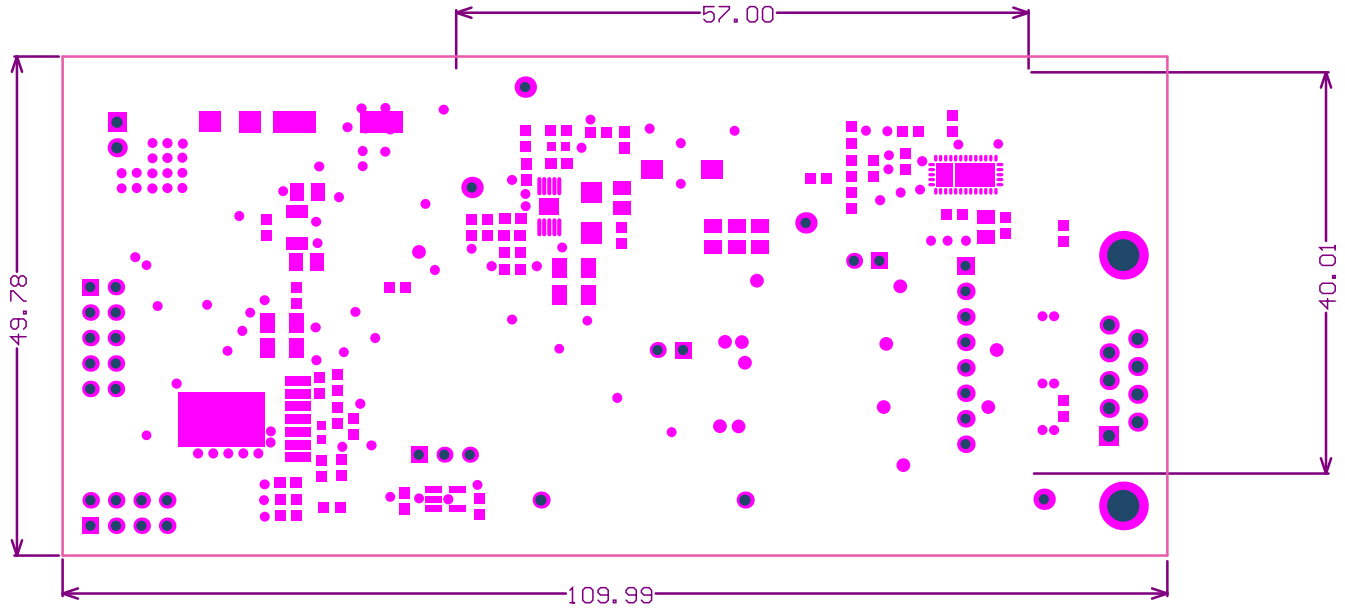

Figure 84. Bottom Solder Mask

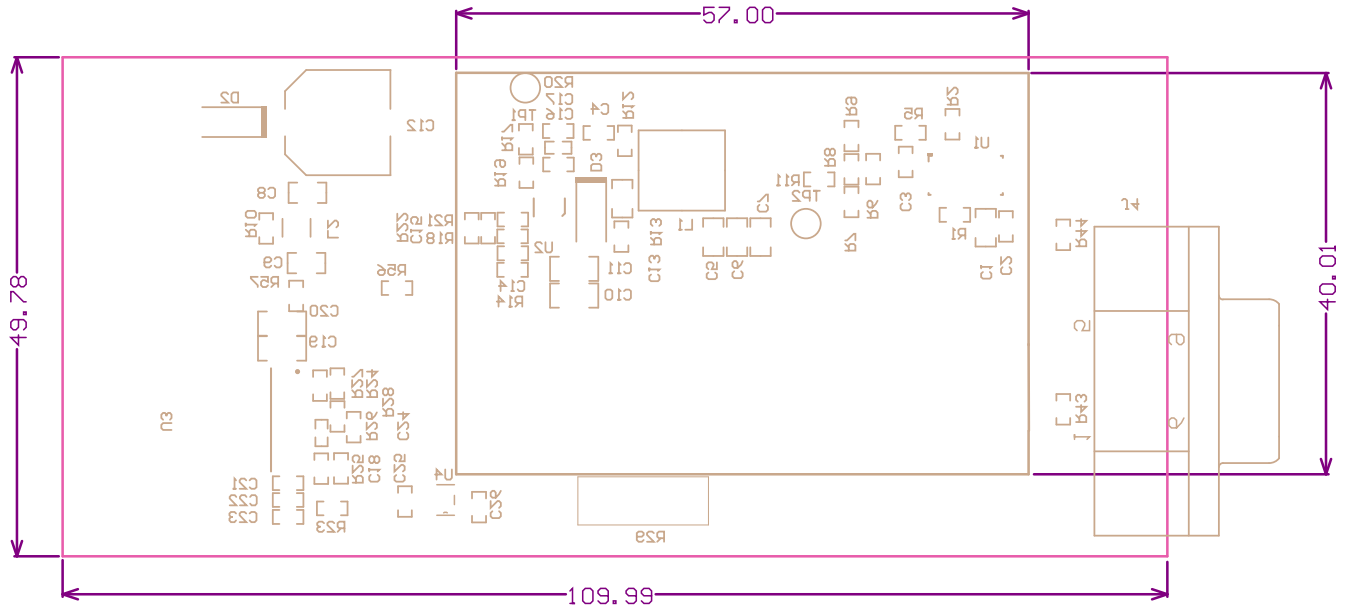

Figure 85. Bottom Overlay

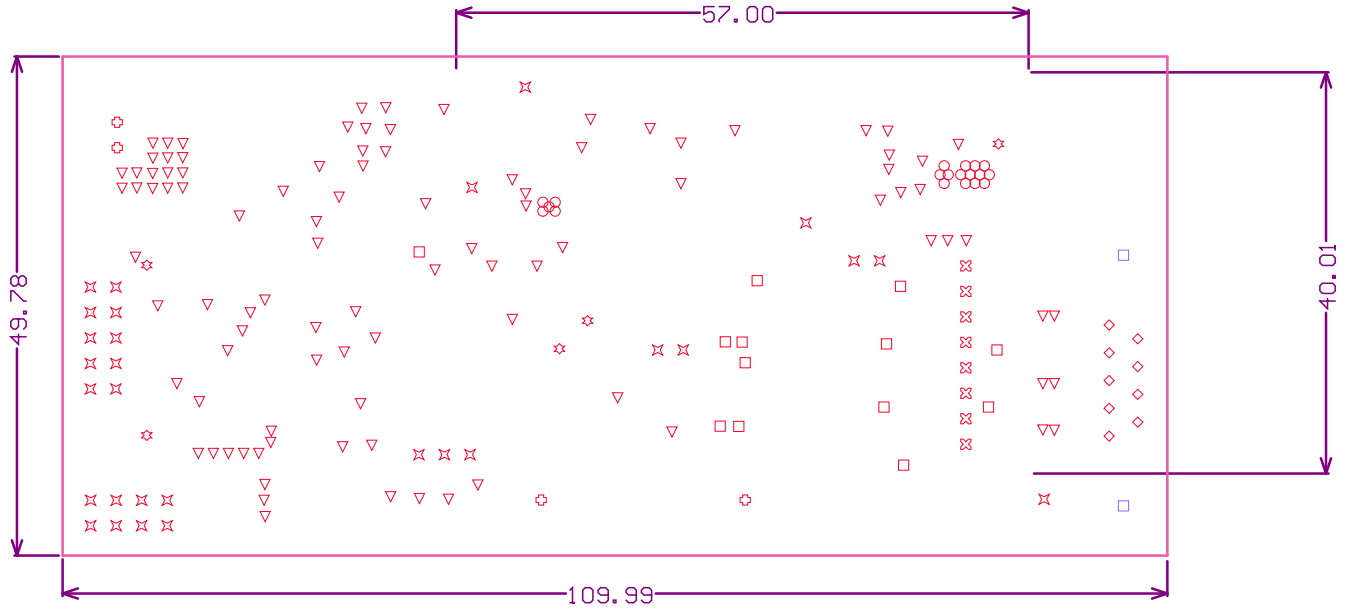

Figure 86. Drill Drawing

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00175.

7.5 Layout Guidelines

To download the Layout Guidelines, see the design files at TIDA-00175.

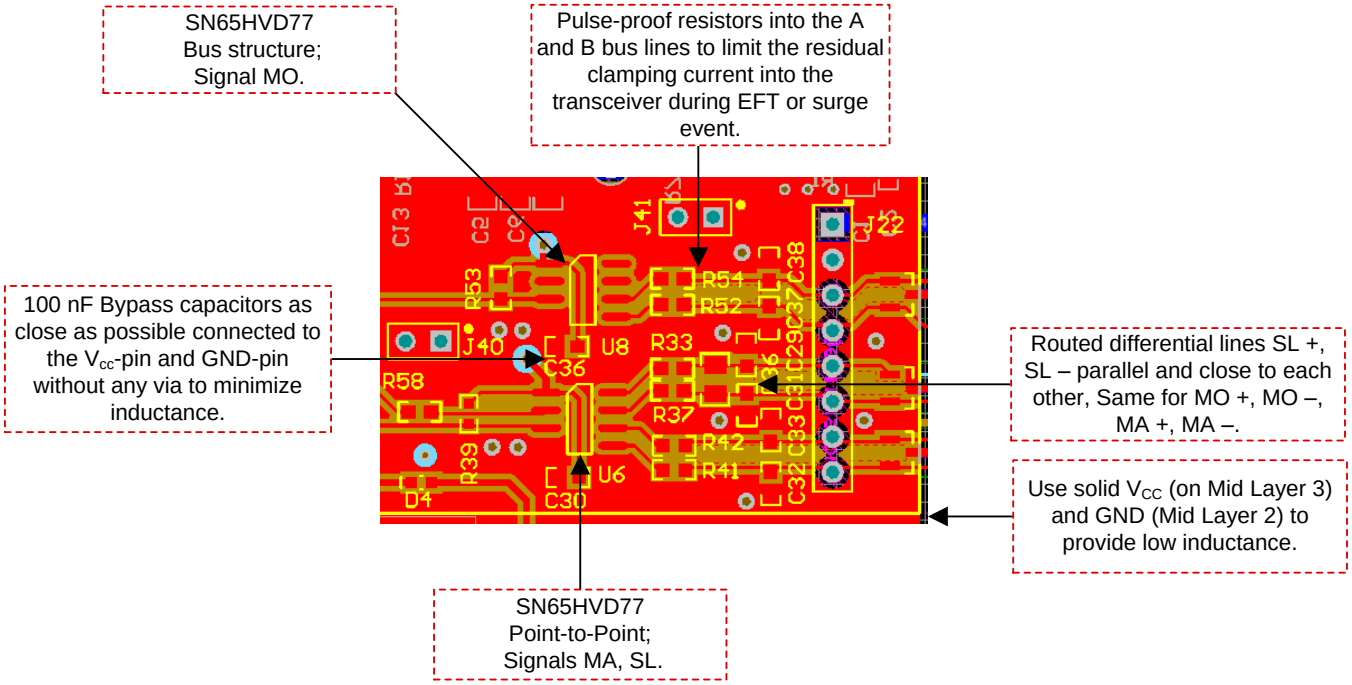

Figure 87. Top Layer with RS485 Transceivers SN65HVD77

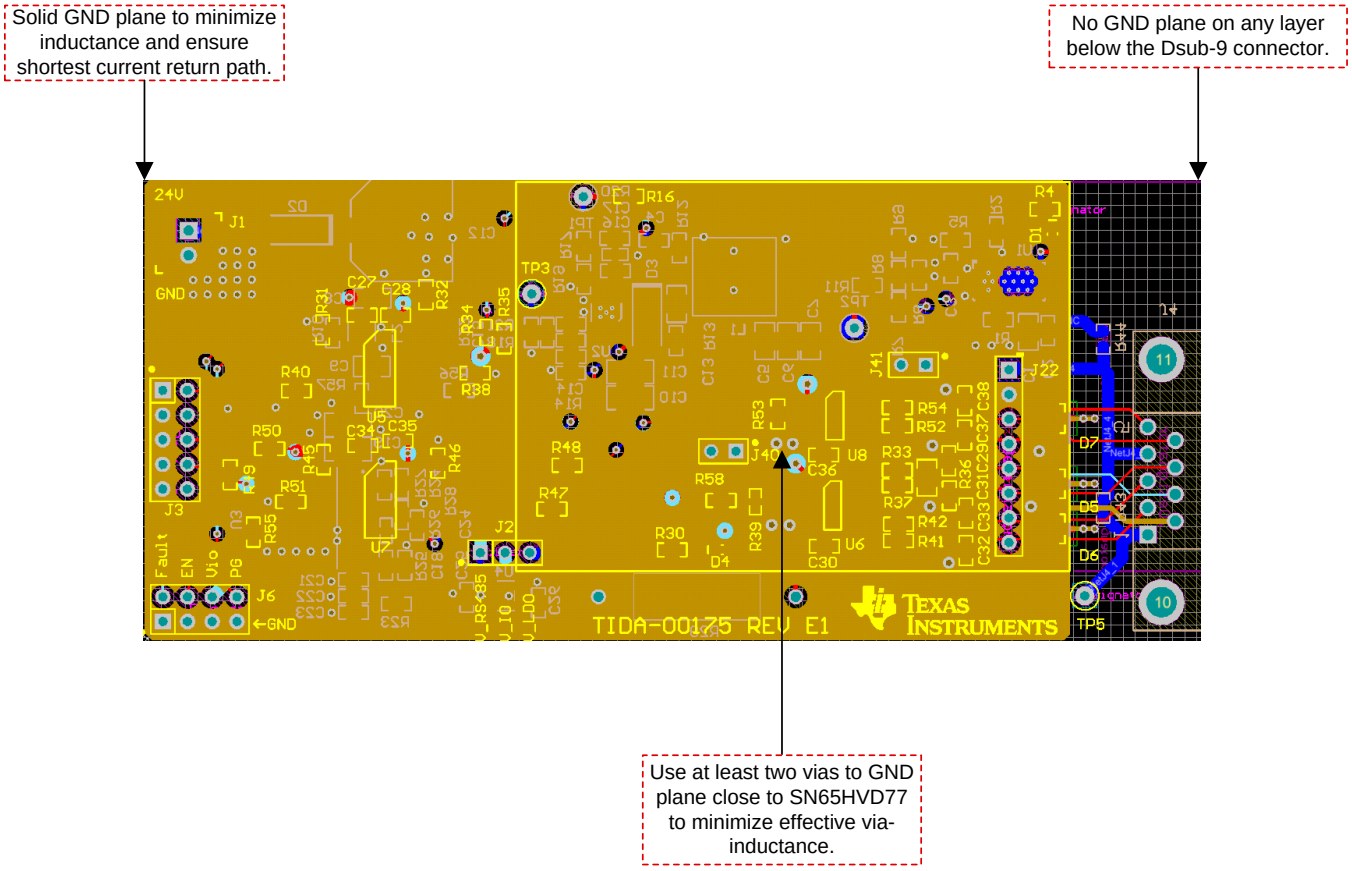

Figure 88. GND Layer

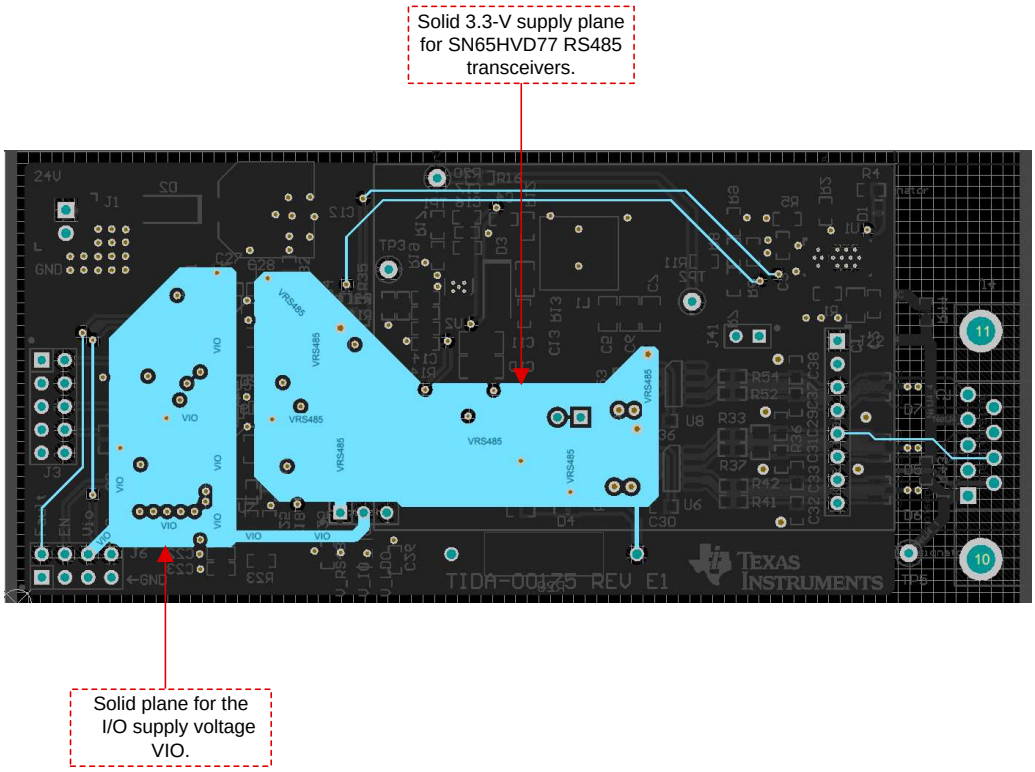

Figure 89. V_{cc} Supply Layer

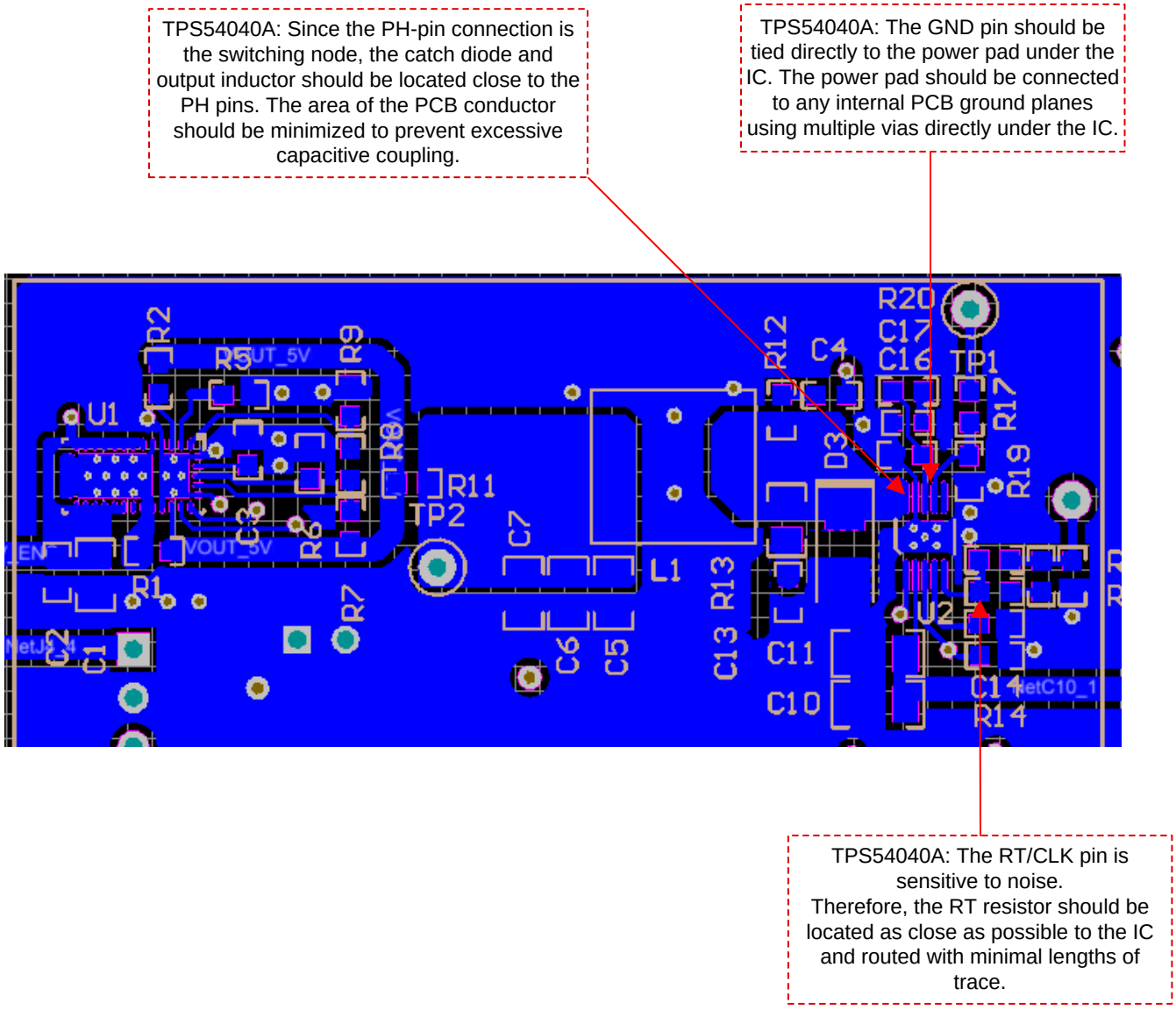

Figure 90. Bottom Layer with DCDC Power Supply TPS54040A (View from Bottom)

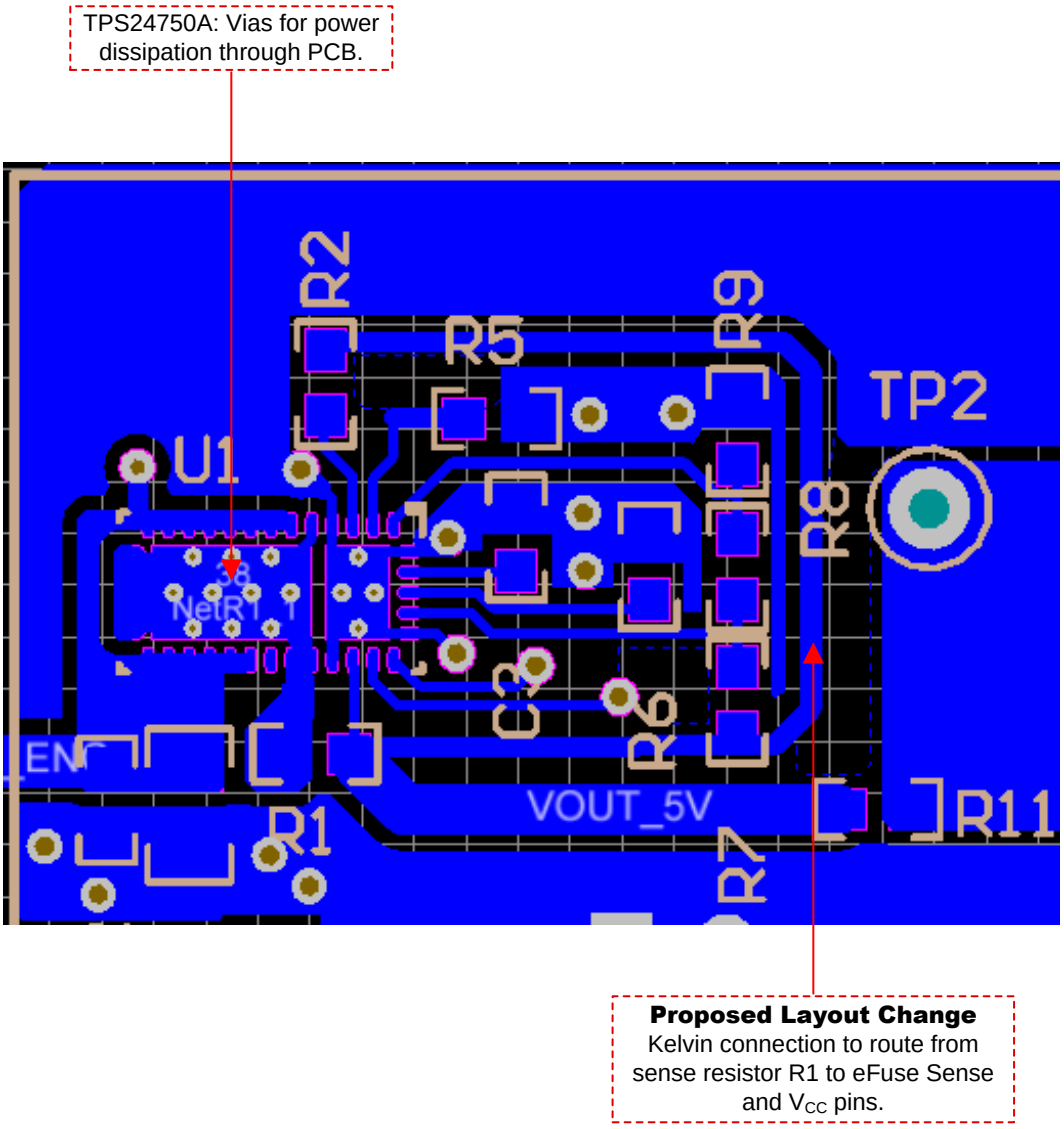

Figure 91. Bottom Layer (View from Bottom) with eFUSE and Proposed Layout Modification for R_{SENSE} (R1) Routing, as Mentioned in Section 6.2.8

7.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00175.

7.7 Assembly Drawings

To download the Assembly Drawings, see the design files at TIDA-00175.

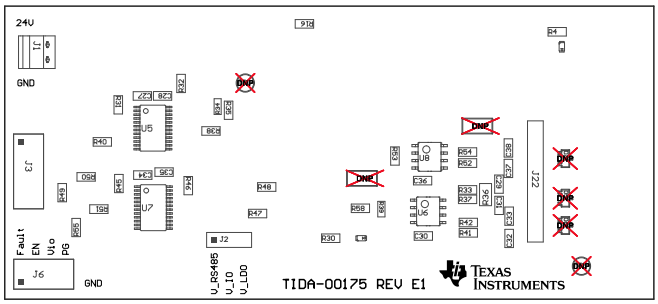

Figure 92. Top Assembly Drawing

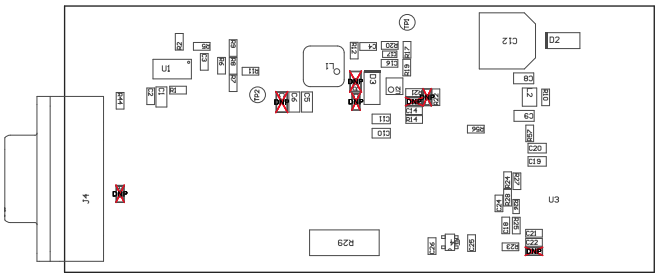

Figure 93. Bottom Assembly Drawing

7.8 Software Files

To download the software files, see the design files at TIDA-00175.

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