TI Designs
One-Phase Metrology With Enhanced ESD Protection

TEXAS INSTRUMENTS

0.1 TI Designs

TI Designs provide the foundation that you need including methodology, testing, and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

0.2 Design Resources

|	
TIDM-1PHMTR-ESD	Design Folder
MSP430F6736A	Product Folder
TPS5401	Product Folder
CC2530	Product Folder
CC2530EMK	Tools Folder
TIDM-LOWEND-IHD	Tools Folder

TI E2E™ Community

ASK Our E2E Experts
WEBENCH® Calculator Tools

0.3 Design Features

- Passed IEC 61000-4-2 Level-4 Air Discharge Tests [1] (See Below for Details)
- TI Energy Library Firmware Calculates All Energy Measurement Parameters Including Active and Reactive Power and Energy, Root Mean Square (RMS) Current and Voltage, Power Factor, and Line Frequency
- Support for ZigBee® Communication to In-Home Display or Connections to Wi-Fi®, Wireless M-Bus, and IEEE-802.15.4g Add-On Communications Modules
- Automated or Manual Switching Between Main and Auxiliary Power Sources for Metrology Engine

0.4 Featured Applications

- Metering
- Street Lighting
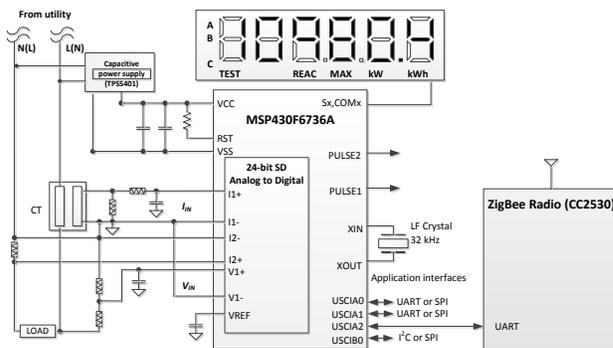
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1 System Description

This design implements an ANSI/IEC Class 0.2 single-phase energy meter with enhanced electrostatic discharge (ESD) protection. The design also features communications through ZigBee™ connectivity. The e-meter system on chip (SoC) is used to perform all metrology functions and sends active power results to the CC2530EM add-on board. Developers can use the companion In-Home Display TI design (TIDM-LOWEND-IHD) to display results remotely [2].

The design guide has a complete metrology source code provided as a downloadable zip file.

1.1 MSP430F6736A

For sensing and calculating the metrology parameters, the MSP430F6736A e-meter SoC is used. This device is the latest metering SoC that belongs to the MSP430F67xxA family of devices. This MSP430F67xxA family of devices offer enhancements when compared to the previous non-A MSP430F67xx devices, such as the MSP430F6736. One of these enhancements addresses improved ESD robustness (see the *Differences Between MSP430F67xx and MSP430F67xxA Devices* application note for more details on this change as well as other changes compared to the non-A MSP430F67xx devices). These ESD enhancements can enable increased ESD immunity when compared to the previous meters that are based on the non-A MSP430F67xx devices.

In regard to metrology, the MSP430F6736A energy library software has support for calculation of various parameters for single-phase energy measurement. The key parameters calculated during energy measurements are: RMS current and voltage; active power, reactive power, and energies; power factor; and frequency. The user can view these parameters from the calibration graphical user interface (GUI) or liquid crystal display (LCD).

1.2 CC2530

For ZigBee communication, the CC2530EMK evaluation kit is used. Place the board of the kit into the EVMs RF connector to enable ZigBee communication. The F6736A e-meter software automatically packages the active power readings into a packet. This packet is then sent to the CC2530 that is connected to the RF connector of the design.

The TIDM-LOWEND-IHD TI design can be used as a receiver. When this receiver is used, the CC2530 on the IHD430 receives the packet from the CC2530 on the design and displays the packet on the IHD430 LCD.

1.3 TPS5401

The TPS5401 device is used in the power supply to help provide a 3.3-V output from an input mains voltage of 120/230-V RMS AC at 50/60 Hz. Figure 8 shows how the TPS5401 is used to create the 3.3-V output from the 120/230-V RMS AC input.
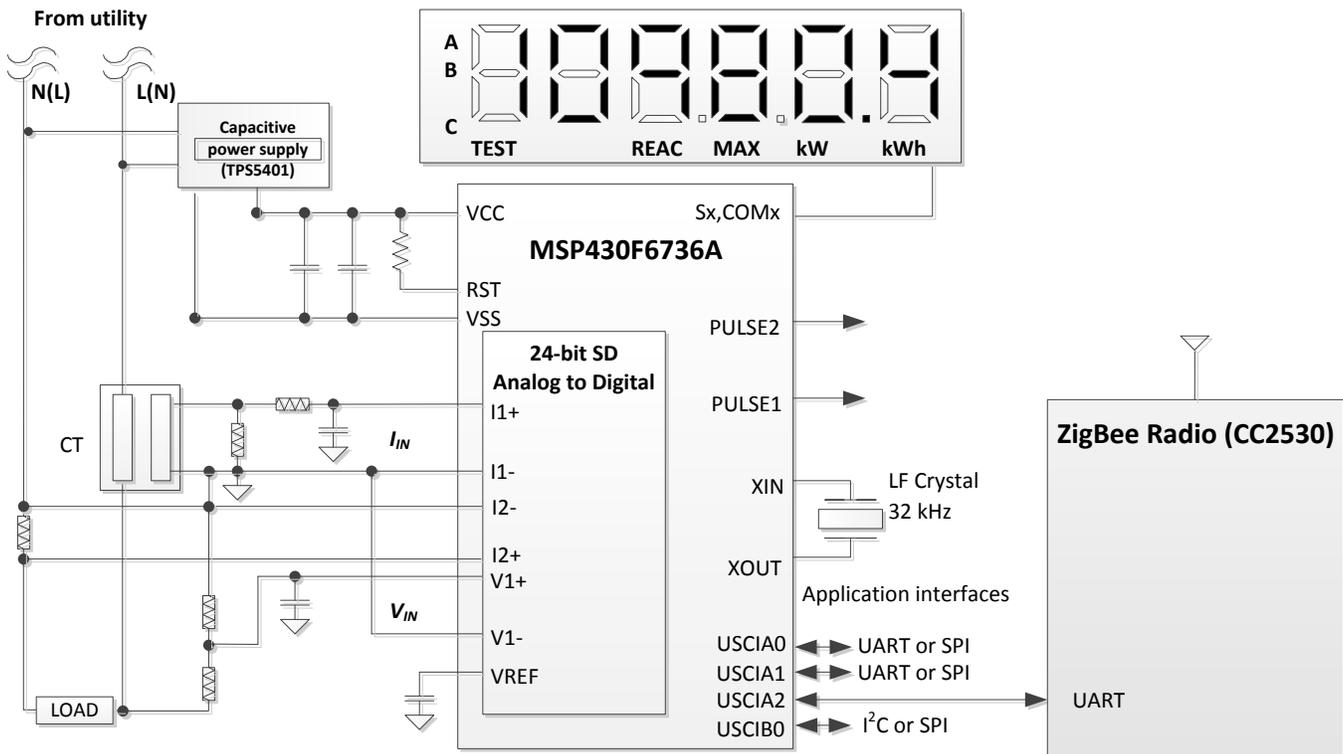
2 Block Diagram

Figure 1. TIDM-1PHMTR-ESD System Block Diagram

Figure 1 shows a block diagram that displays the high-level interface used for a single-phase energy meter application that uses the MSP430F6736A device. In the diagram, a current sensor connects to the current channel and a simple voltage divider is used for the corresponding voltage. The CT has an associated burden resistor that must be connected at all times to protect the measuring device. The selection of the CT and the burden resistor is made based on the manufacturer and current range required for energy measurements. The choice of voltage divider resistors for the voltage channel is selected to ensure the mains voltage is divided down to adhere to the normal input ranges that are valid for the MSP430s SD24_B ADCs. Refer to the MSP4305xx/6xx user's guide [3] and device specific data sheet [4] for the ADC input voltage range.

Other signals of interest in Figure 1 are the PULSE GPIOs (PULSE1 and PULSE2), which are used to transmit active and reactive energy pulses used for accuracy measurement and calibration. In addition, the user can add ZigBee communication to an in-home display by connecting a CC2530EM board into the RF connectors of the design and flashing the CC2530 with the proper software.

2.1 Highlighted Products

2.1.1 MSP430F6736A

Similar to the MSP430F6736, the MSP430F6736A belongs to the powerful 16-bit MSP430F6xx platform. This chip is intended for energy measurement applications and it has the necessary architecture to perform this application. The F6736A has a powerful 25-MHz CPU with MSP430CPUx architecture. The analog front-end (AFE) consists of three independent 24-bit ΣΔ analog-to-digital converters (ADC) based on a second order sigma-delta architecture that supports differential inputs. The sigma-delta ADCs (ΣΔ24_B) operate independently and are capable of 24-bit results. The sigma-delta ADCs can be grouped together for simultaneous sampling of voltages and currents on the same trigger. In addition, the sigma-delta ADC also has an integrated gain stage to support gains up to 128 for amplification of low-output current sensors. A 32-bit x 32-bit hardware multiplier on this chip can be used to further accelerate math-intensive operations during energy computation.

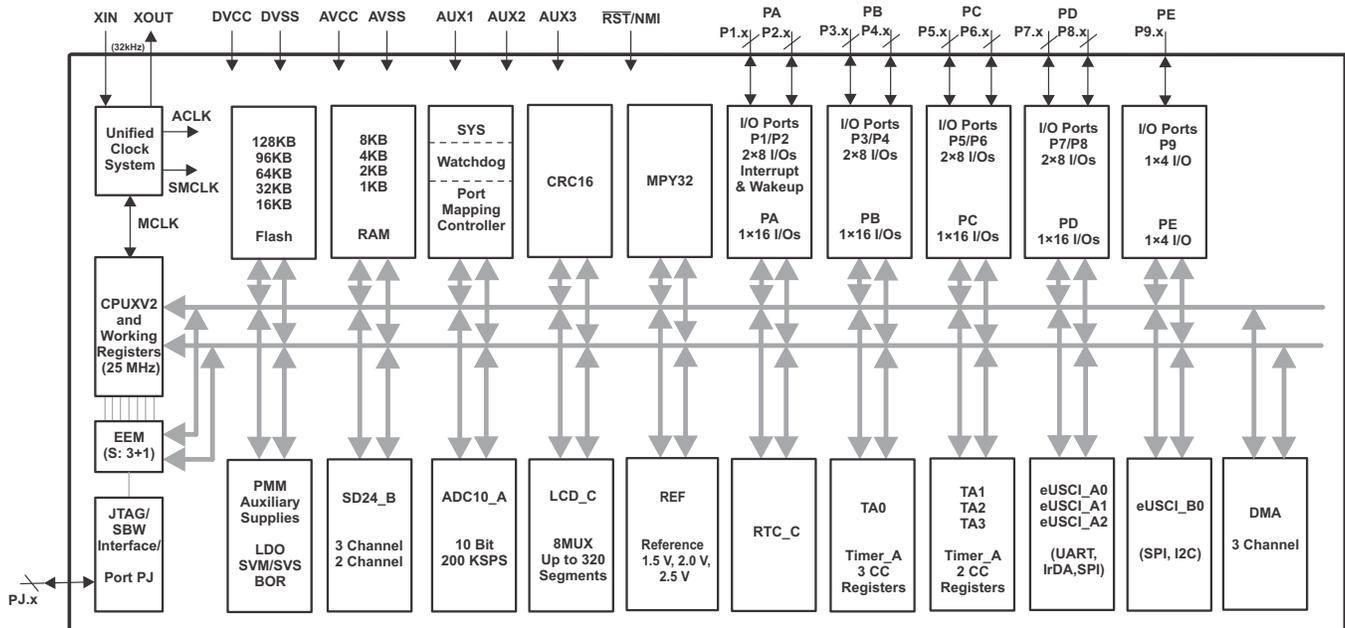shows a block diagram of the chip that displays the features of the MSP430F6736A.

Figure 2. MSP430F6736A Block Diagram

2.1.2 CC2530 Features

The CC2530 device is a true system-on-chip (SoC) solution for IEEE 802.15.4, ZigBee, and Radio Frequency for Consumer Electronics (RF4CE) applications. The CC2530 enables robust network nodes to be built with very-low bill-of-material costs. The CC2530 combines the excellent performance of a leading RF transceiver with an industry-standard enhanced 8051 MCU, in-system programmable flash memory, 8-KB RAM, and many other powerful features. The CC2530 comes in four different flash versions: CC2530F32/64/128/256, with 32/64/128/256KB of flash memory, respectively. The CC2530 has various operating modes, making it highly suited for systems where ultra-low power consumption is required. Short transition times between operating modes further ensure low energy consumption. Combined with the industry-leading and golden-unit-status ZigBee protocol stack (Z-Stack™) software from Texas Instruments, the CC2530F256 provides a robust and complete ZigBee solution.

2.1.3 TPS5401 Features

The TPS5401 device is a 42-V, 0.5-A, step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the supply current to 116 µA when outputting regulated voltage without a load. Using the enable pin, shutdown supply current reduces to 1.3 µA when the enable pin is low.

Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin. The slow-start pin controls the output voltage start-up ramp. The output voltage start-up ramp is controlled by the slow-start pin that can also be configured for sequencing or tracking. In addition, an open-drain power-good signal indicates the output is within 94% to 107% of its nominal voltage

3 System Design Theory

3.1 ESD Introduction

Electrostatic discharge (ESD) is a single-event rapid transfer of electrostatic charge between two objects that are at different voltages. ESD events can have a negative effect on electronic systems such as e-meters. There can be many sources for ESD. For an e-meter in particular, a charged person that is in contact with the meter (such as the operator of a meter) can potentially subject the meter to ESD. Depending on the humidity of the environment, and the material used to charge the charged person, the voltage at which the person is charged varies. Figure 3 shows the electrostatic voltages in relation to the humidity of the environment.
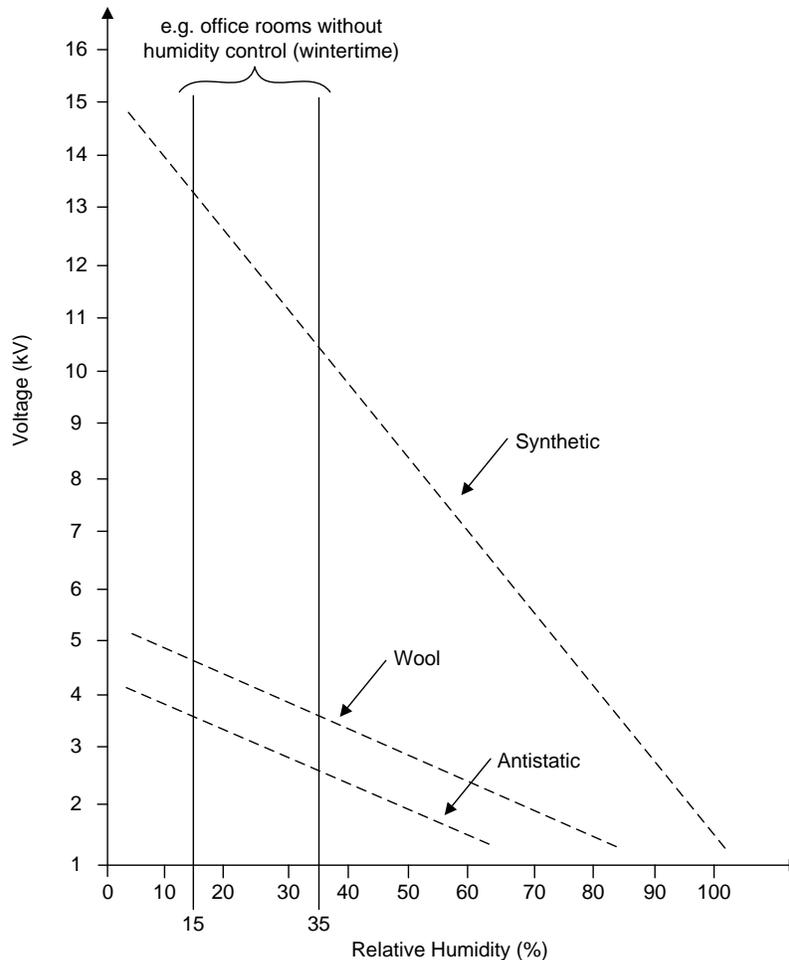
Figure 3. Maximum Values of Electrostatic Voltages People Can Be Charged to When in Contact With Different Materials [1]

Because these devices are used in billing applications and should always remain functional, e-meters must be designed with ESD immunity in consideration. The IEC 62052-11 standard accounts for this consideration by requiring all e-meters that adhere to this standard to pass ESD immunity tests according to IEC 61000-4-2.

The purpose of the IEC 61000-4-2 standard is to ensure that systems are tolerant of ESD exposure that may be present while a system is operating. The scope of the standard is to test electrical and electronic equipment that may be subjected to ESD from operators directly or from personnel to adjacent objects [1]. Depending on the equipment and environment in which the equipment operates, the amount of ESD exposure can vary. The IEC 61000-4-2 defines multiple levels to cover the different types of exposure levels. There are four standard levels; however, depending on special requirements, testing beyond these

conditions may be conducted. The level for testing is selected based on the purpose of the implemented system and the environment where the tests are to be deployed. For each test, a special unit (sometimes referred to as an ESD gun), generates an ESD event that is meant to simulate the necessary ESD waveform. Figure 4 shows an example of such an ESD waveform. Figure 5 shows this ESD gun, along with the entire setup for IEC 61000-4-2.
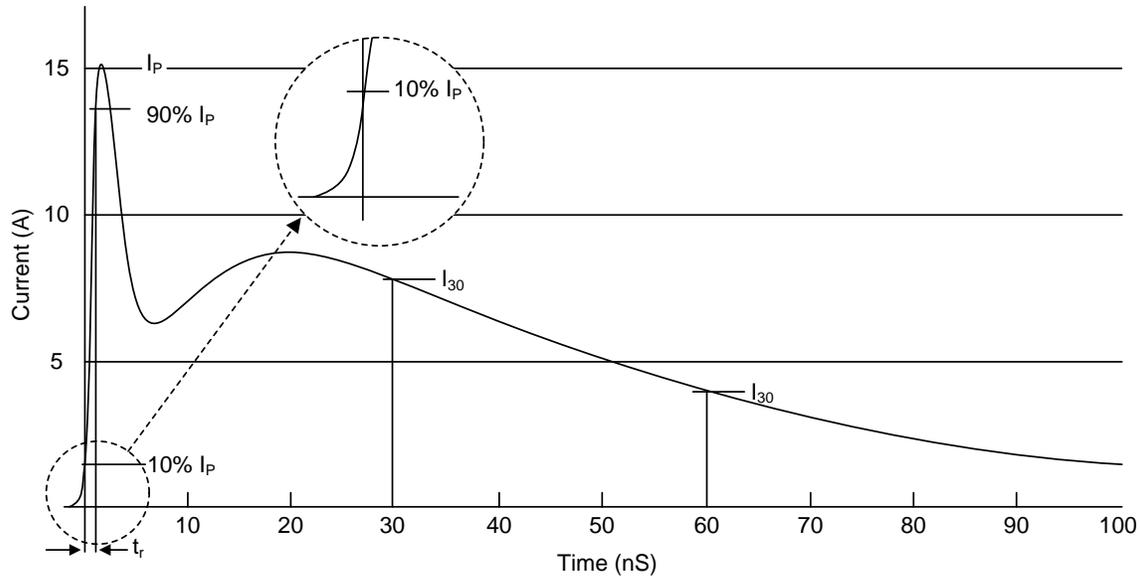

Figure 4. Ideal Contact Discharge Current Waveform at 4 kV (Taken from IEC 61000-4-2) [1]
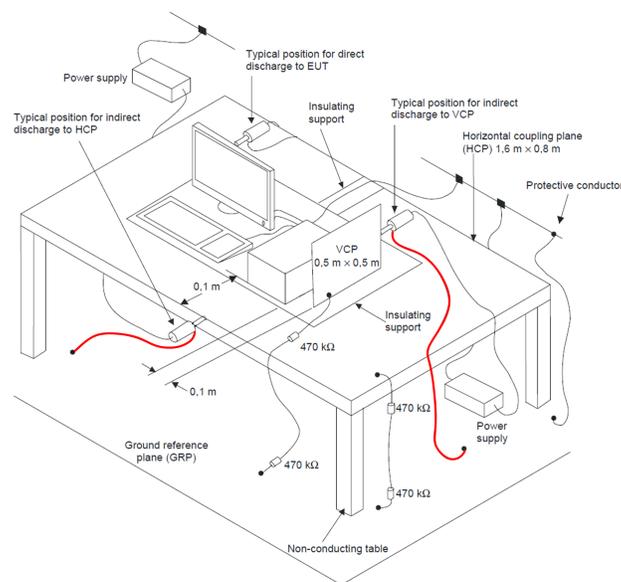
Figure 5. ESD Test Bench for Powered Condition (Taken from IEC 61000-4-2) [1]

For e-meters, IEC 62052-11 specifically mentions that IEC 61000-4-2 should be conducted with contact discharges (if applicable) of 8 kV and air discharges of 15 kV with ten discharge pulses at a rate of 1 Hz. However, based on different region requirements, sometimes a meter may have more stringent requirements and must pass immunity testing at higher ESD voltage levels or larger number of discharge pulses.

3.2   Design Hardware Implementation

3.2.1   Analog Inputs

The MSP430 analog front end consists of ΣΔ ADCs. Each converter is differential and requires that the input voltages at the pins does not exceed ±920 mV (gain = 1) for optimum results. To meet this input voltage specification, the current and voltage inputs must be divided down. In addition, the SD24 allows a maximum negative voltage of −1 V; therefore, AC signals from mains can be directly interfaced without the need for level shifters. This sub-section describes the analog front end used for voltage and current channels.

3.2.1.1   Voltage Inputs

The voltage from the mains is usually 230 V or 120 V and is usually scaled down for optimal accuracy within 920 mV. In the analog front end for voltage, there consists a spike protection varistor, electromagnetic interference (EMI) filter beads (which help for ESD testing), a voltage divider network, and a RC low-pass filter that functions as an anti-alias filter.
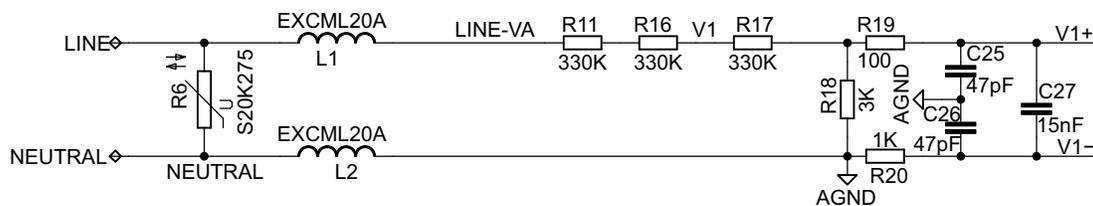

Figure 6. Analog Front End for Voltage Inputs

Figure 6 shows the analog front end for voltage inputs for a mains voltage of 230 V. In this circuitry, the voltage is brought down to approximately 695-mV RMS, which is 982 mV at the peak, and fed to the positive input of the convertor. Although this voltage is slightly higher than the recommended 920-mV input, the degradation in accuracy at these extended ADC voltage ranges is not noticeable for metrology readings for voltage samples. Additionally, it is important to note that the anti-alias resistors on the positive and negative sides are different because the input impedance to the positive terminal is much higher; therefore, a lower value resistor is used for the anti-alias filter. If this input impedance is not maintained, a relatively large phase shift occurs.

3.2.1.2 Current Inputs

The analog front end for current inputs is slightly different from the analog front end for the voltage inputs. Figure 7 shows the analog front end used for the current channels corresponding to the live and neutral currents. The analog front end for current consists of footprints for diodes (not populated on the evaluation module (EVM)) and transorbs for transient voltage suppression (TVS). In addition, the front-end consists of EMI filter beads (which should help for ESD testing), burden resistors for current transformers, and also a RC low-pass filter that acts like an anti-alias filter.
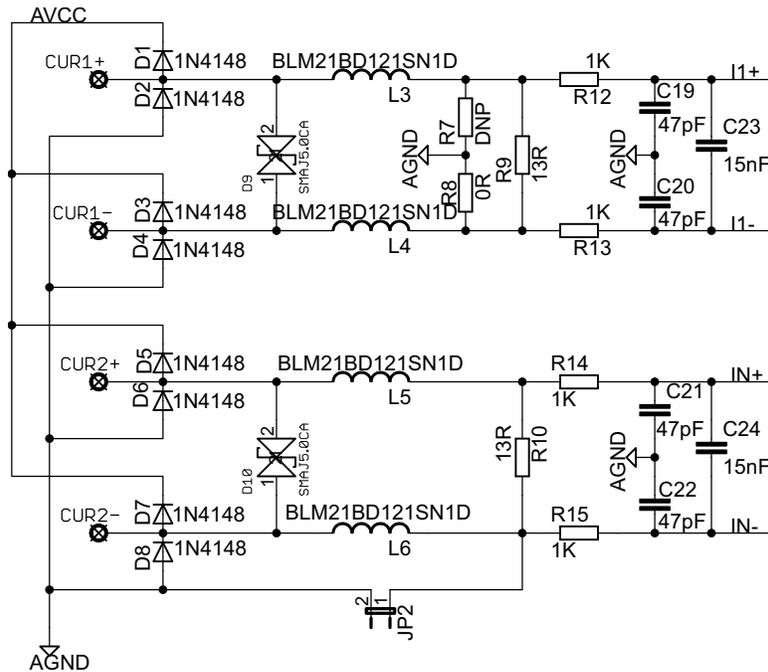
Figure 7. Analog Front End for Current Inputs

In the current front-end implementation, both the neutral and live currents can be measured with a current transformer. In Figure 7 resistors R9 and R10 are the burden resistors that would be selected based on the current range used and the turns ratio specification of the CT (CTs with a turns ratio of 2000:1 are used for this design). The value of the burden resistor for this design is around 13 Ω. Based on the 100-A maximum current of this EVM of 100 A, a CT turns ratio of 2000:1, and a burden resistor of 13 Ω, the input signal to the converter is a fully differential input with a voltage swing of ±919 mV maximum when the maximum current rating of the meter (100 A) is applied. Following the burden resistor is the antialiasing circuitry, which is implemented with resistors and capacitors.

3.2.2 Power Supply

The MSP430 family of microcontrollers support a number of low-power modes in addition to low-power consumption during active (measurement) mode when the CPU and other peripherals are active. Because an energy meter is always interfaced to the AC mains, deriving the DC supply required for the measuring element (MSP430F6736A) is easy using an AC to DC conversion mechanism. The reduced power requirements of this device family allow design of power supplies to be small, extremely simple, and cost-effective. The power supply allows the operation of the energy meter by powering it directly from the mains.

Figure 8 shows a capacitor power supply that provides a single output voltage of 3.3 V directly from the mains of 120-V to 230-V RMS AC at 50/60 Hz.

Figure 8. Simple Capacitive Power Supply for the MSP430 Energy Meter

In Figure 8 the appropriate values of resistor R21 and capacitor C28 are chosen based on the required output current drive of the power supply.

Figure 8 also shows how the voltage from mains is directly fed to an RC-based circuit followed by a rectification circuit to provide a DC voltage for the operation of the MSP430 device. This DC voltage is regulated to 3.3 V for full-speed operation of the MSP430. The design equations for the power supply are given in the application report *Improved Load Current Capability for Cap-Drop Off-Line Power Supply for E-Meter* [5].

3.3 Metrology Software Implementation

The section discusses the software for the implementation of 1-phase metrology. This section discusses the setup of various peripherals of the MSP430 device. Subsequently, the section describes the entire metrology software as two major processes: the foreground process and background process.

3.3.1 Peripherals Setup

The major peripherals of the MSP430F6736A are the 24-bit sigma delta ($\Sigma\Delta24\_B$) ADC, clock system, timer, LCD, watchdog timer (WDT), and so forth.

3.3.1.1 *ΣΔ24 Setup*

The MSP430F6736A has three independent sigma delta data converters. For a single-phase system, at least two $\Sigma\Delta$s are necessary to independently measure one voltage and current. The code accompanying this design guide addresses the metrology for a single-phase system with limited discussion to anti-tampering; however, the code supports the measurement of the neutral current.

The clock to the SD24 (f_M) derives from the digitally controlled oscillator (DCO) running at 16 MHz.

The sampling frequency is defined as $f_s = f_M / OSR$, the OSR is chosen to be 256, and the modulation frequency, is chosen as 1.048576 MHz, resulting in a sampling frequency of 4.096 samples per second. The SD24s are configured to generate regular interrupts every sampling instant.

The following are the $\Sigma\Delta$ channels associations:

- SD0P0 and SD0N0 → Voltage
- SD1P0 and SD1N0 → Current I1 in schematic (Current I' in Figure 17)
- SD2P0 and SD2N0 → Current IN in schematic (Current I in Figure 17)

3.3.1.2   Real Time Clock (RTC_C)

The RTC_C is a real-time clock module that is configured to give precise one second interrupts. Based off these one second interrupts, the time and date are updated in software, as necessary.

3.3.1.3   LCD Controller (LCD_C)

The LCD controller on the MSP430F6736A device can support up to 8-mux displays and 320 segments. The LCD controller is also equipped with an internal charge pump that can be used for good contrast. In the current design, the LCD controller is configured to work in 4-mux mode using 160 segments with a refresh rate set to ACLK/64, which is 512 Hz.

3.3.2   Foreground Process

The foreground process includes the initial setup of the MSP430 hardware and software immediately after a device RESET. Figure 9 shows the flowchart for this process. The initialization routines involve the setup of the ADC, clock system, general purpose input and output (GPIO) port pins, RTC module for clock functionality, LCD, and the USCI_A1 for universal asynchronous receiver and transmitter (UART) functionality. In addition, if ZigBee™ communication is enabled, USCI_A2 is configured.

After the hardware is setup, the foreground process waits for the background process to notify it to calculate new metering parameters. This notification is done through a status flag every time a frame of data is available for processing. The data frame consists of the processed current, voltage, and active and reactive quantities that have been accumulated for one second. This accumulation is equivalent to the accumulation of 50 or 60 cycles of data synchronized to the incoming voltage signal. In addition, a sample counter keeps tracks of how many samples have been accumulated over this frame period. This count can vary as the software synchronizes with the incoming mains frequency.

The data samples set consist of processed current, voltage, active and reactive energy. Processed voltages accumulate in a 48-bit register. In contrast, processed currents, active energies, and reactive energies are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the calculated values of active and reactive power from the foreground, the apparent power is calculated. The frequency (in hertz) and power factor are also calculated using parameters calculated by the background process using the formulas in Section 3.3.2.1).
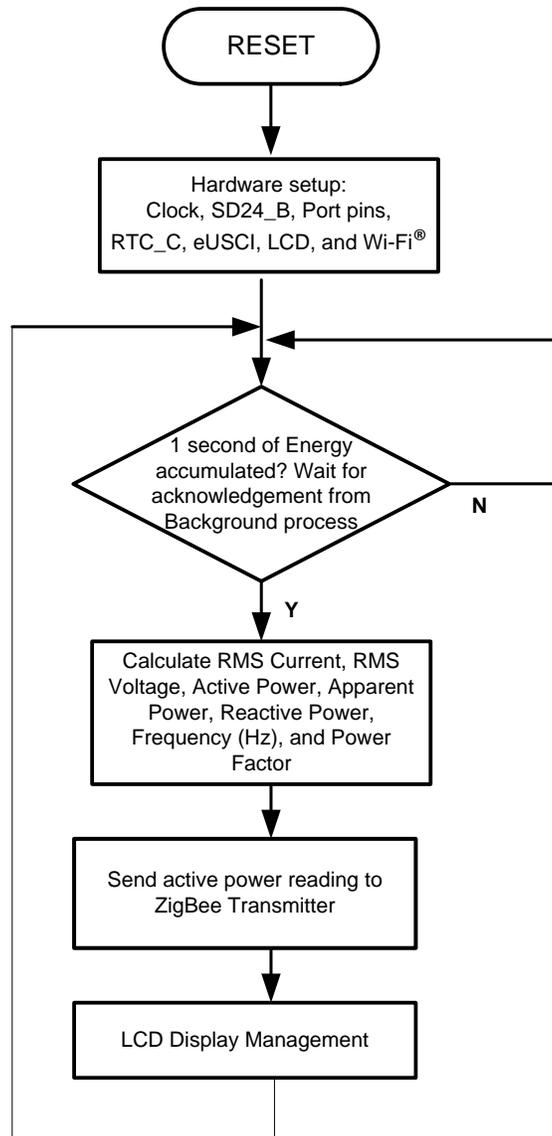
Figure 9. Foreground Process

3.3.2.1 *Formulae*

This section briefly describes the formulas used for the voltage, current, and energy calculations.

As described in the previous sections, voltage and current samples are obtained from the ΣΔ converters at a sampling rate of 4096 Hz. All of the samples that are taken in one second are kept and used to obtain the RMS values for voltage and current. The RMS values are obtained by the following formulas:

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum\limits_{n=1}^{Sample\ count} v_{ph}(n) \times v_{ph}(n)}{Sample\ count}}$$

$$I_{RMS,ph} = K_{i,ph} \times \sqrt{\frac{\sum\limits_{n=1}^{Sample\ count} i_{ph}(n) \times i_{ph}(n)}{Sample\ count}}$$

where

- $v_{ph}(n)$ = Voltage sample at a sample instant 'n',
- $i_{ph}(n)$ = Each current sample at a sample instant 'n',
- Sample count = Number of samples in one second,
- $K_{v,ph}$ = Scaling factor for voltage,
- $K_{i,ph}$ = Scaling factor for each current.

(1)

Power and energy are calculated for the active and reactive energy samples of a frame. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers using the following formulas:

$$P_{ACT,ph} = K_{ACT,ph} \frac{\sum\limits_{n=1}^{Sample\ count} V(n) \times i_{ph}(n)}{Sample\ count}$$

$$P_{REACT,ph} = K_{REACT,ph} \frac{\sum\limits_{n=1}^{Sample\ count} v_{90}(n) \times i_{ph}(n)}{Sample\ count}$$

$$P_{APP,ph} = \sqrt{P_{ACT,ph}^2 + P_{REACT,ph}^2}$$

where

- $v_{90}(n)$ = Voltage sample at a sample instant 'n' shifted by 90°,
- $K_{ACT,ph}$ = Scaling factor for active power,
- $K_{REACT,ph}$ = Scaling factor for reactive power.

(2)

Note that for reactive energy, the 90° phase shift approach is used for two reasons:

- The 90° phase shift approach allows accurate measurement of the reactive power for very small currents.
- The 90° phase shift approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency is used to calculate the 90 degrees-shifted voltage sample using the calculated mains frequency. Because the frequency of the mains varies, it is important to first measure the mains frequency accurately to phase shift the voltage samples accordingly (refer to Section 3.3.3.3 *Frequency Measurement and Cycle Tracking*). The phase shift implementation of the application consists of an integer part and a fractional part. The integer part is realized by providing an n-samples delay. The fractional part is realized by a fractional delay filter (refer to Section 3.3.3.2 *Phase Compensation*).

Using the calculated powers, calculate the energies with the following Equation 3 and Equation 4:

$$E_{ACT,ph} = P_{ACT,ph} \times \text{Sample count}$$

$$E_{REACT,ph} = P_{REACT,ph} \times \text{Sample count}$$

(3)

The background process calculates the frequency in terms of samples per mains cycle. The foreground process then converts this calculation to hertz using the following Equation 4:

$$\text{Frequency (Hz)} = \frac{\text{Sampling Rate (samples / second)}}{\text{Frequency (samples / cycle)}}$$

(4)

After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the meters internal representation of power factor, a positive power factor corresponds to a capacitive load and a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. The internal representation of power factor is calculated by Equation 5:

$$\text{Internal Representation of Power Factor} = \begin{cases} \dfrac{P_{ACT}}{P_{Apparent}}, \text{if capacitive load} \\ -\dfrac{P_{ACT}}{P_{Apparent}}, \text{if inductive load} \end{cases}$$

(5)

3.3.3   Background Process

The background process uses the ΣΔ interrupt as a trigger to collect voltage and current samples (three values in total). These samples are used to calculate intermediate results. Because 16-bit voltage samples are used, the voltage samples are further processed and accumulated in a dedicated 48-bit register. In contrast, because 24-bit current samples are used, the current samples are processed and accumulated in dedicated 64-bit registers. Active power and reactive power are also accumulated in 64-bit registers.

The background function mainly deals with timing critical events in software. As soon as sufficient samples (approximately one seconds worth) are accumulated, then the foreground function triggers to calculate the final values of V_{RMS}; I_{RMS}; active, reactive and apparent powers; active, reactive and apparent energy; frequency; and power factor. The background process is also wholly responsible for the calculation of energy proportional pulses, calculation of frequency (in samples per cycle), and determining current lead and lag conditions. Figure 10 shows the flow diagram of the background process.
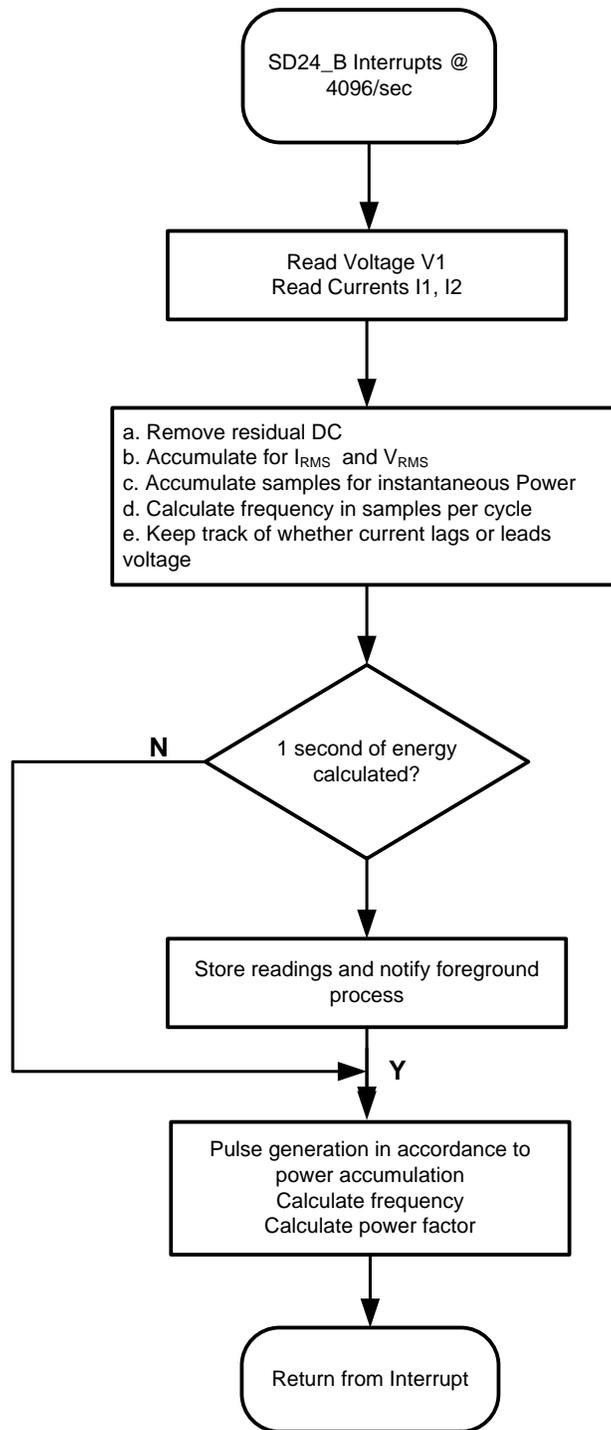
Figure 10. Background Process

3.3.3.1 Voltage and Current Signals

The ΣΔ Converter has fully differential input architecture and each ΣΔ pin can accept negative inputs; therefore, no level-shifting is necessary for the incoming AC voltage (unlike single-ended or pseudo-differential converters).

The output of each ΣΔ is a signed integer and any stray DC or offset value on these ΣΔs are removed using a DC tracking filter. A separate DC estimate for all voltages and currents is obtained using the filter, voltage, and current samples respectively. This estimate is then subtracted from each voltage and current sample.

The resulting instantaneous voltage and current samples are used to generate the following intermediate results:

- Accumulated squared values of voltage and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively
- Accumulated energy samples to calculate active energy
- Accumulated energy samples using current and 90° phase-shifted voltage to calculate reactive energy

The foreground process processes these accumulated values.

3.3.3.2 Phase Compensation

When a current transformer (CT) is used as a sensor, it introduces additional phase shift on the current signals. Also, the passive components of the voltage and current input circuit may introduce another phase shift. The user must compensate the relative phase shift between voltage and current samples to ensure accurate measurements. The ΣΔ converters have programmable delay registers (ΣΔ24PREx) that can be applied to a particular channel. The use of this built-in feature (PRELOAD) is to provide the required phase compensation. Figure 11 shows the usage of PRELOAD to delay sampling on a particular channel.
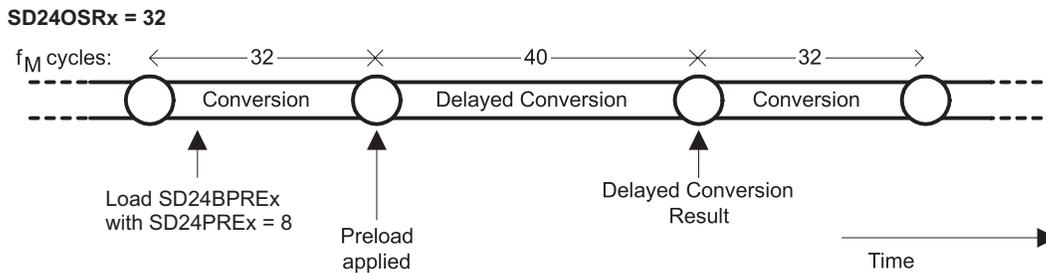
Figure 11. Phase Compensation Using PRELOAD Register

The fractional delay resolution is a function of input frequency (f_{IN}), OSR, and the sampling frequency (f_S).

$$\text{Delay resolution}_{Deg} = \frac{360^o \times f_{IN}}{OSR \times f_S} = \frac{360^o \times f_{IN}}{f_M} \tag{6}$$

In the current application, for an input frequency of 60 Hz, OSR of 256, and sampling frequency of 4096, the resolution for every bit in the preload register is about 0.02° with a maximum of 5.25° (maximum of 255 steps).

3.3.3.3   *Frequency Measurement and Cycle Tracking*

The instantaneous voltage is accumulated in a 48-bit register. In contrast, the instantaneous current, active power, and reactive power are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When approximately one seconds worth of samples have been accumulated, the background process stores these accumulation registers and notifies the foreground process to produce the average results, such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process because it produces very stable results.

For frequency measurements, a straight line interpolation is used between the zero crossing voltage samples. Figure 12 shows the samples near a zero cross and the process of linear interpolation.
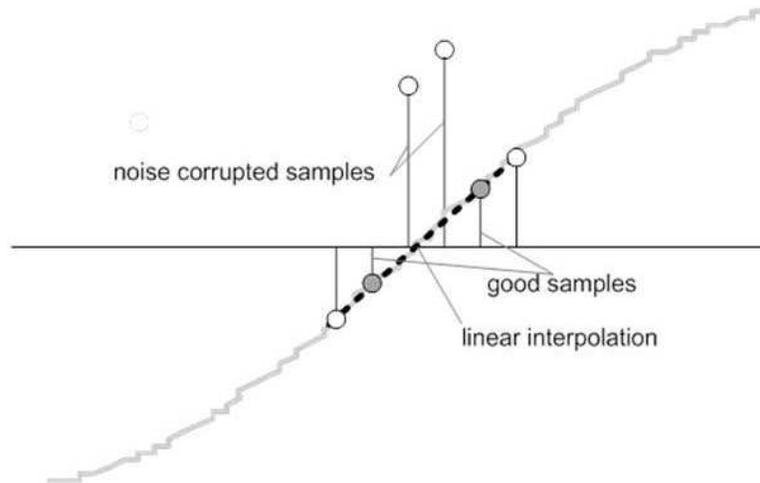
Figure 12. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate-of-change check to filter out the possible erroneous signals and make sure that the two points are interpolated from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair appear as if there is a zero crossing.

The resultant cycle-to-cycle timing goes through a weak, low-pass filter to further smooth out any cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement tolerant of noise.

3.3.3.4   *LED Pulse Generation*

In electricity meters, the energy consumption of the load is normally measured in a fraction of kilowatt-hour (KWh) pulses. This information can be used to accurately calibrate any meter for accuracy measurement. Typically, the measuring element (MSP430) is responsible for generating pulses proportional to the energy consumed. Although, time jitters are not an indication of bad accuracy, time jitters give a negative indication of the overall accuracy of the meter. The jitter must be averaged out due to this negative indication of accuracy.

This application uses average power to generate these energy pulses. The average power (calculated by the foreground process) accumulates at every $\Sigma\Delta$ interrupt, thereby spreading the accumulated energy from the previous one-second time frame evenly for each interrupt in the current one-second time frame. This accumulation process is equivalent to converting power to energy. Once the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and new energy value is added on top of the threshold in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

The threshold determines the energy "tick" specified by meter manufacturers and is a constant. The "tick" is usually defined in pulses/kWh or just in KWh. One pulse must be generated for every energy "tick". For example, in this application, the number of pulses generated/KWh is set to 6400 for active and reactive energies. The energy "tick" in this case is 1 KWh/6400. Energy pulses are generated and available on a header and also through light-emitting diodes (LEDs) on the board. GPIO pins are used to produce the pulses. Figure 13 shows the flow diagram for pulse generation.
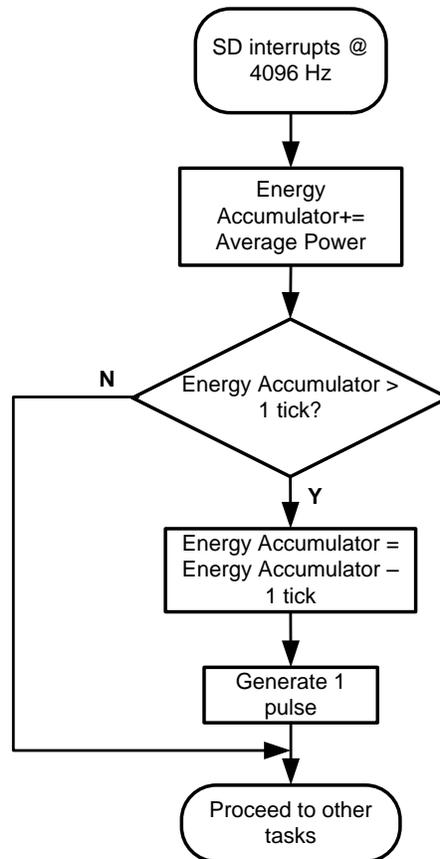
Figure 13. Pulse Generation for Energy Indication

The average power is in units of 0.01 W and a 1-KWh threshold is defined as:

1-KWh threshold = 1 / 0.01 × 1 KW × (Number of interrupts/sec) × (number of seconds in 1 hour) = 100000 × 4096 × 3600 = 0x15752A00000   (7)

3.4 ESD Test Software

When exposing equipment to ESD testing, failures can be classified into three categories:

- Temporary loss of function or degradation of performance that ceases after the disturbance ceases. The equipment under test recovers its normal performance without operator intervention. This is an acceptable failure for an e-meter in IEC 62052-11, assuming the energy readings were not affected by an amount greater than a certain threshold.
- Temporary loss of function or degradation of performance. Recovery requires operator intervention.
- Temporary loss of function or degradation of performance that is not recoverable.

To better diagnose ESD failures from passes (and also distinguish the different failures into the three types of failures), a separate code example was loaded on the MSP430F6736A when performing ESD testing. In this code example, the RST/NMI pin is configured to NMI mode. Additionally, whenever a brownout reset occurs, the red light of the EVM blinks three times before staying ON. Afterward, the green LED of the EVM constantly blinks. If this green LED stops blinking, this indicates that the meter has temporarily stopped working. If the red LED starts blinking again after previously being ON, then a brownout reset event has reoccurred.

4   Getting Started Hardware

For testing this design, the EVM430-F6736 is used and its MSP430F6736 is replaced with a
MSP430F6736A. The following figures of the EVM best describe the hardware: Figure 14 shows the top
view of the energy meter and Figure 15 shows the location of various pieces of the EVM based on
functionality.

Figure 14. Top View of the Single-Phase Energy Meter EVM
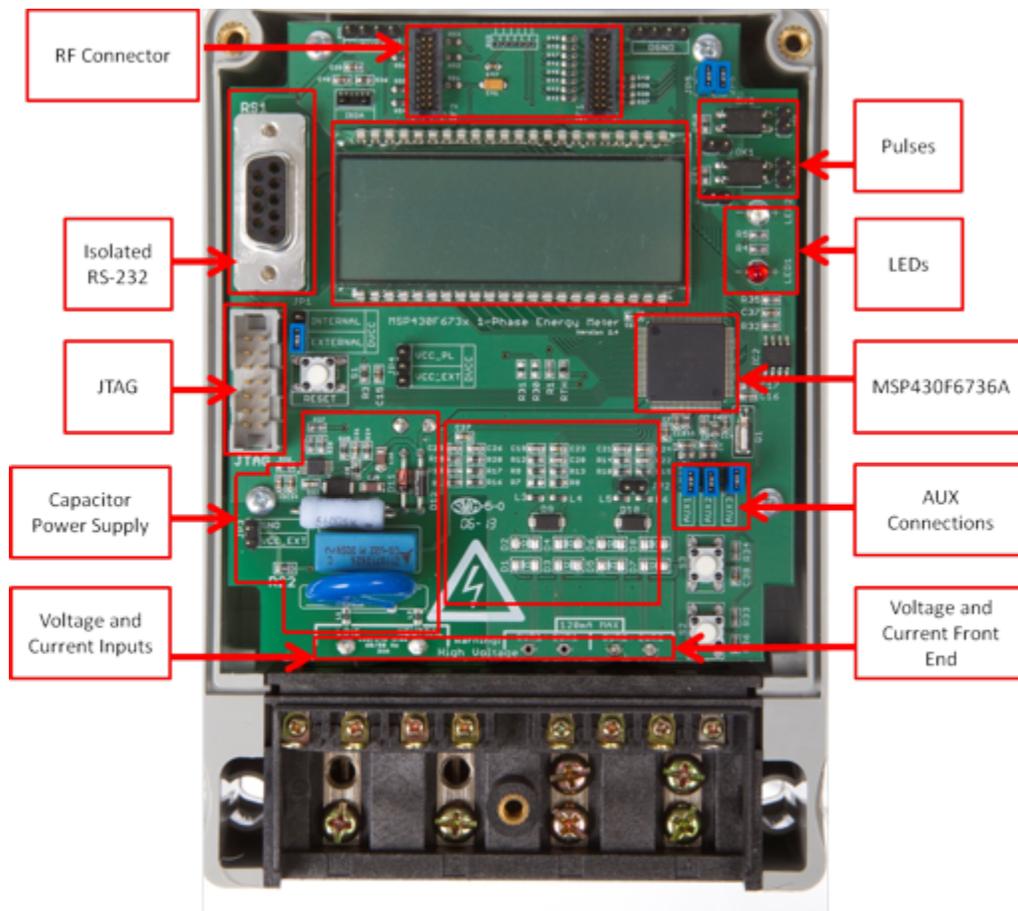
Figure 15. Top View of the Single-Phase Energy Meter EVM with Components Highlighted

4.1 Connections to the Test Setup for AC Voltages

AC voltage or currents can be applied to the board for testing purposes at these points:

- Pad "Line" corresponds to the line connection.
- Pad "Neutral" corresponds to the Neutral voltage. The voltage between Line and Neutral must not exceed 230-V AC at 50/60 Hz.
- Pads CUR1+ and CUR1− are the current inputs after the sensors. When using CT or shunts, make sure that the voltage across CUR1+ and CUR1− does not exceed 920 mV. This is currently not connected to the EVM.
- Pads CUR2+ and CUR2− can also be used as current inputs after the sensors. When using CT or shunts, make sure that the voltage across CUR1+ and CUR1− does not exceed 920 mV. *This is currently connected to a CT on the EVM.*

Figure 16 and Figure 17 show the various connections that must be made to the test setup for proper functionality of the EVM. When a test AC source must be connected, the connections have to be made according to the EVM design. Figure 16 shows the connections from the top view. Figure 17 shows the connections from the front view. In both figures, L and N correspond to the voltage inputs from the test setup. I+ and I− corresponds to one set of current inputs and I'+ and I'− corresponds to the second set of current inputs. Although the EVM hardware and software supports measurement for the second current, the EVM obtained from Texas Instruments does not have the second sensor and any current inputs must be connected to I+ and I−only. If an additional sensor must be placed, please use the two bottom-left slots close to terminals I'+ and I'−. Additional connections must be made to connect the output of these sensors to points CUR1+ and CUR1− on the PCB.
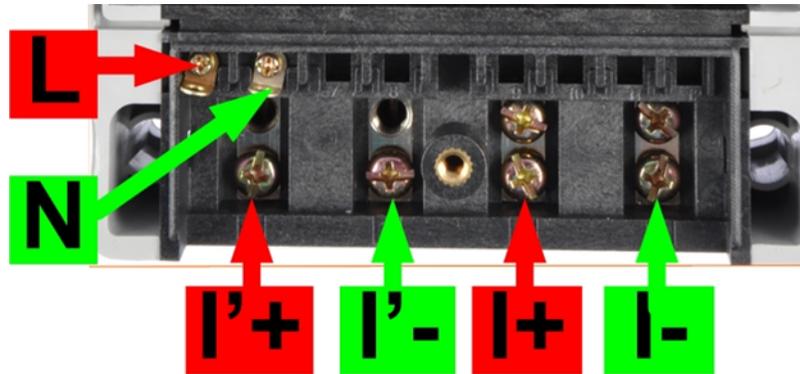
Figure 16. Top View of the EVM With Test Setup Connections
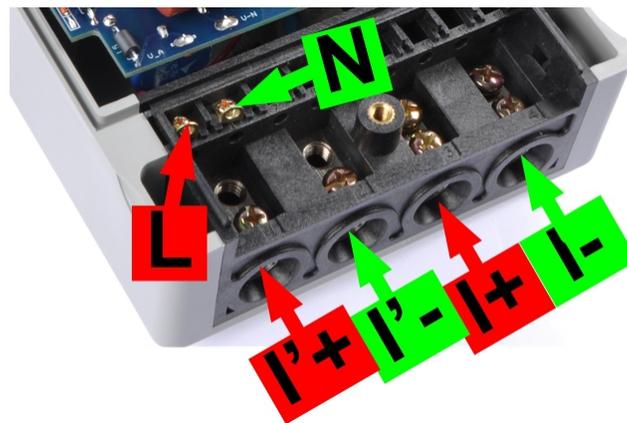
Figure 17. Top-Front View of the EVM With Test Setup Connections

4.2 Power Supply Options and Jumper Settings

A single DC voltage rail (DVCC) powers the entire board and the UART communication. DVCC can be derived either through JTAG, external power, or the AC mains through the capacitive power supply. When ZigBee communication is required, the user can select the EVM to power from an external supply (instead of AC mains through the capacitive power supply) to enable enough power to the CC2530 device. In addition to the support for multiple power sources, various jumper headers and jumper settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for blocks to function correctly. Table 1 shows the functionality of each jumper on the board and the associated functionality.

Table 1. Header Names and Jumper Settings

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
ACT (Not isolated, do not probe)	2-pin header, not a jumper header	Active energy pulses (*WARNING*)	Probe here for active energy pulses.	This header is not isolated from AC voltage so do not connect measuring equipment unless isolators external to the EVM are available See Isolated ACT instead.
AUX1 (Not isolated, do not probe)	2-pin Jumper/ Header	AUXVCC1 selection/External power (*WARNING*)		Place a jumper here to connect AUXVCC1 to GND. This jumper must be present if AUXVCC1 is not used as a backup power supply. Alternatively, the jumper can be used to provide a back-up power supply to the MSP430; to do so, simply connect the alternative power supply to this header and configure the software to use the backup power supply as required.
AUX2 (Not isolated, do not probe)	2-pin Jumper/ Header	AUXVCC2 selection/AUXVCC2 External power (*WARNING*)		Place a jumper here to connect AUXVCC2 to GND. This jumper must be present if AUXVCC2 is not used as a backup power supply. Alternatively, the jumper can be used to provide a back-up power supply to the MSP430. To do so, simply connect the alternative power supply to this header and configure the software to use this backup power supply as required.
AUX3(Not isolated, do not probe)	2-pin Jumper/ Header	AUXVCC3 selection/External power (*WARNING*)		To power the RTC externally regardless of whether DVCC is available, provide external voltage at AUXVCC3, disable the internal AUXVCC3 charger in software, and do not connect a jumper at this header. Alternatively, place a jumper here to connect AUXVCC3 to VDSYS so that AUXVCC3 is powered from whichever supply (DVCC, AUXVCC1, or AUXVCC2) is powering the chip. If this jumper is placed, disable the internal charger in software.
JP1 (Do not connect JTAG if AC mains is the power source. Isolated JTAG or supply is fine)	3-pin jumper Header	JTAG Internal/External power selection option (*WARNING*)		Place a jumper at the external header option to select external voltage for JTAG programming. Place a jumper at the internal header option to power the board using JTAG and to select the voltage from the USB FET for JTAG programming.
JP2	2-pin jumper Header	"IN" current sensor reference		Place a jumper here to reference the negative terminal of the "IN" ΣΔ to ground. This jumper should be present for testing with current transformers (the current configuration of the EVM) and removed when testing with shunts.
JP3	Not a jumper header	External power input		When using an external source for DVCC (such as when desired to use ZigBee), attach the VCC and GND of the external source at this header. Please make sure that a jumper is placed on "VCC_EXT" to select powering the EVM from this header.
JP4	3-pin jumper header	DVCC power selection		Place a jumper on "VCC_PL" to select powering the board via the cap drop power supply on board. Place a jumper on "VCC_EXT" to select powering the board externally via JP3.
JP5	2-pin jumper Header	RF_FIFO/RF_SIMO		Place a jumper here and at JP6 to allow ZigBee communication.

Table 1. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
JP6	2-pin jumper header	RF_FIFOP/RF_SOMI	Place a jumper here and at JP5 to allow ZigBee communication.	
JP7	2-pin Header, not a jumper header	Isolated Active Energy Pulses	Not a jumper header, probe here for active energy pulses.	
JP8	2-pin Header, not a jumper header	Isolated Reactive Energy Pulses	Not a jumper header, probe here for reactive energy pulses.	
SV2 (Not isolated, do not probe)	Header	Ground Voltage Header (*WARNING*)	Not a jumper header, probe here for GND voltage. Connect negative terminal of bench or external power supply when powering the board externally.	Do not probe if board is powered from AC mains, unless the AC mains are isolated. This voltage can be hot or neutral if AC wall plug is connected to the meter.
SV1 (Not isolated, do not probe)	Header	VCC Voltage Header (*WARNING*)	Not a jumper header, probe here for VCC voltage. Connect positive terminal of bench or external power supply when powering the board externally.	Do not probe if board is powered from AC mains, unless the AC mains are isolated.

5 Getting Started Firmware

The source code is developed in the IAR environment using the IAR Embedded Workbench® Integrated Development Environment (IDE) Version 6.30.1 for the MSP430 IDE and Version 7.2.0.3640 for IAR common components. Earlier versions of IAR cannot open the project files. When the project is loaded in IAR version 6.x or later, the IDE may prompt the user to create a backup. Click "YES" to proceed. There are three main parts to the energy metrology software:

- The toolkit that contains a library of mostly mathematics routines
- The metrology code that is used for calculating metrology parameters and application code that is used for the host-processor functionality of the meter (that is communication, LCD display, RTC setup, and so forth)
- The GUI that is used for calibration

Figure 18 shows the contents of the source folder.
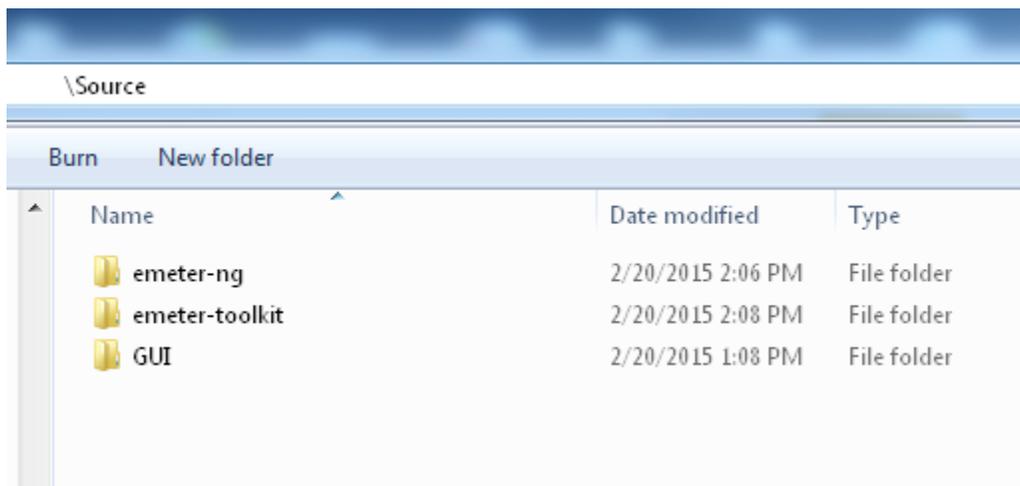
Figure 18. Source Folder Structure

The *emeter-ng* folder contains multiple project files and for this application, use the *emeter-6736A.ewp* project file. The folder *emeter-toolkit* has corresponding project file *emeter-toolkit-6736A.ewp*. For first time use, TI recommends completely rebuilding both the projects by performing the following steps:

1. Open the IAR IDE.
2. Load the *emeter_toolkit_6736A.ewp* project.
3. Click the *Rebuild All* option (see Figure 19).
4. Close the existing workspace and open the main project *emeter-6736A.ewp*.
5. Click *Rebuild All* (see Figure 20) and load this project onto the MSP430F6779.
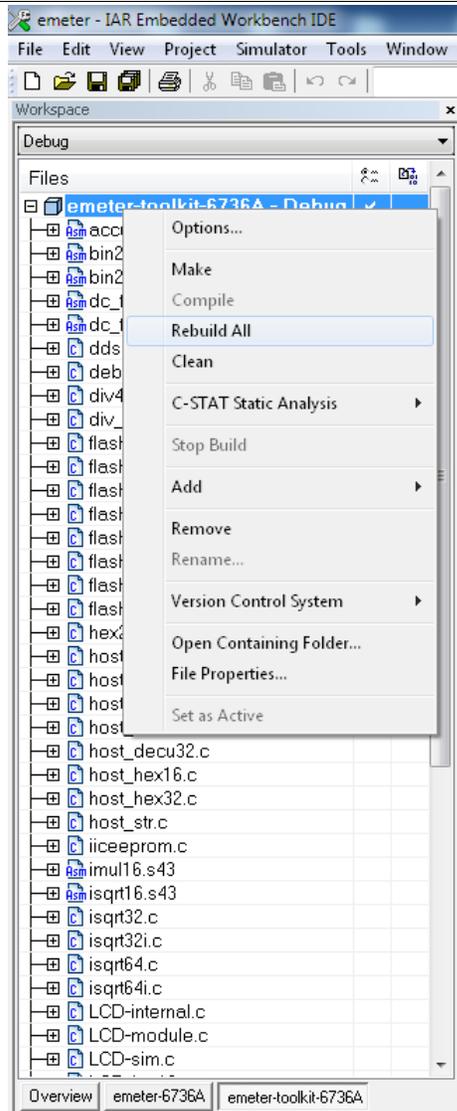
Figure 19. Toolkit Compilation in IAR
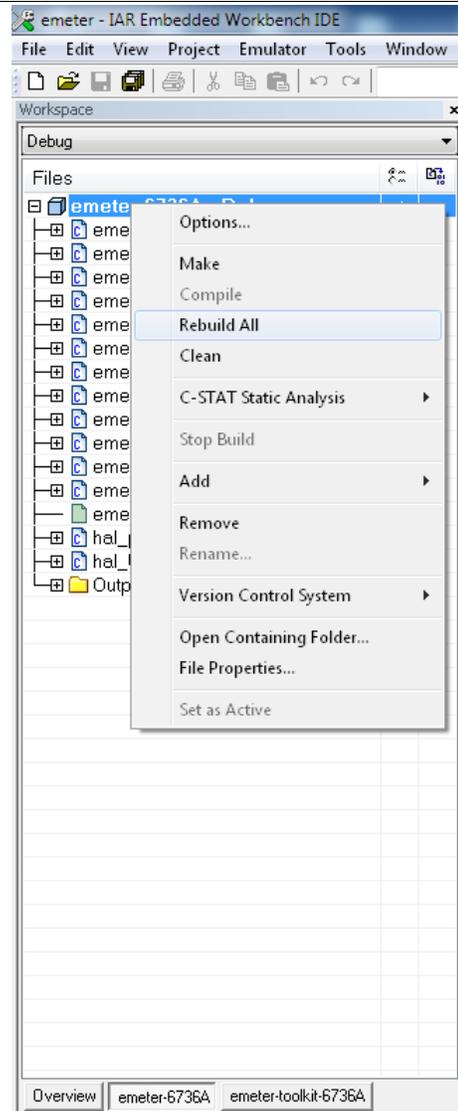
Figure 20. Metrology Project Build in IAR

6 Test Setup

6.1 Metrology Test Setup

For performing metrology testing, a source generator was used to provide the voltage and current to the meter at the proper locations (see Section 4.1). The design tests used a nominal voltage of 230 V, calibration current of 10 A, and nominal frequency of 50 Hz. In the tests, current is varied from 50 mA to 100 A. For each current, a phase shift of 0°, 60°, and −60° is applied between the voltage and current.

When voltage and current are applied to the meter, the meter outputs active energy pulses at a rate of 6400 pulses/kWh. This pulse output feeds into a reference meter that determines the active energy % error (for the equipment used in this test, the reference meter was integrated in the same equipment used for the source generator). The active energy % error is based on the actual energy provided to the meter and the measured energy as determined by the active energy output pulse of the meter. Based on this energy pulse measurement, a plot of active energy % error versus current is created for 0°, 60, and -60° phase shifts as shown in Section 8.2.

6.2 ESD Test Setup

When performing ESD testing, both a MSP430F6736-based meter and MSP430F6736A-based meter were tested to show the ESD improvements of the MSP430F6736A. Both meters use the same board (EVM430-F6736). The only differences between the meters would be whether a MSP430F6736 or MSP430F6736A was actually populated on the boards. Although this test shows the comparative behavior of the MSP430F6736 against the MSP430F6736A, please note that the ESD testing for e-meters is a system-level test. Therefore, improvements from selecting the MSP430F6736A varies based on layout and overall system design. Adhering to good ESD layout guidelines allows for maximum ESD immunity. The presence of the MSP430F6736A cannot compensate for significant design weaknesses because the ESD testing is performed on a system level.

Each meter was tested by applying discharges on the coupling plane, as Figure 21 shows. For each test point, ten strikes were applied. The tested ESD voltages were 2 kV to 20 kV in 2-kV increments with both positive and negative polarities. These voltages were applied from four different orientations with respect to the ESD gun, as Figure 22, Figure 23, Figure 24, and Figure 25 show.
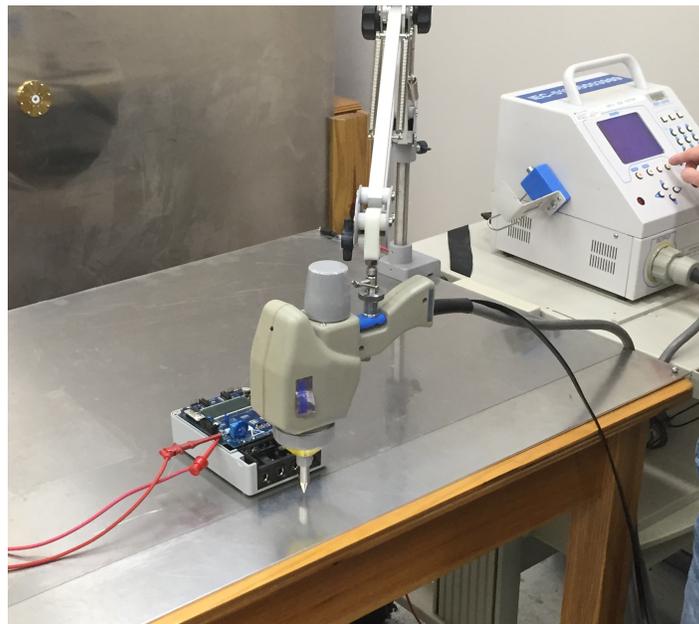
Figure 21. ESD Test Setup
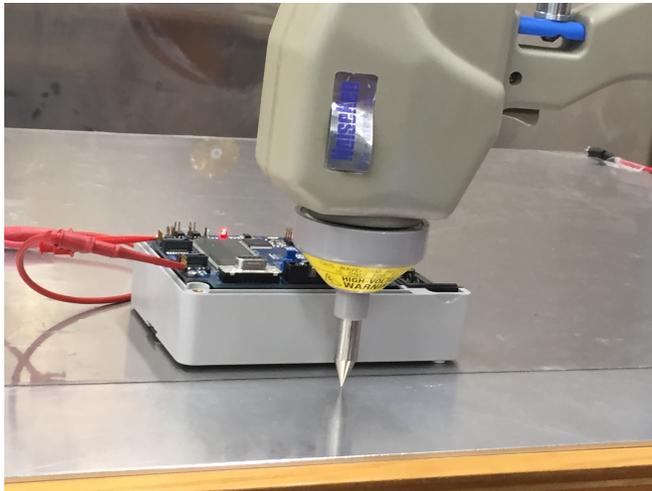
Figure 22. Left Orientation of E-Meter
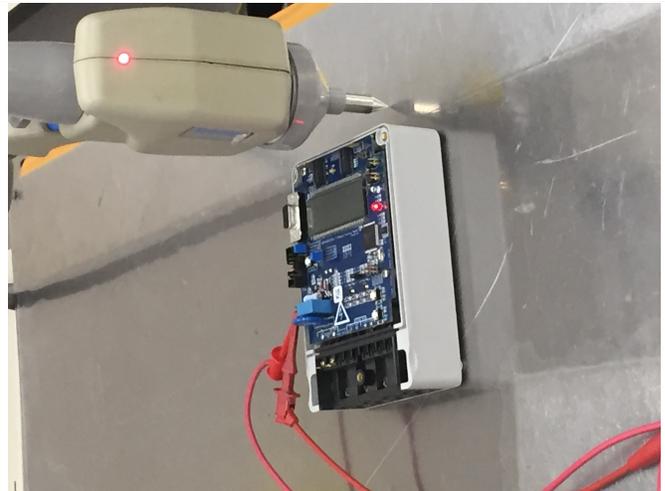
Figure 23. Top Orientation of E-Meter
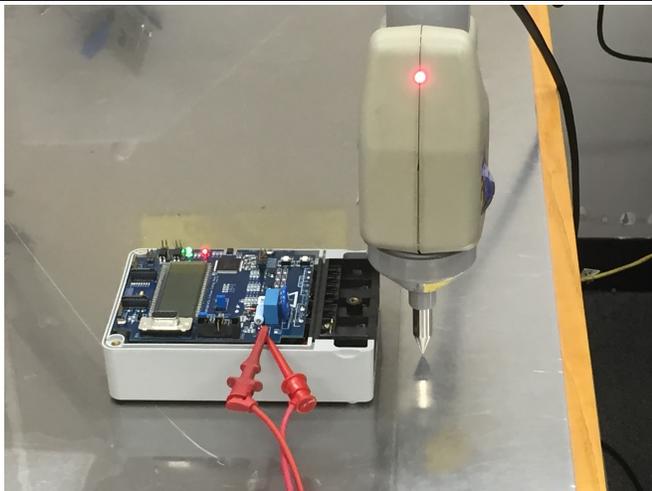
Figure 24. Bottom Orientation of E-Meter
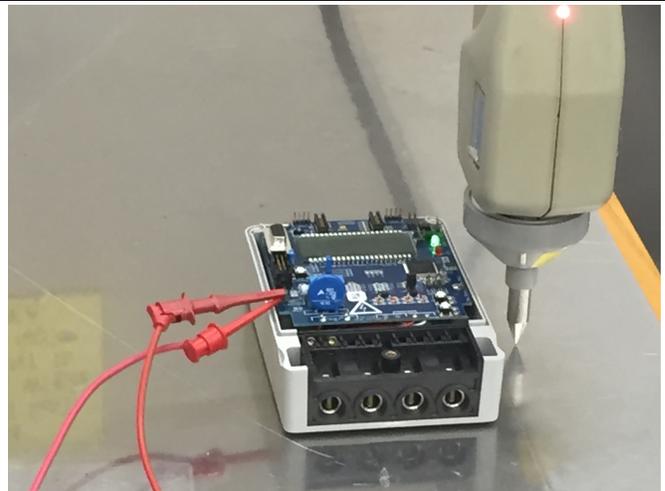
Figure 25. Right Orientation of E-Meter

To easily diagnose the state of the MSP430F6736A device when performing ESD testing, the EVM was loaded with software performing the functions listed in Section 3.4. Using the software, the state of the MSP430F6736A can be determined from the LEDs of the EVM. In addition, the current drawn by the microcontrollers were monitored to determine between latch-up or lock-up conditions.

Section 8.1 shows the results of these ESD tests.

7 Viewing Metrology Readings and Calibration

The values of the metrology parameters can be viewed on the LCD or the GUI. In addition, the active power reading can be viewed from an in-home display that communicates with the meter through ZigBee.

7.1 Viewing Results Through LCD

The LCD scrolls between metering parameters approximately every two seconds. For each metering parameter that shows on the LCD, two items actually show on the screen, a 1 or 2 character symbol, which is used to distinguish the parameter being displayed and the actual value of that parameter. The parameter symbol shows on the left side of the second line of the LCD. The actual value of the parameter shows just to the right of the parameter symbol.

Table 2 shows the different metering parameters that display on the LCD and the associated units in which they are displayed. The SYMBOL column in Table 2 shows which characters correspond to which metering parameter. The COMMENTS column provides a brief interpretation of the displayed metering parameters.

Table 2. Displayed Parameters

PARAMETER NAME	SYMBOL	UNITS	COMMENTS
Voltage		Volts (V)	--
Current		Amps (A)	
Active power		Watt (W)	--
Reactive power		Volt-ampere reactive (var)	--
Apparent power		Volt-ampere (VA)	--
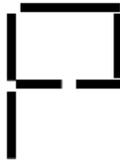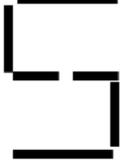
Table 2. Displayed Parameters (continued)

PARAMETER NAME	SYMBOL	UNITS	COMMENTS
Frequency	![F symbol]	Hertz (Hz)	--
Power factor	![PFC symbol] or ![PFL symbol]	Constant between 0 and 1	The characters ![PFC symbol] are used if the load is determined to be a capacitive load. The characters ![PFL symbol] are used if the load is determined to be an inductive load.
Total consumed active energy	![E symbol]	100 "ticks"	Every 10 ticks increments the tenths place by 1.
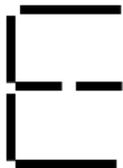
Figure 26 shows an example of the measured RMS voltage of 0 V being displayed on the LCD.
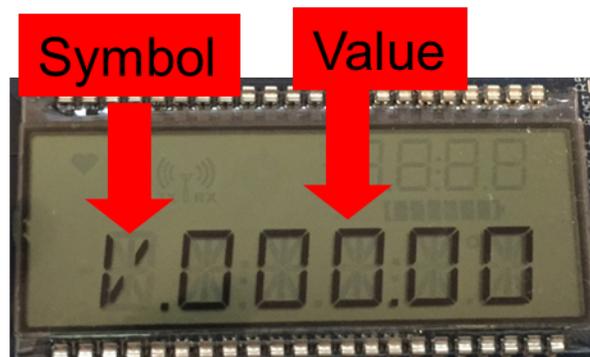
Figure 26. LCD Display

7.2 Viewing Results Using RF Technology (ZigBee)

The CC2530 Evaluation Module (EM) is an add-on and plug-in daughter card for ZigBee and IEEE 802.15.4 radio frequency (RF) applications in the 2.4-GHz, unlicensed industrial, scientific, and medical (ISM) band (see Figure 27). The communication interface to any host/application processor is through UART. The instantaneous power consumption sends periodically to the ZigBee module for wireless transmission.
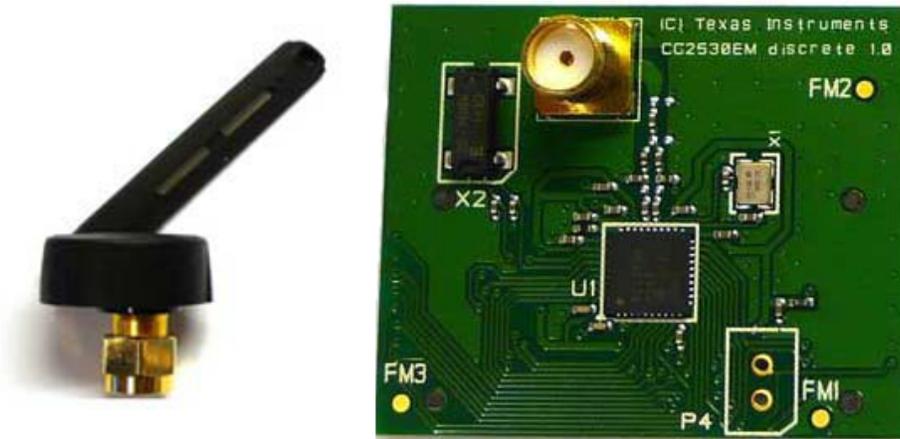
Figure 27. ZigBee Radio

This ZigBee module connects through the UART, which is configured to 115.2 kbaud on the transmit portion of the MSP430F6736A and the receive portion of the MSP430F4618 (IHD430).

7.2.1 In-Home Display

Most IHDs have their own setup mechanism and all of them tend to join the ZigBee network when turned ON. This section describes the in-home display using TI's IHD430 (TIDM-LOWEND-IHD), which Figure 28 shows. The IHD430 has an MSP430F461x device as an application/host processor.

Figure 28. TIDM-LOWEND-IHD Device

Viewing active power readings on the IHD430

Place a CC2530 module in the RF connector socket of the meter EVM430-F6736, making sure that the module is properly oriented. This CC2530 is flashed with code to act as a transmitter. The IHD430 also has a corresponding CC2530 module that has been flashed to act as a receiver. Please note that the CC2530 cannot be powered from the cap drop supply; therefore, the entire EVM must be powered from an external power supply, as mentioned in Section 4.2.

Initializing the IHD430

Power must be provided by 2 AAA batteries or an external supply. The power source is selected by configuring jumpers on the VCC and BATT headers and the power is supplied to the on-board MSP430 by placing a jumper on the PWR1 header. The power setup options are provided in the following list.

1. Jumper settings to provide battery power are:

    (a) Place jumper on BATT header

    (b) Place jumper on PWR1 header

2. Jumper settings to provide flash emulation tool power are:

    (a) Place jumper on pins [1-2] on VCC 3-pin header

    (b) Place jumper on PWR1 header

3. Jumper settings to provide external power are:

    (a) Place jumper on pins [2-3] on VCC 3-pin header

    (b) Place jumper on PWR1 header

4. Ensure jumper is placed on RF_PWR header, which has been provided to enable and disable power to CC2530

The "IHD430_SUPPORT" macro must be defined in the emeter-1ph-neutral-6736(A)_shunt.h file for the MSP430F6736A software to communicate the active power to the IHD430. When this macro is enabled, the active power reading sends to the on-board CC2530 transmitter through 8N1 UART communication at a baud rate of 115.2 k. The CC2530 then sends the data to the CC2530 receiver. The IHD430 receives the active power readings and displays it on the LCD. Please note, the transmitter (meter) must be turned ON before the receiver to ensure proper ZigBee communication. In addition, modifications can be made to the MSP430F6736A software to send different parameters for display onto the IHD430.

7.3 Calibrating and Viewing Results Through PC

7.3.1 Viewing Results

To view the metrology parameter values through the GUI, utilize the following steps:

1. Connect the EVM to a PC through an RS-232 cable.
2. Open the "GUI" folder and open calibration-config.xml in a text editor.
3. Change the "port name" field within the "meter" tag to the COM port connected to the meter. In Figure 29, this field shows COM2.
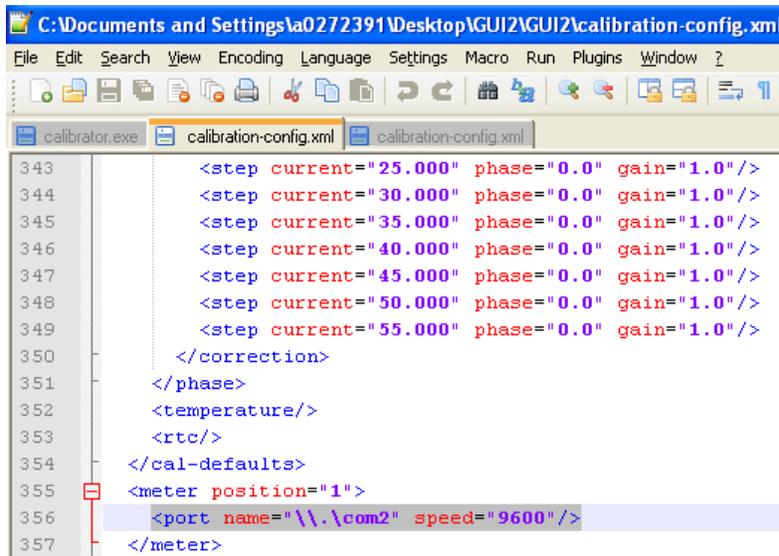
Figure 29. GUI Config File Changed to Communicate With Meter

4. Run the calibrator.exe file, which is located in the GUI folder. If the COM port in calibration-config.xml has been changed (the previous step 3) to the COM port connected to the EVM, the GUI opens (see Figure 30). If the GUI connects properly to the EVM, the top-left button is green. The button is red if there are problems with connections or if the code is not correctly configured. Click the green button to view the results.
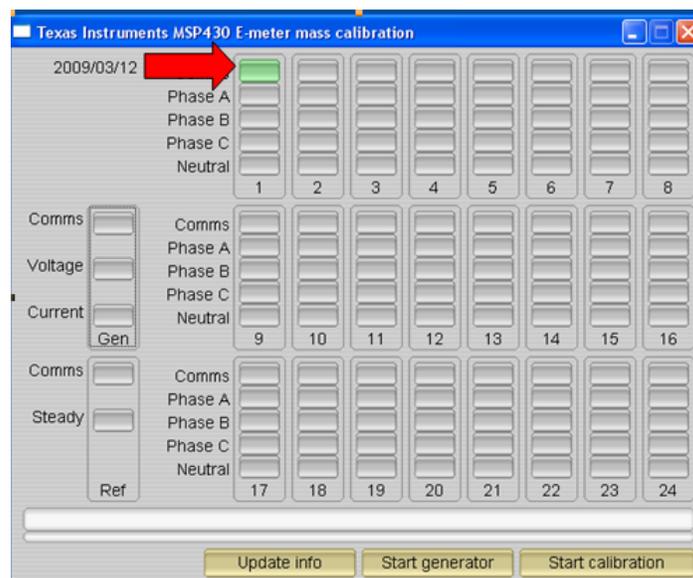
Figure 30. GUI Startup Window

Upon clicking on the green button, the results window opens (Figure 31). In Figure 31, there is a trailing "L" or "C" on the "Power factor" values to indicate an inductive or capacitive load, respectively.
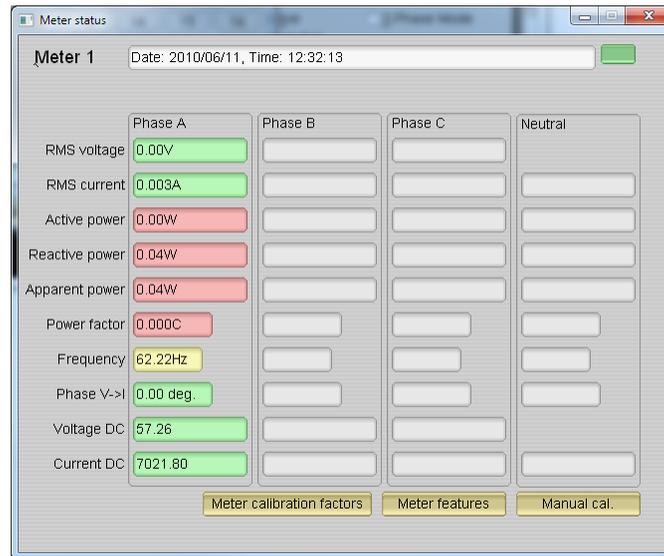
Figure 31. GUI Results Window

From the GUI results window, the user can either view the meter settings by clicking the"Meter features" button, view the meter calibration factors by clicking the "Meter calibration factors" button, or open the window used for calibrating the meter by clicking the "Manual cal." button.

7.3.2 Calibration

Calibration is key to the performance of any meter and is an absolutely necessary process for every meter to undergo. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify the effects of the aforementioned variables, every meter must be calibrated. For calibration to be performed accurately, there should be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration for this single-phase EVM.

The GUI used for viewing results can easily be used to calibrate the EVM. Parameters called calibration factors are modified in the software during the calibration to give the least error in measurement. For this meter, there are four main calibration factors: voltage scaling factor, current scaling factor, power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in the metrology software to real values represented in volts, current, and watts respectively. The phase compensation factor is used to compensate any phase shifts introduced by the current sensors and other passives.

When the meter software is flashed with the code (available in the *.zip file), the default calibration factors are loaded into these calibration factors. These values are to be modified through the GUI during calibration. The calibration factors are stored in INFO_MEM and they remain the same if the meter is restarted. However, if code is re-flashed during debugging operations, the calibration factors are replaced and the meter must be recalibrated. One way to save the calibration values is by clicking on the "Meter calibration factors" button (Figure 31). The "Meter calibration factors" window Figure 32 shows the latest values. This information can be used to directly replace the macro definition of these factors in the source code.
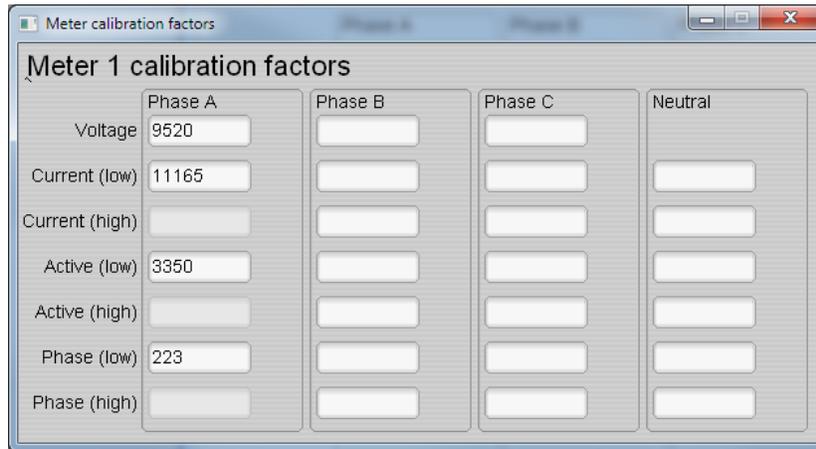
Figure 32. Calibration Factors Window

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factor is referred to as phase correction. For the entire calibration process, the AC test source must be ON, the meter connections must be consistent with Section 4.1, and the energy pulses must be connected to the reference meter.

7.3.2.1 Gain Calibration

Usually gain correction for voltage and current can be done simultaneously for all phases. However, energy accuracy (%) from the reference meter for each individual phase is required for gain correction of active power parameters.

7.3.2.1.1   *Voltage and Current Gain Calibration*

To calibrate the voltage and current readings, utilize the following steps:

1. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.

2. Configure the test source to supply the desired voltage and current. Ensure that these are the voltage and current calibration points with a zero-degree phase shift between the voltage and current (for example 230 V, 10 A, 0º (PF = 1).

3. Click on the "Manual cal." button (see Figure 31). The following screen pops up on the display (Figure 33):
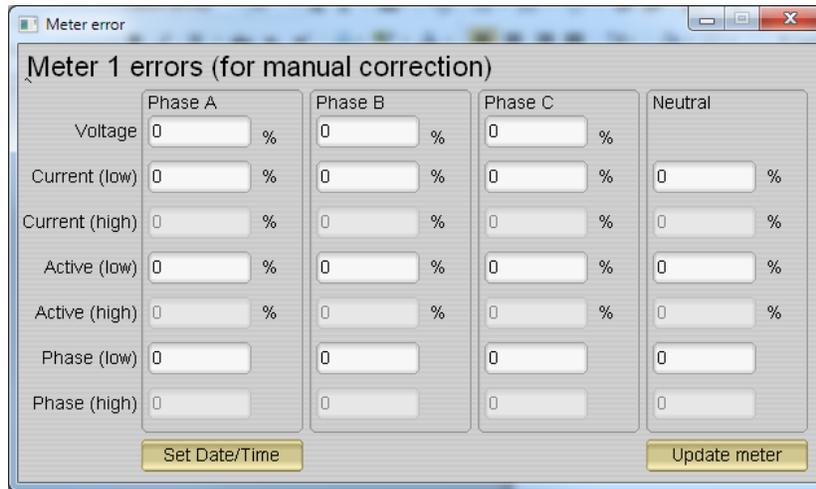
Figure 33. Manual Calibration Window

4. Calculate the correction values for voltage and current. The correction values that must be entered for the voltage and current fields are calculated by:

$$\text{Correction}(\%) = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100$$

where

- $\text{value}_{\text{observed}}$ is the value measured by the TI meter,
- $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source.   (8)

5. After calculating for voltage and current, input these values as is (±) in the "Voltage" and "Current (low)" fields.

6. Click on the "Update meter" button and the observed values for the voltage and current on the GUI update gradually to the desired voltages and currents.

7.3.2.1.2   *Active Power Gain Calibration*

After performing gain correction for voltage and current, gain correction for active power must be done. Gain correction for active power is done differently in comparison to voltage and current. Although, conceptually, calculating using Step 4 with Active power readings (displayed on the AC test source) can be done, it will not be the most accurate method and should be avoided.

The best option to get the is directly from the reference meter's measurement error of the active power. This error is obtained by feeding energy pulses to the reference meter. To perform active power calibration, the following steps must be followed.

1. Turn off the meter and connect the meter's energy pulse output to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.

2. Turn on the AC test source

3. Repeat Steps 1 to 3 from the previous Section 7.3.2.1.1 with the identical voltage, current and 0º phase shift that were used in the previous section.

4. Obtain the % error in measurement from the reference meter. Note that this value may be negative.

5. Enter the error obtained in the above step into the "Active (low)" field under the corresponding phase in the GUI window. This error is already the value and does not need to be calculated.

6. Click on "Update meter" and the error values on the reference meter would immediately settle to a value close to zero.

7.3.2.2   Phase Correction

After performing power gain correction, phase calibration must be performed. To perform phase correction calibration, perform the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform steps 1-3 from Section 7.3.2.1.1 using the identical voltage and current used in that section.

2. Modify only the phase-shift to a non-zero value; typically, +60º is chosen. The reference meter now displays a different % error for active power measurement. Note that this value may be negative.

3. If this error is not close to zero, or is unacceptable, perform phase correction by following these steps:

    (a) Enter a value as an update for "Phase (Low)" field . Usually, a small ± integer should be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: +60º), a positive (negative) error would require a positive (negative) number as correction.

    (b) Click on "Update meter" and monitor the error values on the reference meter.

    (c) If this measurement error (%) is not accurate enough, fine tune by incrementing/decrementing by a value of one based on the previous steps 3a and 3b. Please note, after a point, the fine-tuning will only result in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.

    (d) Change the phase now to –60 Degrees and check if this error is still acceptable. Ideally, errors must be symmetric for same phase shift on lag and lead conditions.

After performing phase correction, calibration is complete. The new calibration factors as shown in Figure 34 can be viewed by clicking the "Meter Calibration factors" button of the GUI metering results window in Figure 31.
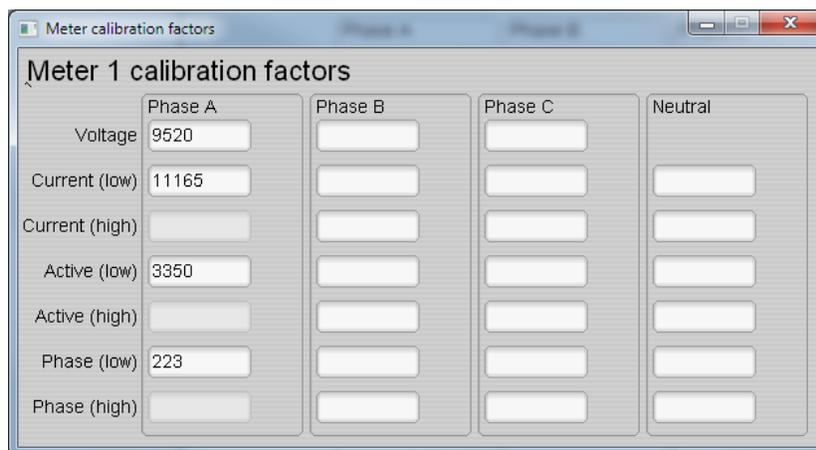
Figure 34. Calibration Factors Window

The configuration of the meter can be viewed by clicking on the "Meter features" button to access screen that Figure 35 shows.
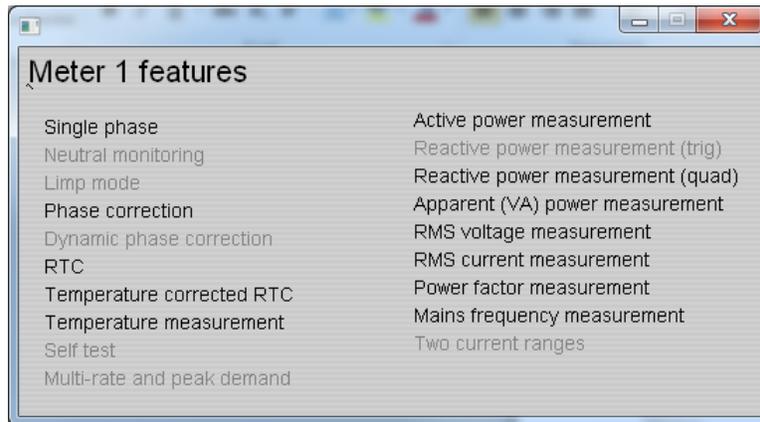
Figure 35. Meter Features Window

8   Test Data

8.1   ESD Results

To test the comparative ESD robustness between the MSP430F6736A and MSP430F6736, an IEC 61000-4-2 test was performed on one EVM430-F6736 that had the MSP430F6736A as the metering SoC and another EVM430-F6736 that had the non-A MSP430F6736 as the metering SoC. Please note that for the EVM430-F6736, some ESD tradeoffs were made to support fully showcasing the features of the silicon and ease of use for evaluation purposes. However, the EVM can still be used as a gauge to show the improvements in using the MSP430F6736A devices instead of the MSP430F6736.

For applying the ESD test on the two test EVMs, both positive and negative polarity discharges were applied on both test boards at the same location. In the tests, recoverable failures (for example, a reset), lock-ups, and latch-ups were logged as failures. Table 3–Table 6 shows the results of these tests. In these tests, voltage levels where both positive and negative polarity tests passed are colored green, tests where only either positive or negative polarity tests passed are colored yellow, and tests where both positive and negative polarity tests failed are colored red. To verify failures in some cases, a second trial of a test was performed so a particular test may have two results that correspond to different trials as was done for the 18-kV negative polarity test for the bottom orientation. As a result, some tests have two results listed.

Table 3. IEC 61000-4-2 Test Results for the MSP430F6736 and MSP430F6736A, Left Orientation

TEST VOLTAGE	F6736 RESULTS (+POLARITY/ −POLARITY)	F6736A RESULTS (+POLARITY/ −POLARITY)
2	Pass/Pass	Pass/Pass
4	Pass/Pass	Pass/Pass
6	Pass/Pass	Pass/Pass
8	Pass/Pass	Pass/Pass
10	Pass/Pass	Pass/Pass
12	Pass/Pass	Pass/Pass
14	Pass/Pass	Pass/Pass
16	Pass/Pass	Pass/Pass
18	Pass/Pass	Pass/Pass
20	Pass/Pass	Pass/Pass

Table 4. IEC 61000-4-2 Test Results for the MSP430F6736 and MSP430F6736A, Right Orientation

TEST VOLTAGE	F6736 RESULTS (+POLARITY/ −POLARITY)	F6736A RESULTS (+POLARITY/ −POLARITY)
2	Pass/Pass	Pass/Pass
4	Pass/Pass	Pass/Pass
6	Pass/Pass	Pass/Pass
8	Pass/Pass	Pass/Pass
10	Pass/Pass	Pass/Pass
12	Pass/Pass	Pass/Pass
14	Pass/Pass	Pass/Pass
16	Fail(anomaly)/Pass	Pass/Pass
18	Pass/Pass	Pass/Pass
20	Fail/Pass	Pass/Pass

Table 5. IEC 61000-4-2 Test Results for the MSP430F6736 and MSP430F6736A, Bottom Orientation

TEST VOLTAGE	F6736 RESULTS (+POLARITY/ −POLARITY)	F6736A RESULTS (+POLARITY/ −POLARITY)
2	Pass/Pass	Pass/Pass
4	Pass/Pass	Pass/Pass
6	Pass/Pass	Pass/Pass
8	Pass/Pass	Pass/Pass
10	Pass/Pass	Pass/Pass
12	Pass/Pass	Pass/Pass
14	Pass/Pass	Pass/Pass
16	Pass/Pass	Pass/Pass
18	Pass/Fail-Pass	Pass/Pass
20	Pass/Fail	Pass/Pass

Table 6. Test Results for the MSP430F6736 and MSP430F6736A, Top Orientation

TEST VOLTAGE	F6736 RESULTS (+POLARITY/ −POLARITY)	F6736A RESULTS (+POLARITY/ −POLARITY)
2	Pass/Pass	Pass/Pass
4	Pass/Pass	Pass/Pass
6	Pass/Pass	Pass/Pass
8	Pass/Pass	Pass/Pass
10	Fail/Pass	Pass/Pass
12	Fail/Fail	Pass/Pass
14	/Fail	Pass/Pass
16		Pass/Fail(Anomaly)-Pass
18		Fail/Fail
20		Fail/

From these results, there is a clear improvement in selecting the MSP430F6736A devices over the MSP430F6736. The MSP430F6736A chips pass up to 20 kV in three of the four orientations tested. In the other orientation, there is still a 4–8-kV improvement. The reduced performance in this orientation is due to the ESD gun being in closer proximity to the LCD and its LCD pins and long traces, which were sensitive to ESD. In this hardware, the LCD lines are not individually decoupled. Decoupling the LCD lines increases the system level ESD performance.

8.2 *Metrology Result Comparison*

Regardless of the improvements made in the MSP430F6736A device, metrology performance is still comparable to the non-A MSP430F6736. To show this, an EVM430-F6736 was tested with a MSP430F6736 and a MSP430F6736A. Table 7, Figure 36, and Figure 37 show the results for these tests. From these results, it is apparent that the MSP430F6736A device can still meet the class 0.2% accuracy requirements fulfilled by the non-A MSP430F6736.

Table 7. Active Energy % Error for MSP430F6736 and MSP430F6736A

Current (Amps)	MSP430F6736			MSP430F6736A		
	0°	60°	−60°	0°	60°	−60 °
0.05	−0.045	0.058	−0.07	0.058	0.006	0.006
0.1	−0.019	0.083	−0.07	0.006	−0.019	0.006
0.25	−0.019	0.0575	−0.0575	0.006	0.032	−0.019
0.5	0.006	0.083	−0.045	−0.0023	0.0233	0.0063
1	0.0147	0.0663	−0.0617	0.0147	0.032	−0.0023
2	−0.007	0.058	−0.07	−0.007	0.0233	−0.019
5	0.0043	0.022	−0.019	0.008	0.011	0.017
10	−0.007	−0.024	0.003	0.014	−0.0007	0.03
20	−0.015	−0.0533	0.0493	0.006	−0.019	0.032
30	0.0003	−0.079	0.0747	0.015	−0.045	0.058
40	−0.0067	−0.096	0.07	0.019	−0.0493	0.0787
50	0.011	−0.106	0.1023	0.03	−0.055	0.119
60	0.0006	−0.099	0.1203	0.032	−0.0643	0.123
70	0.0167	−0.096	0.1187	0.0307	−0.067	0.1307
80	0.0263	−0.098	0.143	0.035	−0.064	0.1407
90	0.0367	−0.096	0.1563	0.043	−0.062	0.1467
100	0.0387	−0.0943	0.16	0.04	−0.06	0.155
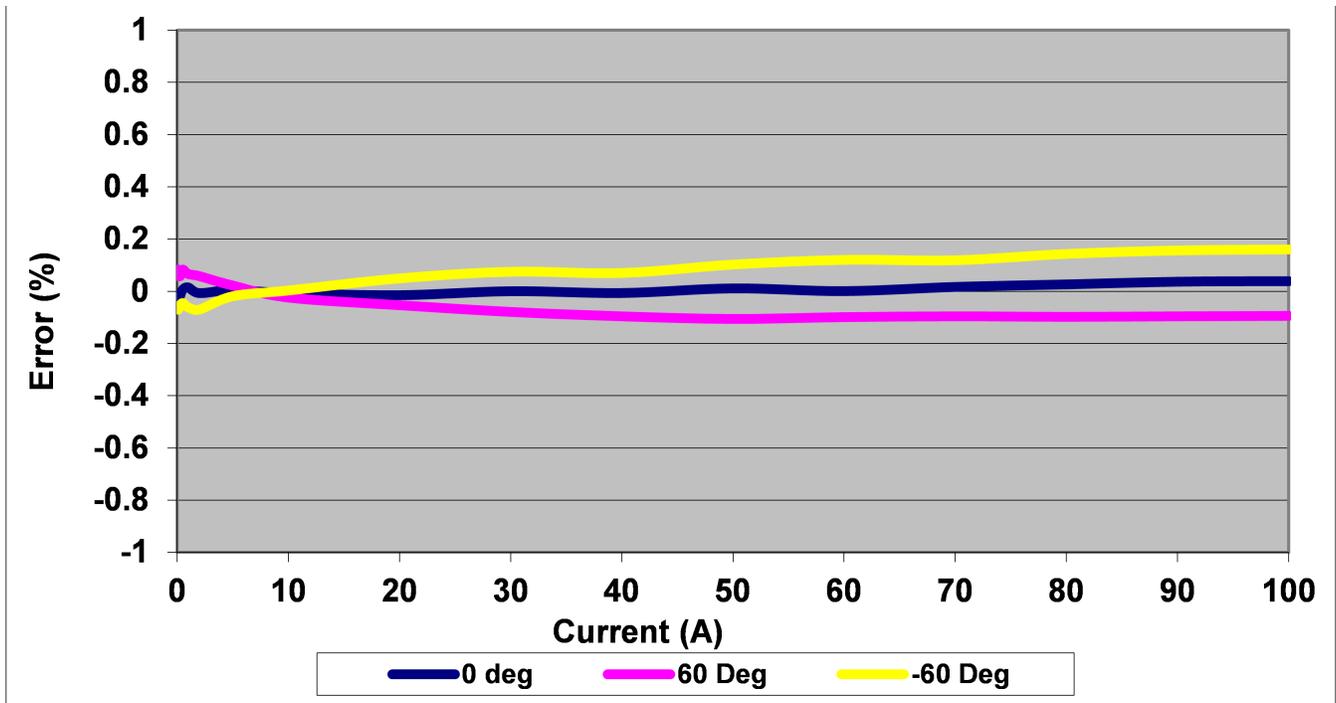
Figure 36. EVM430-F6736 Performance With MSP430F6736
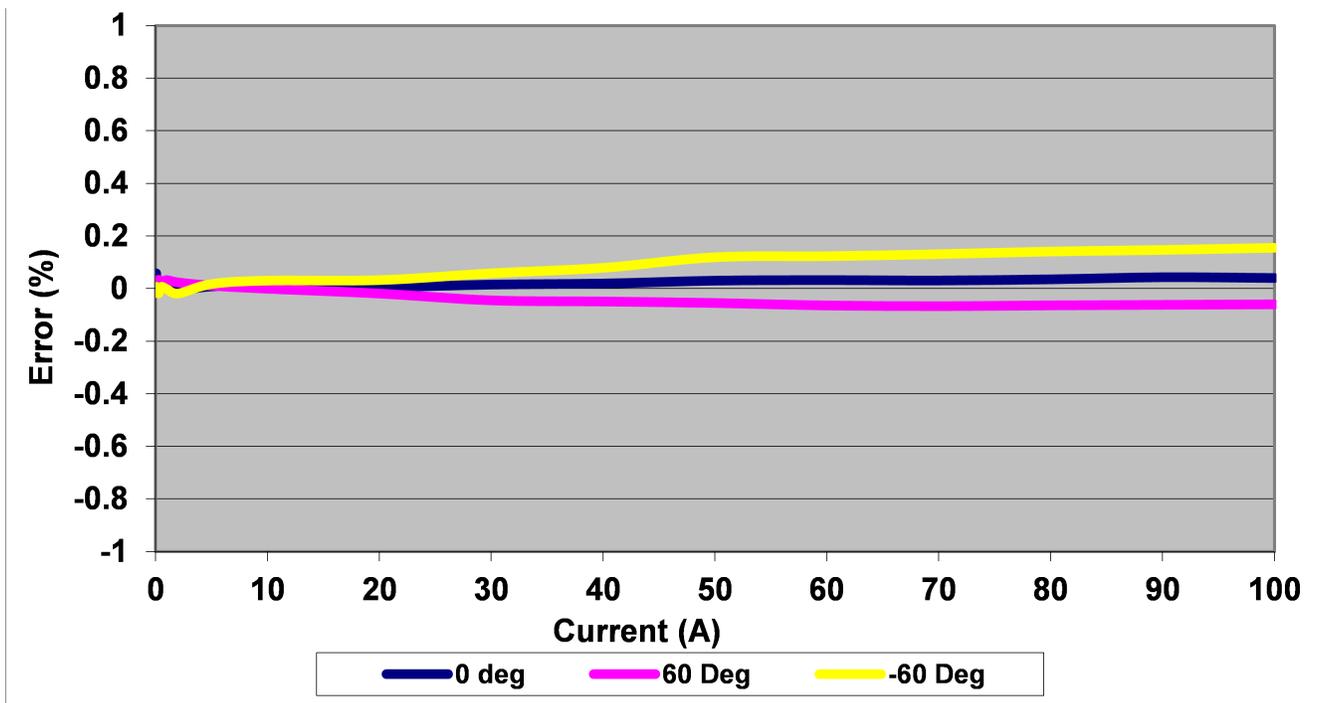
Figure 37. EVM430-F6736 Performance With MSP430F6736A

9   Design Files

9.1   Schematics

To download the Schematics for each board, see the design files at http://www.ti.com/tool/TIDM-1PHMTR-ESD.
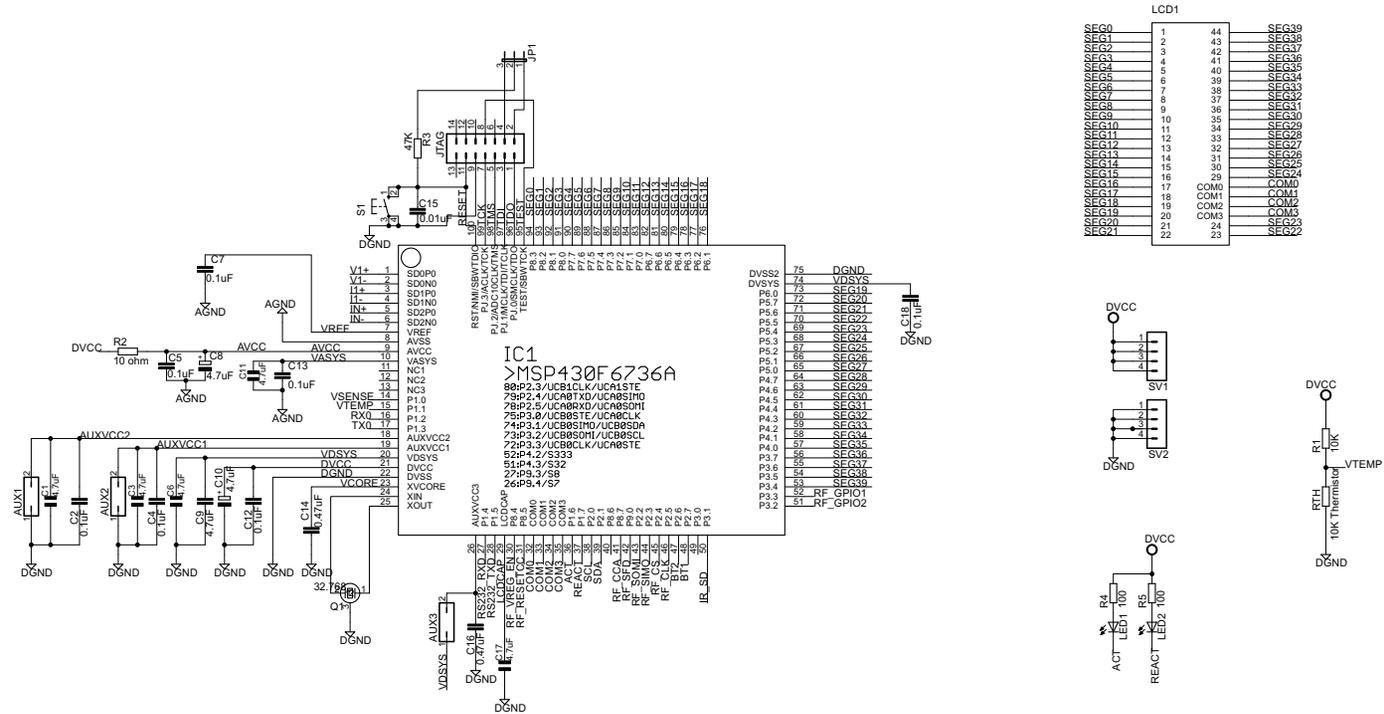
Figure 38. TIDM-1PHMTR-ESD Schematic Page 1
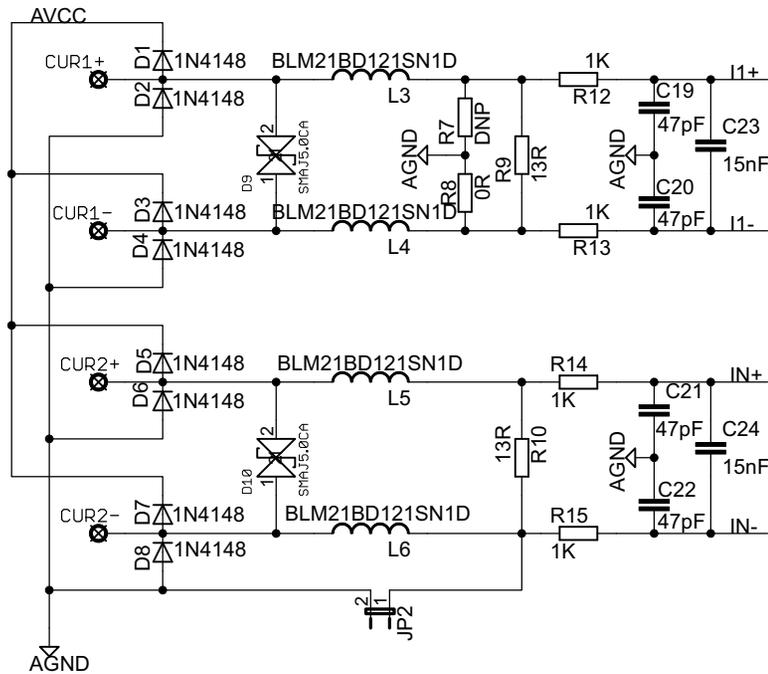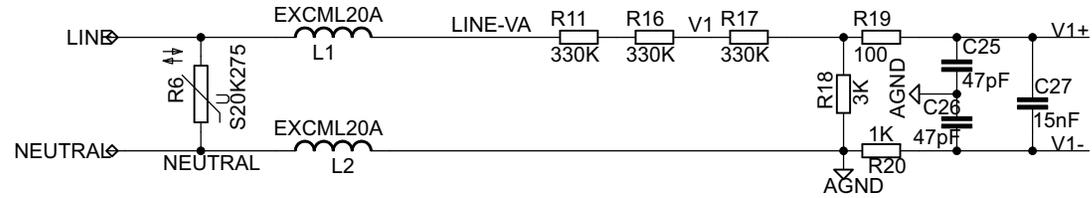
Figure 39. TIDM-1PHMTR-ESD Schematic Page 2
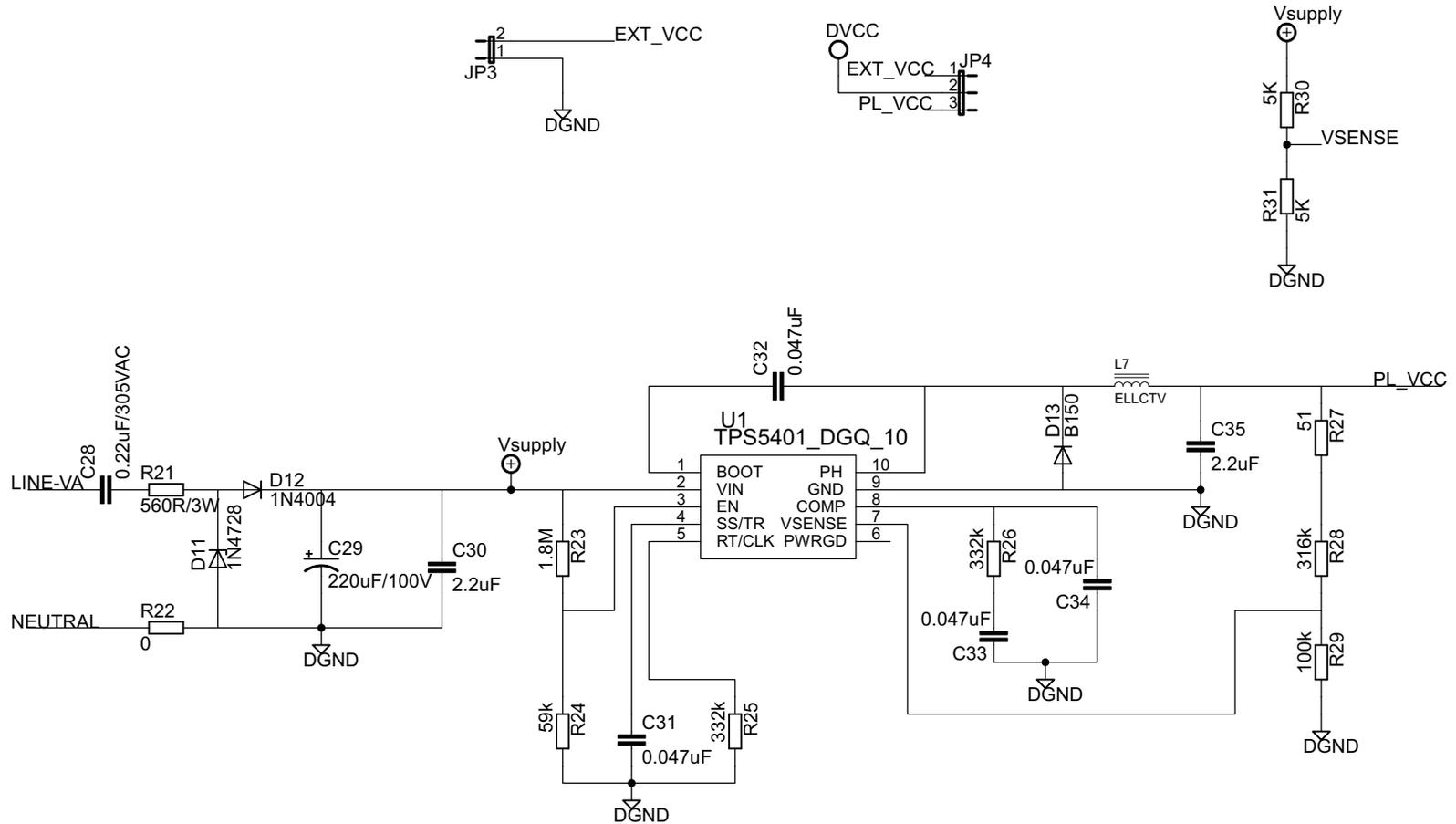
Figure 40. TIDM-1PHMTR-ESD Schematic Page 3
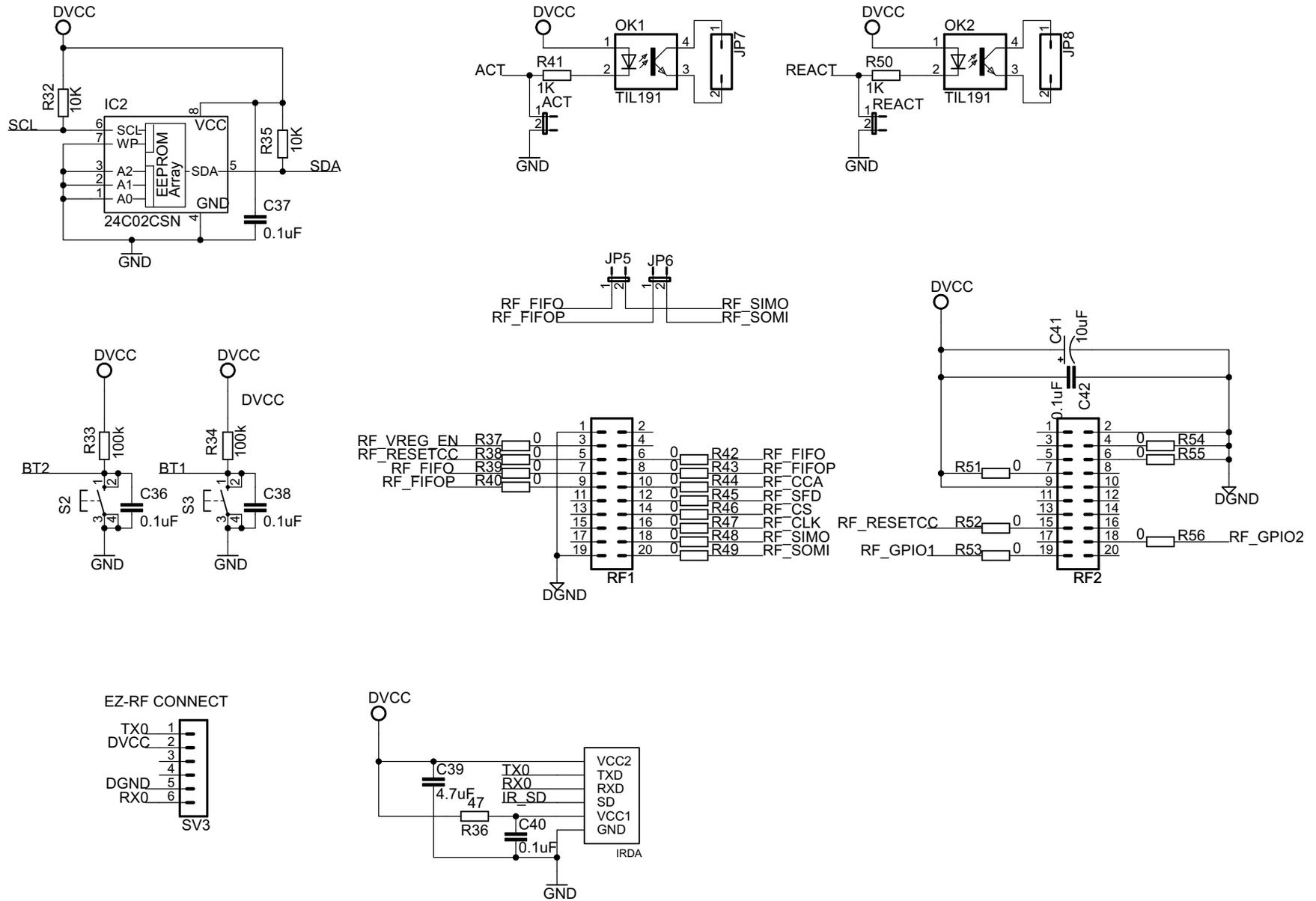
Figure 41. TIDM-1PHMTR-ESD Schematic Page 4
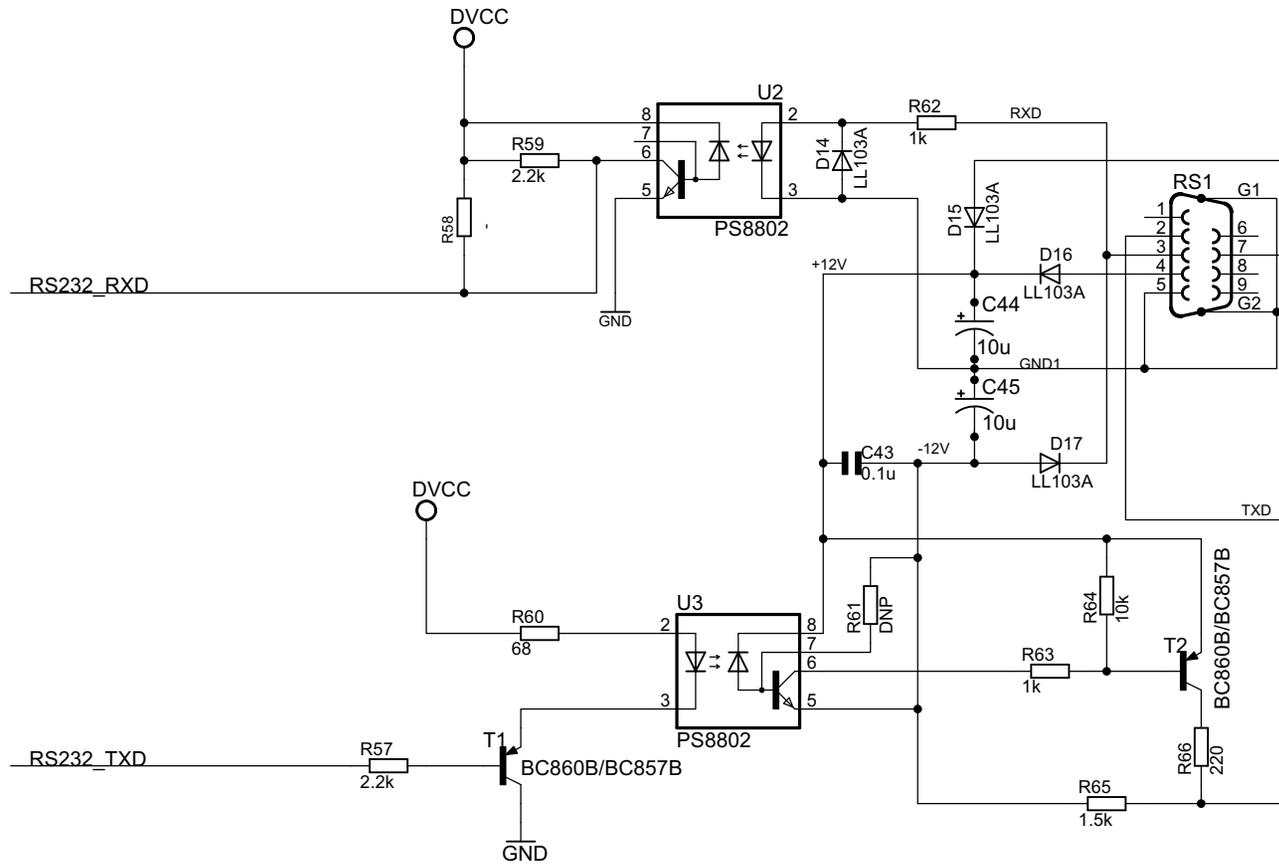
Figure 42. TIDM-1PHMTR-ESD Schematic Page 5

9.2 Bill of Materials

To download the Bill of Materials (BOM), see the design files at http://www.ti.com/tool/TIDM-1PHMTR-ESD.

9.3 PCB Layout Recommendations

PCB layout is an important factor in a meter's ESD immunity performance. The EVM430-F6736 in particular was designed to make it easy to evaluate the MSP430F6736 as an e-meter SoC. As a result, in certain instances, ESD performance was traded off for ease of evaluation of the EVM. However, in general, some PCB layout guidelines for ESD performance are the following:

- Use ground planes instead of ground traces where possible and minimize the cuts in these ground planes(especially for critical traces) in the direction of current flow. Ground planes provide a low-impedance ground path which minimizes induced ground noise. However, cuts in the ground plane can increase inductance. If there are cuts in the ground plane, they should be bridged on the opposite side with a 0-Ω resistor.
- When there is a ground plane on both top and bottom layers of a board (such as in the EVM of this design) ensure there is good stitching between these planes through the liberal use of vias that connect the two planes.
- Keep traces short and wide to reduce trace inductance. If an LCD is used, place it near the microcontroller and prevent long LCD traces to the microcontroller.
- Use wide VCC traces and star-routing for these traces instead of point-to-point routing.
- Minimize the length of the microcontrollers reset trace and other critical edge-triggered traces.
- Isolate sensitive circuitry from noisy circuitry. For example, high voltage and low voltage circuitry must be separated.
- Use transient voltage suppressors, EMI suppressant ferrite beads, and other ESD protection devices to suppress the effects from an ESD discharge. The turn on time of these devices should be small since the rise time of ESD discharge waveform is also small. ESD protection devices can be found at the following link: www.ti.com/esd.
- Keep sensitive circuitry away from PCB edges. If a ground plane is present, put sensitive circuitry near the center of these ground planes.
- Use decoupling capacitors with low effective series resistance (ESR) and effective series Inductance. Place decoupling capacitors close to their associated pins.
- Place connectors all on one edge of the PCB, especially through-hole connectors since they cause breaks in the ground plane.
- Minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there should be clean ground underneath the crystal and placing any traces underneath the crystal should be prevented. Also, keep high frequency signals away from the crystal.

For more ESD recommendations, please refer to SLAA530 [6].

9.3.1 Layer Plots

To download the layer plots, see the design files at http://www.ti.com/tool/TIDM-1PHMTR-ESD.

9.4 CAD Project

To download the CAD project files, see the design files at http://www.ti.com/tool/TIDM-1PHMTR-ESD.

9.5 Gerber Files

To download the Gerber files for each board, see the design files at http://www.ti.com/tool/TIDM-1PHMTR-ESD.

10 Software Files

To download the software files, see the design files at http://www.ti.com/tool/TIDM-1PHMTR-ESD.

11   References

1. International Electrotechnical Commission, IEC 61000-4-2, Electromagnetic capability (EMC)—Part 4: Testing and measurement techniques – Electrostatic discharge immunity test, Ed. 2.0.
2. Texas Instruments, *Segment LCD-Based Low-End In-Home Display with Wireless RF Communication* , User's Guide, (TIDU203).
3.
4. Texas Instruments, *MSP430x5xx and MSP430x6xx Family*, User's Guide, (SLAU208).
5. Texas Instruments, *MSP430F673xA, MSP430F672xA Mixed-Signal Microcontrollers*, Data Sheet, (SLASE46).
6. Texas Instruments, *Improved Load Current Capability for Cap-Drop Off-Line Power Supply for E-Meter* , Application Report, (SLVA491).
7. Texas Instruments, *MSP430 ™ System-Level ESD Considerations*, Application Report, (SLAA530).

12   About the Author

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